NASA Technical Memorandum 104309

# A Conversion of Wheatstone Bridge to Current-Loop Signal Conditioning For Strain Gages

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1995


National Aeronautics and
Space Administration

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## ABSTRACT

Current loop circuitry replaced Wheatstone bridge circuitry to signal-condition strain gage transducers in more than 350 data channels for two different test programs at NASA Dryden Flight Research Center. The uncorrected test data from current loop circuitry had a lower noise level than data from comparable Wheatstone bridge circuitry, were linear with respect to gage-resistance change, and were uninfluenced by varying lead-wire resistance. The current loop channels were easier for the technicians to set up, verify, and operate than equivalent Wheatstone bridge channels. Design choices and circuit details are presented in this paper in addition to operational experience.

## NOMENCLATURE

| | |
|---|---|
| C | capacitors on the circuit card |
| DACS | data acquisition and control system |
| $EU_{cal}$ | engineering units represented by calibration |
| EX | excitation |
| GF | gage factor |
| F | fuse |
| FLL | Flight Loads Laboratory |
| $I$ | current, A |
| IN | input |
| $\Delta I$ | current change, A |
| $\Delta I_{cal}$ | current change through the gage during calibration, A |
| $I_g$ | gage current, A |
| $I_{ref}$ | reference resistance current, A |
| J | circuit board jack |
| JP | circuit board jumper |
| OUT | output |
| OVP | over-voltage protection |
| R | resistors on the circuit card |
| $R$ | initial strain gage resistance, Ω |
| $\Delta R$ | resistance change, Ω |
| ΔR/R | resistance change–to–gage resistance ratio |
| $\Delta R_{cal}$ | apparent gage resistance change caused by $\Delta I_{cal}$, Ω |
| $R_g$ | gage resistance, Ω |
| $R_{cal}$ | calibration resistance, Ω |
| $R_{ref}$ | reference resistance, Ω |
| $R_{ref_a}$ | apparent reference resistance, Ω |
| U | integrated circuit components |
| $V_g$ | gage voltage, V |
| $V_o$ | output voltage, V |
| $\Delta V_{cal}$ | output voltage change caused by $\Delta I_{cal}$, V |
| $V_{ref}$ | reference voltage, V |
| $V_{sp}$ | set-point voltage, V |

*Senior Measurement Systems Engineer

## INTRODUCTION

The Flight Loads Laboratory (FLL) at the NASA Dryden Flight Research Center has used large-scale (more than 1,000 data channels), computer-controlled data acquisition systems since it opened in 1967. The FLL test programs frequently involve strain measurements during high-temperature (higher than 2,000 °F) test operations. Until recently, the ubiquitous Wheatstone bridge circuit was the only reasonable choice for static strain-gage signal conditioning. Current-loop circuit topology was invented at NASA Dryden in 1992, demonstrated in the laboratory, and reported in comparison with the Wheatstone bridge.[1]

Significant improvements have been made at NASA Dryden in the circuitry that implement the current loop paradigm.[2] These improvements are as follows:

- An effective method has been found to design a stable voltage-difference measuring system without the switching circuitry initially used in practical current-loop implementations
- Regulating loop current by controlling the reference voltage to be constant has been found to be especially advantageous
- Various means have been designed to accomplish an analog offset that is a function of the excitation current level
- End-to-end electrical calibration for strain is accomplished without the need to know the initial resistance of the strain gage
- Ratiometric measurement of the output with respect to the reference voltage removes the need to regulate loop current
- Signal conditioning has been demonstrated that separately indicates strain and temperature using the same four connecting wires.[3] These innovations are the subject of various patent applications, and a patent[4] has been issued on the fundamental current-loop circuit topology

The NASA Dryden FLL has a 1,280-channel data acquisition and control system (DACS) in current use known locally as the "DACS II." The system is equipped with 640 channels of Wheatstone bridge signal conditioning, each with a plug-in card containing bridge completion and shunt calibration components and a presampling filter. A prototype current-loop signal-conditioning circuit was designed to replace the DACS II Wheatstone bridge circuit. The prototype was built on an external, solderless breadboarding system that connected with shielded cables in place of the Wheatstone bridge card. This circuit was demonstrated to the FLL technicians and engineers.

The prototype current-loop signal-conditioning circuit provided measurement data from the DACS II with a standard deviation of less than two data counts. This standard deviation is less than 5 μV of deviation caused by electrical noise, representing typically less than 2 μin/in of strain. Deviation from perfect linearity was unobservable within the resolution and accuracy of the DACS II. Performance was stable and fully predicted by current loop theory, and random variations in lead-wire resistance had no appreciable influence on the output.

After witnessing the prototype demonstrations and reviewing its performance data, the technicians and engineers were convinced the current-loop signal conditioning offered superior performance and more versatility than the Wheatstone bridge. Several of these improvements provided such key benefits that the test engineers for two test programs involving approximately 350 strain measurements chose to require current-loop signal conditioning for their test programs. A printed circuit board (fig. 1) was developed that directly replaces the old DACS II Wheatstone bridge circuitry with new current loop circuitry. This paper reports the design of this modification, the test data, and user experience with several hundred current-loop measurement channels installed in the DACS II.

## DESIGN REQUIREMENTS

The system requirements were to include current-loop signal conditioning and to avoid system changes beyond the new current-loop printed circuit board while retaining the operational features, measurement accuracy, and precision of the existing DACS II. The DACS II allowable system measurement errors, based on the connection of a

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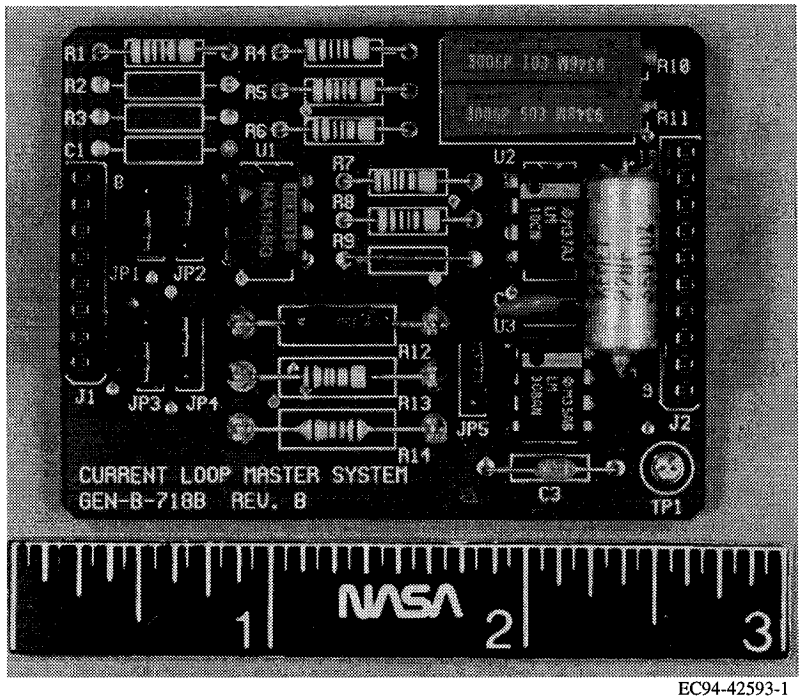


EC94-42593-1

Figure 1. The DACS II current-loop printed circuit board.

perfect transducer and including all system error sources (other than common-mode rejection), are no greater than ±0.15 percent or ±20 μV, whichever is greater, of the selected measurement range with a three-sigma level of confidence. Conformance to these specifications is required for a minimum of 6 operational hours after a 30-minute warmup period that is followed by an automatic calibration cycle.

From these basic requirements, several other design requirements emerged. These requirements were as follows:

- Fit the physical space, connectors, and signal assignments of the previously used Wheatstone bridge printed circuit card
- Power the current loop electronics with the Wheatstone bridge excitation supply
- Provide a calibration that appears to the system software as though it were a Wheatstone bridge shunt calibration
- Monitor the excitation level
- Presample-filter the measurement ahead of the system analog/digital converter
- Optionally connect either three or four lead wires to single strain gages
- Optionally connect to a rosette of three strain gages in a single current loop
- Maintain high-voltage fault protection in the connections to a test article
- Provide an adjustable analog offset based on excitation current level
- Design for ease in setup and use by the technical staff

## THE CURRENT LOOP DESIGN

The design requirements led to basic design choices for excitation, voltage-difference measurement, offset adjustment, and calibration circuitry from among the available alternatives.[2] Instrumentation amplifier–based voltage-difference measurement was selected because it had been demonstrated to meet the accuracy and noise

floor requirements in a single component. The current change, $\Delta I$, off-set adjustment was selected because of its demonstrated stability and circuit simplicity. The $\Delta I$ calibration was selected because it directly identifies system sensitivity to the resistance change–to–gage resistance ratio, $\Delta R/R$, and appears like a Wheatstone bridge shunt calibration to the rest of the DACS II. Strain gage wiring to system input connectors had to differ for current loop circuitry because of signal conflicts with dedicated Wheatstone bridge functions within the DACS II.

## Circuit Functions

The DACS II current-loop electronics (fig. 2) accomplish several different functions. The circuit components and their associated functions are as follows:

- The U2, R7, R8, and R13 components comprise a combined voltage reference source and, in conjunction with the R12 resistor, a current regulator
- The R1, R5, and C4 components provide presample filtering. The R2, R3, and C1 components substitute

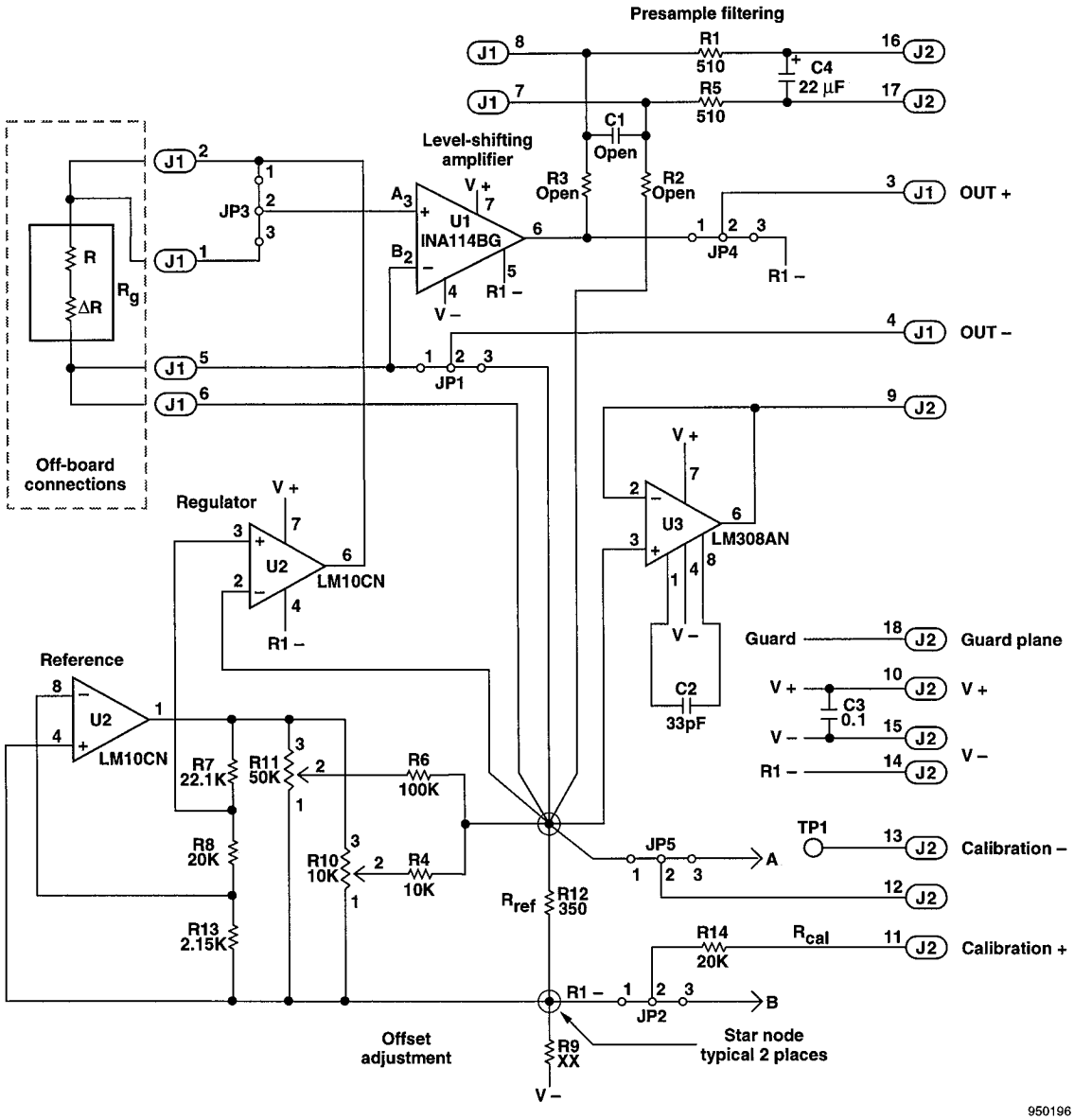


Figure 2. The production circuit schematic.

for an additional stage of presample filtering when the circuit is used with multigage current loops

- The U1 and R12 components comprise the voltage-difference calculation circuit, with two- or three-wire gage connection selected by the JP1 and JP3 circuit board jumpers. The circuit output is connected through the JP4 circuit board jumper or the substitute presample filter

- The R4 and R10 resistors provide "coarse" offset adjustment. The R6 and R11 resistors provide "fine" offset adjustment

- The R14 resistor and off-board relays implement automatic shunt calibration connected through the JP2 and JP5 circuit board jumpers

- The U3 and C2 components comprise a buffer amplifier to monitor loop-current excitation level

- The R9 resistor is typically a jumper wire. A resistor or light-emitting diode can be inserted here to raise the input common-mode voltage level to the U1 component

To achieve good measurement stability, the R12 resistor (from which the reference resistance, $R_{ref}$, is taken) is the type used for Wheatstone bridge completion. All other resistors are metal film components with a tolerance of 1 percent and a temperature coefficient of 100 ppm/°C. Various jumper shunts configure the board to accommodate a variety of gage wiring configurations. The circuit schematic (fig. 2) shows the electrical details of the design.

Input and output signal connections to the card are made using two connectors, J1 and J2. The J1 jack connects the signal-conditioning card to the strain gage through overvoltage protection (OVP) circuitry. The J2 jack connects the card to the system power supply, output indicator (a data amplifier with low-level multiplexed inputs connected to a 12-bit analog-to-digital converter), and calibration control functions. Card connector pin numbers, which are numbered consecutively from J1 pins to J2 pins, remain the same as in the DACS II design.

### Current Regulator

The current regulator comprises an LM10CN integrated reference amplifier and operational amplifier contained together in the U2 component. The set-point voltage, $V_{sp}$, provided to the constant current regulator is the desired gage voltage. The regulator reference $V_{sp}$ is derived by amplifying the LM10CN internal reference of 0.20 V, ±0.01 V. The stability of the internal reference is 0.002 percent/°C. The gage and reference $V_{sp}$ command is developed at the junction of the R7 and R8 resistors. The level of this voltage is nominally

$$V_{sp} = 0.20(1 + R8/R13) \quad (1)$$

where R8 = 20,000 Ω and R13 is selected for the particular measurement application. The circuit arrangement results in

$$V_{ref} \approx V_{sp} \quad (2)$$

and

$$V_g \approx V_{sp} \quad (3)$$

The current regulator operates by delivering the appropriate output voltage at the U2 component pin 6 to cause the current flowing through the R12 reference resistor to result in a reference voltage, $V_{ref}$, approximately equal to the $V_{sp}$. This result is not exact because of observable and stable input offsets in the LM10CN operational amplifier. The R13 resistor sets the output voltage and is user selectable. The R13 resistor is installed on bifurcated solder posts for ease in changing. Once set, the $V_{sp}$ is extremely stable because it is controlled by the LM10CN reference. However, the actual $V_{ref}$ will vary because of the tolerance of the LM10CN reference. The gage voltage, $V_g$, will additionally vary because of any offset adjustment the user may make.

### Gage Resistance

The regulated constant current is connected to flow through one or more gages arranged in a series string. The series string also includes the R12 reference resistor, which is located on the circuit card. Any gage resistance in common use can be accommodated.

### Lead Wires

Ideally, two lead wires carry excitation current to the gage(s), and two additional lead wires sense the voltage

drop across the gage(s). Gage voltage–sense lines are connected as close as possible to the resistance of the gages, typically at the gage terminals. Some voltage-sense line duties may be shared when two gages are located sufficiently close to each other. This arrangement is practical when connecting to strain gage rosettes in order to reduce the total number of connecting wires required. The objective is to sense the $V_g$ drop across no more lead-wire resistance than is absolutely necessary. If there is a substantial wire distance between gages in a current loop, then separate sense lines are required.

A set of four lead wires is ideal for connecting a single gage to the current loop because the circuit is unaffected by random lead-wire resistance changes. However, three lead wires may be sufficient. In most practical situations, the resistances of typical lead wires vary almost identically with temperature. Any small difference in lead-wire resistance that may develop usually contributes no significant measurement error. When using four lead wires, the JP1 circuit board jumper pins 2 and 3 and JP3 circuit board jumper pins 2 and 3 are shunted on the signal-conditioning card. When using three lead wires, the JP1 circuit board jumper pins 1 and 2 and JP3 circuit board jumper pins 1 and 2 are shunted on the signal-conditioning card.

### Reference Resistor

The current, $I$, which is regulated, proceeds from the current regulator +I output through the wiring and gages in the current loop and returns through the R12 reference resistor, a particularly stable component selected to match the gage resistances in the loop. To achieve good measurement stability, the R12 reference resistor is the type used for Wheatstone bridge completion. The R12 resistor is installed on bifurcated solder posts for ease in changing.

The $V_{ref}$ across the R12 reference resistor is used for four purposes:

1. The $V_{ref}$ is compared with the $V_{sp}$ to regulate the loop current.

2. The $V_{ref}$ is used by the voltage-difference calculation circuit(s) to subtract "the $R_{ref}$ worth" of voltage drop caused by the excitation current from each $V_g$ in the loop.

3. The $V_{ref}$ is used to develop the additional calibration current that flows through the gages during a $\Delta I$ calibration.

4. The $V_{ref}$ provides an indication of excitation level to the DACS II excitation monitoring function.

### Voltage-Difference Calculation

The voltage-difference calculation circuit is accomplished by the U1 component, an INA114BG instrumentation amplifier integrated circuit. The U1 component operates at essentially unity gain, so it operates to reproduce the sensed $V_g$ between its output terminal, pin 6, and its reference terminal, pin 5. The reference terminal is tied to the more negative end of the R12 reference resistor. Therefore, the sum of voltages from the U1 component pin 6 to the positive end of the R12 reference resistor is equal to $V_g - V_{ref}$. When the same current flows through both the $R_{ref}$ and the $R_g$, the output voltage is essentially equal to the excitation current times the resistance difference between the initial strain gage resistance, $R$, and the $R_{ref}$ of the measurement channel. This result can be altered for operational convenience by using offset adjustments that vary the gage current, $I_g$, while holding the $V_{ref}$ constant.

When the $V_{ref}$ is less than 1 V, it is possible to operate U1 component pin 3, the inverting input terminal of the instrumentation amplifier, at a voltage too close to its negative supply. A resistor or light-emitting diode can be installed at the R9 resistor location to avoid this problem.

### Offset Adjustment

An offset adjustment is provided to set the desired initial output level of the data channel. This adjustment is derived from a voltage developed by the reference section of the U2 component at pin 1 that is approximately twice the level of $V_{sp}$. This voltage is connected to two offset adjustment potentiometers, R10 and R11. The output levels of the potentiometers track the current excitation level because they are all controlled by the same voltage reference source in the U2 component. A resistance voltage divider comprised of the R7, R8, and R13 resistors in the feedback path of the reference section of the LM10CN component develops the $V_{sp}$ for the regulator section of the U2 component.

The R10 potentiometer and the R4 limiting resistor serve as a "coarse" offset control. The R11 potentiometer and a large limiting resistor, R6, serve as a "fine" offset control. The R4 and R6 resistors act similar to the "balance limit" resistances in Wheatstone bridge circuits but cause no nonlinearity or loading in the current loop.

### Excitation Sensing

The DACS II measurement channels separately sense the excitation voltage applied to each Wheatstone bridge measurement channel. The equivalent information in a current loop channel is the $V_{ref}$, measured across the R12 resistor.

The input resistance of the DACS II excitation-sensing circuitry is approximately 50,000 Ω, an unacceptably large load on the current loop. The U3 buffer amplifier, an LM308AN, is used to isolate the load of the excitation-sensing circuitry from the current loop.

### Channel Outputs

The end result of the voltage-difference calculation is a differential channel output voltage observed from the U1 component pin 6 (+) to the $+V_{ref}$ (–). This output voltage is directly proportional to any resistance change, $\Delta R$, in the gage. In a practical application, the initial differential-output voltage (as with a Wheatstone bridge) will not be exactly 0 V, but may be made acceptably small by adjusting the coarse and fine offset adjustments (the R10 and R11 resistors, respectively). Adjusting these offset controls causes the effective value of the $R_{ref}$, the R12 resistor, to approach the $R$ or some other value that achieves the desired initial conditions.

### Presampling Output Filter

The R2, R3, C1, and JP4 components configure the circuit card for one or more gages in the current loop. When only one gage is in the current loop, the resistor-capacitor filter network in the DACS II OVP circuitry is included as a part of the presampling filter for the DACS II sampled data system input. When more than one gage is in the current loop, signal-conditioning cards are configured to be master channels that provide all excitation, calibration, and reference functions or as slave channels that provide only voltage subtraction and reference buffering functions. The +OUT line of the master channel provides the $-V_{ref}$ to the other channels in the same current loop through the connection of JP4 circuit board jumper pins 2 and 3. This connection makes the DACS II OVP card filter components unavailable to the master channel. The R2, R3, and C1 components provide the filter stage that would otherwise be included on the DACS II OVP card. The master and slave channel circuit options are discussed in the "Transducer Connection Examples" section.

## DATA CALIBRATION

Data may be observed and recorded to establish the sensitivity and validate the performance of the DACS II measurements by activating the shunt calibration and output short features designed into the current-loop evaluation board. Excitation defeat is not available because the DACS II system Wheatstone bridge excitation is used to power the amplifier components on the DACS II current loop card. The card electronics simply quit operating when the excitation is turned off by the DACS II excitation defeat function.

### Calibration

System calibration is accomplished by connecting the R14 resistor, which provides the calibration resistance, $R_{cal}$, to parallel either the $R_{ref}$ (the R12 resistor) or a remote gage resistance. The JP2 and JP5 circuit board jumpers are provided to make this circuit choice.

### Resistance Change Calibration

When the JP2 circuit board jumper pins 2 and 3 and JP5 circuit board jumper pins 2 and 3 are selected, activating the shunt calibration relay parallels a remote gage resistance with the R14 calibration resistor. The engineering unit, $EU_{cal}$, worth of strain, simulated by activating the shunt calibration relay is given by

$$EU_{cal} = [R\,(10^6)] \,/\, [(R + R_{cal})(GF)]\ \mu in/in \qquad (4)$$

where gage factor, GF, is the effective channel gage factor; $R$ is the gage resistance shunted; and $R_{cal}$ is the value of R14. In three-wire circuits, $R$ and a lead-wire resistance is shunted by the $R_{cal}$. Lead-wire resistance may not be accurately known. For this reason, a $\Delta R$ calibration is not normally recommended.

### Current Change Calibration

When the JP2 circuit board jumper pins 1 and 2 and JP5 circuit board jumper pins 1 and 2 are selected, activating the shunt calibration relay parallels the effective $R_{ref}$ (the R12 resistor ± any apparent change caused by an offset adjustment, discussed later) with the R14 shunt calibration resistor. The resulting increase in $I_g$ during calibration is

$$\Delta I_{cal} = V_{ref} / R_{cal} \quad (5)$$

The $V_g$ of each gage in a multigage current loop is increased by

$$\Delta V_{cal} = \Delta I_{cal} R \quad (6)$$

and appears in the output of the channel(s) as though a strain had been felt in the gage(s). The calibration output can be interpreted as strain, $\Delta R$, or whatever physical quantity is being sensed by the gage. When using a 350 Ω strain gage, a 50,000 Ω resistor is used for the $R_{cal}$ (R14). For a 120 Ω strain gage channel, a 20,000 Ω resistor is used for the $R_{cal}$.

The $EU_{cal}$ worth of strain simulated by activating the shunt calibration relay when using a $\Delta I$ calibration circuit is given by

$$EU_{cal} = R_{ref}(10^6) / R_{cal}(GF)\ \mu in/in \quad (7)$$

where GF is the effective channel gage factor, $R_{ref}$ is the apparent reference resistance being shunted, and $R_{cal}$ is the value of the R14 resistor. As discussed later, the actual resistance value installed at R12 is not necessarily the appropriate value to be used as $R_{ref}$ in eq. (7) for calculating the $EU_{cal}$ worth of a DACS II calibration to use as the $EU_{cal}$ value of the channel.

NOTE: *This $EU_{cal}$ value does not depend on R.* The $\Delta I$ calibration technique identifies ΔR/R, not merely $\Delta R$. This result is a unique feature of using a $\Delta I$ calibration with current-loop signal conditioning.

### Apparent Reference Resistance With Current Change Offset Adjustment

The DACS II current-loop signal-conditioning card achieves offset adjustment by causing the $I_g$ (and therefore the $V_g$) to vary while holding the $V_{ref}$ constant. This simple and reliable circuit is electrically equivalent to varying the R12 resistor but does not require a stable and variable low resistance component in the circuit.

The actual $R$ is often so close to the apparent value of the R12 resistor that the $R_{ref}$ can be taken as the R12 resistor without significant error in establishing the appropriate $EU_{cal}$ value. However, if a large offset exists, then it is likely that the value of the R12 resistor should *not* be used as the $R_{ref}$ value. An "apparent" reference resistance, $R_{ref_a}$, is defined as the reference resistance value that, if it were installed as $R_{ref}$ without offset circuitry, would yield the same output offset as is actually being observed:

$$R_{ref_a} = V_{ref} / I_g \quad (8)$$

where the $I_g$ is the actual gage current with offset applied. The $R_{ref_a}$ can be estimated by

$$R_{ref_a} = R / (1 + V_o / V_{ref}) \quad (9)$$

where $V_o$ is the offset voltage observed by the measurement system when the shunt calibration is going to be applied. If measuring the gage resistance is inconvenient, then $R_{ref_a}$ can be estimated by

$$R_{ref_a} = R_{cal}\, \Delta V_{cal} / [V_{ref}(1 + V_o / V_{ref})] \quad (10)$$

where $\Delta V_{cal}$ is the change in output that results from paralleling $R_{ref}$ with $R_{cal}$.

### Sense Line Connections

Gage voltage–sense lines that monitor the voltage drops across the various gages in a current loop must be connected as closely as possible to the terminals of the gages. System insensitivity to lead-wire resistance variations depends on sensing only the voltage drop across the gages without including the voltage drop across interconnecting lead wires. Sharing sense lines between gages to reduce the total wire count is only practical when gages are so physically close that essentially no lead-wire resistance appears between gages. This close proximity is the case for most strain-gage rosette installations.

### Printed Circuit Layout

The sense-line concept is also used in the printed circuit layout to observe the $V_{ref}$ across the $R_{ref}$. This circuit arrangement is made to minimize the influence of any loop current flowing through printed circuit traces on the voltage drop sensed as $V_{ref}$.

The printed circuit layout includes a guard plane consisting of all otherwise unused copper on the component side of the card. This ground plane is arranged to carry no current and is connected at one point to the system analog common through J2 circuit board jack pin 18.

### Three- and Four-Wire Circuits

Three-wire current loop circuits have all the advantages of four-wire circuits with one important exception. Although four-wire current loop circuits cause lead-wire resistance variations to be irrelevant, three-wire current loop circuits compensate for lead-wire resistance variations only when lead-wire resistances vary identically.

The standard practice of using three-wire connection of gages to Wheatstone bridge circuits depends on identical wire resistance variations to compensate for zero shifts that would occur if only two wires were used to connect a gage. Unlike the Wheatstone bridge, current-loop signal conditioning does not change sensitivity when lead-wire resistance changes.

### Excitation Level

The LM10CN component that regulates the loop current can deliver up to 20 mA of $I_g$ at approximately the same voltage powering the LM10CN. It is important to ensure the regulator remains within compliance. Regulator overload can occur when the voltage drop across the sum of all loop resistances (gages, wires, and $R_{ref}$) approaches the available power supply voltage (typically 10 V direct current).

The DACS II includes an excitation measurement channel for each gage channel. The current-loop signal-conditioning card uses this "sense" channel to monitor the voltage drop across the R12 reference resistor through the U3 buffer amplifier. The current regulator is operating satisfactorily as long as the sense channel observes the expected voltage drop across the $R_{ref}$ (the R12 resistor). The sense channel indication is equal to the $V_{ref}$ for both three- and four-wire gage circuits.

## TRANSDUCER CONNECTION EXAMPLES

The DACS II current-loop signal-conditioning card will support a variety of transducer configurations. The circuit card can be configured for three- or four-wire gage connections. More than one gage may be included in the current loop. For multigage current loops, the quantity of lead wires required is three plus the number of gages in the circuit.

Figure 3 shows the functional schematic of the DACS II current-loop signal-conditioning card and connection examples for four-wire gage connections. Figure 4 shows the same for three-wire gage connections. The connection drawings for each configuration illustrate the essence of the current loop circuit: the signals carried to and from the card, the wiring for cables and connectors, and the placement of jumper shunts.

Multigage current-loop measurements have been demonstrated on the DACS II but have not yet been used in test operations. Figure 5 shows connection of a three-gage rosette to the DACS II. Channel 3 serves as the "master" channel in this example by providing excitation, hosting $R_{ref}$, and accomplishing $\Delta I$ calibration. "Slave" channels 1 and 2 accomplish only voltage-difference measurement and excitation-sense functions and depend on the "master" channel to provide all other functions.

## USER EXPERIENCE

The FLL technicians report the current-loop signal-conditioning card output to be quiet and, after warmup, stable. The technicians especially appreciate the separate coarse and fine offset adjustability that eliminates trips back to the bench to solder in different balance-limit resistors. The strain gage channels were particularly easy to install and set up (after making the necessary cable pin assignment changes). A channel validity check was performed by replacing a strain gage and its connecting cable with a decade resistance box. The results showed the channel balanced with a setting within 0.01 Ω of the measured $R_g$. Wheatstone bridge channel validity check results are

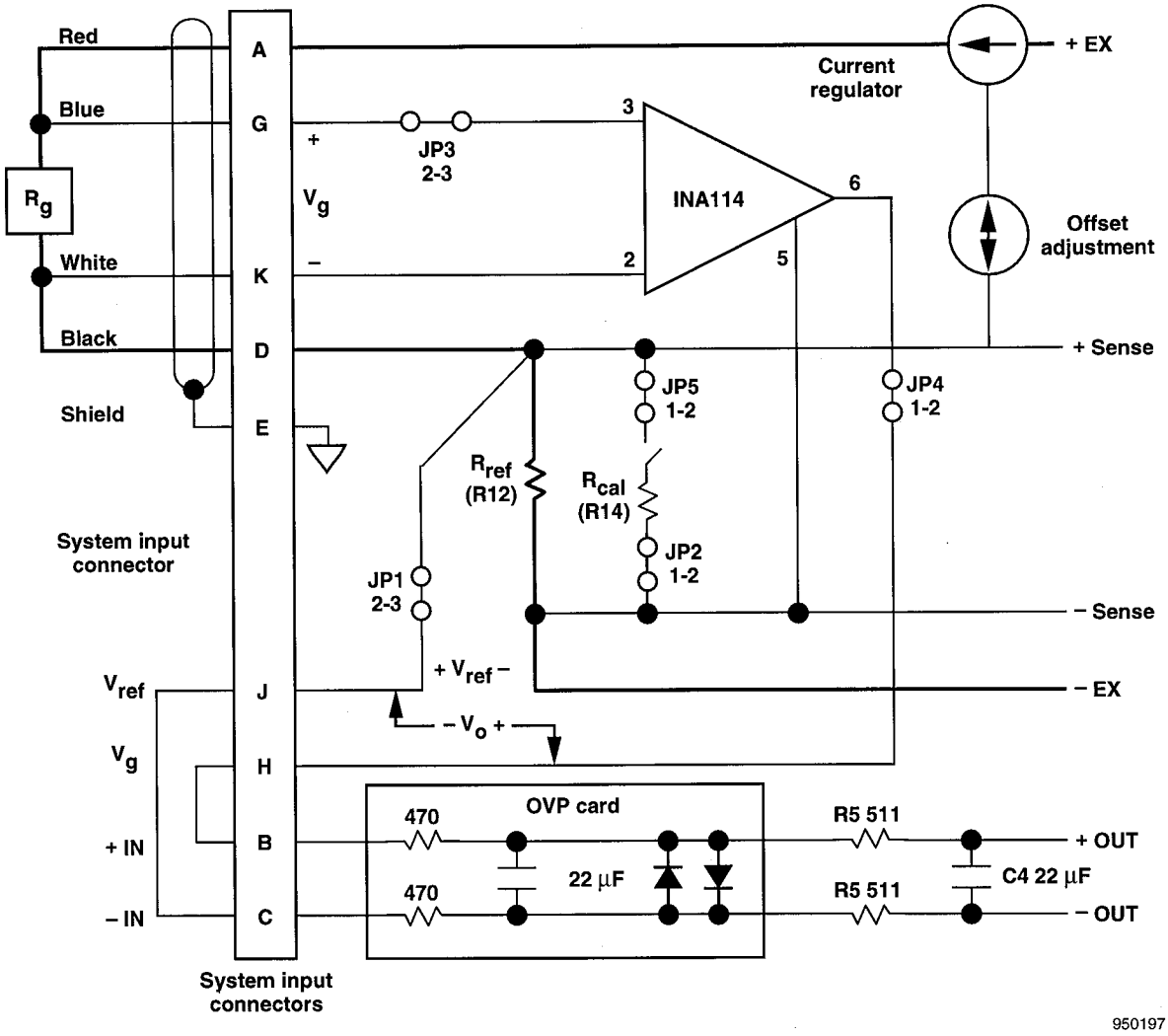


Figure 3. Four-wire gage connections.

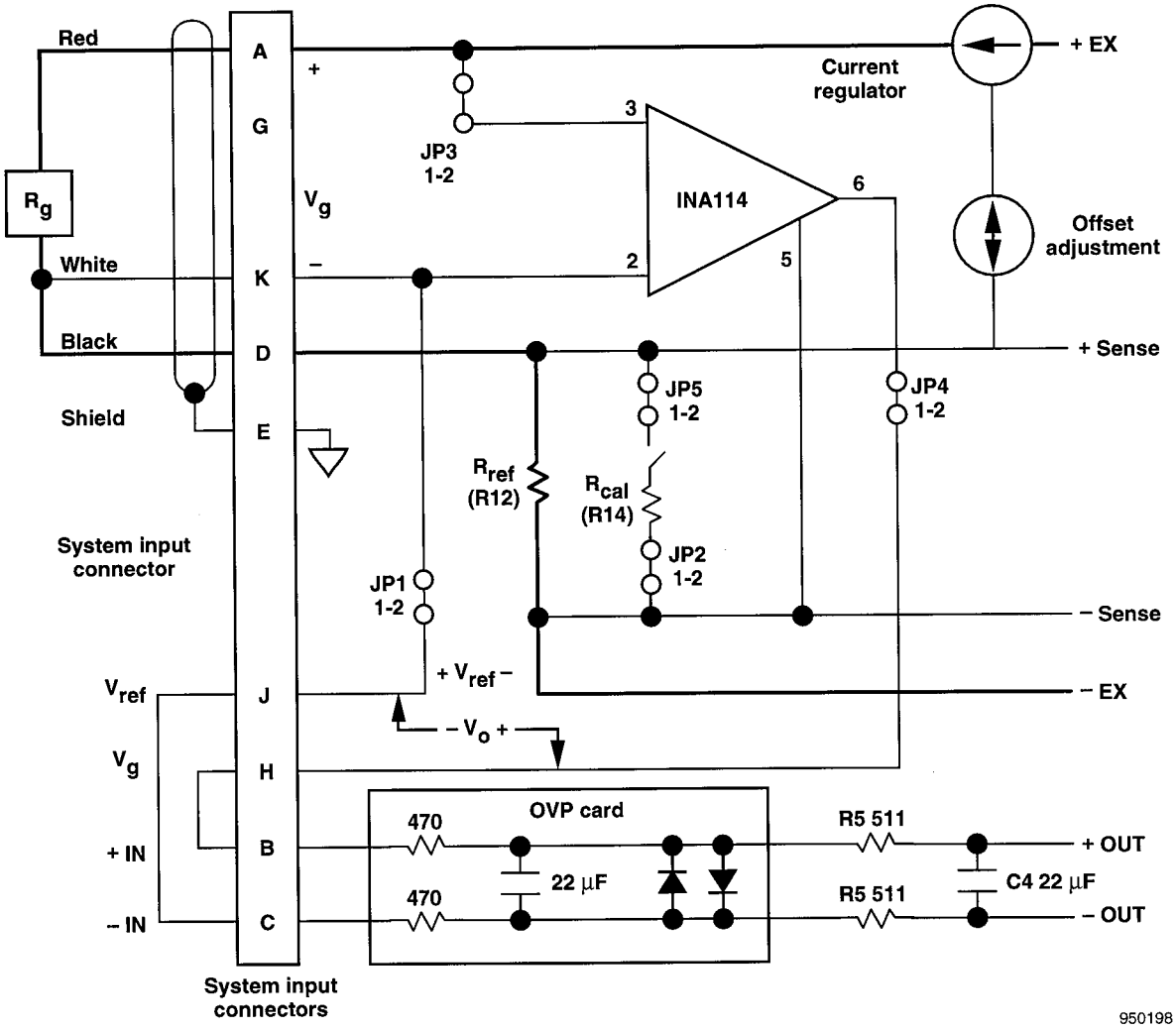


Figure 4. Three-wire gage connections.

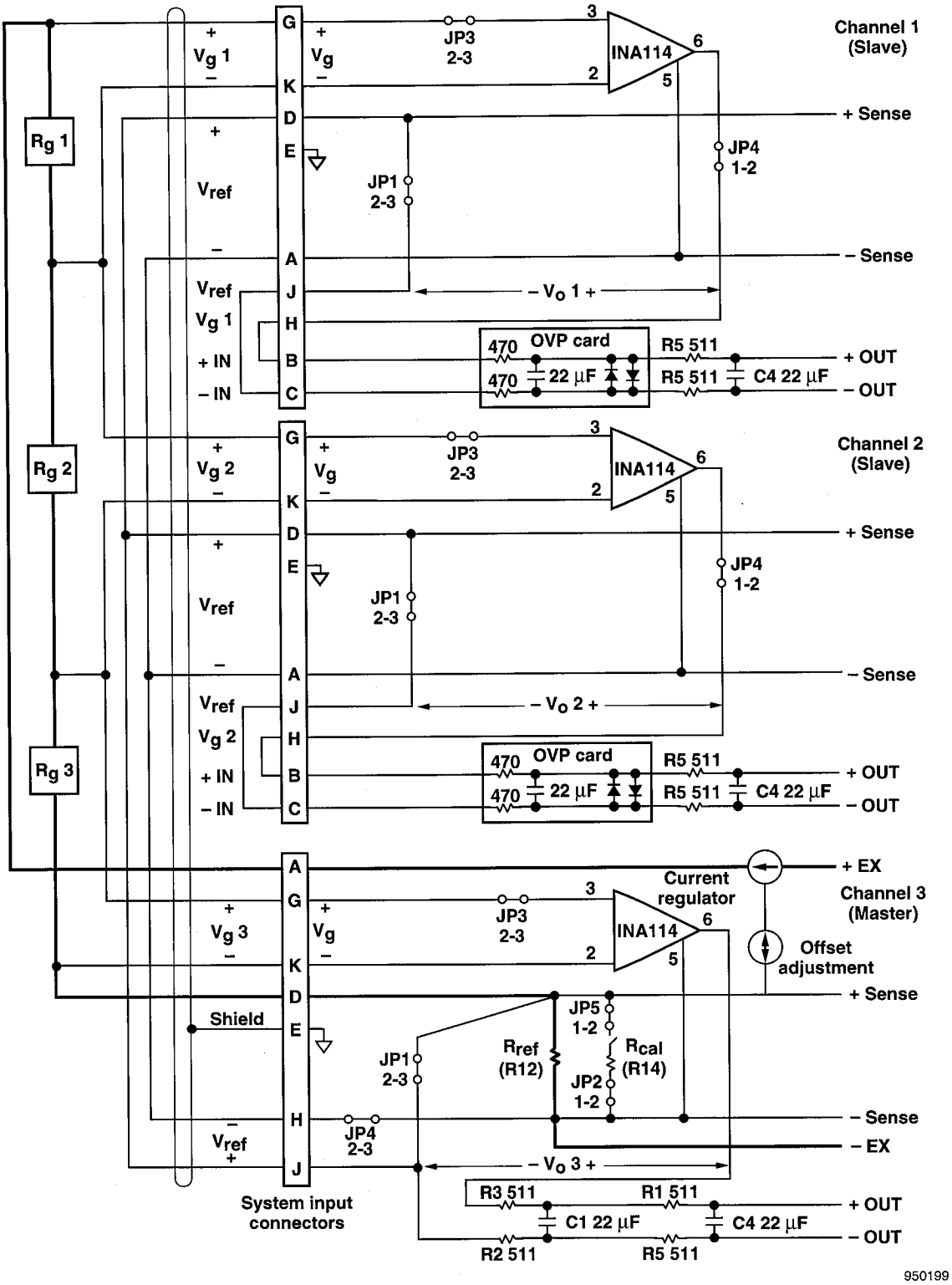


Figure 5. Three-gage rosette current-loop wiring.

typically not this close because of the influence of inner-bridge wiring resistance.

The FLL test engineers report that current loop data are more quiet than those obtained from comparable Wheatstone bridge strain-measurement channels. This quietness happens because channel outputs are double what a Wheatstone bridge delivers for the same gage power dissipation, although the electrical noise floor remains essentially the same. Otherwise, the presence of current-loop signal conditioning instead of Wheatstone bridge circuitry is transparent to the user until the need to remove systematic errors caused by signal-conditioning circuitry from data after a test arises. The current loop data require no measurements or assumptions to correct for lead-wire resistance desensitization of the measurement channel. Also, no corrections are needed to deal with any inherent circuit nonlinearities like those found with Wheatstone bridge circuits.

## LESSONS LEARNED

Experience with over 350 operational current-loop measurement channels has now been gained. Based on this experience, some design choices would be made differently today. A power-off zero activated by some presently unused calibration relay contacts would be included, and $\Delta V$ offset circuitry would be used in place of $\Delta I$ offset circuitry.

The power-off zero is a key troubleshooting and measurement validation tool. A means was developed, after the DACS II circuit was produced, to include this function while operating the amplifier components within their common mode voltage limits.

The $\Delta V$ offset circuitry would be chosen to avoid the need to determine the $R_{ref_a}$ value as the overall channel sensitivity to $\Delta R/R$ is established. The first test operation using current-loop signal conditioning required the initial offset to be set at approximately +60 mV. This setting allows apparent strain to pull the output indication to approximately 0 mV, where the DACS II offers the greatest measurement resolution. This technique gave the best strain data resolution at the elevated temperature where mechanical loads were applied to the test article. But the technique also required identifying a separate value of the $R_{ref_a}$ for each channel that would not have been necessary with the $\Delta V$ offset circuitry.

## CONCLUSIONS

Current loop circuitry was included in a system originally designed for Wheatstone bridge circuitry. No internal system hardware or software changes were required other than the design of a plug-on signal-conditioning card to replace the original Wheatstone bridge completion and calibration circuit board. The resulting test data from over 350 operational channels in two different test programs had a lower noise level than data from Wheatstone bridge circuitry, were linear with respect to gage resistance change, and were uninfluenced by the presence of lead-wire resistance. The current loop channels were easier for the technicians to set up, verify, and operate than equivalent Wheatstone bridge channels.

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# REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188



| 1. AGENCY USE ONLY (Leave blank) | 2. REPORT DATE | 3. REPORT TYPE AND DATES COVERED |
|---|---|---|
| | April 1995 | Technical Memorandum |

**4. TITLE AND SUBTITLE**

A Conversion of Wheatstone Bridge to Current-Loop Signal Conditioning for Strain Gages

**5. FUNDING NUMBERS**

WU 505-70-XX

**6. AUTHOR(S)**

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**7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)**

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**8. PERFORMING ORGANIZATION REPORT NUMBER**

H-2049

**9. SPONSORING/MONOTORING AGENCY NAME(S) AND ADDRESS(ES)**

National Aeronautics and Space Administration
Washington, DC 20546-0001

**10. SPONSORING/MONITORING AGENCY REPORT NUMBER**

NASA TM-104309

**11. SUPPLEMENTARY NOTES**

Presented at the SEM Western Regional Strain Gage Committee Conference in El Segundo, California Feb. 7–8, 1995.

**12a. DISTRIBUTION/AVAILABILITY STATEMENT**

Unclassified—Unlimited
Subject Category 33

**12b. DISTRIBUTION CODE**

**13. ABSTRACT (Maximum 200 words)**

Current loop circuitry replaced Wheatstone bridge circuitry to signal-condition strain gage transducers in more than 350 data channels for two different test programs at NASA Dryden Flight Research Center. The uncorrected test data from current loop circuitry had a lower noise level than data from comparable Wheatstone bridge circuitry, were linear with respect to gage-resistance change, and were uninfluenced by varying lead-wire resistance. The current loop channels were easier for the technicians to set up, verify, and operate than equivalent Wheatstone bridge channels. Design choices and circuit details are presented in this paper in addition to operational experience.

**14. SUBJECT TERMS**

Bridge circuits; Circuit theory; Electrical engineering; Electronic circuits; Electronic test equipment; Electronics; Gages; Instrumentation; Measuring instruments; Remote sensors; Resistance temperature detectors; Resistors; Sensors; Strain gage instruments; Structural testing; Test facility instruments; Testing of materials; Transducers

**15. NUMBER OF PAGES**
13

**16. PRICE CODE**
AO3

| 17. SECURITY CLASSIFICATION OF REPORT | 18. SECURITY CLASSIFICATION OF THIS PAGE | 19. SECURITY CLASSIFICATION OF ABSTRACT | 20. LIMITATION OF ABSTRACT |
|---|---|---|---|
| Unclassified | Unclassified | Unclassified | Unlimited |