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Electrical Impact of SiC Structural Crystal Defects on High Electric Field Devices

Philip G. Neudeck
Glenn Research Center, Cleveland, Ohio

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Philip G. Neudeck
National Aeronautics and Space Administration
Glenn Research Center
21000 Brookpark Road, M.S. 77-1
Cleveland, OH 44135 USA

Abstract: Commercial epilayers are known to contain a variety of crystallographic imperfections, including micropipes, closed core screw dislocations, low-angle boundaries, basal plane dislocations, heteropolytypic inclusions, and non-ideal surface features like step bunching and pits. This paper reviews the limited present understanding of the operational impact of various crystal defects on SiC electrical devices. Aside from micropipes and triangular inclusions whose densities have been shrinking towards manageably small values in recent years, many of these defects appear to have little adverse operational and/or yield impact on SiC-based sensors, high-frequency RF, and signal conditioning electronics. However high-power switching devices used in power management and distribution circuits have historically (in silicon experience) demanded the highest material quality for prolonged safe operation, and are thus more susceptible to operational reliability problems that arise from electrical property nonuniformities likely to occur at extended crystal defects. A particular emphasis is placed on the impact of closed-core screw dislocations on high-power switching devices, because these difficult to observe defects are present in densities of thousands per cm^2 in commercial SiC epilayers, and their reduction to acceptable levels seems the most problematic at the present time.

Introduction: As illustrated by the invited paper of Dudley [1] at this conference, SiC wafers and epilayers contain a variety of crystallographic structural imperfections. The degree to which each kind of crystal defect impacts a given device is quite application-specific, strongly dependent on a combination of both the electrical operating requirements and the physical layout of each particular SiC device structure. Almost all useful semiconductor electronic devices require rectifying junctions in order to function properly. The fundamental properties of transistors (i.e., gain, voltage and current ratings, operating speeds, etc.), be they unipolar (MESFET, JFET, MOSFET, etc.), bipolar (BJT, Thyristor, GTO, etc.), or hybrid (IGBT, etc.) depend largely on the fundamental conduction and/or blocking characteristics of Schottky and/or pn junctions within the transistor device structure. Therefore, the primary failure mode addressed in this work is the loss or degradation of 2-terminal junction rectifying characteristics, particularly at high electric fields (on the order of megavolts per cm) where SiC is expected to operate with the largest benefits over conventional silicon and GaAs electronics in high-power applications. Only commercially available slightly-off (0001) wafer orientations are considered, as other potential wafer orientations have not yielded advantageous high-field device results to date. While not addressed in this paper, there are likely to be other application-specific consequences of crystal imperfections beyond degradation of junction rectifying properties.

Crystal Defects: Most envisioned SiC devices are fabricated so that their electrically active regions reside entirely within homoepilayers grown on top of mass-produced 6H- and 4H-SiC wafers cut and polished a few degrees off the (0001) crystallographic surface. Therefore, the defects contained in these epilayers are of greatest interest to electrical device and circuit manufacturers. Figure 1 schematically depicts some of the SiC epilayer defects that could impact electrical device performance, including micropipes, closed-core screw dislocations, small growth pits, and triangular inclusions. Other defects not pictured in Figure 1 include basal plane dislocations, edge dislocations, low-angle boundaries, and carrot and comet-tail defects [2-4]. It is important to note that the vast network of basal plane dislocation loops found in the commercial PVT-grown bulk wafers are not found in subsequently grown epilayers [5], so that homoepitaxial 6H and 4H devices automatically contain significantly fewer crystal defects than similar devices fabricated directly in bulk wafers.

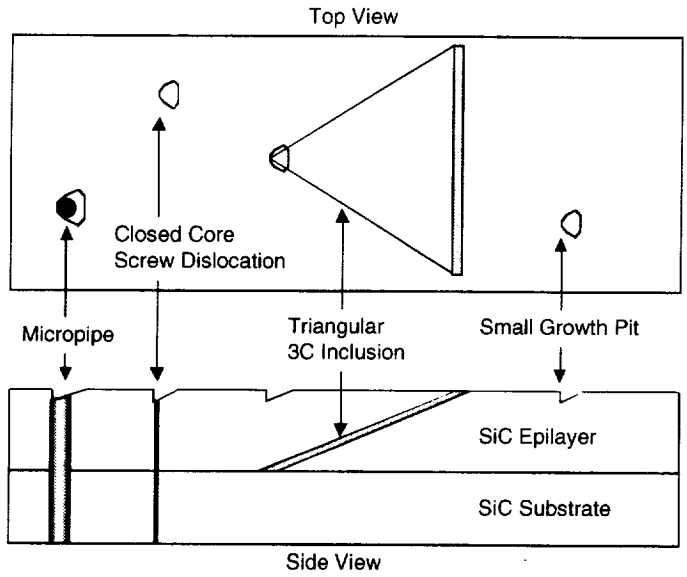

Figure 1: Some common SiC epilayer defects that impact high-field device properties.

The density of each specific defect determines the size and numerical yield of devices that hit or miss each defect. It is also important to consider the root causes of each defect and whether or not certain kinds of defects will be greatly reduced in density in the near future as crystal growth processes improve. The reported densities of some of the various defects in commercial epilayers are summarized in the first two columns of Table I.

Epitaxial Growth Defects: SiC Schottky-based rectifiers offer large benefits to high-power systems because their unipolar conduction enables much faster high-voltage switching that will enable shrinking of power system passives as well as increased power converter efficiency. The quality and smoothness of the semiconductor surface is well-known to critically control the electrical properties of rectifying Schottky diode junctions, especially since peak electric fields occur near the metal-semiconductor interface while current is exponentially controlled by the metal-semiconductor potential barrier [6]. The presence of non-smooth surface features routinely observed by atomic force microscopy on SiC epilayer surfaces could perturb the local electric field and thermionic carrier emission properties, which could result in locally increased current under both forward and reverse. Previous works have forcefully argued that SiC Schottky diode I-V properties are controlled by small localized surface defects that have a lower effective Schottky barrier height [7-9]. However, conclusive links between specific types of SiC surface defects and specific non-ideal Schottky I-V properties remain to be experimentally proven.

It is plausible that pn junction devices are perhaps less-affected by SiC surface defects, primarily due to the fact that the peak electric field and current conduction mechanisms (primarily recombination) occur at the metallurgical junction buried within the semiconductor. However, pn junction forward and/or reverse characteristics can be expected to track with surface imperfections in those cases where the surface defect arises due to an extended defect that actually runs through the thickness of the epilayer to intersect the metallurgical pn junction. Such behavior has been observed by Kimoto for 3C triangular inclusions, which were found to greatly increase leakage

Table 1: Selected Properties of SiC Epilayer Extended Structural Defects in High-Field Devices

SiC Epilayer Defect [References]	Density (#/cm^2)	Observed Defect Sources	Observed Impact on High-Field Junction	Summary Comments (see text)
Micropipe Hollow Core Screw Dislocation [1, 4, 11, 13]	< 30 (commercial) < 1 (best)	Substrate micropipes that propagate into epilayer.	> 50% breakdown voltage reduction. Microplasmas. Increased leakage currents.	Densities improving to where they may not be present in most ~ 1 cm^2 power devices in a few years.
Closed Core Screw Dislocation [1, 10, 14-16, 18]	~ 3000 to ~ 10000	Substrate screw dislocations that propagate into epilayer.	~10-30 % breakdown voltage reduction. Softened breakdown Microplasmas. Carrier lifetime reduction.	**Densities slowly improving, but will be present and affect ~ 1 cm^2 sized power devices for many years .**
Triangular 3C Inclusions [2-4, 10]	< 5	Wafer preparation and epitaxial growth process.	> 50% breakdown voltage reduction. Increased leakage currents.	Densities improving to where they may not be present in most ~ 1 cm^2 power devices in a few years.
Carrots & Comet Tails [2-4]	< 5	Undetermined.	Some increase in pn junction leakage. Non-smooth surface seems likely to impact Schottky rectifying properties.	Densities improving to where these may not be present in most ~ 1 cm^2 power devices in a few years.
Small Growth Pits [2, 3, 9, 18]	> 3000	Closed core screw dislocations. Wafer preparation and epitaxial growth.	Non-smooth surface seems likely to impact Schottky rectifying properties.	Densities improving, but closed-core screw dislocation density may represent a limiting floor for these defects.

current and decrease breakdown voltage for kV-class epitaxial pn junction diodes [3]. Kimoto also observed an increase in reverse leakage current due to carrot/comet tail defects.

The X-ray studies of Si et al. [10] found no evidence that epilayer triangular inclusions nucleated at substrate screw dislocations. Powell et al. [2] demonstrated that many morphological imperfections in the as-grown SiC epilayer surface are greatly impacted by surface polish as well as epitaxial growth initiation process. Off-axis polish angle has been increased to successfully reduce 3C triangular inclusions in 4H-SiC epilayers [10]. Thus, while by no means trivial, it appears that defects arising from pre-epitaxial and epitaxial growth processing should become less important as these processes are optimized. Since present-day densities of triangular inclusions and carrot/comet tail defects are already less than 5 per cm^2 in commercial epiwafers [4], it appears that ~1 cm^2 power devices free of these particular defects could be manufacturable within a few years.

Micropipes (Hollow Core Screw Dislocations): SiC screw dislocations are well-known to originate in commercial 6H- and 4H-SiC wafers and propagate parallel to the crystallographic c-axis through the entire thickness of standard homoepilayers grown by CVD. As discussed by Dudley [1], screw dislocations with large Burgers vectors form hollow cores and are thus referred to as tubular voids or micropipes. Micropipes are well documented to cause premature reverse failure in high-field SiC devices [3,11,12]. However, SiC electronics designed to operate all internal device junctions at relatively low electric fields are least affected by crystal defects. SiC pn junction

diodes, FET's and integrated circuits have all demonstrated an ability to function despite the presence of micropipes running through key rectifying junctions as long as junction fields are kept to a small percentage of the theoretical SiC breakdown field. Steady improvements in SiC wafer quality has reduced SiC wafer micropipe densities from several hundreds per cm^2 in 1993 to less than 1 per cm^2 in 1998 in the best reported wafers [13], so that micropipe-free power devices on the order of 1 cm^2 area rated for 100's of amps on-state current would become feasible in the near term if other non-micropipe defects turn out to be harmless or are eliminated.

Closed Core Screw Dislocations: When the Burgers vector of an SiC screw dislocation is small enough, hollow core formation is avoided [1,14]. Nevertheless, the closed core screw dislocation possesses many properties similar to micropipes, starting with a propensity to undesirably propagate through bulk crystals and epilayers [1,5,15,16]. These defects are present in average densities on the order of several thousands (best) to around ten thousand per cm^2 in commercial wafers [1]. Because they have not declined in density over time as fast as micropipes, it would appear that all devices manufactured on mass-produced wafers whose active areas exceed ~1 mm^2 will contain these defects for the forseeable future.

While not as detrimental to device characteristics as micropipes, experimental evidence is emerging that closed core screw dislocations somewhat negatively impact the electrical properties of high-field SiC junctions. Much of the evidence is indirect largely because screw dislocations cannot be observed by conventional microscopic methods, and must instead be non-destructively observed in devices by X-ray topographic mapping. Unfortunately, few SiC device studies have sufficiently tracked device performance as a function of closed core screw dislocations. One study that did use X-ray topography to map closed core screw dislocations demonstrated that elementary screw dislocations are somewhat detrimental to the reverse leakage and breakdown properties of low-voltage (< 250 V) 4H-SiC p^+n diodes [15,16]. Examples of remarkably similar observations of increased reverse leakage, soft breakdown, and/or microplasmas not associated with micropipes are independently reported in the literature [12,17], even though none of these works carried out X-ray mapping to conclusively ascertain the presence of screw dislocations within their devices. The impact of closed core screw dislocations on higher voltage (> 1 kV) junctions and bipolar gain devices remains to be ascertained, as do physical mechanisms and models for the exact electrical behavior of these dislocations.

The work of Schnabel et al. reported at this conference [18], in which a combination of Electron Beam Induced Current (EBIC) measurements were correlated with X-ray screw dislocation mapping and surface growth pit mapping, reveals two important observations regarding screw dislocations in SiC. First, all closed core screw dislocations mapped by X-ray were found to have clear EBIC signatures indicating a local reduction in the minority carrier lifetime in the immediate vicinity of the defect. This observation experimentally confirms previous suggestions that closed core screw dislocations were responsible for some (but clearly not all) of the defects observed in earlier SiC Schottky EBIC studies [7,8]. This also re-raises the possibility that closed core screw dislocations were responsible for destructive Schottky diode failure and localized negative temperature coefficient of breakdown observed in [8], which are clearly undesirable properties for high-power rectifier usefulness and reliability. The second important finding of [18] is that all closed core screw dislocations mapped by X-ray resulted in a corresponding small growth pit on the as-grown epilayer. This suggests that epilayer process improvements may not be able to reduce small growth pit densities below bulk wafer screw dislocation densities.

It is worth noting that some non-conventional epitaxial growth techniques have been attempted to prevent the propagation of micropipes and screw dislocations through SiC epilayers [19,20]. While these approaches seem to physically close and cover up micropipes, there has been little demonstrated performance improvement in high-field devices fabricated in the resulting material

prior to this conference. Further studies into alternative growth approaches that reduce epilayer screw dislocations seem warranted, but proof of feasibility must be demonstrated by greatly improved large-area high-field SiC diode performance.

High Power Devices and Circuits: As pointed out by Fazi et al. [21], crystal defects are clearly much more harmful to devices that operate junctions at high electric fields (i.e., power devices), especially when the crystal defects perpendicularly cross the high-field metallurgical junction boundaries as is the case with screw dislocations on commercial SiC epiwafers. Steady reductions in SiC micropipe densities have enabled initial prototype DC demonstrations of high current SiC diodes in the neighborhood of 100 A. It is important to note, however, that most high-current SiC power devices reported to date are significantly derated, in that the experimentally demonstrated blocking voltages are usually significantly less than the theoretical blocking voltages calculated from epilayer doping and thickness. Similarly, the highest reported blocking voltage SiC devices (> 7 kV) have to date been very small-area (~10^{-4} cm^2, small enough to be free of closed core screw dislocations) with low on-state current rating well under 1 A. If micropipes are the only defect limiting SiC high power devices, much better experimental results combining optimum (i.e., near theoretical) high voltage and high current in a single large-area device should be obtainable.

Independent studies of micropipe-free pn high-voltage rectifiers have documented a clear trend that yield and standoff voltage decrease significantly as device area increases beyond ~5 x 10^{-4} cm^2 on any given SiC diode wafer [3,22,23]. Depending upon selection of specific yield criteria (i.e., the reverse voltage and leakage current used to define a "good" device), the defect densities extracted from these studies are on the order of thousands per cm^2. While these extracted densities are more consistent with close core screw dislocation and small growth pit densities than other known SiC defects, additional evidence that links specific defects to device degradation is clearly needed.

While SiC devices promise some of the largest operational benefits to electric power conversion and motor-drive systems, these circuits also impose the harshest operational stresses on semiconductor switches. Solid-state devices in modern day power conversion circuits are often subjected to demanding overvoltage, overcurrent, dI/dt, and/or dV/dt stresses not found in other applications, which they must withstand without damage or degradation in order for the system to function reliably. Thus, it is possible that non-micropipe SiC crystal defects, which appear relatively benign when subjected to conventional DC characterization methods and used in less-demanding applications, could cause device/system failure when operated in demanding high-power circuits, as historically is the case with silicon-based power devices whose design specifications today are still governed by safe operating area (SOA) reliability considerations. In silicon power electronics experience, undesired nonuniformities in semiconductor properties across the high field region of a power device (sometimes caused by crystal dislocation defects and/or undesired impurity clusters) have historically led to reliability problems (i.e., reduced SOA) in demanding high-power systems, with higher voltage devices being most susceptible to failure [24].

SiC has strong material property advantages that should make it inherently more durable to electrothermal stresses that govern SOA than silicon, such as higher thermal conductivity, higher melting temperature, lower impurity diffusion, etc. It is therefore quite possible that SiC-based high power devices may be able to much-better tolerate the presence of localized currents and crystal defects than silicon power devices. Previous works indicate this is the case for properly fabricated SiC pn junction diodes with voltage ratings of less than 600 V [25-27]. When subjected to reverse-breakdown avalanche energy testing, no significant difference was noted between devices with and without closed-core screw dislocations, apparently due to the fact that space-charge effects restrict the breakdown power density and temperatures at the dislocation-related microplasmas [27]. As of this writing, however, no high power SiC rectifier (V_R > 1 kV, I_{ON} > 10 A) has demonstrated reverse

avalanche breakdown energy ratings (normalized to device anode area) significantly (> 2X) above silicon, even though most SiC rectifiers are expected operate in circuits at much higher (> 2X) power densities than silicon. Most experimental observations of poor SiC breakdown energy appear attributable to edge-related breakdown and other non-optimum device processing issues. However, because microplasma power density and thermal stresses could increase with device blocking voltage, closed core screw dislocations presently cannot be ruled out as a possible cause of low avalanche energy in larger-area kV-class SiC rectifiers. Clearly, more work to better understand the electrophysical properties and SOA ramifications of closed core screw dislocations is warranted.

Conclusion: Because present-day commercial SiC wafers and epilayers contain plenty of non-micropipe crystal defects in densities as high as thousands per cm^2, virtually all multi-amp SiC high voltage devices manufactured in the near term seem guaranteed to contain electrical nonuniformities that could potentially impact SiC high-power device operation. It is therefore critical to understand the impact of these various non-micropipe defects (particularly closed core screw dislocations) on the SOA of various SiC power device structures, as understanding of device SOA is necessary for design of reliable high-power circuits. Significant changes in high-power circuit topologies and device derating and paralleling practices may be required if closed core screw dislocation defects are found to greatly reduce the SOA of SiC-based power devices.

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