Germanium JFET for Cryogenic Applications

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ABSTRACT

The n-channel Germanium junction field effect transistor (Ge-JFET) was designed and fabricated for cryogenic applications. The Ge-JFET exhibits superior noise performance at liquid nitrogen temperature (77 K). From the device current voltage characteristics of n-channel JFETs, it is seen that transconductance increases monotonically with the lowering of temperature to 4.2 K (liquid helium temperature).

Introduction

In modern focal plane array (FPA) applications, the preamplifier stage should be placed at the isothermal platform in order to be in close proximity to the detector array [1]. There are three advantages to placing the preamplifier stage near the detector array: 1) reduced noise; 2) improved frequency response; and 3) no need for additional mounting for the high temperature requirement of the preamplifier stage.

Because of their superior noise characteristics, silicon junction field effect transistors (Si-JFET) are used at the input stage of preamplifier circuits in FPA. However, the Si-JFETs are not operable at liquid helium temperature (4.2 K), which is the typical temperature of many infrared (IR) detector operations. Germanium (Ge) JFETs, manufactured by Texas Instruments, were been explored some 30 years ago [2,3] as a suitable candidate for low-temperature applications. However, despite an inherent desire among the cryogenic research community for low noise Ge-JFETs for liquid helium

operation, these devices are no longer produced. Most of the more recent published papers have reported work on p-channel Ge-JFETs, [4,5] also manufactured by Texas Instruments.

In 1998, we reported on initial developmental work on Ge-JFETs operating at 4.2 K temperature [6]. In this paper, we report on the fabrication and characterization of Ge-JFETs for cryogenic applications, describing detailed device performance at temperatures ranging from 4.2 to 300 K(room temperature).

Fabrication

The n-channel Ge-JFET was fabricated on a <111> orientation p-type substrate with an n-type Arsenic doped epitaxial layer of 5 X $10^{15}/cm^3$ doping density and 1.0 μm thickness. A cross-sectional view of the JFET is shown in Fig. 1. The epitaxial layer was grown on a heavily doped p-type substrate at Germanium Power Devices (GPD) in Massachusetts. The low temperature chemical vapor deposition method was used for silicon dioxide deposition as the surface passivation layer. After device isolation by trench etching and low-temperature silicon dioxide (LTO) deposition, boron implantation was used to form a gate region. . The device isolation process by trench etching technique improves the cryogenic noise performance [7]. The gate length and width of the transistor is 5 μm and 250 μm respectively.

The gate opening was such that both top and bottom gates are shorted by the p^+ implant process. This process is different from the device fabrication process reported earlier [6] in which gate and substrate terminals are not shorted to enable biasing independently. Source and drain were formed by arsenic implantation followed by a thin layer (4000 Å) of LTO deposition. Only one high-temperature annealing step was used for both boron and arsenic dopant activation. After contact window opening, titanium (300 Å) and gold (4000 Å), metal depositions were made. The metal pattern was defined by chemical etching. Contact alloying was done at 390 °C in a nitrogen environment. The devices were mounted on a ceramic package along with a heater and a temperature sensor to be used to take variable temperature measurements. Low-temperature noise measurement was done by mounting the JFET package in a cryostat.

Results and Discussion

The transistor's DC characteristic was measured using a Tektronics 576 curve tracer. Figs. 2 (a), (b), and (c) show the families of drain voltage-current characteristics at room temperature (RT), for immersion in liquid nitrogen (77 K) and liquid helium (4.2 K) respectively. Saturation and turn-off were good, and no appreciable effects of light on device DC characteristics were observed. In fig. 2 (c), a decrease in drain current for Vg=0 is observed for higher drain voltages. This may be due to channel heating because of high current. The device I-V curve shows a linear increase of drain current for $V_g = 0$ with lowering of temperature. There is a substantial increase of drain current (~ 25%) for Vg=0 V in saturation mode, at 4.2 K in comparison to 77 K operation.

The JFETs are depletion mode n-channel devices, and the turn off voltage at room temperature is approximately –1.3 V. Because these devices are fabricated on 1.7 μm epi layer, they require large negative gate bias for complete turn off. The devices have low turn-on voltage (< 0.1 V) even at liquid helium temperature, as is evident from the V_D-I_D curve at low V_D values.

The low frequency noise spectra of the JFET at three temperatures are shown in Fig. 3. The noise measurements were done in source follower mode with the gate grounded and a drain bias of 3.0 V. Biasing was done by batteries. Typical device current during noise measurement was 100 μA. The measurements were performed with a low noise preamplifier coupled to an HP 35665A dynamic signal analyzer and were carried out in a shielded screen room to avoid any spurious noise due to the line voltage or external electrical disturbances.

The transistor has a gain of 0.9 throughout the spectral region, with no appreciable change at low temperature. We observed 1/f dependence of noise spectra in the low frequency range (less than 100 Hz), beyond which the noise voltage does not change appreciably. The low noise spectra taken at 77 K has the least value for the entire region of the measurements.

It is well known that noise voltage for the Si-JFET is inversely proportional to the transconductance (gm) of the device [1] at various temperatures. The measured gm for

Ge-JFET at different temperatures, along with the noise voltage, are plotted in Fig. 4. In our experiment we tested three devices and took the average for plotting. As shown in Fig. 4, there is no direct correlation between an increase in gm and a decrease in noise voltage at low temperatures. As seen in Figs. 2 and 4, gm increases linearly with the lowering of temperature. However, the noise value decreases initially from room temperature data, attains minima at 77 K and then increases as the temperature lowers. We believe the increase in gm is the result of increased carrier mobility due to reduced lattice scattering at low temperature [8,9]. From the noise spectra it is seen that both 10 Hz and 100 Hz noise curves have predominant minima at 77 K. This is also true for all other frequency values in the measured spectrum range between 1 and 100 Hz.

The observed minima at 77 K implies that Ge-JFETs are better suitable for liquid nitrogen operation than Si-JFETs. Si-JFETs require additional heating to attain the desired temperature (120 K) for minimum noise value [7]. At present we do not know which types of defects contribute to the noise figure of the Ge-JFETs. We believe additional analysis is required to determine the nature of defects responsible for noise the voltage in Ge-JFETs.

Conclusions

The transconductance of Ge-JFETs increases linearly from room temperature to liquid helium temperature. However, the noise spectra have minimum value at liquid nitrogen temperature. Hence, the noise minima for Ge-JFET does not occur at the transconductance maxima which is generally true for Si-JFET. Ge-JFETs can be used for IR detector applications, which require liquid helium temperature operation.

Acknowledgements

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References

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Figure Captions

Figure 1. Cross-sectional view of Ge-JFET.

Figure 2. Transistor I_D vs. V_D characterics, (a) room temperature, (b) 77 K, and (c) 4.2 K.

Figure 3. Noise spectra at three different temperatures, (a) room temperature, (b) 77 K, and (c) 4.2 K.

Figure 4. Noise voltage and transconductance of the device at different temperatures.

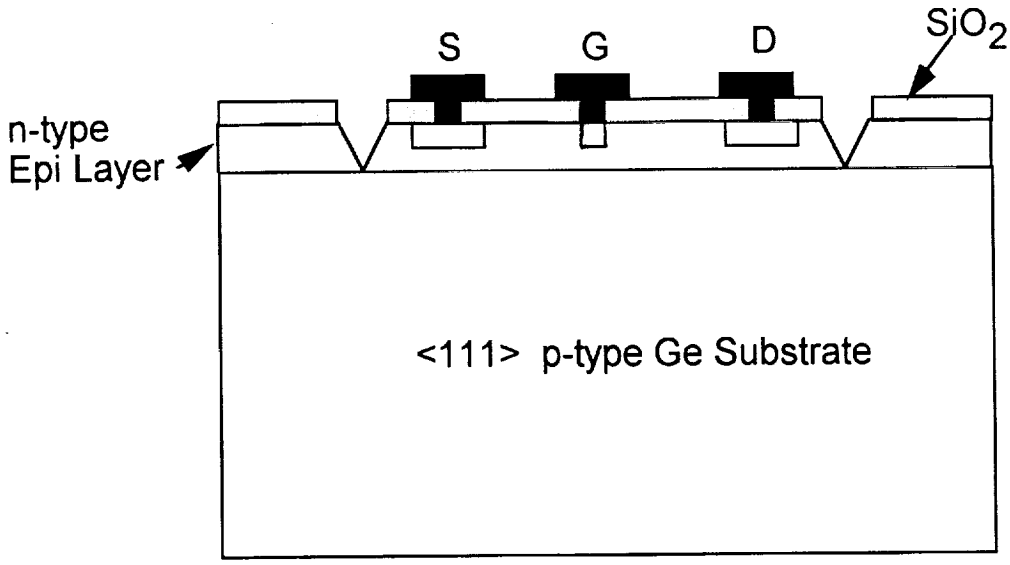
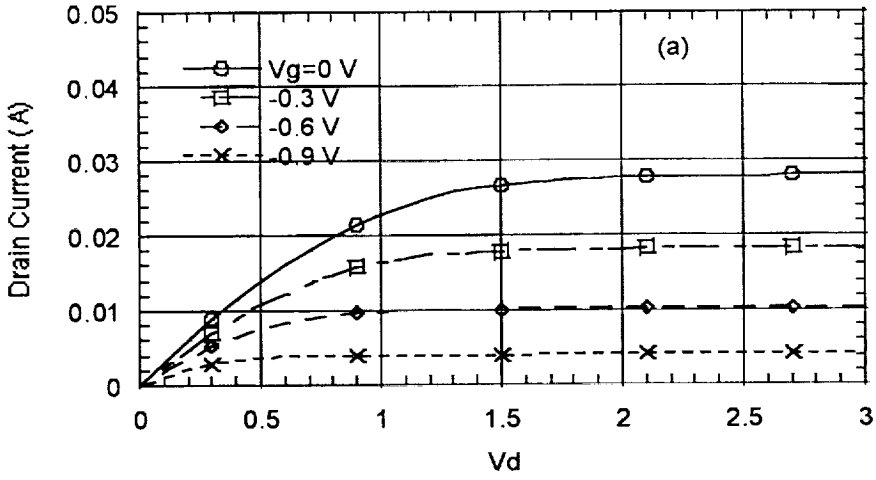
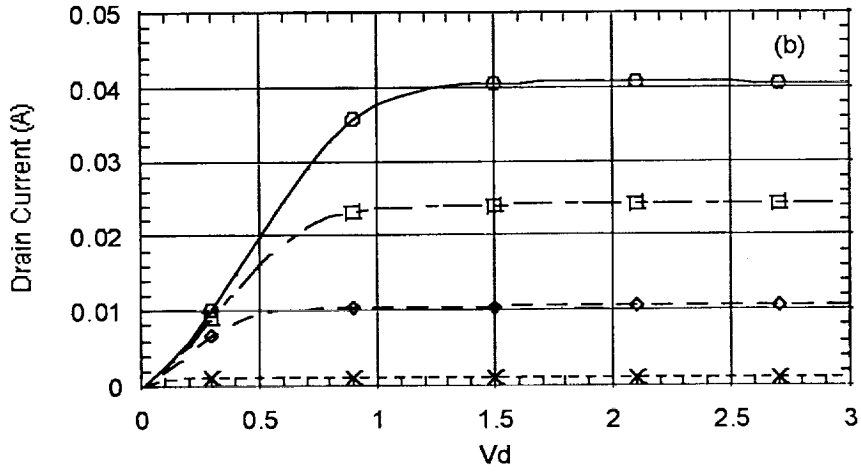


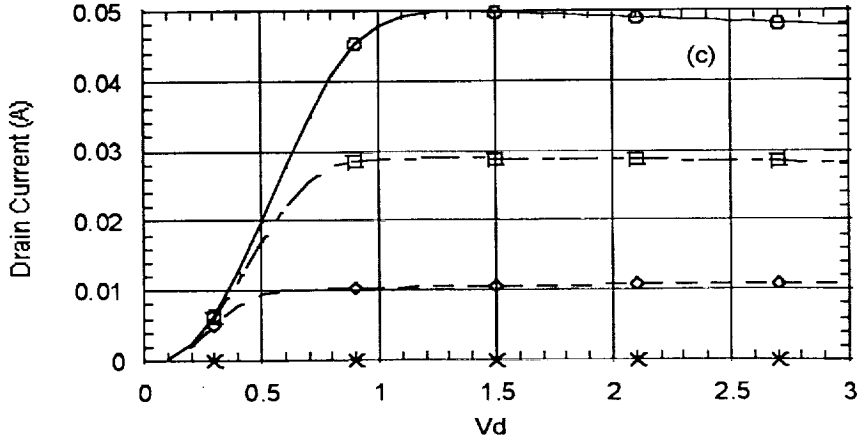
Fig. 1



(a) I-V Curves at Room Temperature



(b) I-V Curves at 77 K



(c) I-V Curves at 4.2 K

Fig. 2

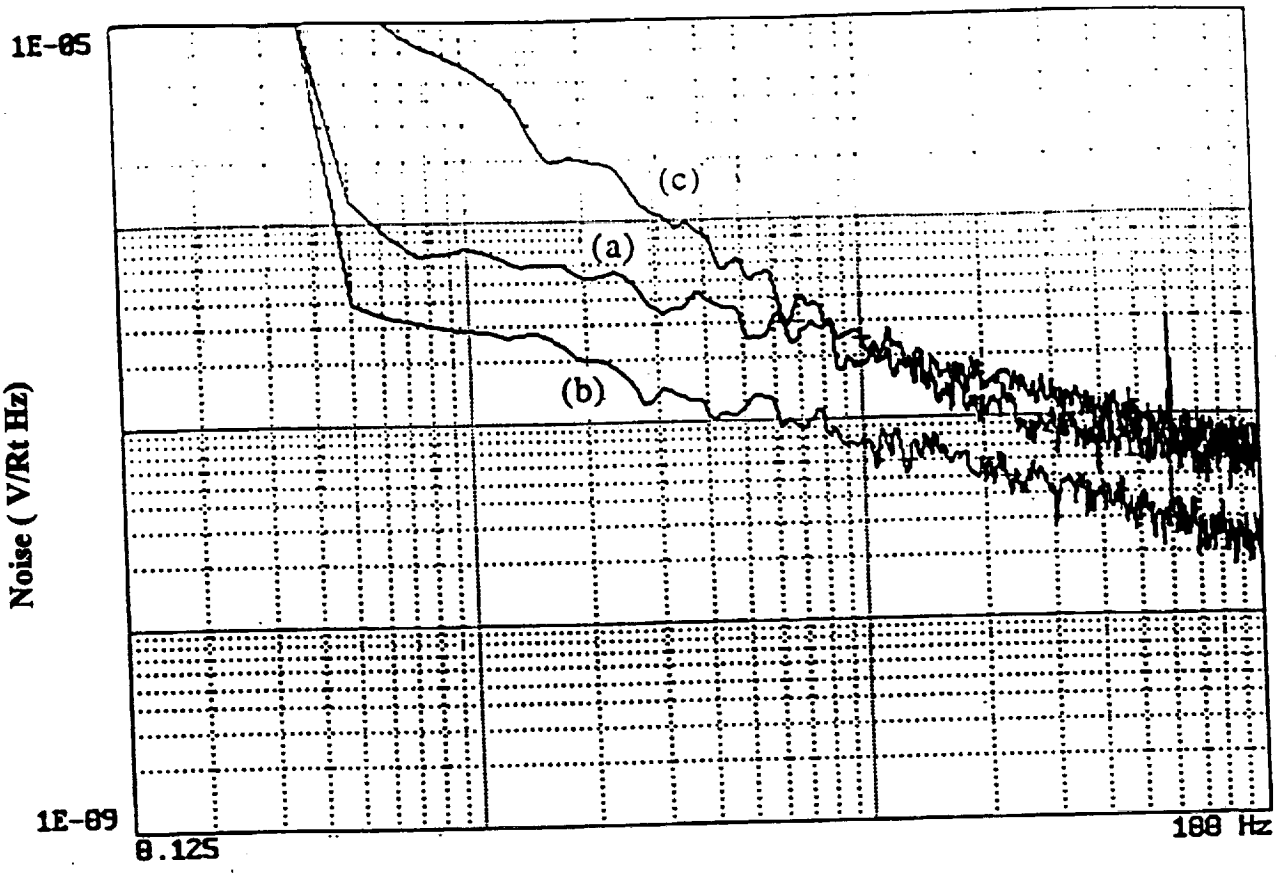


Fig. 3

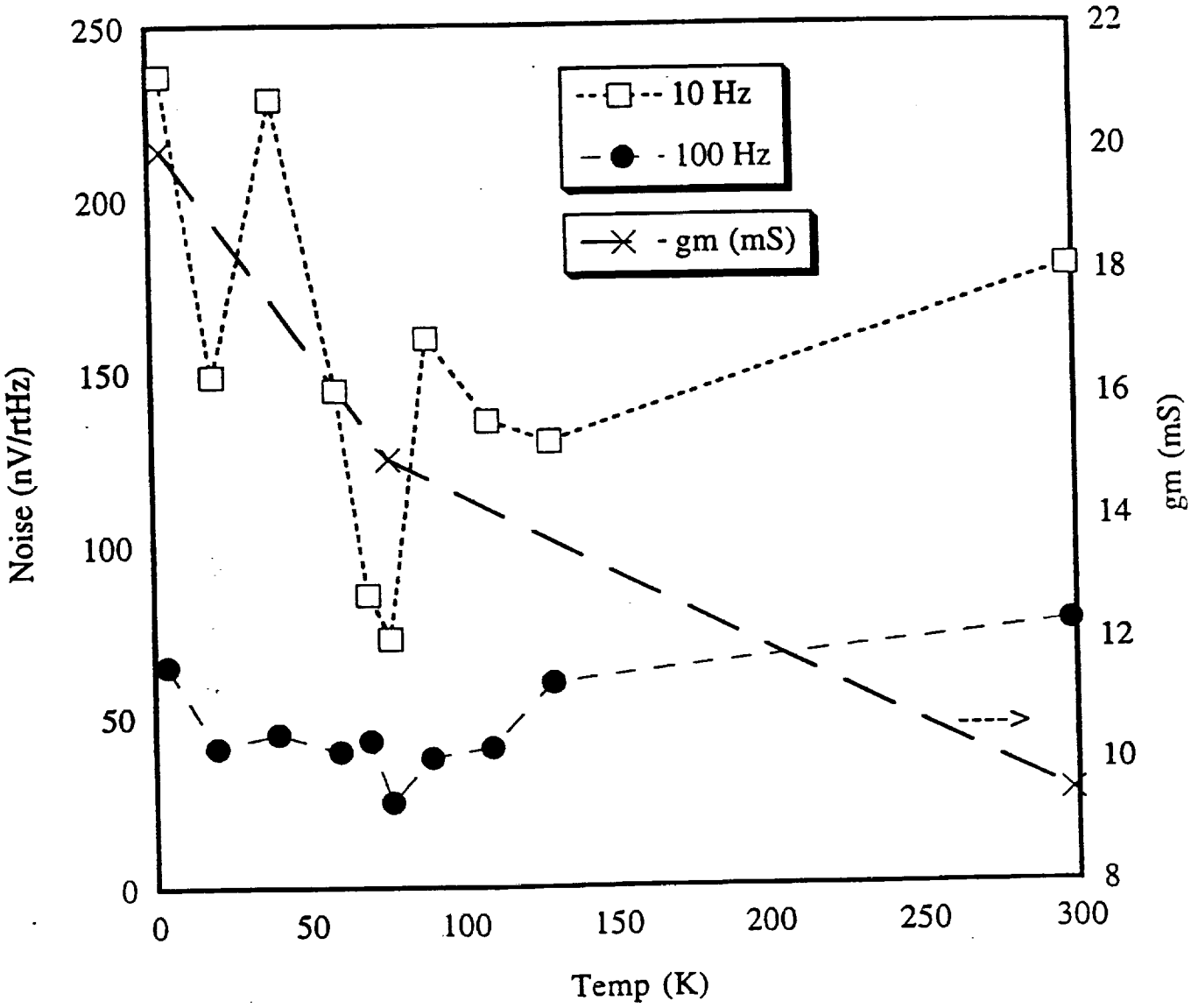

250
200
150
100
50
0
Noise (nV/rtHz)
22
20
18
16
14
12
10
8
gm (mS)
0
50
100
150
200
250
300
Temp (K)
10 Hz
100 Hz
gm (mS)

Fig. 4