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Full Duplex, Spread Spectrum Radio System

Bruce A. Harvey, Ph.D.
Assistant Professor
Department of Electrical Engineering
Florida A&M University – Florida State University College of Engineering

KSC Colleague: Richard Nelson

ABSTRACT

The goal of this project was to support the development of a full duplex, spread spectrum voice communications system. The assembly and testing of a prototype system consisting of a Harris PRISM spread spectrum radio, a TMS320C54x signal processing development board and a Zilog Z80180 microprocessor was underway at the start of this project. The efforts under this project were the development of multiple access schemes, analysis of full duplex voice feedback delays, and the development and analysis of forward error correction (FEC) algorithms. The multiple access analysis involved the selection between code division multiple access (CDMA), frequency division multiple access (FDMA) and time division multiple access (TDMA). Full duplex voice feedback analysis involved the analysis of packet size and delays associated with full loop voice feedback for confirmation of radio system performance. FEC analysis included studies of the performance under the expected burst error scenario with the relatively short packet lengths, and analysis of implementation in the TMS320C54x digital signal processor. When the capabilities and the limitations of the components used were considered, the multiple access scheme chosen was a combination TDMA/FDMA scheme that will provide up to 8 users on each of three separate frequencies. Packets to and from each user will consist of 16 samples at a rate of 8,000 samples per second for a total of 2 ms of voice information. The resulting voice feedback delay will therefore be 4 – 6 ms. The most practical FEC algorithm for implementation was a convolutional code with a Viterbi decoder. Interleaving of the bits of each packet will be required to offset the effects of burst errors.

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1. INTRODUCTION

The primary focus for this summer's efforts was the development of a prototype full-duplex, spread spectrum, digital voice radio system. This system is intended to provide open voice communications between at least 4-7 persons in large rooms (i.e. high bays) or in open outdoor areas (i.e. landing strip). The persons using the system are expected to be able to conduct normal conversation as if they were located in close proximity. This differs from push-to-talk systems where there is only half-duplex operation (only 1 speaker at a time). The spread spectrum operation of the system allows license-free operation in the 2.4 GHz ISM band and alleviates much of the fading and signal loss due to signal multipath.

The goals for the prototype communication system included:
1) Minimum of 4 – 7 users,
2) Full loop audio feedback to ensure transmit and receive operation,
3) Feedback delay much less than 20 milliseconds to avoid speech interference,
4) 8000 samples/second with 8 or more bit pulse code modulation (PCM), and
5) Operating ranges from a few hundred feet to approximately 3 miles.

The hardware for the design of the prototype devices had already been selected and were in the process of being assembled and debugged at the start of the effort. The Harris PRISM radio set (HWB1151) was chosen to provide the spread spectrum modulation, RF devices and baseband processing. The Texas Instruments TMS320C54x signal processor and evaluation board was selected to provide analog-to-digital and digital-to-analog conversion, signal processing and error control. A Zilog Z80180 microprocessor provides overall control of the system. The analysis and designs under this effort were to be used in this existing prototype design.

The primary tasks under this effort were trade-off analysis of multiple access protocols, analysis of communication link performance and development of forward error correction (FEC) algorithms for the prototype.

2. MULTIPLE ACCESS PROTOCOL DEVELOPMENT

A digital communications system can use a number of techniques or protocols to allow multiple users access to the communications channel. The three general techniques are frequency division multiple access (FDMA), time division multiple access (TDMA) and code division multiple access (CDMA). FDMA, TDMA and CDMA may be used individually or in combinations to meet the requirements and conditions of the communication system. Typically, very high bandwidth channels use a combination of FDMA with either TDMA or CDMA to obtain the benefits of TDMA or CDMA while allowing a narrower bandwidth receiver design.

The PRISM chip set provides the baseband to RF components necessary to implement a spread spectrum communications system in the 2.400 – 2.483 GHz band. It is capable of transmission rates of 1, 2, 5.5 and 11Mbps in a null-to-null bandwidth of 22 MHz. It is designed for packet communication and includes a baseband processor that controls preambles and headers. It uses direct sequence spread spectrum (DSSS) technology. Media access control (MAC) is provided by a Z80180 microprocessor.

The HFA3860B baseband processor controls the preamble and header generation, modulation and demodulation, spreading and de-spreading, and digital interfacing of the PRISM system. The preamble and header are always transmitted using differential binary phase shift keying (DBPSK) at 1 bit per symbol while the data can be transmitted in one of several different formats with up to 8 bits per symbol. One of the most significant factors concerning the preamble and header is that they total 146 to 322 symbols and are always transmitted at 1 Msymbols/sec regardless of the symbol rate of the data.. The data symbol rate for the PRISM is 1 Msymbols/sec. for the 1 and 2 MBPS data rates, and 1.375 Msymbols/sec. for the 5.5 and 10 Mbps data rates. Thus increasing the data symbol rate has no impact on the transmit time required for the preamble and header.

The PRISM chip set can have an 11- to 16-bit spreading sequence depending on the version used and the user settings. However, 16 bits is insufficient to provide adequate isolation between CDMA users. The PRISM system is thus not capable of implementing a useful CDMA protocol for this application. The PRISM is capable of operating in 3 non-overlapping 22 MHz channels within the total 83 MHz operating band. This allows the implementation of a 3-channel FDMA scheme. The radio is designed to operate as a packet radio and thus is also well suited for the implementation of a TDMA protocol. A combination TDMA/FDMA protocol will provide even more flexibility and was chosen for implementation in the prototype system. [1]

Several protocols for establishing a TDMA system have been proposed or implemented. Many of these protocols are wholly inappropriate for this application. These protocols include ALOHA or Slotted ALOHA, token ring, and carrier sense multiple access (CSMA) or ethernet. For continuous communication with fixed data rate requirements, the most efficient TDMA protocol will include fixed and allotted time slots. Each user (transceiver) will be allocated a specific slot in a TDMA time frame in which to transmit its data. For reliability, monitoring and interconnection with other voice systems, the TDMA system will include a Central Controller through which all communications will be conducted. The Central Controller (CC) will be a set of up to three (3) transceivers each operating in its own frequency band. The CC will receive transmission from every user transceiver, combine the voice signals and transmit the combined voice communications back to each transceiver. Also, the transmitted frame from the CC will be used to establish the starting time for each TDMA frame.

The most obvious first approach to TDMA implementation for voice applications is for each transmitter to take each voice sample and form a packet that is then transmitted during a prescribed timeslot. Since sampling is intended to have an 8 kHz rate, then there is 125

microsecond (µs) between each sample. However, the minimum preamble/header size for a packet is 146 µs. Therefore, this method will not work.

Multiple samples of the audio input must be sent in a single packet to increase the time between packets and the amount of data sent per preamble/header. Storing multiple samples for transmission introduces delay into the communications channel. A delay of 20 – 30 milliseconds (ms) or even longer is generally not noticeable in most voice communication systems. However, one of the goals for this system is full feedback of the audio signal to the users ear for confirmation of operation. Delayed feedback of auditory information to the speaker of over 20 – 50 ms has been shown to cause speech and concentration problems for the speaker. Thus, the feedback delay will be kept well under 20 ms to avoid these problems.

A maximum auditory feedback delay of 5-6 ms was chosen for the prototype system; longer delays may be tested in the future. Since the transmission and reception of the data will each introduce a delay, then the delay due to storage of samples must be no greater than 2.5 ms. To allow for processing delays, 2 ms was chosen as the storage time for each packet of data. A storage time of 2 ms is equivalent to storing 16 samples at an 8 kHz rate for each packet of data.

Sixteen samples using 8-bit pulse-code modulation (PCM) results in 128 bits of data for each packet. If rate ½ FEC is used, then the data will be 256 bits (512 bits for 16-bit PCM). At the 1 Mbps data rate the number of bits per symbol is 1 and therefore a packet with preamble, header and 256 bits of data is a minimum of 402 symbols or 402 µseconds. There is 2 ms in each frame and thus 4 TDMA time slots can be implemented in a single frequency channel. Table 2-1 shows the packet size and maximum number of users possible for each transmit data rate. Preamble synchronization lengths of 80 and 128 symbols (146 and 194 symbol preamble & header) are considered. The 128 symbol synchronization length is the minimum suggested for use with antenna diversity and is the required length for the IEEE 802.11 standard. The data packet is assumed to be 256 bits The results in parenthesis assume 512 bits per packet (16 samples of 16-bit PCM with rate ½ FEC). The actual prototype uses 14-bit PCM padded to 16 bits using the 14-bit analog-to-digital converters included on the DSP card used.

Data Rate (Mbps)	Symbol Rate (Msym/sec)	Synch. Length (symbols)	Packet Length (symbols)	Packet Time (µsec)	# TDMA Slots / Freq.	
					Minimum	50 Symbol Guard Band
1	1	80	402	402	4 (3)	4 (2)
		128	450	450	4 (3)	4 (2)
2	1	80	274	274	7 (4)	6 (4)
		128	322	322	6 (4)	5 (4)
5.5	1.375	80	210	192.55	10 (8)	8 (7)
		128	258	240.55	8 (6)	7 (6)
11	1.375	80	178	169.3	11 (10)	9 (8)
		128	226	217.3	9 (8)	7 (7)

( ) – Data packet assumed to be 512 bits = 16 samples × 16 bits/sample × 2

Table 2-1. TDMA Slot Analysis

The TDMA slots in operation require guard bands (time) in order to assure no overlapping transmitted signals. The guard band was chosen to be 50 symbols to allow for the propagation (maximum of 3 mile range), timing and shut down periods. The addition of these guard bands increase the TDMA time slot requirements and consequently reduces the number of allowable users in each frequency band. The numbers of available TDMA slots with guard bands are listed in the final column of Table 2-1.

The HFA3860B Baseband included in the most recent PRISM chipset accomplishes the DSSS acquisition. The HFA3860B uses a parallel correlator to detect the 11-bit PN sequence (Barker code) used to spread the signal in the header and preamble. The timing and phase of the received signal is detected and used to synchronize the serial correlators used in data decoding. To improve the signal-to-noise ratio (SNR) for detection the acquisition process uses the average of 15 received symbols. The de-spreading by the correlators improve the SNR by $10\log(11) = 10.4$ dB. The averaging improves the SNR by another 11.7 dB to ensure reliable PN detection and accurate timing and phase information. Detailed information on the HFA3860B can be found in the Harris data sheet "HFA3860B Direct Sequence Spread Spectrum Baseband Processor." [2]

The preamble SNR is improved by 10.4 dB by the de-spreading of the PN code, the same as for data demodulation. However, the preamble SNR is improved during acquisition by an additional 11.7 dB above that of the data demodulation by averaging. If the received signal level is sufficient to provide a high enough SNR for reliable data demodulation, then the SNR will be more than 10 dB higher for acquisition and thus reliable acquisition will be achieved. Therefore, the reliability of the communication and link budget analysis will be determined by the bit error rate (BER) of the data demodulation.

3. LINK BUDGET AND OPERATING RANGE ESTIMATES

The initial link budget for this implementation of the full duplex, spread spectrum system relies heavily on the receiver sensitivity specifications in the Harris PRISM MACless DSSS Radio HWB1151 User's Guide [1]. The receiver sensitivity is given for each possible data rate and are listed in Table 3-1. The specification lists the minimum received signal level to achieve 8% packet error rate (PER) assuming a packet size of 1000 bytes. Assuming random bit errors (not bursty), this is equivalent to the minimum received signal level for a bit error rate (BER) of 10^{-5}.

Transmitter Data Rate and Modulation	Receiver Sensitivity
1 Mbps DBPSK	-89 dBm
2 Mbps DQPSK	-86 dBm
5.5 Mbps CCK	-86 dBm
11 Mbps CCK	-83 dBm

Table 3-1. MACless PCMCIA PRISM Receiver Sensitivity (8% PER)

According to the Harris data sheet for the HFA3860B Baseband Processor (used in the newest versions) [2], the observed errors occur in groups (i.e. burst errors). The 1 and 2 Mbps modes

had errors in groups of 4 and 6 bits due to the differential decoding and de-scrambling error propagation. The 5.5 and 11 Mbps CCK modes had errors in symbols of 4 and 8 bits, respectively. These burst errors will be extended if the de-scrambler is used. An 8% PER over a 1000 byte packet translates into a 4×10^{-5} and 8×10^{-5} symbol or burst error rate for bursts of 4 and 8 bits, respectively.

The receiver sensitivities given in Table 3-1 can be used to estimate the range of operation for the communications system. The version of the PRISM currently being used has a transmit power P_t of 18 dBm. An external amplifier is being considered which will bring the transmitter power up to 27 dBm (1/2 Watt). If all values are expressed in decibels (dB), then the transmit power P_t and receive power P_r can be related by $P_r = P_t + G_t + G_r - L_p - FM$ where $G_{t,r}$ = transmitter, receiver antenna gain in dB, L_p = propagation loss in dB, and FM = the designed fade margin in dB.

There is no set level for the fade margin that will compensate for all signal variability in signal level. Rather, the fade margin provides a measure of protection. A larger fade margin improves the likelihood of compensation for the variability and hence the reliability of the link. In a Harris application note "Tutorial on Basic Link Budget Analysis" [3] the authors suggest the fade margin be 20 – 30 dB, even for this spread spectrum system. However, in a clear, unobstructed outdoor environment, the fade margin may be reducible to 10 – 15 dB.

The propagation loss L_p is highly dependent on the environment in which the system is operating. In free space,

$$L_p = L_{fs} = 20\log\left(4\pi D/\lambda\right)$$

where D = the transmit distance and λ = the wavelength. However, if the antennas are outdoors close to the ground, then the plane earth model for propagation is more appropriate.

$$L_p = L_{pe} = 20\log\left(D^2/h_t h_r\right)$$

where $h_{t,r}$ = the height of the transmit, receive antenna. The plane earth model is more accurate whenever

$$D > 4\pi h_t h_r/\lambda .$$

Models for indoor communications are widely varied and highly dependent on room sizes, building construction and orientation of the antennas. The authors of the Harris application note [3] suggest a simple and conservative estimate for indoor communications. Their model uses free space communication for up to 20 feet and then 30 dB attenuation for each additional 100 feet. This model probably assumes an office environment consisting of individual offices and conference rooms. Thus much of the propagation loss is likely to be walls, furniture and other obstructions.

The environment for indoor communications required at NASA will likely include large processing room or high bays. While the room will be larger than a typical office, a high-bay will likely contain many large metallic objects and structures which will translate into increased multipath and attenuation. Therefore, the model proposed in the Harris application note will suffice for initial designs. Tests of the prototype system in a working environment will be required to ascertain the multipath effects and propagation models to be used.

The maximum operating ranges for outdoor and indoor environments can now be calculated using the receiver sensitivity, link budget equation and propagation models. A relatively modest fade margin of 10 dB will be assumed for this prototype analysis. Maximum operating ranges are listed in Table 3-2 as a function of antenna heights and transmitter power. The 18 dBm transmit power of the Harris PCMCIA version of the PRISM and the 27 dBm output of a ½ Watt amplifier are depicted in the table. An antenna height of 5 feet is assumed for the mobile unit carried by a person. The base or central controller antenna height is varied.

Antenna Height (ft.)		Maximum Range (ft.) +18 dBm			Maximum Range (ft.) +27 dBm		
Mobile	Base	Outdoor	Model	Indoor	Outdoor	Model	Indoor
5	5	942	Plane	138	1879	Plane	178
5	10	1158	Free	138	2658	Plane	178
5	15	1158	Free	138	3255	Plane	178
5	20	1158	Free	138	3758	Plane	178
5	25	1158	Free	138	4202	Plane	178

Plane = plane earth outdoor model, Free = free space outdoor model

Table 3-2. Estimated Operating Ranges for Prototype System

The results in Table 3-2 indicated several important facts. First, outdoor maximum operating range will ultimately be limited by plane earth propagation. Increasing the base or central controller antenna height will increase the range of operation, but it will limit the mobility of the system. The ½ Watt transmit power and 25 ft. base antenna resulted in a maximum range of 0.8 miles. The indoor propagation model used resulted in an operating range of less than 200 ft. even for ½ Watt transmit powers. This model is expected to be overly conservative for operation in a high bay and testing is suggested.

4. FORWARD ERROR CORRECTION

Many voice communications use a minimum or no forward error correction. Speech communications is rather tolerant to random and burst errors and thus FEC is not implemented. However, there are two factors that make an analysis of FEC for this system necessary. First, this system may be used in mission critical or safety-related operations where clear communications is required. Second, one possible extension of this system is the overlay of data on the voice network that requires higher reliability than voice. For these reasons, an analysis of error correction techniques and capabilities was conducted.

The TDMA protocol selection described previously resulted in voice data packets of 128 to 256 bits depending on whether 8-bit or 16-bit PCM encoding is used. These relatively small data packets will be subject to burst errors due to the modulation, scrambling and detection of the transmitted symbols. The 11 Mbps mode of the PRISM chipset is the likely operating mode of the prototype system to maximize the number of users. This mode is characterized by 8-bit burst errors; longer if scrambling is used. A single burst error in a 256-bit packet lowers the average bit error rate of the packet to about 0.016. This burst error will result in a very brief noise burst in voice communication, but is unacceptable for data communications.

The TMS320C54x signal processor has been designed to facilitate the decoding of the convolutional codes using the Viterbi decoder. Efficient implementation algorithms have been designed and estimates of the processing time required to decode blocks of data using the Viterbi decoder have been provided in application notes. Block codes can provide the burst error protection desired, but these codes generally have fixed lengths that limit the flexibility and reduce the efficiency of the system. Therefore, convolutional coding with Viterbi decoder was selected for the prototype system.

Convolutional codes are well suited to provide increased reliability in the presence of random bit errors during transmission. Interleavers will be used to distribute the burst errors to make them appear more like random bit errors. Interleavers require less processing and memory storage, and are more flexible than other approaches such as concatenated codes or specially designed burst error correcting convolutional codes. [4] Interleavers for this effort were assumed to distribute burst errors over the entire length of the coded data packet.

Encoding a packet of data using a convolutional code with k inputs, n outputs and memory length m requires the encoding of $k{\times}m$ additional input zeros in order to "complete the code". [4,5] The number of added output bits to the packet after completing the code is $n{\times}m$ bits and is often referred to as the "tail" of the encoded packet. For example, if 100 bits were encoded using a rate 2/3, memory length 4 convolutional code (m = 4, k = 2 inputs and n = 3 outputs) then the number of bits in the encoded packet will be $100 \times 3/2 + 3 \times 4 = 150 + 12 = 162$ bits. This makes the effective rate of the code 100/162 = 0.62.

For analysis purposes, it is assumed that the burst errors are randomly distributed over the entire packet by the interleaver and thus are effectively modeled as an increase in bit error rate for the packet. For example, a burst error of length 8 in a 162-bit packet will result in an average of 4 bit errors in the packet. The simulation models the burst error after interleaving as random probability of bit error (bit error rate) or 4/162 = 0.025.

Simulations were conducted to quantify the effects of the burst errors on short packets with convolutional codes. A Viterbi decoder was simulated to decode convolutionally encoded packets with randomly occurring burst errors. The length of the burst errors was chosen to be 8 bits to correspond to characteristics the 11 Mbps mode of the Harris PRISM without data scrambling. The simulations were conducted on packets of 128 and 256 data bits (before encoding) to bound the expected range of data bits for 16 samples of voice data (8 to 16-bit

PCM). For easy comparison to decoding with random bit errors, the simulations were conducted as a function of the average bit error rate of the system.

The results of the simulations for rate ½ convolutional codes with a memory length of 2 (constraint length K of 3) are shown in Figure 4-1. The abbreviations in the legends are defined as follows: NB = no burst errors (random only), 8B = 8-bit burst errors, Est = analytical estimate of 8-bit burst errors assuming only 1 burst error per packet, and BK = the length of data (uncoded) in the blocks. The simulation results demonstrate that the burst errors significantly degrade the performance of the Viterbi decoder for short packets. Longer packet lengths have better (lower decoded BER) performance. However, the convolutional code and Viterbi decoder still provide a significant BER improvement even at short constraint lengths. Longer codes provide lower decoded BER at the cost of greater processing and memory requirements.
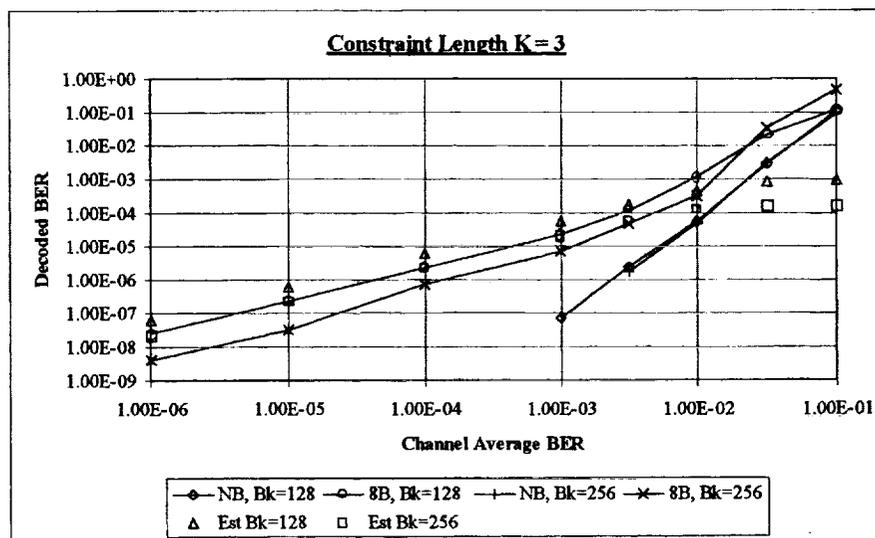
Figure 4-1. Viterbi Decoder Performance vs. Burst Errors and Short Blocks

Implementing the Viterbi decoder on the TMS320C54x series DSP is simplified through a special function designed especially for this decoder. Key algorithms are found in a TI application report "Viterbi Decoding Techniques in the TMS320C54x Family." [6] Further explanation is available in the "TMS320C54x DSP Reference Set, Volume 4: Application Guide" in Section 7.2. [7] Also, a complete Viterbi decoder assembly code and application report [8] is available for the earlier TMS320C5x processor. The 'C5x processor does not have the 'C54x special instruction, but the memory handling and processing algorithms are similar. All the TI application notes and source listings discussed here are available on the TI web pages at "http://www.ti.com/sc/docs/apps/dsp".

The TI application report "Viterbi Decoding Techniques in the TMS320C54x Family" [6] also provides benchmarks for determining the processing speed (in MIPS) required to implement a Viterbi decoder. This benchmarks considers, the code rate R, constraint length K, code puncturing rate PR, frame size FS before coding (# data bits) and the number of frames per

second *FR*. The benchmarks for rate ½ convolutional codes with various constraint lengths were calculated. Recall that the frame period was calculated as the time required for 16 samples at 8,000 samples per second. Therefore the frame rate is 1/(2 ms.) or 500 frames per second. For 16-bit PCM, the frame size will be 256 bits. The calculated benchmarks are listed in Table 4-1.

Code Rate, R	Constraint Length, K	Required MIPS
½	3	3.9
½	5	7.84
½	7	24.0
½	8	45.0

Table 4-1. Benchmarks for Viterbi Decoder on TMS320C54x

The benchmarks in Table 4-1 reveal that even a convolutional code with constraint length as high as 8 can be implemented on a TMS320C54x with a clock speed of 60 MHz. Note that the $K = 8$ code is the defacto (2,1,7) convolutional code used in many applications including satellite and mobile communications, often concatenated with a Reed-Solomon code for combined burst and random bit error protection.

For voice communications alone the FEC algorithms may be used to increase the operating range and reduce noise at longer operating ranges. A rate ½ convolutional code can provides significant error reduction for the short packets in the presence of burst errors (implemented with an interleaver). For voice communications, constraint lengths as low as $K = 3$ will provide significant improvements, while longer constraint length codes will be required for high data reliability applications.

5. CONCLUSIONS AND DISCUSSIONS

The prototype full duplex, spread spectrum voice communication system specifications are:

- Data Rate: 11 Mbps
- Voice Coding: 14-bit PCM (padded to 16 bits) at 8,000 samples per second
- Packets: 16 samples = 256 bits
- Frame Rate: 1 / 2 ms = 500 Hz
- TDMA Slots: 9 slots (8 users, 1 CC) per frequency (0.22 ms per slot)
- Frequencies: 3 frequency bands
- Maximum Users: 24

The prototype system will initially be implemented without forward error correction. If test results warrant or data transmission is added to the system, the FEC can be added at a later time. If rate ½ FEC coding is added, then the packets size will increase to 512 bits, the number of TDMA slots per frequency will reduce to 8 (7 users, 1 central controller), and the maximum number of users will reduce to 21.

The prototype system currently under construction can provide full duplex voice communication for groups of up to 24 people. The system will have 3 frequency channels that can be configured for 3 separate talk groups of up to 8 users or combined into a single 24-person talk group. The system can be operated with open microphones, push-to-talk or combinations of open and push-to-talk users. Potential applications include Ad Hoc wireless communications, remote communication where other radio systems do not exist, and transportable communications. The full duplex system is currently configured to be a standalone communication system.

This system can be extending by interfacing the central controller to other existing communication systems such as the Operational Intercommunication System – Digital (OIS-D), or T1 (or T3) wired or wireless links. The wireless operating range can be extended by increasing the transmit powers or raising the height of the central controller's antenna. More time slots can be made available by using rapid acquisition techniques such as SAW filters [9], or by reducing the data rates required for voice communication through vocoders such as [10]. Future versions of this system can employ advanced channel management techniques to allow more users to share the existing time/frequency slots and thus increase the number of users.

REFERENCES

[1]   Abrahams, Richard L., "2.4 GHz 11 Mbps MACless DSSS Radio HWB1151 User's Guide," Application Note 9835.1, Harris Semiconductor, 1999.

[2]   "HFA3860B Direct Sequence Spread Spectrum Baseband Processor," Data Sheet, File Number 4595, Harris Semiconductor, December 1998.

[3]   Zyren, Jim and Petrick, Al, "Tutorial on Basic Link Budget Analysis," Application Note AN9804.1, Harris Semiconductor, June 1998.

[4]   Lin, Shu and Costello, Jr., Daniel J., *Error Control Coding: Fundamentals and Applications*, Prentice-Hall, Inc., Englewood Cliffs, N.J., 1983.

[5]   Wicker, Stephen B., *Error Control Systems for Digital Communication and Storage*, Prentice-Hall, Inc., Upper Saddle River, N.J., 1995.

[6]   Hendrix, Henry, "Viterbi Decoding Techniques in the TMS320C54x Family," Application Report, Literature Number SPRA071, Texas Instruments, June 1996.

[7]   "TMS320C54x DSP Reference Set, Volume 4: Application Guide," Literature Number SPRU173, Texas Instruments, October 1996

[8]   Chishtie, Mansoor A., "U.S. Cellular Error-Correction Coding Algorithm Implementation on the TMS320C5x," Application Report, Literature Number SPRA137, Texas Instruments, October 1994. (Also Viterbi Decoder assembly program listing.)

[9] "STEL-2000A Digital, Fast Acquisition, Spread Spectrum Burst Processor," Stanford Telecom, Web Site: www.stelhq.com/index.htm.

[10]   Preliminary Data Sheet for the AMBE-2000 Vocoder Chip, Digital Voice Systems, Inc., Burlington, MA, Web Site: www.dvsinc.com.