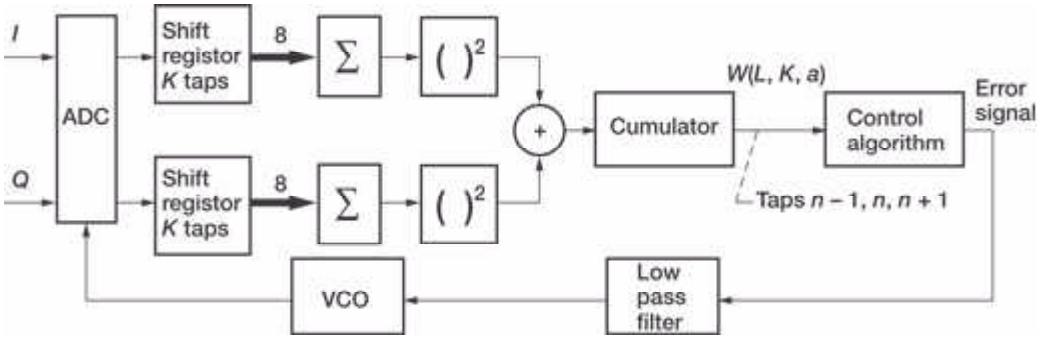
Robust Sliding Window Synchronizer Developed

The development of an advanced robust timing synchronization scheme is crucial for the support of two NASA programs--Advanced Air Transportation Technologies and Aviation Safety. A mobile aeronautical channel is a dynamic channel where various adverse effects--such as Doppler shift, multipath fading, and shadowing due to precipitation, landscape, foliage, and buildings--cause the loss of symbol timing synchronization.

Tests from a ground-based mobile vehicle through a geosynchronous communications satellite, using the EB200 direct-sequence spread spectrum modem, lost synchronization at a signal-to-noise ratio E_b/N_0 as high as 11 dB. At this signal-to-noise ratio, the modulations could still maintain an adequate bit error rate of about 1×10^{-6} if the synchronization was not lost.

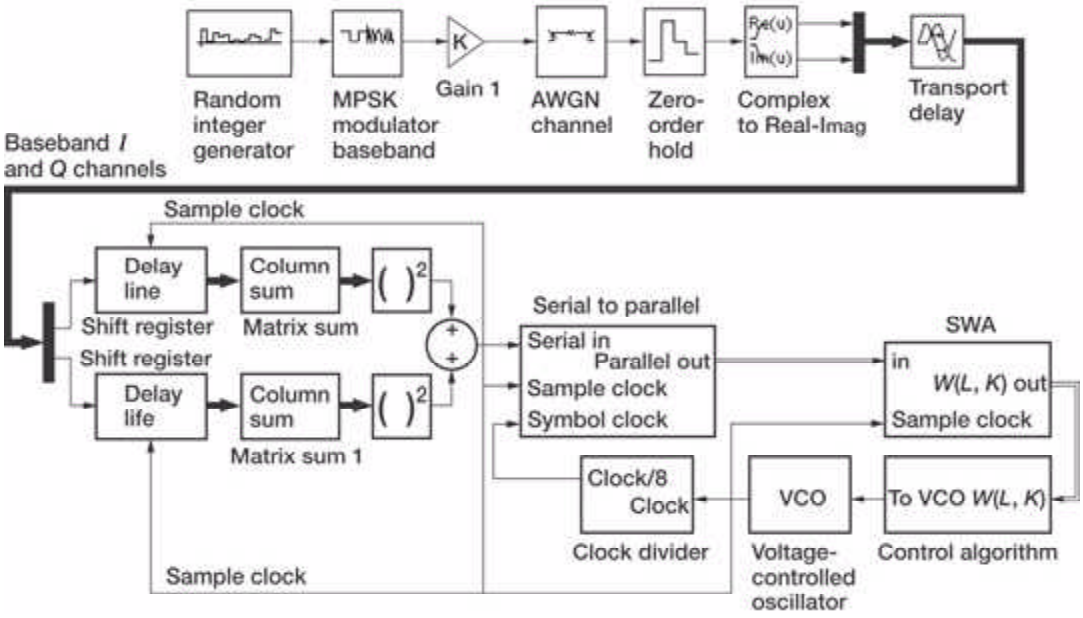


Sliding-window symbol synchronizer.

Long description. Block diagram of the robust sliding-window average (SWA) symbol synchronizer. The synchronizer consists of an analog-to-digital converter (ADC), two shift registers, computing logics, a cumulator, a controller, and a voltage-controlled oscillator (VCO). The I- and Q-channel baseband signals are digitized by the ADC and sent to two shifter registers, respectively. The sampling clock is synchronized with the local symbol-timing clock generated by the VCO. The shift registers act as two simultaneous sliding windows. At the symbol rate, the K samples of I- and Q-channels in the window are summed and squared, and the results are added to form the signal W(n) at the adder output. The time instant of summing the register contents is at the end of a period of the local symbol clock. The cumulator computes the average of the W(n) over a sufficient time length to produce the phase detector characteristic W(L, K, a), where L is the symbol timing offset (delay or advance) in samples between the sliding window and the incoming data symbol timing and where a is the ratio of the correct sampling frequency over the local sampling frequency. The controller computes three points on the phase detector characteristic and compares them to decide what control signal (+ or -) should be sent to the VCO.

Consequently, a novel non-data-aided symbol timing synchronizer for M-ary phase-shift-keying (MPSK) modulation schemes was studied at the NASA Glenn Research Center. It calculates the post demodulation baseband signal energy in a sliding window. If the symbol timing is correct, the average signal energy will be the maximum. On the basis of this principle, the synchronizer detects the phase errors and/or frequency errors. The synchronizer structure is designed and simulated using MATLAB/Simulink. The following

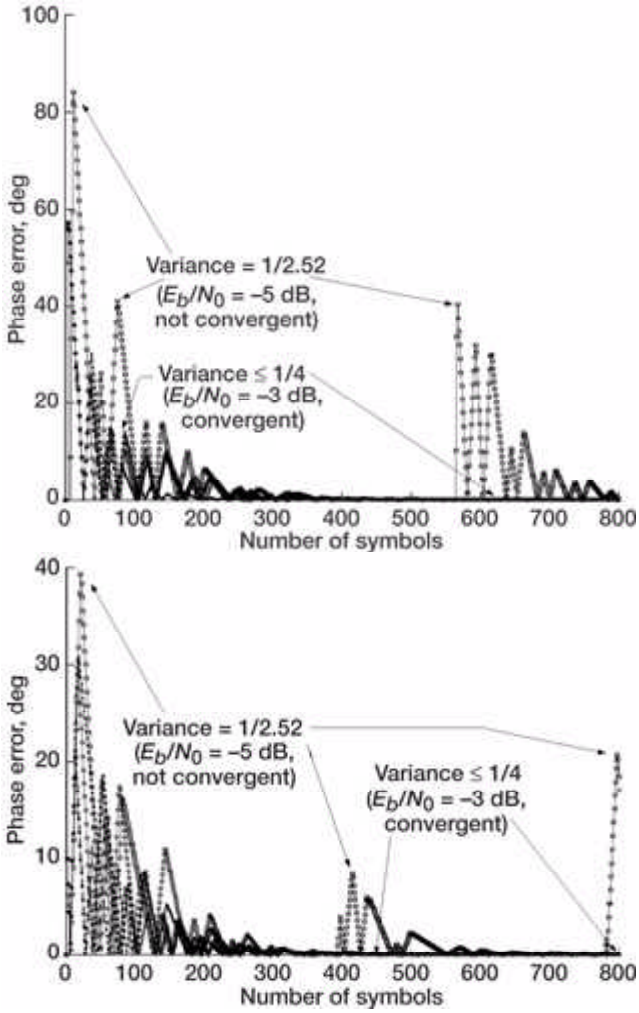
block diagram shows the robust sliding-window average (SWA) synchronizer. The *I* (in-phase) and *Q* (quadrature-phase) channel baseband signals are digitized by the analog-to-digital converter (ADC) and sent to two shift registers, respectively. The sampling clock is generated by the voltage-controlled oscillator (VCO), and the shift registers act as two simultaneous sliding windows. At the symbol rate, the *K* samples of *I* and *Q* channels in the window are summed and squared, and the results are added to form the signal *W*(*n*) at the adder output. When the local symbol clock and the incoming data symbol clock are synchronized, the output of the adder is the maximum. The control algorithm computes the control signal (+ or -) to send to the VCO as it attempts to obtain the maximum *W*(*n*).



MatLab-Simulink simulation program for the sliding-window symbol synchronizer.
Long description. Simulation model of the sliding-window average (SWA) synchronizer. The performance is evaluated in an added white gaussian noise (AWGN) channel. The synchronizer model consists of an eight-tap delay line, two shifters, summers and squarers for the in-phase (I) and quadrature-phase (Q) baseband channels, a serial-to-parallel converter, the SWA, a controller, and a voltage-controlled oscillator (VCO). The output of the delay line is summed and squared at each sample time. The summed and squared signals from both the I and Q branches are then added and fed into a serial-to-parallel converter. Each sample period, the parallel data are forwarded to the SWA of length 128. These data are then sent to the control algorithm, which in turn adjusts the VCO to achieve phase and frequency lock with the incoming data.

A simulation model of the SWA synchronizer is shown in the diagram on the next page. The performance is evaluated in an added white gaussian noise (AWGN) channel. The synchronizer model consists of an eight-tap delay line for the*I* and *Q* baseband channels. The output of the delay line is summed and squared each sample time. Then, these data are added and fed into a serial-to-parallel converter. Each sample period, the parallel data are forwarded to the SWA of length 128. The data are then sent to the control algorithm, which in turn adjusts the VCO to achieve phase and frequency lock with the incoming data.

Simulations for 45° and 90° phase errors are shown in the graphs on the next page. The synchronizer can achieve phase lock for a ratio of symbol energy to noise energy E_s/N_0 as low as 0 dB (E_b/N_0= -3 dB for quadrate phase shift keying, QPSK) with a convergence time less than 100 symbols. For comparison, when the old popular early-late-gate symbol timing synchronizer was simulated, the minimum working E_b/N_0 was 3 dB, which is 6 dB higher than for the SWA synchronizer with about the same convergence time. Because the sliding-window symbol timing synchronizer can work at a very low signal-to-noise ratio, the modem can work in unconventionally noisy environments, which include aeronautical satellite communications.



Left: Phase error versus symbol count for initial phase error of 1 tap (45°). Right: Phase error versus symbol count for initial phase error of 2 taps (90°).

Research on robust carrier synchronization and pseudonoise (PN) code acquisition and tracking is needed to further improve the robustness of a code division multiple access (CDMA) communications satellite for aeronautical applications. The SWS will be useful in the development of the new PN code tracking scheme. This research will support the newly initiated NASA Exploratory Technology for National Air Space (NExTNAS).

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