

individual cover glasses on the cells and serves as an additional unitary structural support that offers the advantage, relative to glass, of the robust, forgiving nature of the silicone material. The cover contains pockets that hold the solar cells in place during the lamination process. The cover is coated with indium tin oxide to make its surface electrically conductive, so that it serves as a contiguous, electrically grounded electromagnetic shield over the entire panel surface.

The cells are mounted in proximity to metallic printed wiring. The printed-wiring layer comprises metal-film traces on a sheet of Kapton (or equivalent) polyimide. The traces include contact

pads on one side of the sheet for interconnecting the cells. Return leads are on the opposite side of the sheet, positioned to form the return currents substantially as mirror images of, and in proximity to, the cell sheet currents, thereby minimizing magnetic moments. The printed-wiring arrangement mimics the back-wiring arrangement of conventional solar arrays, but the current-loop areas and the resulting magnetic moments are much smaller because the return-current paths are much closer to the solar-cell sheet currents.

The contact pads are prepared with solder for electrical and mechanical bonding to the cells. The pocketed cover/shield,

the solar cells, the printed-wiring layer, an electrical-bonding agent, a mechanical-bonding agent, a composite structural front-side face sheet, an aluminum honeycomb core, and a composite back-side face sheet are all assembled, then contact pads are soldered to the cells and the agents are cured in a single lamination process.

This work was done by Theodore G. Stern and Anthony E. Kenniston of DR Technologies, Inc. for Glenn Research Center.

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4-8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18156-1.

Logic Gates Made of N-Channel JFETs and Epitaxial Resistors

Gates could be implemented in SiC ICs for operation at high temperatures.

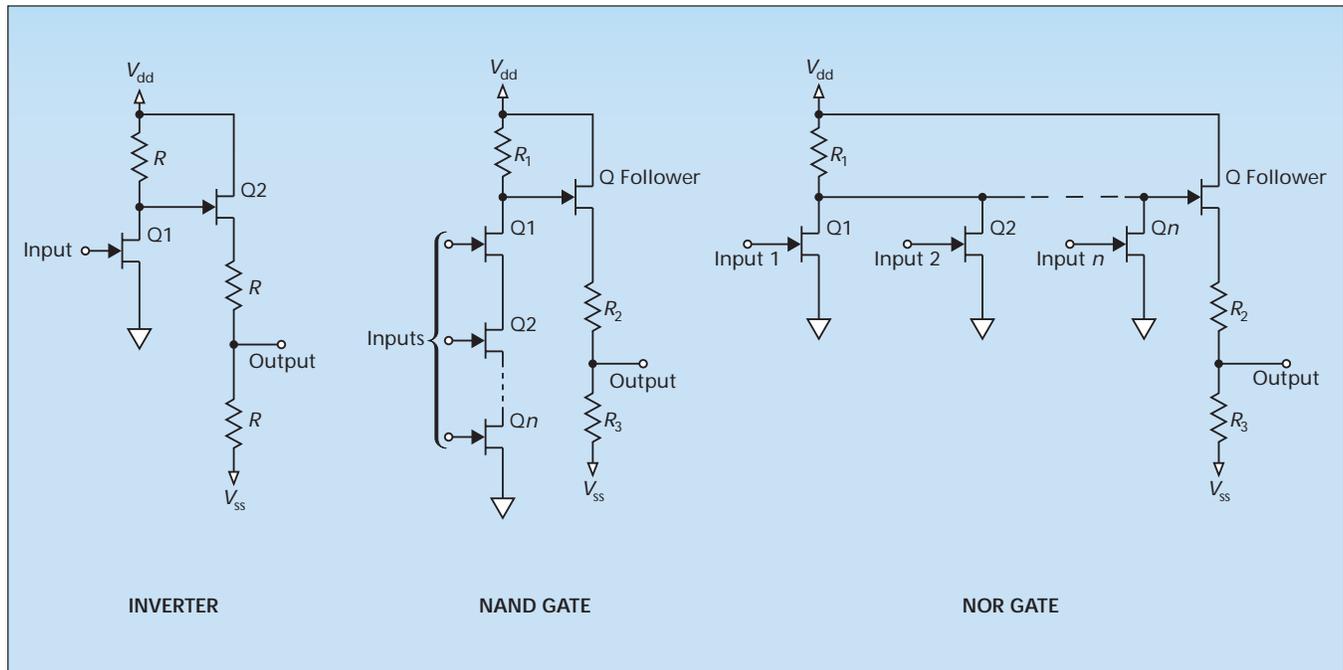
John H. Glenn Research Center, Cleveland, Ohio

Prototype logic gates made of n-channel junction field-effect transistors (JFETs) and epitaxial resistors have been demonstrated, with a view toward eventual implementation of digital logic devices and systems in silicon carbide (SiC) integrated circuits (ICs). This development is intended to exploit the inherent ability of SiC electronic devices to function at temperatures from 300 to somewhat above 500 °C and withstand large doses of ionizing radiation. SiC-based

digital logic devices and systems could enable operation of sensors and robots in nuclear reactors, in jet engines, near hydrothermal vents, and in other environments that are so hot or radioactive as to cause conventional silicon electronic devices to fail.

At present, current needs for digital processing at high temperatures exceed SiC integrated circuit production capabilities, which do not allow for highly integrated circuits. Only single to small

number component production of depletion mode n-channel JFETs and epitaxial resistors on a single substrate is possible. As a consequence, the fine matching of components is impossible, resulting in rather large direct-current parameter distributions within a group of transistors typically spanning multiples of 5 to 10. Add to this the lack of p-channel devices to complement the n-channel FETs, the lack of precise dropping diodes, and the lack of en-



This Inverter, NAND Gate, and NOR Gate are examples of logic circuits designed according to the principles described in the text. Other gates having greater complexity have also been designed.

hancement mode devices at these elevated temperatures and the use of conventional direct coupled and buffered direct coupled logic gate design techniques is impossible.

The presented logic gate design is tolerant of device parameter distributions and is not hampered by the lack of complementary devices or dropping diodes. In addition to n-channel JFETs, these gates include level-shifting and load re-

sistors (see figure). Instead of relying on precise matching of parameters among individual JFETs, these designs rely on choosing the values of these resistors and of supply potentials so as to make the circuits perform the desired functions throughout the ranges over which the parameters of the JFETs are distributed. The supply rails V_{dd} and V_{ss} and the resistors R are chosen as functions of the distribution of direct-current op-

erating parameters of the group of transistors used.

This work was done by Michael J. Krawski of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4-8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18256-1.

Improved Short-Circuit Protection for Power Cells in Series

Lyndon B. Johnson Space Center, Houston, Texas

A scheme for protection against short circuits has been devised for series strings of lithium electrochemical cells that contain built-in short-circuit protection devices, which go into a high-resistance, current-limiting state when heated by excessive current. If cells are simply connected in a long series string to obtain a high voltage and a short circuit occurs, whichever short-circuit protection device trips first is exposed to nearly the full string voltage, which, typically, is

large enough to damage the device. Depending on the specific cell design, the damage can defeat the protective function, cause a dangerous internal short circuit in the affected cell, and/or cascade to other cells.

In the present scheme, reverse diodes rated at a suitably high current are connected across short series sub-strings, the lengths of which are chosen so that when a short-circuit protection device is tripped, the voltage across it

does not exceed its rated voltage. This scheme preserves the resetting properties of the protective devices. It provides for bypassing of cells that fail open and limits cell reversal, though not as well as does the more-expensive scheme of connecting a diode across every cell.

This work was done by Francis Davies of Hernandez Engineering Inc. for Johnson Space Center. Further information is contained in a TSP (see page 1). MSC-23446-1

Communication Limits Due to Photon-Detector Jitter

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A theoretical and experimental study was conducted of the limit imposed by photon-detector jitter on the capacity of a pulse-position-modulated optical communication system in which the receiver operates in a photon-counting (weak-signal) regime. Photon-detector jitter is a random delay between impingement of a photon and generation of an electrical pulse by the detector.

In the study, jitter statistics were computed from jitter measurements made on several photon detectors. The proba-

bility density of jitter was mathematically modeled by use of a weighted sum of Gaussian functions. Parameters of the model were adjusted to fit histograms representing the measured-jitter statistics. Likelihoods of assigning detector-output pulses to correct pulse time slots in the presence of jitter were derived and used to compute channel capacities and corresponding losses due to jitter.

It was found that the loss, expressed as the ratio between the signal power needed to achieve a specified capacity

in the presence of jitter and that needed to obtain the same capacity in the absence of jitter, is well approximated as a quadratic function of the standard deviation of the jitter in units of pulse-time-slot duration.

This work was done by Bruce E. Moision and William H. Farr of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-45809