Spaceborne Hybrid-FPGA System for Processing FTIR Data

NASA's Jet Propulsion Laboratory, Pasadena, California

Progress has been made in a continuing effort to develop a spaceborne computer system for processing readout data from a Fourier-transform infrared (FTIR) spectrometer to reduce the volume of data transmitted to Earth. The approach followed in this effort, oriented toward reducing design time and reducing the size and weight of the spectrometer electronics, has been to exploit the versatility of recently developed hybrid field-programmable gate arrays (FPGAs) to run diverse software on embedded processors while also taking advantage of the reconfigurable hardware resources of the FPGAs.

The specific FPGA/embedded-processor combination selected for this effort is the Xilinx Virtex-4 FX hybrid FPGA with one of its two embedded IBM PowerPC 405 processors. The effort has involved exploration of various architectures and hardware and software optimizations. By including a dedicated floating-point unit and a dot-product coprocessor in the hardware and utilizing optimized single-precision math library functions and a modified PowerPC performance library in the software, it has been possible to reduce execution time to an eighth of that of a non-optimized software-only implementation. A concept for utilizing both embedded PowerPC processors to further reduce execution time has also been considered.

This work was done by Dmitriy L. Bekker, Jean-Francois L. Blavier, and Paula J. Pingree of Caltech and Marcin Lukowiak and Muhammad Shaaban of Rochester Institute of Technology for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-45957

FPGA Coprocessor for Accelerated Classification of Images

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An effort related to that described in the preceding article focuses on developing a spaceborne processing platform for fast and accurate onboard classification of image data, a critical part of modern satellite image processing. The approach again has been to exploit the versatility of recently developed hybrid Virtex-4FX field-programmable gate array (FPGA) to run diverse science applications on embedded processors while taking advantage of the reconfigurable hardware resources of the FPGAs. In this case, the FPGA serves as a coprocessor that implements legacy C-language support-vector-machine (SVM) image-classification algorithms to detect and identify natural phenomena such as flooding, volcanic eruptions, and sea-ice break-up. The FPGA provides hardware acceleration for increased onboard processing capability than previously demonstrated in software.

The original C-language program — demonstrated on an imaging instrument aboard the Earth Observing-1 (EO-1) satellite — implements a linear-kernel SVM algorithm for classifying parts of the images as snow, water, ice, land, or cloud or unclassified. Current onboard processors, such as on EO-1, have limited computing power, extremely limited active storage capability and are no longer considered state-of-the-art. Using commercially available software that translates C-language programs into hardware description language (HDL) files, the legacy C-language program, and two newly formulated programs for a more capable expanded-linear-kernel and a more accurate polynomial-kernel SVM algorithm, have been implemented in the Virtex-4FX FPGA. In tests, the FPGA implementations have exhibited significant speedups over conventional software implementations running on general-purpose hardware.

This work was done by Paula J. Pingree, Lucas J. Scharenbroich, and Thomas A. Werne of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-45961

SiC JFET Transistor Circuit Model for Extreme Temperature Range

Simple modifications of common silicon model provide reasonable approximation from 25 to 500 °C.

John H. Glenn Research Center, Cleveland, Ohio

A technique for simulating extreme-temperature operation of integrated circuits that incorporate silicon carbide (SiC) junction field-effect transistors (JFETs) has been developed. The technique involves modification of NGSPICE, which is an open-source version of the popular Simulation Program with Integrated Circuit Emphasis (SPICE) general-purpose analog-integrated-circuit-simulating software. NGSPICE in its unmodified form is used for simulating and designing circuits made from silicon-based transistors that operate at or near room temperature.

Two rapid modifications of NGSPICE source code enable SiC JFETs to be simulated to 500 °C using the well-known "Level 1" model for silicon metal oxide semiconductor field-effect transistors (MOSFETs). First, the default value of the MOSFET surface potential must be changed. In the unmodified source code, this parameter has a value of 0.6,

which corresponds to slightly more than half the bandgap of silicon. In NGSPICE modified to simulate SiC JFETs, this parameter is changed to a value of 1.6, corresponding to slightly more than half the bandgap of SiC. The second modification consists of changing the temperature dependence of MOSFET transconductance and saturation parameters. The unmodified NGSPICE source code implements a $T^{-1.5}$ temperature dependence for these parameters. In order to mimic the temperature behavior of experimental SiC JFETs, a $T^{-1.3}$ temperature dependence must be implemented in the NGSPICE source code.

Following these two simple modifications, the "Level 1" MOSFET model of the NGSPICE circuit simulation program reasonably approximates the measured high-temperature behavior of experimental SiC JFETs properly operated with zero or reverse bias applied to the gate terminal. Modification of additional silicon parameters in the NGSPICE source code was not necessary to model experimental SiC JFET current-voltage performance across the entire temperature range from 25 to 500 °C.

This work was done by Philip G. Neudeck of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18342-1.

TDR Using Autocorrelation and Varying-Duration Pulses

Signal-to-noise ratios may be increased.

John F. Kennedy Space Center, Florida

In an alternative to a prior technique of time-domain-reflectometry (TDR) in which very short excitation pulses are used, the pulses have very short rise and fall times and the pulse duration is varied continuously between a minimum and a maximum value. In both the present and prior techniques, the basic idea is to (1) measure the times between the generation of excitation pulses and the reception of reflections of the pulses as indications of the locations of one or more defects along a cable and (2) measure the amplitudes of the reflections as indication of the magnitudes of the defects.

In general, an excitation pulse has a duration T. Each leading and trailing edge of an excitation pulse generates a reflection from a defect, so that a unique pair of reflections is associated with each defect. In the present alternative technique, the processing of the measured reflection signal includes computation of the autocorrelation function

$$R(\tau) \equiv \int x(t)x(t-\tau)dt$$

where t is time, $x(t)$ is the measured reflection signal at time t, and τ is the correlation interval. The integration is performed over a measurement time interval short enough to enable identification and location of a defect within the corresponding spatial interval along the cable. Typically, where there is a defect, $R(\tau)$ exhibits a negative peak having maximum magnitude for τ in the vicinity of T. This peak can be used as a means of identifying a leading-edge/trailing-edge reflection pair.

For a given spatial interval, measurements are made and $R(\tau)$ computed, as described above, for pulse durations T ranging from the minimum to the maximum value. The advantage of doing this is that the effective signal-to-noise ratio may be significantly increased over that attainable by use of a fixed pulse duration T.

This work was done by Angel Lucena, Pam Mullinex, PoTien Huang, and Josephine Santiago of Kennedy Space Center and Pedro Medelius, Carlos Mata, Carlos Zavala, and John Lane of ASRC Aerospace Corp. Further information is contained in a TSP (see page 1).

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Update on Development of SiC Multi-Chip Power Modules

Modules and a modular power system have been built and tested.

John H. Glenn Research Center, Cleveland, Ohio

Progress has been made in a continuing effort to develop multi-chip power modules (SiC MCPMs). This effort at an earlier stage was reported in "SiC Multi-Chip Power Modules as Power-System Building Blocks" (LEW-18008-1), *NASA Tech Briefs*, Vol. 31, No. 2 (February 2007), page 28.

The following unavoidably lengthy recapitulation of information from the cited prior article is prerequisite to a meaningful summary of the progress made since then:

- SiC MCPMs are, more specifically, electronic power-supply modules containing multiple silicon carbide power integrated-circuit chips and silicon-on-insulator (SOI) control integrated-circuit chips. SiC MCPMs are being developed as building blocks of advanced expandable, reconfigurable, fault-tolerant power-supply systems. Exploiting the ability of SiC semiconductor devices to operate at temperatures, breakdown voltages, and current densities significantly greater than those of conventional Si devices, the designs of SiC MCPMs and of systems comprising multiple SiC MCPMs are expected to afford a greater degree of miniaturization through stacking of modules with reduced requirements for heat sinking.
- The stacked SiC MCPMs in a given system can be electrically connected in series, parallel, or a series/parallel combination to increase the overall power-handling capability of the system. In addition to power connections, the modules have communication connections. The SOI controllers in the modules communicate with each other as nodes of a decentralized control network, in which no single controller exerts overall command of the system. Control functions effected via the network include synchronization of switching of power devices and rapid reconfiguration of power connections to