Figure 2. **Drain-Source Current vs Drain–Source Voltage Characteristics** are shown for the split gate field-effect transistor at different gate-source voltages.

and is controlled by applying either 0 or –10 volts to each of the gate electrodes. When –10 volts are simultaneously applied to both gates, the transistor is conductive (ON), while any other combination of gate voltages renders the transistor highly resistive (OFF). The p-type carrier charge mobility is about $5 \times 10^{-4} cm^2/V\text{-}s$. The low mobility is attributed to the sharp contours of the RRP3HT film between the drain and the source contacts, and to defects in the RRP3HT film itself.

The device substrates are fabricated with a starting wafer that is n-type doped Si (10 ohm-cm), with a 200-nm thick, ther-mally grown oxide layer. First, the gate metals, comprising 20-nm Cr/100-nm Au, are vacuum deposited in a thermal evaporator and patterned using conventional photolithographic and liftoff techniques. Next, a 100-nm-thick silicon nitride (Si_3N_4) film is deposited over this using chemical vapor deposition (CVD). Access to the gate metallization is obtained by etching windows into the silicon nitride. The source and drain metallization, comprising 20-nm Cr/100-nm Au, is deposited on the CVD-grown silicon nitride on either side of the buried split gates using conventional photolithographic and liftoff techniques. The electrode "fingers" are about 20 microns wide and 600 microns long. The spacing between the electrodes is approximately 4 microns.

The split-gate architecture for logic circuitry is demonstrated via a two-input logic AND circuit. To create the device, a 10-Megohm load resistor is connected between the ground and the transistor source terminals, with the two gate terminals serving as the inputs. The output (V_R) is taken at the source terminal across the load resistor. A low frequency (0.01 Hz) square-wave signal serves as the input gate bias. For all combinations of V_{GS1} and V_{GS2}, except $V_{GS1} = V_{GS2} = -10$ V, the transistor is in the resistive "OFF" state, and -0.3 mV $< V_R < 0$ V. For $V_{GS1} = V_{GS2} - 10$ V, the transistor is in the more conductive "ON" state, causing a greater portion of the voltage drop to occur across the load resistor. As a result, V_R is a more negative value (-1.8 mV$< V_R < -1.7$ mV).

When the device functions as an AND logic circuit, V_{GS1} and V_{GS2} are functions of time, while corresponding change in the output of voltage V_R is a function of time for the four possible combinations of V_{GS1} and $V_{GS2} = 0$ or -10 V. Larger outputs are observed only when both gates are simultaneously biased "high."

High-Density, High-Bandwidth, Multilevel Holographic Memory
Multiple terabytes could be read or written at a multigigahertz rate.

NASA's Jet Propulsion Laboratory, Pasadena, California

A proposed holographic memory system would be capable of storing data at unprecedentedly high density, and its data-transfer performance in both reading and writing would be characterized by exceptionally high bandwidth. The capabilities of the proposed system would greatly exceed even those of a state-of-the art memory system, based on binary holograms (in which each pixel value represents 0 or 1), that can hold ≈1 terabyte of data and can support a reading or writing rate as high as 1 Gb/s.

The storage capacity of the state-of-the-art system cannot be increased without also increasing the volume and mass of the system. However, in principle, the storage capacity could be increased greatly, without significantly increasing the volume and mass, if multilevel holograms were used instead of binary holograms. For example, a 3-bit (8-level) hologram could store 8 terabytes, or an 8-bit (256-level) hologram could store 256 terabytes, in a system having little or no more size and mass than does the state-of-the-art 1-terabyte binary holographic memory.

The proposed system would utilize multilevel holograms. The system (see figure) would include lasers, imaging lenses and other beam-forming optics, a block photorefractive crystal wherein the holograms would be formed, and two multilevel spatial light modulators in the form of commercially available deformable-mirror-device spatial light modulators (DMDSLMs) made for use

in high-speed input conversion of data up to 12 bits. For readout, the system would also include two arrays of complementary metal oxide/semiconductor (CMOS) photodetectors matching the spatial light modulators. The system would further include a reference-beam-steering device (equivalent of a scanning mirror), containing no sliding parts, that could be either a liquid-crystal phased-array device or a microscopic mirror actuated by a high-speed micro-electromechanical system. Time-multiplexing and the multilevel nature of the DMDSLM would be exploited to enable writing and reading of multilevel holograms. The DMDSLM would also enable transfer of data at a rate of 7.6 Gb/s or perhaps somewhat higher.

This work was done by Tien-Hsin Chao of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

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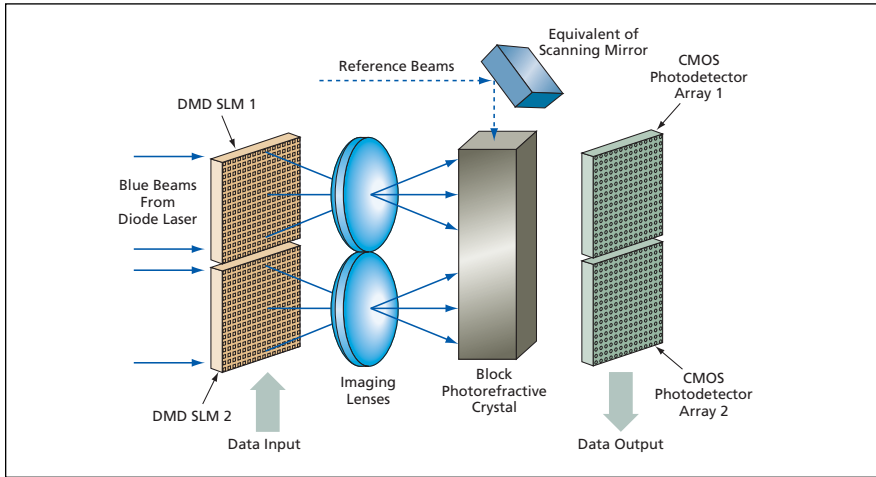
Multilevel Holograms would be written to, and read from, the photorefractive crystal in this holographic memory system.