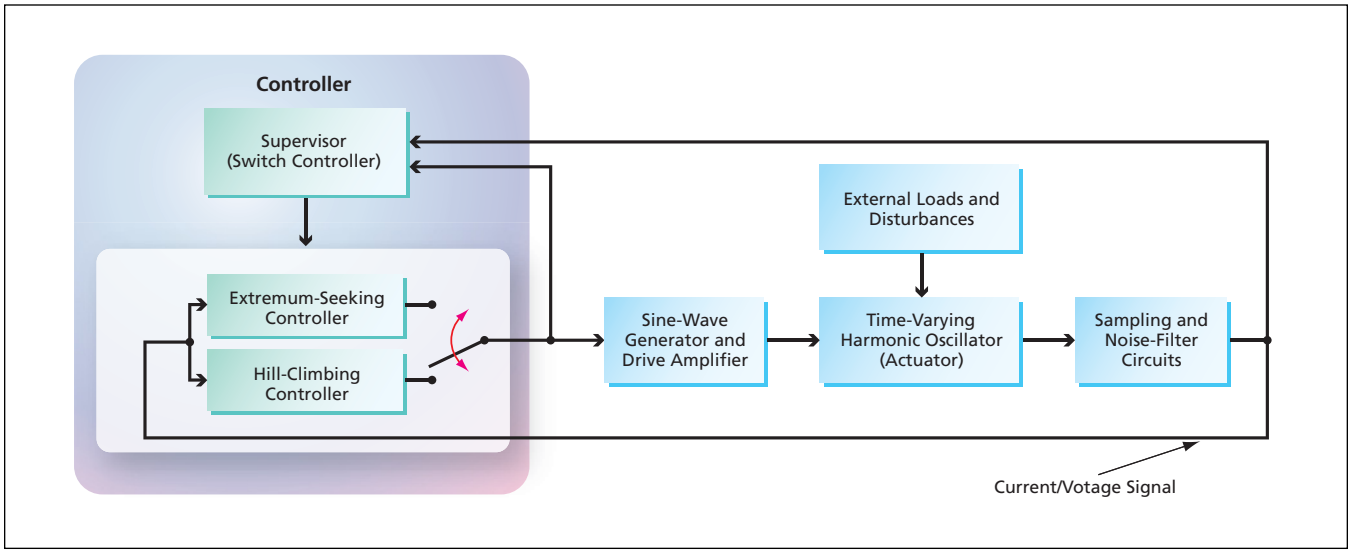

This **Resonance-Tracking Controller** includes three main subsystems that function together to effect a combination of coarse and fine frequency tracking optimized to maintain operation at a desired resonance and avoid undesired resonances.

For the purpose of the control algorithm, the performance of the actuator is quantified in terms of the ratio between the time-averaged drive-voltage amplitude and the time-averaged drive current amplitude during a sampling time period. In the hill-climbing algorithm, the excitation frequency during the next sampling period is incremented or decremented by an arbitrary fixed step. If the increment or decrement results in an increase in the current/voltage ratio, then the direction of change (increase or decrease, respectively) of frequency is accepted and another such change (increment or decrement, respectively) is made during the following sampling period. If, on the other hand, the increment or decrement results in a decrease in the current/voltage ratio, then the direction of change of frequency during the following sampling period is reversed. The process as described thus far is repeated, causing the current/voltage performance to climb to one of the resonance peaks and eventually to oscillate about the peak. In order to prevent climbing of one of the undesired higher-frequency resonance peaks, it is necessary to choose the starting excitation frequency near the desired peak and to impose a limit on the excursion from the starting frequency.

Once the excitation frequency has begun to oscillate about the peak, the supervisory algorithm switches operation to the ESC algorithm, which uses past as well as present input/output data to make a least-squares estimate of the resonance frequency. The estimation task involves updating two scalar parameters of a quadratic model that represents the input/output map of the actuator resonance. After each sampling period, the new input/output data pair is added to the collection of past data pairs, such that information regarding the input/output relationship of the actuator increases over time; in other words, as the input/output information comes in, the algorithm tries to improve the fit between the quadratic model near resonance and all the past input/output data up to the current time. Once the estimated parameters have converged sufficiently, the excitation frequency is updated according to a simple formula that represents a maximizer associated with the quadratic model. In the event that the estimates begin to diverge beyond a specified limit, the supervisory algorithm switches operation back to the hill-climbing algorithm.

This work was done by Jack Aldrich, Yoseph Bar-Cohen, Stewart Sherrit, Mircea Badescu, Xiaoqi Bao, and Zensheu Chang of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-43519

Coaxial Electric Heaters

These devices can be used safely where magnetic fields are not tolerated.

NASA's Jet Propulsion Laboratory, Pasadena, California

Coaxial electric heaters have been conceived for use in highly sensitive instruments in which there are requirements for compact heaters but stray magnetic fields associated with heater electric currents would adversely affect operation. Such instruments include atomic clocks and magnetometers that utilize heated atomic-sample cells, wherein stray magnetic fields at picotesla levels could introduce systematic errors into instrument readings.

A coaxial electric heater (see Figure 1) is essentially an axisymmetric coaxial cable, the outer conductor of which is deliberately made highly electrically resistive so that it can serve as a heating element. As in the cases of other axisymmetric coaxial cables, the equal-magnitude electric currents flowing in opposite directions along the inner and outer conductors give rise to zero net magnetic field outside the outer conductor. Hence, a coaxial electric heater can be placed near an atomic-sample cell or other sensitive device.

A coaxial electric heater can be fabricated from an insulated copper wire, the copper core of which serves as the inner conductor. For example, in one ap-

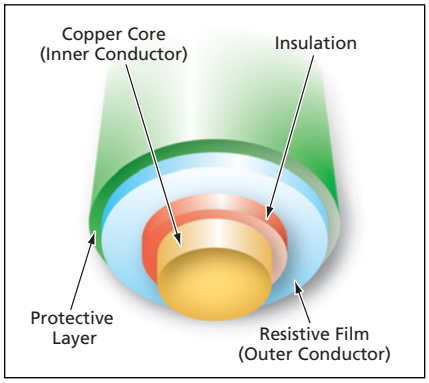

Figure 1. A **Typical Coaxial Electric Heater** as shown in cross section resembles conventional signal-transmission coaxial cables, except that its outer conductor is deliberately made highly resistive.

proach, the insulated wire is dipped in a colloidal graphite emulsion, then the emulsion-coated wire is dried to form a thin, uniform, highly electrically resistive film that serves as the outer conductor. Then the film is coated with a protective layer of high-temperature epoxy except at the end to be electrically connected to the power supply. Next, the insulation is stripped from the wire at that end. Finally, electrical leads from the heater power supply are attached to the exposed portions of the wire and the resistive film.

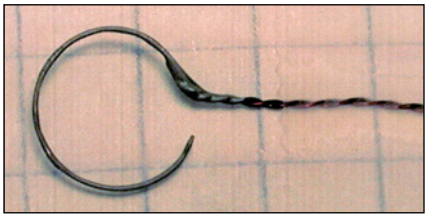

Figure 2. This **Coaxial Electric Heater**, shown here in a side view, was bent into a circular arc for edge heating of a circular window. This heater was made from copper wire of 0.01-in. (0.254-mm) diameter. Its resistance is about 2 kΩ.

The resistance of the graphite film can be tailored via its thickness. Alternatively, the film can be made from an electrically conductive paint, other than a colloidal graphite emulsion, chosen to impart the desired resistance. Yet another alternative is to tailor the resistance of a graphite film by exploiting the fact that its resistance can be changed permanently within about 10 percent by heating it to a temperature above 300 °C. Figure 2 depicts a coaxial heater, with electrical leads attached, that has been bent into an almost full circle for edge heating of a circular window. (In the specific application, there is a requirement for a heated cell window, through which an optical beam enters the cell.)

This work was done by Dmitry Strekalov, Andrey Matsko, Anatoliy Savchenkov, and Lute Maleki of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).
NPO-43569

Dual-Input AND Gate From Single-Channel Thin-Film FET

These transistors show potential as large-area, low-cost electronic circuitry on rigid and flexible substrates.

John H. Glenn Research Center, Cleveland, Ohio

A regio-regular poly(3-hexylthiophene) (RRP3HT) thin-film transistor having a split-gate architecture has been fabricated on a doped silicon/silicon nitride substrate and characterized. RRP3HT is a semiconducting polymer that has a carrier mobility and on/off ratio when used in a field effect transistor (FET) configuration. This commercially available polymer is very soluble in common organic solvents and is easily processed to form uniform thin films. The most important polymer-based device fabricated and studied is the FET, since it forms the building block in logic circuits and switches for active matrix (light-emitting-diode) (LED) displays, smart cards, and radio frequency identification (RFID) cards.

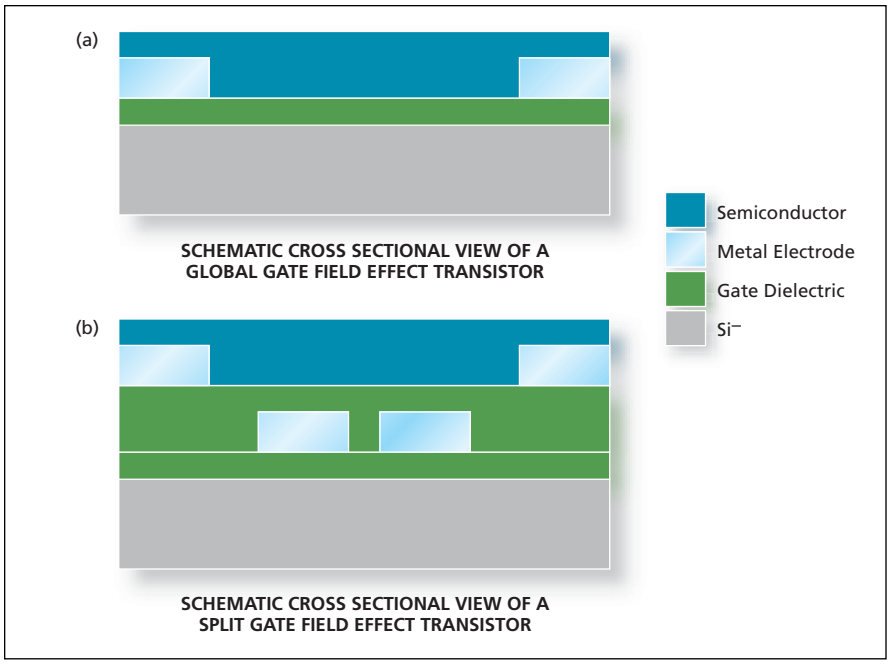

Figure 1. This cross-sectional view of the **Basic FET** shows (a) the global gate FET and (b) split-gate FET.

Figure 1(a) shows a schematic cross-sectional view of the basic FET using an insulating gate dielectric layer over a doped silicon substrate. Two metal leads patterned over the insulator serve as the source and drain terminals of the device while the doped silicon serves as the global gate electrode. In this basic configuration, the gate voltage is applied to the bottom side of the wafer. To complete the FET, an organic semiconducting channel is placed between the source and drain terminals either via electrochemical deposition, vacuum deposition, or spin coating of the semiconductor material, resulting in a two-dimensional thin-film morphology; or via electrospinning, resulting in a one-dimensional nanofibrous morphology. In the dual-input architecture shown in Figure 1(b), metal contacts are located beneath the gate dielectric, and are accessed from the top side of the wafer by vias etched into the gate dielectric and semiconducting layers. Each gate contact serves as a device input, thus allowing for the design of various types of logic gates.

The dual-input device demonstrates AND logic functionality (see Figure 2),