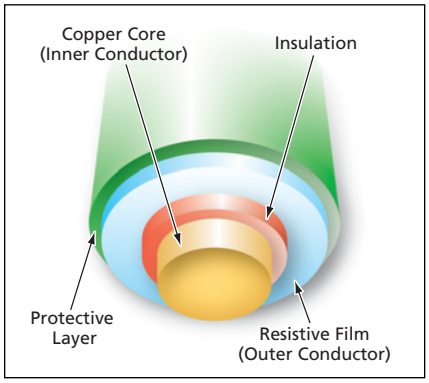

Figure 1. A **Typical Coaxial Electric Heater** as shown in cross section resembles conventional signal-transmission coaxial cables, except that its outer conductor is deliberately made highly resistive.

proach, the insulated wire is dipped in a colloidal graphite emulsion, then the emulsion-coated wire is dried to form a thin, uniform, highly electrically resistive film that serves as the outer conductor. Then the film is coated with a protective layer of high-temperature epoxy except at the end to be electrically connected to the power supply. Next, the insulation is stripped from the wire at that end. Finally, electrical leads from the heater power supply are attached to the exposed portions of the wire and the resistive film.

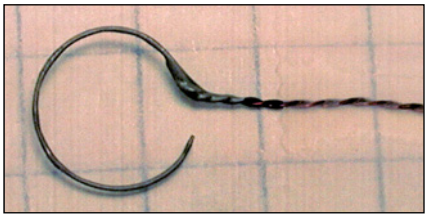

Figure 2. This **Coaxial Electric Heater**, shown here in a side view, was bent into a circular arc for edge heating of a circular window. This heater was made from copper wire of 0.01-in. (0.254-mm) diameter. Its resistance is about 2 kΩ.

The resistance of the graphite film can be tailored via its thickness. Alternatively, the film can be made from an electrically conductive paint, other than a colloidal graphite emulsion, chosen to impart the desired resistance. Yet another alternative is to tailor the resistance of a graphite film by exploiting the fact that its resistance can be changed permanently within about 10 percent by heating it to a temperature above 300 °C. Figure 2 depicts a coaxial heater, with electrical leads attached, that has been bent into an almost full circle for edge heating of a circular window. (In the specific application, there is a requirement for a heated cell window, through which an optical beam enters the cell.)

This work was done by Dmitry Strekalov, Andrey Matsko, Anatoliy Savchenkov, and Lute Maleki of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).
NPO-43569

Dual-Input AND Gate From Single-Channel Thin-Film FET

These transistors show potential as large-area, low-cost electronic circuitry on rigid and flexible substrates.

John H. Glenn Research Center, Cleveland, Ohio

A regio-regular poly(3-hexylthiophene) (RRP3HT) thin-film transistor having a split-gate architecture has been fabricated on a doped silicon/silicon nitride substrate and characterized. RRP3HT is a semiconducting polymer that has a carrier mobility and on/off ratio when used in a field effect transistor (FET) configuration. This commercially available polymer is very soluble in common organic solvents and is easily processed to form uniform thin films. The most important polymer-based device fabricated and studied is the FET, since it forms the building block in logic circuits and switches for active matrix (light-emitting-diode) (LED) displays, smart cards, and radio frequency identification (RFID) cards.

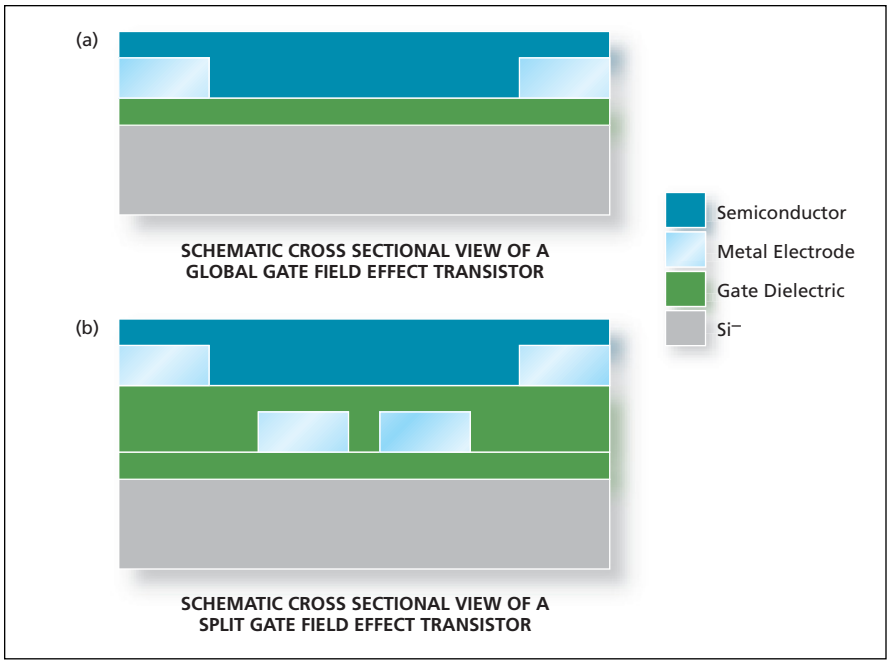

Figure 1. This cross-sectional view of the **Basic FET** shows (a) the global gate FET and (b) split-gate FET.

Figure 1(a) shows a schematic cross-sectional view of the basic FET using an insulating gate dielectric layer over a doped silicon substrate. Two metal leads patterned over the insulator serve as the source and drain terminals of the device while the doped silicon serves as the global gate electrode. In this basic configuration, the gate voltage is applied to the bottom side of the wafer. To complete the FET, an organic semiconducting channel is placed between the source and drain terminals either via electrochemical deposition, vacuum deposition, or spin coating of the semiconductor material, resulting in a two-dimensional thin-film morphology; or via electrospinning, resulting in a one-dimensional nanofibrous morphology. In the dual-input architecture shown in Figure 1(b), metal contacts are located beneath the gate dielectric, and are accessed from the top side of the wafer by vias etched into the gate dielectric and semiconducting layers. Each gate contact serves as a device input, thus allowing for the design of various types of logic gates.

The dual-input device demonstrates AND logic functionality (see Figure 2),

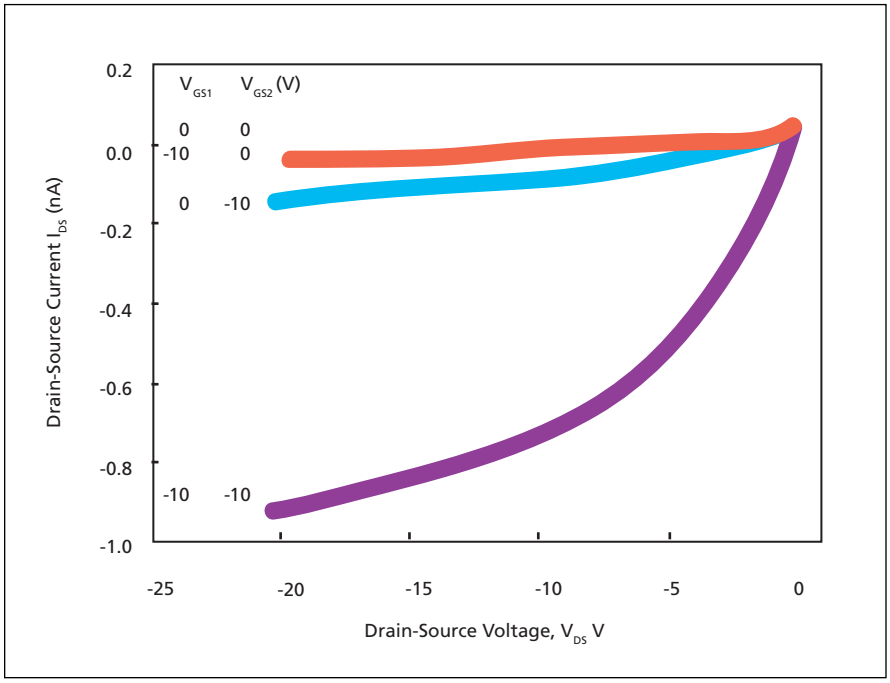

Figure 2. **Drain-Source Current vs Drain–Source Voltage Characteristics** are shown for the split gate field-effect transistor at different gate-source voltages.

and is controlled by applying either 0 or –10 volts to each of the gate electrodes. When –10 volts are simultaneously applied to both gates, the transistor is conductive (ON), while any other combination of gate voltages renders the transistor highly resistive (OFF). The p-type carrier charge mobility is about 5×10^{-4} cm^2/V-s. The low mobility is attributed to the sharp contours of the RRP3HT film between the drain and the source contacts, and to defects in the RRP3HT film itself.

The device substrates are fabricated with a starting wafer that is n-type doped Si (10 ohm-cm), with a 200-nm thick, thermally grown oxide layer. First, the gate metals, comprising 20-nm Cr/100-nm Au, are vacuum deposited in a thermal evaporator and patterned using conventional photolithographic and liftoff techniques. Next, a 100-nm-thick silicon nitride (Si_3N_4) film is deposited over this using chemical vapor deposition (CVD). Access to the gate metallization is obtained by etching windows into the silicon nitride. The source and drain metallization, comprising 20-nm Cr/100-nm Au, is deposited on the CVD-grown silicon nitride on either side of the buried split gates using conventional photolithographic and liftoff techniques. The electrode "fingers" are about 20 microns wide and 600 microns long. The spacing between the electrodes is approximately 4 microns.

The split-gate architecture for logic circuitry is demonstrated via a two-input logic AND circuit. To create the device, a 10-Megohm load resistor is connected between the ground and the transistor source terminals, with the two gate terminals serving as the inputs. The output (V_R) is taken at the source terminal across the load resistor. A low frequency (0.01 Hz) square-wave signal serves as the input gate bias. For all combinations of V_{GS1} and V_{GS2}, except $V_{GS1} = V_{GS2} = –10$ V, the transistor is in the resistive "OFF" state, and $–0.3 \text{ mV} < V_R < 0$ V. For $V_{GS1} = V_{GS2} – 10$ V, the transistor is in the more conductive "ON" state, causing a greater portion of the voltage drop to occur across the load resistor. As a result, V_R is a more negative value ($–1.8 \text{ mV} < V_R < –1.7 \text{ mV}$).

When the device functions as an AND logic circuit, V_{GS1} and V_{GS2} are functions of time, while corresponding change in the output of voltage V_R is a function of time for the four possible combinations of V_{GS1} and $V_{GS2} = 0$ or –10 V. Larger outputs are observed only when both gates are simultaneously biased "high."

This work was done by N. Theofylaktos and F.A. Miranda of Glenn Research Center; N.J. Pinto and R. Perez of the University of Puerto Rico-Humacao; and C.H. Mueller of Analex Corporation. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18214-1.

High-Density, High-Bandwidth, Multilevel Holographic Memory

Multiple terabytes could be read or written at a multigigahertz rate.

NASA's Jet Propulsion Laboratory, Pasadena, California

A proposed holographic memory system would be capable of storing data at unprecedentedly high density, and its data-transfer performance in both reading and writing would be characterized by exceptionally high bandwidth. The capabilities of the proposed system would greatly exceed even those of a state-of-the art memory system, based on binary holograms (in which each pixel value represents 0 or 1), that can hold ≈1 terabyte of data and can support a reading or writing rate as high as 1 Gb/s.

The storage capacity of the state-of-the-art system cannot be increased without also increasing the volume and mass of the system. However, in principle, the storage capacity could be increased greatly, without significantly increasing the volume and mass, if multilevel holograms were used instead of binary holograms. For example, a 3-bit (8-level) hologram could store 8 terabytes, or an 8-bit (256-level) hologram could store 256 terabytes, in a system having little or no more size and mass than does the state-of-the-art 1-terabyte binary holographic memory.

The proposed system would utilize multilevel holograms. The system (see figure) would include lasers, imaging lenses and other beam-forming optics, a block photorefractive crystal wherein the holograms would be formed, and two multilevel spatial light modulators in the form of commercially available deformable-mirror-device spatial light modulators (DMDSLMs) made for use