Fabrication of Gate-Electrode Integrated Carbon-Nanotube Bundle Field Emitters

Emission tips and a gate electrode are integrated into a monolithic device.

NASA's Jet Propulsion Laboratory, Pasadena, California

A continuing effort to develop carbon-nanotube-based field emitters (cold cathodes) as high-current-density electron sources has yielded an optimized device design and a fabrication scheme to implement the design. One major element of the device design is to use a planar array of bundles of carbon nanotubes as the field-emission tips and to optimize the critical dimensions of the array (principally, heights of bundles and distances between them) to obtain high area-averaged current density and high reliability over a long operational lifetime — a concept that was discussed in more detail in "Arrays of Bundles of Carbon Nanotubes as Field Emitters" (NPO-40817), *NASA Tech Briefs*, Vol. 31, No. 2 (February 2007), page 58. Another major element of the design is to configure the gate electrodes (anodes used to extract, accelerate, and/or focus electrons) as a ring that overhangs a recess wherein the bundles of nanotubes are located [see Figure 1(a)], such that by virtue of the proximity between the ring and the bundles, a relatively low applied potential suffices to generate the large electric field needed for emission of electrons.

A fabrication process to monolithically integrate multiple electrodes is as follows. The starting workpiece is a commercially available double silicon-on-insulator (SOI) wafer comprising, from top layer to the bottom, a silicon device layer (1), a silicon dioxide (buried oxide) layer (2), another silicon device layer (3) on top of a silicon dioxide (buried oxide) layer (4), and a thick silicon substrate (bottom) layer (5). A schematic representation of the starting substrate is shown in Figure 2(a). After lithographic patterning followed by a combination of wet etching, deep reactive-ion etching (DRIE) and isotropic silicon etch by xenon difluoride (XeF_2) gas, overhanging gate and undercutting recess profiles are defined in the substrate. The iron catalytic dots are prepared at the bottom surface of the hole and carbon nanotube bundles are grown from them. Figures 1(a) shows a 3-D sketch and (b) shows an SEM micro-

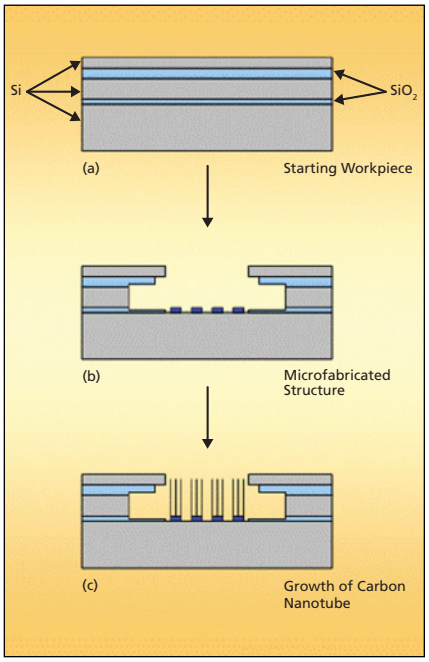
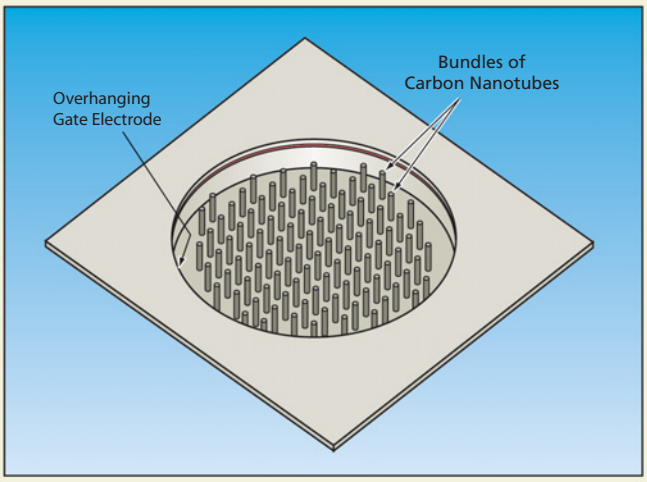
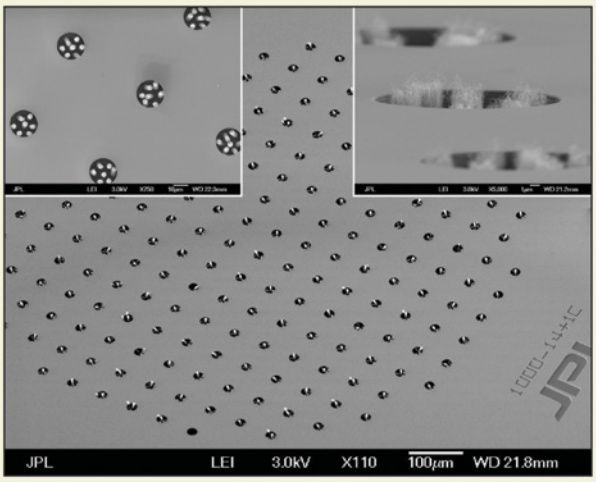


Figure 2. These are **Simplified Cross Sections** (not to scale) of the device of Figure 1 at various stages of fabrication.



(a)



(b)

Figure 1. A **Gate Electrode Overhangs** a recess containing an array of bundles of carbon nanotubes (see part a). In part (b) are scanning electron micrograph (SEM) images of fabricated field-emitter devices.

graph of a completed device. In a completed device, the layer (1) acts as the gate electrode and layer (3) provides the mechanical support to achieve overhanging. However, layer (3) can also be used as an additional electrode for beam tailoring if required. Similarly, by using multiple-silicon-layer SOI substrates, monolithic integration of multiple electrodes can be achieved.

This work was done by Risaku Toda, Michael Bronikowski, Edward Luong, and Harish Manohara of Caltech for NASA's Jet Propulsion Laboratory.

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

Innovative Technology Assets Management
JPL
Mail Stop 202-233
4800 Oak Grove Drive
Pasadena, CA 91109-8099
E-mail: iaoffice@jpl.nasa.gov

Refer to NPO-44996, volume and number of this NASA Tech Briefs *issue, and the page number.*