those locations. The magnitudes of both the permittivity and the dielectric loss of a ferroelectric material are reduced by application of a DC field. Because the concentration of the DC field in the constriction(s) magnifies the permittivity- and loss-reducing effects of the applied DC voltage, the permittivity and dielectric loss in the constriction(s) are smaller in the constriction(s) than they are in the wider parts of the ferroelectric film. Furthermore, inasmuch as displacement current must flow through either the constriction(s) or the low-loss dielectric substrate, the net effect of the constriction(s) is equivalent to that of incorporating one or more low-loss, low-permittivity region(s) in series with the high-loss, high-permittivity regions. In a series circuit, the properties of the low-capacitance series element (in this case, the constriction) dominate the overall performance. Concomitantly, the capacitance between the metal terminals is reduced.

By making the capacitance between the metal terminals small but tunable, a constriction increases the upper limit of the frequency range amenable to ferroelectric tuning. The present patterning concept is expected to be most advantageous for devices and circuits that must operate at frequencies from about 4 to about 60 GHz. A constriction can be designed such that the magnitude of the microwave electric field and the effective width of the region occupied by the microwave electric field become functions of the applied DC electric field, so that tunability is enhanced. It should even be possible to design the constriction to obtain a specific tuning-versus-voltage profile.

This work was done by Félix A. Miranda of Glenn Research Center and Carl H. Mueller of Analex Corp. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-17411.

Micron-Accurate Laser Fresnel-Diffraction Ranging System

This system would exploit the variation of Fresnel diffraction with distance.

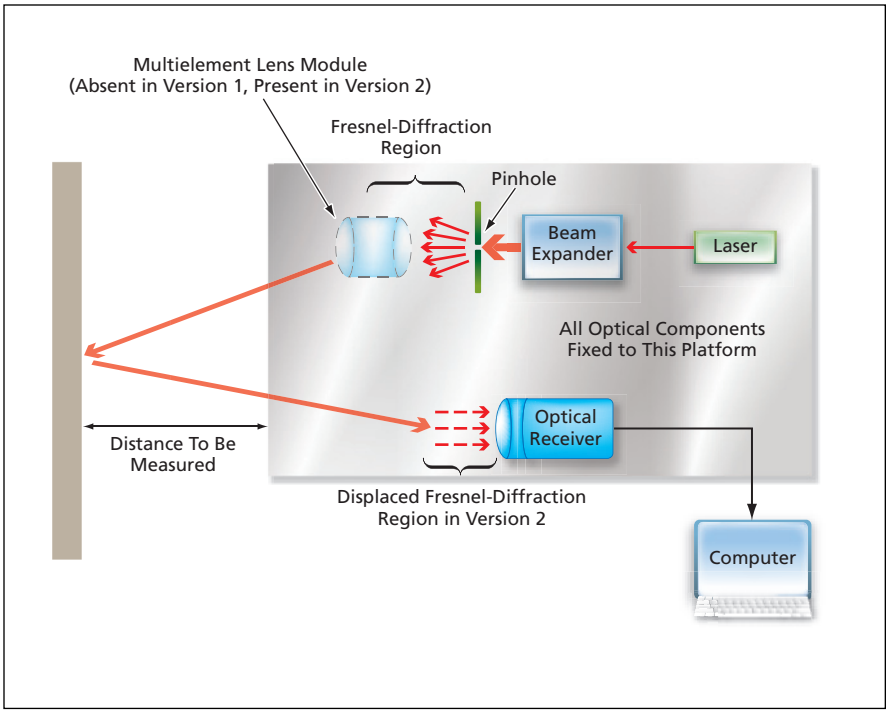
Marshall Space Flight Center, Alabama

The figure schematically depicts two versions of an optoelectronic system, undergoing development at the time of reporting the information for this article, that is expected to be capable of measuring a distance between 2 and 10 m with an error of no more than 1 μm. The system would be designed to exploit Fresnel diffraction of a laser beam. In particular, it would be designed to take advantage of the fact that a Fresnel diffraction pattern is ultrasensitive to distance.

In either version, a Fresnel diffraction pattern would be generated by aiming a laser beam at a pinhole, the size of which could be varied. The diffracted laser light would illuminate the object, the distance to which was to be measured. The diffracted laser light reflected from that object would be collected by an optical receiver comprising a telescope equipped with an imaging photodetector array at its focal plane. The resulting Fresnel-diffraction-pattern readout from the array would be digitized and sent to a computer. In principle, the digitized Fresnel diffraction pattern could be compared computationally with a set of known Fresnel diffraction patterns for known distances. Once a match was found, the distance of the observed Fresnel pattern would be determined to within a micron. The range of the system would be limited only by the power of the laser, the maximum laser power tolerated by the optical train of the system, and the sensitivity of the photodetector array.

The two versions would differ in the following respects:

- In version 1, the focus of the telescope would be in the Fresnel region, and the telescope would have a small depth of focus. As a consequence, the Fresnel pattern would be imaged directly onto the photodetector array.
- In version 2, a multielement lens module would displace the Fresnel region from the vicinity of the pinhole to the vicinity of the optical receiver. As the distance to be measured varied, the location of the receiver relative to the displaced Fresnel-diffraction region would



An **Object Would Be Illuminated** with a Fresnel-diffracted laser beam. The distance to the object would be determined by, in effect, inverting the known dependence of the diffraction pattern upon the distance.

vary, thereby causing the Fresnel diffraction pattern on the focal plane to vary. The multielement lens module would also correct for aberrations.

The processing of the digitized Fresnel diffraction pattern in the computer might be accelerated by using only parts of the pattern or even only one small part — the central pixel. As the distance from the pinhole increased, the central pixel would rapidly cycle between maximum and minimum light intensity. This in itself would not be sufficient to uniquely determine the distance. However, by varying the size of the pinhole or the wavelength of the laser, one could obtain a second cycle of variation of intensity that, in conjunction with the first cycle, could enable a unique determination of distance. Alternatively, for a single wavelength and a single pinhole size, it should suffice to consider the data from only two different key pixels in the Fresnel pattern.

This work was done by David Lehner, Jonathan Campbell, and Kelly Smith of Marshall Space Flight Center; Duncan Earl and Alvin Sanders of the University of Tennessee; Stephen Allison of Oak Ridge National Laboratory; and Larry Smalley of the University of Alabama in Huntsville.

This invention is owned by NASA, and a patent application has been filed. For further information, contact Sammy Nabors, MSFC Commercialization Assistance Lead, at sammy.a.nabors@nasa.gov. Refer to MFS-31649-1.

Efficient G^{4}FET-Based Logic Circuits

Fewer G^{4}FETs than conventional transistors would be needed to implement logic functions.

NASA's Jet Propulsion Laboratory, Pasadena, California

A total of 81 optimal logic circuits based on four-gate field-effect transistors (G^{4}FETs) have been designed to implement all Boolean functions of up to three variables. The purpose of this development was to lend credence to the expectation that logic circuits based on G^{4}FETs could be more efficient (in the sense that they could contain fewer transistors), relative to functionally equivalent logic circuits based on conventional transistors.

The theoretical basis of this development was summarized in "G^{4}FETs as Universal and Programmable Logic Gates" (NPO-41698) *NASA Tech Briefs*, Vol. 31, No. 7 (July 2007), page 44. To recapitulate: A G^{4}FET is a combination of a junction field-effect transistor (JFET) and a metal oxide/semiconductor field-effect transistor (MOSFET) superimposed in a single silicon island and can therefore be regarded as two transistors sharing the same body. A G^{4}FET can also be regarded as a single device having four gates: two side junction-based gates, a top MOS gate, and a back gate activated by biasing of a silicon-on-insulator substrate. Each of these gates can be used to control the conduction characteristics of the transistor; this possibility creates new options for designing analog, radio-frequency, mixed-signal, and digital circuitry. One such option is to design a G^{4}FET to function as a three-input NOT-majority gate, which has been shown to be a universal and programmable logic gate. The universality and programmability could be exploited to design logic circuits containing fewer discrete components than are required for conventional transistor-based circuits implementing the same logic functions.

Optimal NOT-majority-gate, G^{4}FET-based logic-circuit designs were obtained in a comparative study that also included formulation of functionally equivalent logic circuits based on NOR and NAND gates implemented by use of conventional transistors. [NOT gates (inverters) were also included, as needed, in both the G^{4}FET- and the NOR- and NAND-based designs.] In the study, the problem of finding the optimal design for each logic function and each transistor type was solved as an integer-programming optimization problem. The table summarizes results obtained in this study for the first four Boolean functions, showing that in most cases, fewer logic gates are needed in the NOT-majority (G^{4}FET) implementation than in the NOR- and

Function	NOT-Majority (G^{4}FET) Implementation		Conventional NOR Implementation		Conventional NAND Implementation	
	Number of NOT-Majority Gates	Number of NOT Gates	Number of NOR Gates	Number of NOT Gates	Number of NAND Gates	Number of NOT Gates
{1,0,0,0,0,0,0,0} = $\overline{A}\overline{B}\overline{C}$	2	1	2	1	4	3
{0,1,0,0,0,0,0,0} = $A\overline{B}\overline{C}$	2	1	3	1	4	2
{0,0,0,1,0,0,0,0} = $AB\overline{C}$	2	0	2	3	3	2
{0,0,0,0,0,0,0,1} = ABC	2	1	2	4	3	1

Numbers of Logic Gates were calculated for optimal circuits implementing several Boolean functions of the three input variables (A,B,C). Each entry in the "Function" column includes an octuple binary representation of the noted Boolean function, namely {f(0,0,0),f(0,0,1),f(0,1,0),f(0,1,1),f(1,0,0),f(1,0,1),f(1,1,0),f(1,1,1)}.