vary, thereby causing the Fresnel diffraction pattern on the focal plane to vary. The multielement lens module would also correct for aberrations.

The processing of the digitized Fresnel diffraction pattern in the computer might be accelerated by using only parts of the pattern or even only one small part — the central pixel. As the distance from the pinhole increased, the central pixel would rapidly cycle between maximum and minimum light intensity. This in itself would not be sufficient to uniquely determine the distance. However, by varying the size of the pinhole or the wavelength of the laser, one could obtain a second cycle of variation of intensity that, in conjunction with the first cycle, could enable a unique determination of distance. Alternatively, for a single wavelength and a single pinhole size, it should suffice to consider the data from only two different key pixels in the Fresnel pattern.

This work was done by David Lehner, Jonathan Campbell, and Kelly Smith of Marshall Space Flight Center; Duncan Earl and Alvin Sanders of the University of Tennessee; Stephen Allison of Oak Ridge National Laboratory; and Larry Smalley of the University of Alabama in Huntsville.

This invention is owned by NASA, and a patent application has been filed. For further information, contact Sammy Nabors, MSFC Commercialization Assistance Lead, at sammy.a.nabors@nasa.gov. Refer to MFS-31649-1.

Efficient G^{4}FET-Based Logic Circuits

Fewer G^{4}FETs than conventional transistors would be needed to implement logic functions.

NASA's Jet Propulsion Laboratory, Pasadena, California

A total of 81 optimal logic circuits based on four-gate field-effect transistors (G^{4}FETs) have been designed to implement all Boolean functions of up to three variables. The purpose of this development was to lend credence to the expectation that logic circuits based on G^{4}FETs could be more efficient (in the sense that they could contain fewer transistors), relative to functionally equivalent logic circuits based on conventional transistors.

The theoretical basis of this development was summarized in "G^{4}FETs as Universal and Programmable Logic Gates" (NPO-41698) *NASA Tech Briefs*, Vol. 31, No. 7 (July 2007), page 44. To recapitulate: A G^{4}FET is a combination of a junction field-effect transistor (JFET) and a metal oxide/semiconductor field-effect transistor (MOSFET) superimposed in a single silicon island and can therefore be regarded as two transistors sharing the same body. A G^{4}FET can also be regarded as a single device having four gates: two side junction-based gates, a top MOS gate, and a back gate activated by biasing of a silicon-on-insulator substrate. Each of these gates can be used to control the conduction characteristics of the transistor; this possibility creates new options for designing analog, radio-frequency, mixed-signal, and digital circuitry. One such option is to design a G^{4}FET to function as a three-input NOT-majority gate, which has been shown to be a universal and programmable logic gate. The universality and programmability could be exploited to design logic circuits containing fewer discrete components than are required for conventional transistor-based circuits implementing the same logic functions.

Optimal NOT-majority-gate, G^{4}FET-based logic-circuit designs were obtained in a comparative study that also included formulation of functionally equivalent logic circuits based on NOR and NAND gates implemented by use of conventional transistors. [NOT gates (inverters) were also included, as needed, in both the G^{4}FET- and the NOR- and NAND-based designs.] In the study, the problem of finding the optimal design for each logic function and each transistor type was solved as an integer-programming optimization problem. The table summarizes results obtained in this study for the first four Boolean functions, showing that in most cases, fewer logic gates are needed in the NOT-majority (G^{4}FET) implementation than in the NOR- and

Function	NOT-Majority (G^{4}FET) Implementation		Conventional NOR Implementation		Conventional NAND Implementation	
	Number of NOT-Majority Gates	Number of NOT Gates	Number of NOR Gates	Number of NOT Gates	Number of NAND Gates	Number of NOT Gates
{1,0,0,0,0,0,0,0} = $\overline{A}\overline{B}\overline{C}$	2	1	2	1	4	3
{0,1,0,0,0,0,0,0} = $A\overline{B}\overline{C}$	2	1	3	1	4	2
{0,0,0,1,0,0,0,0} = $AB\overline{C}$	2	0	2	3	3	2
{0,0,0,0,0,0,0,1} = ABC	2	1	2	4	3	1

Numbers of Logic Gates were calculated for optimal circuits implementing several Boolean functions of the three input variables (A,B,C). Each entry in the "Function" column includes an octuple binary representation of the noted Boolean function, namely {f(0,0,0),f(0,0,1),f(0,1,0),f(0,1,1),f(1,0,0),f(1,0,1),f(1,1,0),f(1,1,1)}.

NAND-based conventional implementations. Considering all 81 non-equivalent Boolean functions included in the study, it was found that in 63 percent of the cases, fewer logic gates (and, hence, fewer transistors) would be needed in the G^4FET-based implementations.

This work was done by Farrokh Vatan of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

Innovative Technology Assets Management, JPL, Mail Stop 202-233, 4800 Oak Grove Drive, Pasadena, CA 91109-8099, E-mail: iaoffice@jpl.nasa.gov.

Refer to NPO-44407, volume and number of this NASA Tech Briefs *issue, and the page number.*

Web-Enabled Optoelectronic Particle-Fallout Monitor

A user can interrogate this instrument from a remote location.

John F. Kennedy Space Center, Florida

A Web-enabled optoelectronic particle-fallout monitor has been developed as a prototype of future such instruments that (l) would be installed in multiple locations for which assurance of cleanliness is required and (2) could be interrogated and controlled in nearly real time by multiple remote users. Like prior particle-fallout monitors, this instrument provides a measure of particles that accumulate on a surface as an indication of the quantity of airborne particulate contaminants. The design of this instrument reflects requirements to:

- Reduce the cost and complexity of its optoelectronic sensory subsystem relative to those of prior optoelectronic particle fallout monitors while maintaining or improving capabilities;
- Use existing network and office computers for distributed display and control;
- Derive electric power for the instrument from a computer network, a wall outlet, or a battery;
- Provide for Web-based retrieval and analysis of measurement data and of a file containing such ancillary data as a log of command attempts at remote units; and
- Use the User Datagram Protocol (UDP) for maximum performance and minimal network overhead.

The sensory subsystem of the Web-enabled optoelectronic particle-fallout monitor includes an infrared light-emitting diode (LED) that illuminates a silicon wafer. Highly discriminating photodiodes measure the light scattered at right angles to the illumination. The scattered light is measured both (1) during illumination by the LED and (2) when the LED is turned off so that only ambient light is present. The ambient infrared scattered-light reading is subtracted from the illumination scattered-light reading to obtain a net scattered-light reading. In principle, the amount of scattering attributable to particles on the wafer, and thus the number of particles on the wafer, is closely related to the ratio between the net scattered-light reading and the LED output, with a correction for temperature that affects the photodiode junction and a small additional correction for ambient light. Photodiode readings of the LED output are taken for eventual use in calculating the ratio, and temperature is measured for eventual use in calculating photodiode junction corrections, but at the present prototype stage of development, the ratio and corrections are not calculated and, instead, the number of particles accumulated on the wafer is estimated as being simply proportional to the net scattered-light reading. Other features of the instrument design include the following:

- The instrument includes a built-in Ethernet/Web server communication subsystem and a microprocessor tied directly to this subsystem.
- A power-over-Ethernet feature provides for the use of one wire for control, data communication, and power supply. This feature is also compatible with battery or wall-outlet power.
- The microprocessor receives commands via the Web and/or the Ethernet, initiates and controls operation of the sensory subsystem, and collects data.
- The instrument communicates with a desktop personal computer that is capable of gathering information from as many as 1,000 instruments like this one. The personal computer, in turn, provides information to a Web server computer for archiving and analysis.
- Photodiode outputs are sampled by 24-bit analog-to-digital converters (ADCs), controlled by the microprocessor, at a repetition rate of 20 Hz. Included within the ADCs are filters that suppress, by more than 80 dB, interfering signal components at the 60-Hz power-line frequency that have been found to be present in photodetector outputs of similar prior instruments. An ADC output exhibits a differential count of >25,000 between the clean and 0.5-percent-obscured wafer conditions. The normal sample-to-sample range is within 32 counts.
- Optionally, the instrument can be set to send an electronic-mail message directly to a designated person when an out-of-bounds condition (e.g., a particle count in excess of a prescribed limit) occurs.
- Integrity of data is ensured by use of both UDP checksums and cyclical redundancy checks.

This work was done by Lewis P. Lineberger of Kennedy Space Center. For further information, contact the Kennedy Innovative Partnerships Program Office at (321) 861-7158. KSC-12984