Design and Development of the Solar Dynamics Observatory (SDO) Electrical Power System

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The SDO spacecraft was designed to help us understand the Sun's influence on Earth and Near-Earth space by studying the solar atmosphere on small scales of space and time and in many wavelengths simultaneously. It will perform its operations in a geosynchronous orbit of the earth. This paper will present background on the SDO mission, an overview of the design and development activities associated specifically with the SDO electrical power system (EPS), as well as the major driving requirements behind the mission design. The primary coverage of the paper will be devoted to some of the challenges faced during the design and development phase. This will include the challenges associated with development of a compatible CompactPCI (cPCI) interface within the Power System Electronics (PSE) in order to utilize a "common" processor card, implementation of new solid state power controllers (SSPC) for primary load distribution switching and over current protection in the PSE, and the design approach adopted to meet single fault tolerance requirements for all of the SDO EPS functions.

Nomenclature

A	= ampere	*m2*	= square meters
ACE	= attitude control electronics	*MAP*	= Microwave Anisotropy Probe
A/D	= analog to digital	*Mbps*	= Megabits per second
AM0	= air mass zero	*mosfet*	= metal–oxide–semiconductor field-effect transistor
oC	= degrees Celsius	*mV*	= milli-volt
cPCI	= compact Peripheral Component Interconnect	*NASA*	= National Aeronautics and Space Administration
C&DH	= command and data handling	*NiCd*	= nickel-cadmium
dc	= direct current	*NiH2*	= nickel-hydrogen
DDC	= Data Devices Corporation	*OVP*	= overvoltage protection
EEPROM	= electrically erasable programmable read only memory	*oz.*	= ounce
EPS	= electrical power system	*PCC*	= power converter card
ETU	= engineering test unit	*PRT*	= platinum resistance thermometer
FPGA	= field programmable gate array	*PSE*	= power system electronics
GEO	= geostationary or geosynchronous orbit	*PWM*	= pulse width modulated
GSE	= ground support equipment	*RAM*	= random access memory
GSFC	= Goddard Space Flight Center	*SAM*	= solar array module
Isc	= short circuit current	*SDN*	= subsystem data node
I2t	= current squared multiplied by time	*SDO*	= Solar Dynamics Observatory
kg	= kilogram	*SEE*	= single event effects
kRad	= kilorads	*SSPC*	= solid state power controller
LET	= lower energy threshold	*TID*	= total ionizing dose
LEO	= low earth orbit	*UTJ*	= ultra triple junction
Li-Ion	= Lithium-Ion	*V*	= Volts
LPSC	= low power switch card	*Vdc*	= Volts dc
LWS	= Living with a Star	*Voc*	= open circuit voltage

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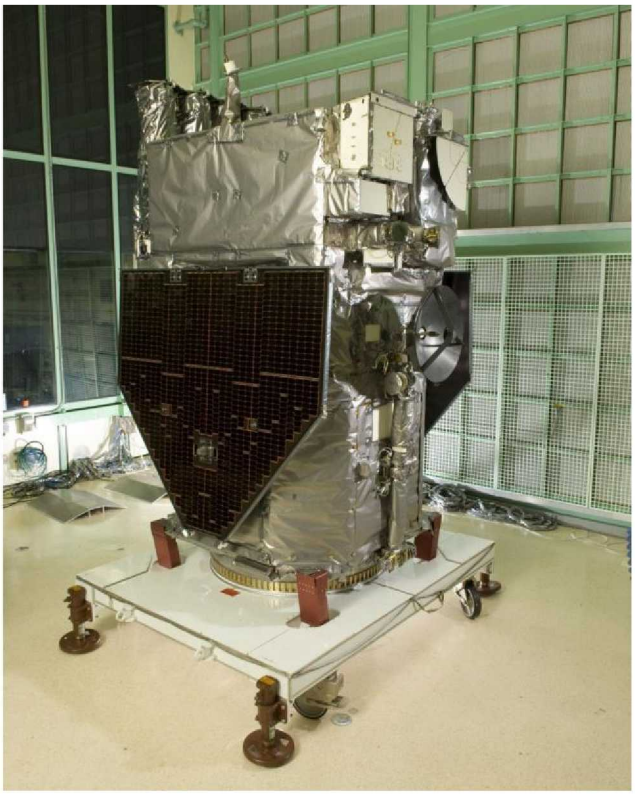
I. Introduction

THE Solar Dynamics Observatory is the first mission to be launched for NASA's Living With a Star (LWS) Program. LWS is a program designed to understand the causes of solar variability and its impacts on Earth with SDO designed to help understand the Sun's influence on Earth and Near-Earth space by studying the solar atmosphere on small scales of space and time and in many wavelengths simultaneously. SDO's goal is to understand the solar variations that influence life on Earth and humanity's technological systems by determining: (1) how the Sun's magnetic field is generated and structured and (2) how this stored magnetic energy is converted and released into the heliosphere and geospace in the form of solar wind, energetic particles, and variations in the solar irradiance.

SDO is a sun-pointing semi-autonomous spacecraft that will allow near continuous observations of the Sun with a continuous science data downlink rate of 130 Megabits per second (Mbps). The spacecraft is 4.5 meters high and over 2 meters on each side, weighing a total of 3100 kg (fuel included). SDO's inclined geosynchronous orbit was chosen to allow continuous observations of the Sun and enable its exceptionally high data rate through the use of a single dedicated ground station. The rapid cadence and continuous coverage required for SDO observations led to placing the satellite into an inclined geosynchronous orbit. This allows for a nearly-continuous, high-data-rate, contact with a single, dedicated, ground station. Nearly continuous observations of the Sun can be obtained from other orbits, such as low Earth orbit (LEO) and the Libration point L-1 however; if SDO were placed into one of these orbits it would be necessary to store large volumes of scientific data onboard until a downlink opportunity. The large data rate of SDO, along with the difficulties in managing a large on-board storage system, resulted in a requirement of continuous contact. The disadvantages of this orbit include higher launch and orbit acquisition costs (relative to LEO) and eclipse (Earth shadow) seasons twice annually (compared to L-1), during these 13 day eclipse periods, SDO will experience a daily interruption of solar observations ranging from roughly 15 minutes up to a maximum of 72 minutes. There will also be three lunar shadow events each year from this orbit. This orbit is located on the outer reaches of the Earth's radiation belt which results in high radiation dose effects. Additional shielding was added to the instruments and electronics to reduce the problems caused by exposure to radiation.



Solar Dynamics Observatory during Integration and Test Activities at NASA Goddard Space Flight Center (GSFC)

This paper will present an overview of the design and development activities associated specifically with the SDO electrical power system (EPS), as well as the major driving requirements behind the design. In addition, the coverage contains some of the more significant challenges faced during the design and development phase of the EPS.

II. Overview and Major Design Requirement Drivers for the SDO EPS Design

The SDO EPS is a direct energy transfer system specifically developed to utilize Lithium-Ion battery energy storage capabilities. Figure 1 provides a simple overview of the observatory electrical power system including the major components. The primary top level driving requirements imposed on the EPS by the project are the ability to provide 1380 Watts of continuous power to the observatory (excluding battery charging) as well as 1500 Watts of peak power.

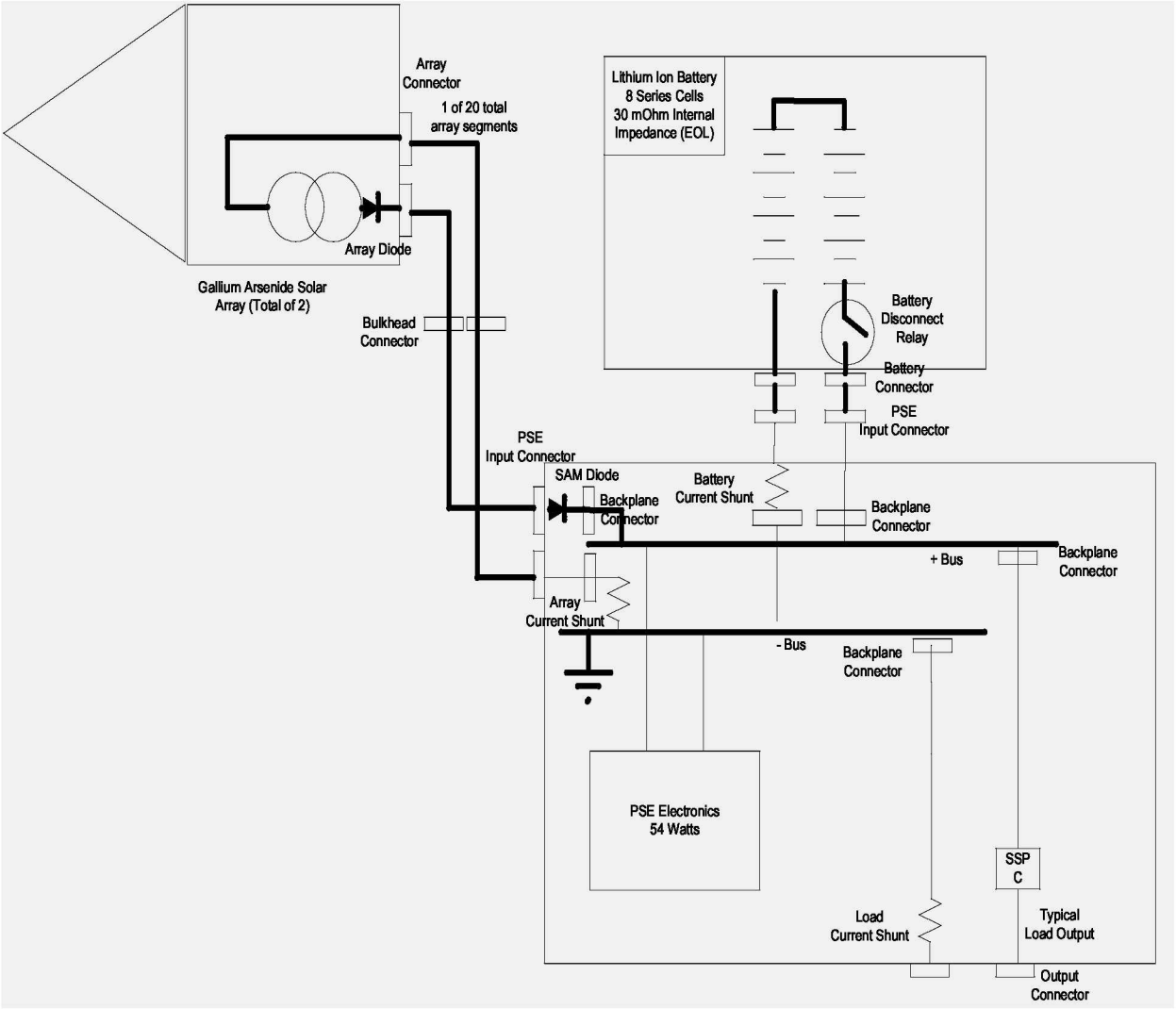


Figure 1. Simple Block Diagram of SDO Electrical Power Subsystem

The SDO EPS collects solar energy from a pair of solar array panels containing triple junction Gallium Arsenide cells with a total collection area of 6.22 m2 containing 130 parallel solar array strings and 18 solar cells in series per string. The Ultra Triple Junction (UTJ) solar cells are manufactured by Spectrolab and provide a nominal efficiency rating of 28.3% at 28°C and 1 AM0 conditions. Each solar array panel is configured to provide ten solar array circuits, five circuits are composed of 7 array strings in parallel and the other five contain 6 parallel strings. The two solar array panels are identical in size and configuration. All solar array strings are isolated via JANTXV 1N5811 diodes which are mounted on diode boards on the back side of the solar array panels. One short circuit current (Isc) sensor and one open circuit voltage (Voc) sensor are also mounted on each panel to monitor panel performance

throughout the mission. The solar array circuits are routed into the Power System Electronics (PSE) and connect to the Solar Array Module (SAM) cards within the PSE.

SDO's energy storage is provided by one 120 ampere-hour capacity (nominal) Lithium Ion battery. The battery was built by ABSL Power Solutions and utilizes 832 Sony 18650 cells configured in a series/parallel approach designed to provide a nominal 32 Vdc bus voltage. The battery contains two Hartman (Tyco) 100 ampere electro-mechanical relays. These relays are designed to provide isolation between the battery and the SDO observatory during off hours of ground testing. The relays also provide a means to disconnect the battery from the spacecraft bus at the end of the mission. The battery contains four Platinum Resistance Thermometer (PRT) sensors used to monitor the temperature within the battery cell blocks as well as provide the means for temperature compensated voltage control.

The PSE contains a total of 15 discrete printed wire boards and one backplane. There are two dc/dc power converter cards (PCC) providing voltages of 2.5Vdc, 3.3Vdc, +5Vdc_and +/- 15Vdc for operating the PSE electronics. There are also two Subsystem Data Node (SDN) cards. The SDN cards contain generic processing capabilities (Coldfire processor based) used throughout the various subsystems on SDO as well as containing application specific algorithms programmed into an Actel RTSX32-SU field programmable gate array (FPGA). The PSE contains a total of 6 output module cards (3 cards per side) designed to provide switched and un-switched power to all of the observatory loads. There are two Solar Array Module (SAM) cards that process the solar array power for use by the observatory electrical loads as well as providing hardware controlled overvoltage processing, if necessary. Each SAM contains one Pulse Width Modulated (PWM) control segment controlling two solar array circuits with only one of the PWMs in control at any given time. The inactive PWM segment is available to be used as a digital shunt segment. There are 7 digitally switched solar array segments controlled by each SAM as well as one unswitched segment. The Battery Module is a fully redundant printed wire card that monitors the battery parameters as well as controls the power to the battery heaters. The PSE also contains a fully redundant deployment module card primarily used for initial deployments of the solar array panels and high gain antennas shortly after launch. The last card contained within the PSE is a diode assembly card. The diode assembly card is mounted in a cavity on the end of the PSE and is used to isolate power provided by an external solar array simulator during ground test.

Of significant concern during the design and development process were the requirements associated with radiation effects over the course of the design mission life (5 years). The Geostationary position selected for SDO is an altitude of 35,788 km, longitude of 105° W, and a 28.7° angle of inclination. Although the mission life is 5 years, The EPS was designed for a mission goal of 10 years. This 10 year goal imposes both a high total ionizing dose (TID) tolerance requirement as well as single event effects (SEE) concern. The TID estimate for the PSE was calculated to be 23.2 kRad-Si for the 5 year mission and includes a factor of 2 for margin. The integral linear energy transfer (LET) requirements impose tolerance to single event effects up to 100 MeV-cm2/mg for heavy ions. Additionally, SDO imposed a single failure tolerance requirement on the electrical power system which requires full mission functionality after any single failure.

III. Major EPS Issues Encountered During Development

During the course of the SDO power system development, the EPS team was faced with some unique challenges associated with the mission requirements as well as incorporating evolving technology into the spacecraft. A description of some of the more challenging issues faced during the development of SDO are presented here.

A. PSE Overview and Development Challenges

The SDO PSE is a multipurpose power system component combining the power conditioning and battery regulation function with the power distribution function. The single fault tolerant, fully redundant design contains both the primary and redundant sides in a single enclosure. The PSE utilized the NASA GSFC MAP modular architecture as a reference for design. However, to meet the SDO requirements, SDO's PSE added full redundancy (to provide single fault tolerance), increased the power processing capability (to accommodate 1450W of observatory power including battery charging), added Li-Ion battery charging control, altered the design to utilize a common cPCI backplane, and added cross-strapped power distribution functionality utilizing radiation hard power distribution switches.

1. cPCI Backplane

The SDO Observatory bus components were all required to use a common processor/interface card design and a common low voltage power supply card. The SDN contains a processor, a 1553 interface, on board RAM and EEPROM, a common analog acquisition system for digitizing analog signals, and a CompactPCI (cPCI) backplane interface. The cPCI interface was chosen by SDO for several reasons. It is a well defined standard with commercially available design and test tools. It is also a commonly available interface for commercial cards which allowed for use of those cards for breadboard testing. The cPCI interface is also the interface used by standard off - the-shelf processor cards.

While the cPCI interface was the obvious choice for other subsystem boxes, the cPCI interface created some unique challenges for the PSE design and development. The PSE backplane was designed to distribute the 28V spacecraft bus power, transmit critical analog telemetry and control signals and provide communication between the cards. Primarily due to the increased power distribution requirements of the backplane, the printed circuit design necessitated a twelve layer board using 2oz. copper layers. This approach allowed for a high power path from the solar array circuit inputs to the battery interface as well as the power distribution switch outputs. Because of the generic versatility of the interface communication bus, cPCI requires a large number of signals and therefore a large number of connector pins. The standard cPCI specification requires that the large number of signals be routed as 65ohm, impedance controlled traces on the backplane. With 2oz. copper layers, and a stack-up dictated primarily by the high power requirements, the impedance controlled signals had to be achieved using large dielectric spacing which also drove the overall thickness of the SDO PSE backplane. The cPCI specification also requires a specific high density connector type be used for the cPCI interface. The connector used in the PSE was developed by Hypertronics specifically for flight use, as the commercially available cPCI connectors were not deemed acceptable for flight application. Because of the unique nature of the application in the PSE, NASA GSFC funded a research task to develop the process for aligning and soldering these high density connectors into such a thick and copper heavy printed circuit board. After considerable time and effort, a process was ultimately developed to handle this unique cPCI backplane. The use of the cPCI interface also utilized about half of the physical space for routing on the backplane. This limitation resulted in less space available for routing the 28V bus spacecraft power even though the SDO PSE was designed to accommodate a larger total current carrying requirement than the MAP predecessor. The approach ultimately adopted to handle the higher current carrying capability in less space was a bus bar design incorporated into the backplane assembly. This was designed to lower the overall impedance across the long PSE backplane and assist in carrying the higher currents with lower voltage drop. A picture of the flight SDO PSE backplane with the bus bar installed is shown in Figure 2.

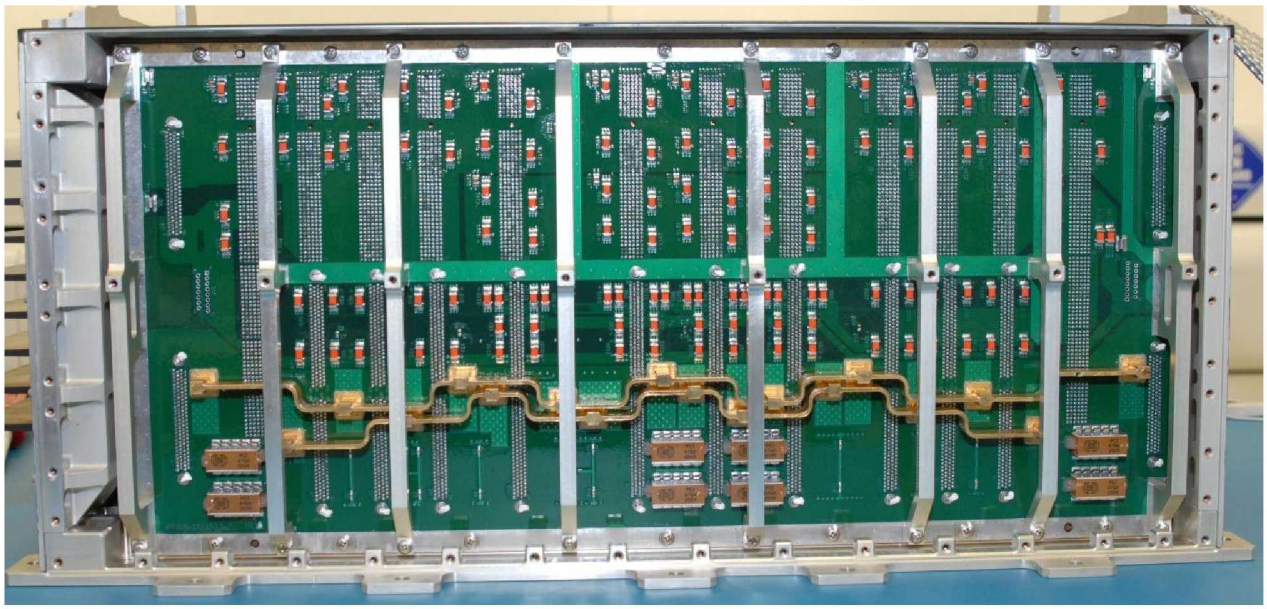


Figure 2. SDO Flight PSE Backplane With Bus Bar

2. *SDN Common Design*

The SDO common processor card, or SDN, was provided to each subsystem as a core common design. Each subsystem was responsible for incorporating their application specific circuitry and finalizing the card design for their subsystem. The PSE specific SDN added a few application specific circuits to the common SDN design. A digital to analog converter, which provides a precision current reference for the battery charge current control loop, was added along with an expanded analog acquisition system to read additional external thermistors and PRTs. The primary challenge associated with utilizing the SDN was the need to manage within the common design constraints. There are certainly some potential advantages of a common design from the spacecraft or system standpoint when considering cost perspectives if efficiently implemented. Utilizing this approach the design is only performed once, rather than multiple times. The common software development for each of the specific SDN cards was also simplified due to the commonality of card design. However, the common design approach did create some challenges both technically and programmatically. The SDN design had to handle the envelope of requirements from all the users rather than specific application oriented. While the needs of all the users were obviously similar to a certain extent, such as communications with the C& DH system, it was not identical. The result was that the design effort and schedule required for this common design was more substantial than a typical application specific design. The common SDN design also required all users to adopt the cPCI backplane standard for the card to card interface since the processor card itself was designed and supported only with this interface. Some of the difficulty resulted from the fact that 90% of the design was common, but the resultant printed circuit assembly was not. If the common design had resulted in a common printed circuit board that was the same for all users then the commonality would have been even more beneficial. With only the electrical design being common, each user application still had to perform individual printed circuit board designs.

The other primary challenge faced with the SDN card was with the need for critical telemetry measurement. The SDN provides the PSE with the Analog Acquisition Circuit, which is used for muxing and digitizing all the PSE analog telemetry. Much of the telemetry is housekeeping data and is only required to have accuracy to about 2% of full scale. However, the PSE is required to read the Li-Ion battery voltage accurately to within 50mV. Knowing the battery voltage precisely is important with regard to the Li-Ion chemistry since it is very sensitive to over-charge. This battery voltage reading from the analog to digital (A/D) converter is used by the software for the battery charge control regulation. When integrating the SDN card with the rest of the PSE battery voltage measurement circuitry, it was discovered that the telemetry reading was not meeting the accuracy requirement. The performance specifications on the A/D converter for the SDN design were as good, if not better, than the equivalent on the heritage design. However, the A/D component selected and the circuitry designed around it were different. Considering this was a common design, no other application users had detected the problem since they did not have as tight accuracy requirements that the PSE has imposed. Considerable time was spent troubleshooting the A/D circuit. Ultimately, the problem was found to be related to the implemented design of the A/D. This design was clocking the A/D much faster than any application required and the amplifier driving the A/D input was not settling out fast enough for the A/D's internal sample and hold. While the solution was relatively simple and painless, it was another example of how a common design can be developed to meet the needs of many but, not necessarily optimized for a specific application.

3. *Solid State Power Controller (SSPC)*

The power distribution function of the SDO PSE was designed with over-current protected switched services to protect the power bus in the event of a fault. This approach was also a heritage consideration from the MAP program; however a significantly increased number of higher power switches were required for SDO. The SDO implementation uses distributed power switch architecture with the PSE providing a significant number of 5A, 10A, and 15A switched services as well as 5A un-switched fused services used for critical functions that always remain powered. Some of the services from the PSE feed power to Low Power Switch Cards (LPSC) in various other subsystem components. These cards provide additional distributed switched power using 1A and 2A SSPCs. The PSE contains three identical Output Module Cards on each side with each spacecraft load receiving a total of two power feeds; one from PSEA side and one from PSEB side. This approach was implemented to provide power cross-strapping of the observatory for increased reliability and single fault tolerance.

The SDO Output Module card design uses a Solid State Power Controller (SSPC) for all switch service functions. The SSPC is a power hybrid device. The SSPC provides a mosfet power switch device with I^2T over-current protection. This I^2T characteristic causes the SSPC performance to be similar to that of an electronic circuit breaker. Like a fuse, the I^2T protection allows for higher short duration current flows for inrush and load transients

without tripping, but provides a lower trip point, slightly above the service rating of the SSPC, for steady state short circuit protection. The SSPC provides a logic level on/off control interface as well as a logic status feedback indicating the state of the switch. This control and status interface is electrically isolated from the power side of the device. The Engineering Test Unit (ETU) PSE was initially designed and fabricated with Data Device Corporation (DDC) SSPCs. It was during the ETU phase of the project that the NASA GSFC Parts Branch determined, through radiation testing and subsequent review of the hybrid design, that the DDC SSPC would not meet the SDO radiation environment specified. The primary concern uncovered was with Single Event Transients (SET) that could inadvertently cause the device to turn off and/or cause the device to provide an incorrect status. Unfortunately, one of the areas of significant concern was the custom ASIC within the hybrid and therefore the part could not be easily modified to meet the mission radiation requirements.

Ultimately for the flight development unit NASA GSFC turned to Micropac, Inc. Micropac also builds SSPC hybrid devices. The NASA GSFC parts engineer worked closely with Micropac to modify a version of their SSPC design to meet the radiation environment requirements. Micorpac was also able to provide the replacement part with a pin for pin compatible package to the DDC part used in the ETU development. This resulted in eliminating the need to completely redesign the Output Module for the flight component. This was never the less still a large undertaking since it meant switching a major component of the power system at a later point in the PSE development. Micropac provided preliminary engineering unit part versions sufficient for one Output Module prior to the flight build. This allowed testing of the new parts in the ETU PSE to verify functionality. During testing there were still several problems identified. Most of the problems were a result of the inherent nature of the design and assembly of hybrid devices. Ideally, the ETU would have been built with the first full manufacturing run of the new parts and this approach would have provided an opportunity to resolve any problems. During the testing of the first lot of devices at the vendor, excess leakage was discovered testing following final bake-out. It was subsequently determined that something in the assembly process resulted in excess flux application which, following bake-out, was establishing a path across the device for leakage current to flow. This particular problem was deemed unacceptable and Micropac addressed the problem and was able to provide new parts quickly. As the problems were identified and addressed the primary concern became getting qualified parts in time to meet the spacecraft schedule. With these particular hybrid parts the substrates are laid out well in advance and the parts that make up the internal circuits are also ordered far in advance. The ongoing concern persisted; if a problem was found late in the build, and many parts had to be scrapped, there might not be enough material and substrates to build up the quantity of parts necessary for the PSE. In the event the build process had to start over, the SDO project would likely have seen at least a one year slip in the schedule due only to the SSPC. In addition, the Micropac SSPC was already the back-up device to the original design with DDC parts. So there was ultimately no other flight qualified SSPC alternative. As a potential mitigation approach, the SDO project funded an effort to design a separate discrete mosfet switch circuit which could be coupled with an inline fuse plug to replace the SSPCs, if necessary. This alternative would have provided less functionality than the Micropac SSPC, particularly since it was not resettable. However, the decision was made that this would be an acceptable alternative if the SSPCs encountered a major problem or unacceptable schedule delay. The alternative circuit design was required to be pin for pin compatible and packaged into the same small space as the hybrid. This approach remained a back-up but, fortunately was not needed. The Micropac SSPCs were subsequently reworked with the new process and re-tested successfully. In order to accommodate the project schedule during this delay, the ETU PSE was installed on the SDO Observatory for early Spacecraft Integration and Test. After completion of component level qualification testing the ETU version was replaced with the Flight PSE.

B. Li-Ion battery Charging and Monitoring

As mentioned earlier, the power conditioning portion of the SDO PSE is a direct energy transfer topology with the battery directly connected to the spacecraft electrical bus. The fine control of the battery charge current is performed using a pulse width modulated boost converter, while the rest of the solar array power is either shunted or connected to the bus, as needed. The software control loop function, designed to regulate the battery charge, is performed in the SDN processor. As the voltage control monitoring circuit determines more power is required from the solar array, the software commands more segments to the bus. This is done in a similar manner to the heritage MAP PSE design, with a few distinct differences. Since SDO uses a Li-Ion battery, the PSE is required to measure the battery voltage more accurately than its predecessor and is required to regulate the battery voltage within 100mV, which is considerably tighter than that required for other previous missions. The battery voltage monitoring is performed by two separate monitors, one fine voltage monitor and one coarse voltage monitor. In order to achieve the highest precision for the control loop the fine voltage measurement is scaled between only 26V and 34V. This provides a digital resolution at the A/D converter of about 2mV/count. This approach was adopted primarily because

it was determined that this would cover the entire anticipated battery voltage range during normal operations. The coarse voltage measurement was designed to cover a 0V to 40V range in order to provide measurement coverage of all possible abnormal conditions.

Li-Ion chemistry is much more susceptible to over-charge. Because of this, the SDO PSE uses only a voltage clamp control with a maximum charge rate of 10A available until it reaches the commanded clamp voltage. Once the commanded voltage is reached, the PSE begins to taper the charge current while precisely controlling the battery voltage until fully charged. Unlike the heritage MAP design which would trickle charge the battery, SDO's control remains in this voltage clamp regulation mode, never reverting to trickle charge. With the low self discharge of Li-Ion, even a very small trickle charge current could be enough to cause an over-charge condition of the battery.

C. Solar Array Power Processing Challenges:

The SDO solar array module (SAM) was also initially based on the MAP/EO-1 architecture with the two SDO Solar Array panel string segments combined into 20 discreet channels connected to the PSE.

One of the early challenges was how to fit the solar array charging electronics for 20 Solar segments into the given form factor of the PSE., It was determined early in the design phase that two SAM cards would be required to handle the twenty segments with each SAM designed to process one half of the total solar array capability, or 10 segments. As previously mentioned one of the 10 segments is directly connected to the spacecraft bus through a diode. Seven channels are digital shunts and the remaining 2 channels are combined to provide the input to a PWM converter used to perform fine control of the spacecraft bus current. Each of the SAM cards contains a PWM, but one of these PWMs performs the fine control function at any given time. The PWM not performing the fine control is relegated to operate as a digital shunt segment. This is accomplished by setting the duty cycle at 100% (fully shunting the current from the PWM segment) or 0% (allowing all of the PWM segment current onto the spacecraft bus).

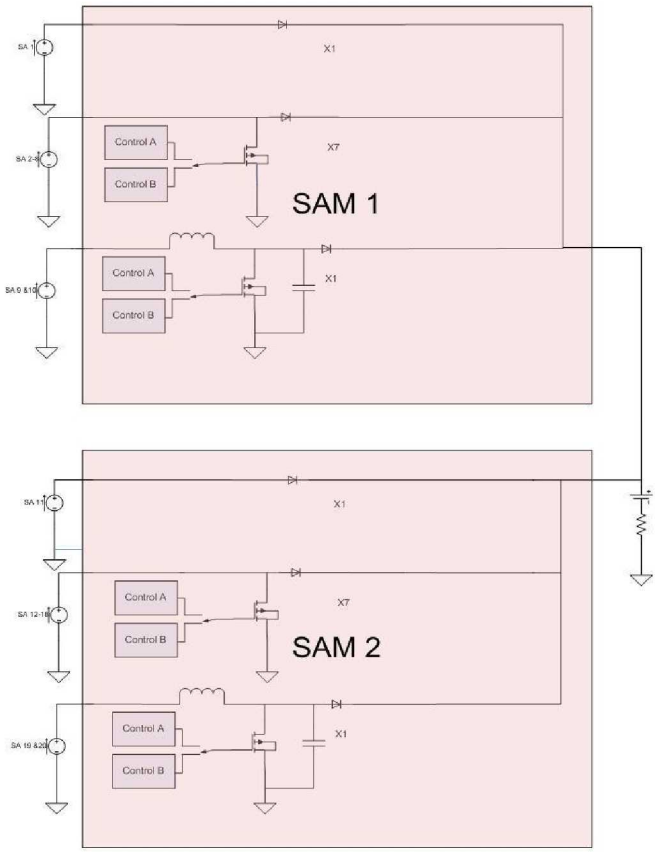


Figure 3. Solar Array Module Control

Perhaps the largest challenge in the PSE design was that spacecraft requirements dictate that no single power system related failure should reduce the available observatory power by more than 10% (the equivalent of two Solar Array segments). However, requirements also imposed the necessity that a single failure could not cause degradation to the charge control of the spacecraft bus. A control scheme was devised and implemented that was intended to meet these redundancy requirements for both the digital shunts and the PWM sections. Figure 3 depicts the control architecture adopted for the digital shunt segments.

1. Digital Shunt Control

The mosfet drive in Figure 3 is self powered directly from the spacecraft bus. This allows the mosfet and driver for each segment to be totally independent from the other segments and prevents a failure in one segment from affecting any other segment. Control A and Control B shown in the figure are each powered and commanded from their respective A and B sides of the PSE. Both the A and B sides are always actively attempting to control the digital shunts. However, the digital shunts are only capable of being commanded by the side in control and ignore the commands provided from the inactive side. The A and B controls are also connected to the mosfet drive through an optical coupler in order to

provide electrical isolation between the A and B sides of the PSE and retain single fault tolerance requirements.

2. The PWM Section Control

A similar control scheme exists for the PWM circuits on each SAM card. Both the A and B sides are monitoring the battery current and voltage and both are attempting to control the PWM. In this application, only the active side's control circuitry will actually be permitted to send signals to the gates of the PWM mosfets. Similar to the digital shunts, the Control A and Control B functions are isolated from the PWM circuitry; however the PWM isolation is performed using a transformer instead of the optical coupler approach used for the digital shunts.

3. Handover of Control between A and B Sides

Given the control architecture adopted for the PSE above, a significant challenge of the design involved how to switch control between the A and B sides when necessary and avoid inadvertent side switching. An "exclusive-Or" arrangement between the two sides was ultimately determined to be the most robust fit for this architecture and is shown in Figure 4.

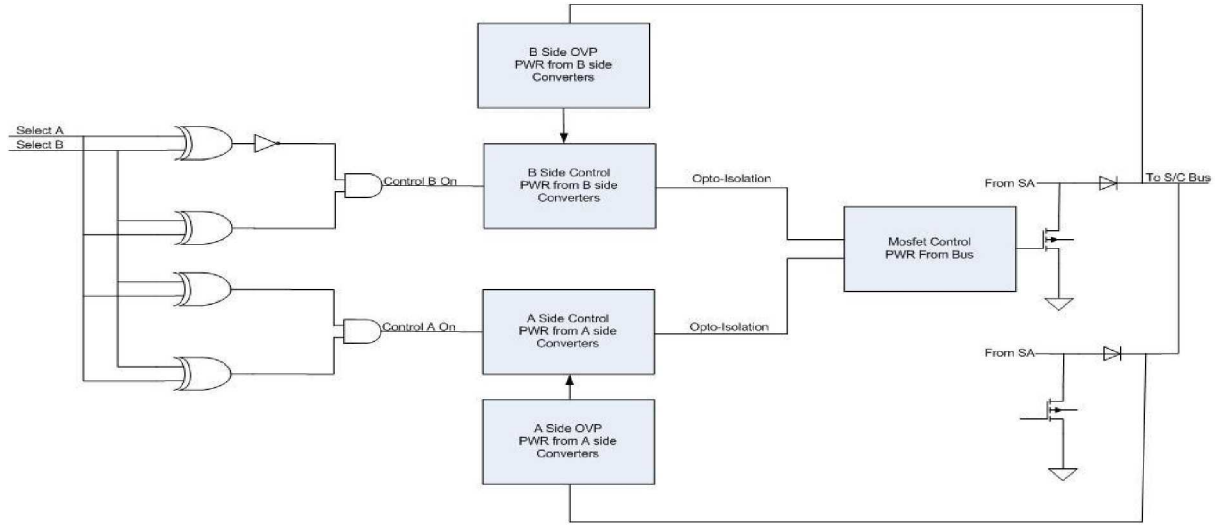


Figure 4 Side Select Circuitry

The A side of the PSE controls the "A" Select Bit and the B side of the PSE controls the "B" Select Bit. The read back (telemetry) of these signals is cross-strapped so the status can be read by either side of the PSE. The Select Bits are further buffered between each of the "exclusive OR" gates using high impedance resistors in order to prevent a failure in the gate from propagating across sides.

4. Over Voltage Protection

Since Li-Ion batteries cannot be trickle charged, any continuous current provided into the battery will result in over charging the battery and subsequently cause the voltage to rise until the battery is at risk of permanent damage. One significant challenge of the PSE design was to make sure that the solar array segments were never permitted to overcharge the battery. This particular concern resulted in the design and implementation of an over voltage protection (OVP) circuit capable of being controlled by either the A or B side control circuits.

The over voltage protection circuits monitor the spacecraft bus and reside on the SAM modules. In the event the voltage on the bus continues to rise beyond the commanded value, each SAM begins to sequentially shunt solar array segments. Each SAM is designed to begin the process of shunting the first digital segment at 34V (nominally). As the voltage continues to rise, each SAM will shunt an additional segment after every 0.125V rise on the bus. The last digital segment on each module will be shunted at approximately 34.75V with the PWM segments designed to be shunted at approximately 34.875V. This approach insures that the OV circuit will not shunt any segments until after the bus voltage has gone above the full battery charge voltage of 33.6V and yet prevents the bus from going above the maximum specified voltage limit of 35V. In the event the upper limit bus voltage level is reached all shunt-able segments will have been removed from the bus. The only remaining available power on the bus from the

Solar Arrays are the two diode segments (providing approximately 5.5A). This direct array connection to the bus requires a minimum spacecraft load of 200 Watts on the bus at all times. Although each SAM was designed to have the same voltage set-points for the over voltage protection, slight differences in measurement accuracy result in only one segment from each of the SAMs being shunted at a time during the operation of the OVP. With each succeeding segment being shunted, if the power into the battery is still positive, the next segment on the other SAM will be shunted. PSE functional testing confirmed the expected staggered operation and resulted in segments from each SA wing alternately being shunted as the bus voltage increased.

Figure 5. OVP Response Without Battery Connected to Bus

In the unlikely event the primary control circuits fail, the OVP circuitry can also serve as a last resort backup method to maintain the spacecraft bus voltage within the safe operating voltage range of the Li-Ion battery. Under nominal conditions any voltage above 33.6V is generally considered too high of a sustained voltage on the battery without incurring significant battery capacity degradation. In order to address this concern, the PSE was designed with an additional ability to command a lower threshold for the OVP protection, if desired. The lower threshold is designed to begin shunting segments of the solar array at 32.6V (instead of 34V) and will remove the last PWM channel at approximately 33.6V. Due to the very nature of secondary storage batteries, under normal conditions the battery prevents the bus voltage from changing rapidly, especially considering the maximum available charge rate is 10A, which is less than 1/10th the capacity rating of the SDO battery. As a result, when the battery is on the bus the process of shunting the segments typically occurs over a long duration (many hours). Although the SDO power system was specifically designed to be able to disconnect the battery at the end of the mission, in the event the battery relays are inadvertently opened either on orbit, or during ground testing, the OVP is forced to operate much more rapidly in concert with only the PSE bus capacitance (approximately 4000 microfarads) as opposed to the battery. When this happens the OVP circuitry is required to connect and disconnect segments every few milliseconds (not taking on the order of hours under normal conditions). A simulation of the OVP response without a battery connected to the bus is shown in Figure 5. This particular

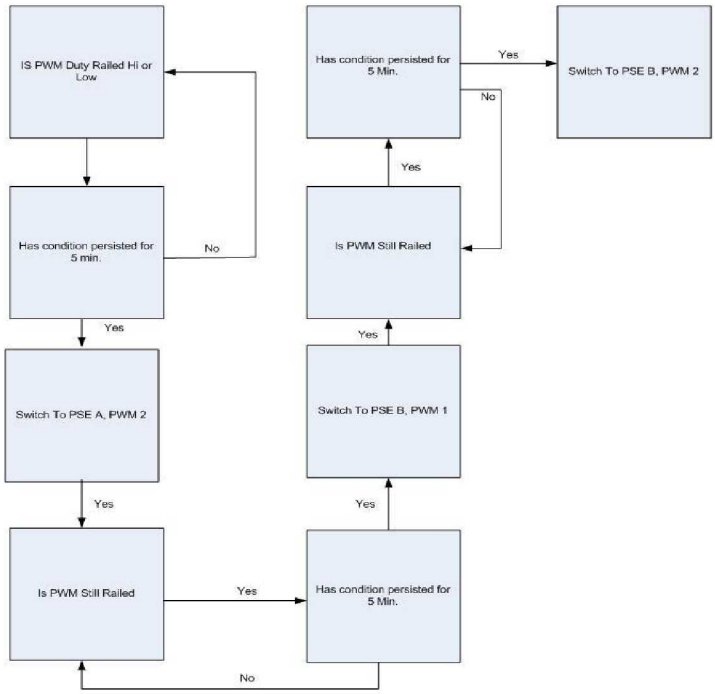


Figure 6. Logic Flow for PSE PWM Fault Detection and Correction

challenge forced the implementation of the circuit design to turn the shunt mosfets on and off quickly to limit switching losses (and subsequently reduce the thermal concern) in the mosfets.

5. FDC control

Once the redundant hardware was designed, the next challenge became how to autonomously determine when to switch from the primary to the redundant circuitry. Because of the availability of a processor within the PSE, the PSE incorporates Fault Detection and Correction algorithms (FDC) in the SDN. One of the continuously running algorithms is designed to monitor the duty cycle of the active PWM. In the event the active PWM duty cycle remains at either 100% or 0% for more than 5 minutes with indication that the Solar Arrays are in the sun, the PSE autonomously assumes that the PWM is damaged. After the initial timeout occurs the PSE changes the active PWM from Solar Array Module 1 to Solar Array Module 2. In the event PWM 2 also remains at 100% or 0% duty cycle for more than 5 minutes with indications the solar arrays are sun pointed, the PSE again autonomously switches to the B side and reverts back to PWM1 control on the SAM. Once again, if this configuration does not resolve the railed PWM condition (100% or 0% duty cycle) within 5 minutes, the last combination is commanded autonomously and the FDC switches the active PWM control from PWM 1 to PWM 2. The FDC logic for the side switch function is provided in Figure 6. After all combinations listed have been attempted the PSE will not automatically switch back to the PSE A but, would have to be implemented via ground command, if necessary.

IV. Conclusion

The SDO EPS provided a number of unique challenges during the design and development phases as a result of the mission requirements imposed. Fortunately, all of the challenges were handled without compromising the mission performance desired and in time to meet the scheduled launch date which is currently anticipated in late 2009.

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