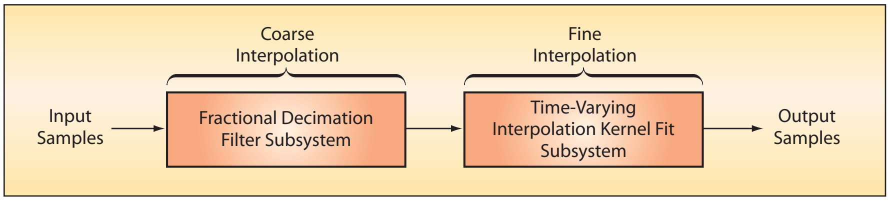
Electronics/Computers

Two-Stage Variable Sample-Rate Conversion System

A filtering/coarse-interpolation process would precede a fine-interpolation process.

NASA's Jet Propulsion Laboratory, Pasadena, California



This **Two-Stage System** would be capable of converting from an input sample rate to a desired lower output sample rate that could be variable and not necessarily a rational fraction of the input rate.

A two-stage variable sample-rate conversion (SRC) system has been proposed as part of a digital signal-processing system in a digital communication radio receiver that utilizes a variety of data rates. The proposed system would be used as an interface between (1) an analog-to-digital converter used in the front end of the receiver to sample an intermediate-frequency signal at a fixed input rate and (2) digitally implemented tracking loops in subsequent stages that operate at various sample rates that are generally lower than the input sample rate.

Traditional SRC systems are constructed from multirate building blocks that typically include integer/fractional decimation filter subsystems. Traditional SRC systems work well when SRC factors are fixed at rational values, but not when SRC factors vary or are irrational.

The input to the proposed two-stage SRC system would be the input sampled signal, $r[l] = r_d[l] + r_u[l]$, where $r_d[l]$ is the desired component (the signal of interest); $r_u[l]$ is the undesired component, which may include noise plus out-of-desired-frequency-band artifacts of the sampling process (alias components); and l is an integer denoting the current sample time index. In the proposed system (see figure), the first stage would be a fractional decimation filter subsystem that would suppress the alias components and would effect a coarse interpolation in the sense that it would convert to a sample rate approximating the desired value. The second stage would effect a fine interpolation from the approximate to the desired sample rate by means of a fit to a temporally varying interpolation kernel.

Several approaches to implementation of both the coarse- and the fine-interpolation stages have been studied theoretically and their strengths and weaknesses have been examined by analyzing results of computational simulations. For the coarse-interpolation stage, single and cascaded sets of filters and decimation filter subsystems were considered, with emphasis on the cascaded subsystems because of their modularity. For the fine-interpolation stage, the computationally efficient Farrow structure (a multirate, continuously-variable-delay filter structure, a description of which would exceed the space available for this article) was used in conjunction with a variety of piecewise-polynomial interpolation kernels, with emphasis on the cubic B-spline kernel on account of its commendable performance.

This work was done by Andre Tkacenko of Caltech for NASA's Jet Propulsion Laboratory.

The software used in this innovation is available for commercial licensing. Please contact Karina Edmonds of the California Institute of Technology at (626) 395-2322. Refer to NPO-44539.

Estimating Transmitted-Signal Phase Variations for Uplink Array Antennas

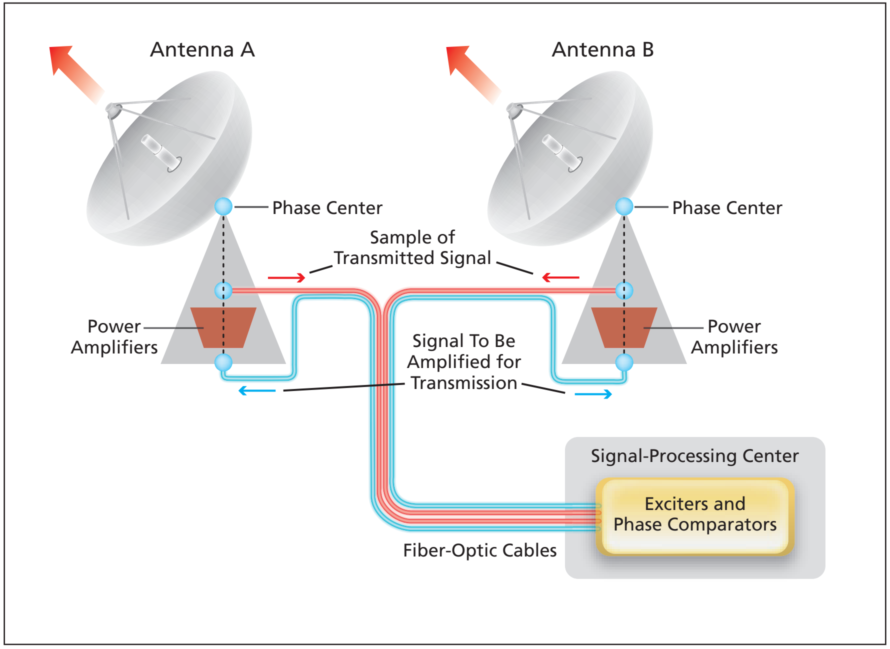
Transmitted signals serve as their own phase references.

NASA's Jet Propulsion Laboratory, Pasadena, California

A method of estimating phase drifts of microwave signals distributed to, and transmitted by, antennas in an array involves the use of the signals themselves as phase references. The method was conceived as part of the solution of the problem of maintaining precise phase calibration required for proper operation of an array of Deep Space Network (DSN) antennas on Earth used for communicating with distant spacecraft at frequencies between 7 and 8 GHz. The method could also be applied to purely terrestrial phased-array radar and other radio antenna array systems.

In the DSN application, the electrical lengths (effective signal-propagation path lengths) of the various branches of the system for distributing the transmitted signals to the antennas are not precisely known, and they vary with time. The variations are attributable mostly to thermal expansion and contraction of fiber-optic and electrical signal cables and to a variety of causes associated with aging of signal-handling components. The variations are large enough to introduce large phase drifts at the signal frequency. It is necessary to measure and correct for these phase drifts in order to maintain phase calibration of the antennas.

A prior method of measuring phase drifts involves the use of reference-frequency signals separate from the trans-



The **Signal-Distribution and Phase-Measurement Subsystems** for two antennas in an array are depicted here in greatly simplified form to illustrate the present phase-measurement method.

mitted signals. A major impediment to accurate measurement of phase drifts over time by the prior method is the fact that although DSN reference-frequency sources separate from the transmitting signal sources are stable and accurate enough for most DSN purposes, they are not stable enough for use in maintaining phase calibrations, as required, to within a few degrees over times as long as days or possibly even weeks. By eliminating reliance on the reference-frequency subsystem, the present method overcomes this impediment.

In a DSN array to which the present method applies (see figure), the microwave signals to be transmitted are generated by exciters in a signal-processing center, then distributed to the antennas via optical fibers. At each antenna, the signals are used to drive a microwave power-amplifier train, the output of which is coupled to the antenna for transmission. A small fraction of the power-amplifier-train output is sent back to the signal-processing center along another optical fiber that is part of the same fiber-optic cable used to distribute the transmitted signal to the antenna. In the signal-processing center, the signal thus returned from each antenna is detected and its phase is compared with the phase of the signal sampled directly from the corresponding exciter. It is known, from other measurements, that the signal-propagation path length from the power-amplifier-train output port to the phase center of each antenna is sufficiently stable and, hence, that sampling the signal at the power-amplifier-train output port suffices for the purpose of characterizing the phase drift of the transmitted signal at the phase center of the antenna.

In this method, the phase comparison is performed continuously while the transmitting frequency is ramped as a known function of time. On the basis of the fundamental relationships among frequency, phase, and signal-propagation path length, it can be shown that if the sweep for a given antenna is started at frequency f and the phase-comparison measurement is found to change by an amount $\Delta\theta$ when the frequency has changed by an amount $\Delta\Delta_f$, then

$$\Delta\theta = (2\pi/c)(f\Delta_d + d\Delta_f + \Delta_d\Delta_f),$$

where c is the speed of light in the fiber-optic cable or other signal-propagation medium and Δ_d is the change in the path length during the frequency-sweep interval. If the frequency is ramped over an interval just large enough to cause $\Delta\theta = 2\pi$ and the ramp is rapid enough that Δ_d is negligible during the measurement time interval, then after straightforward algebraic manipulation of the above equation for $\Delta\theta$, the electrical length can be estimated by the simple equation $d = c/\Delta_f$,

It must be recognized that the phase-comparison measurement used in this method is a round-trip phase-difference measurement: as such, it does not inherently distinguish between round-trip and one-way phase effects. Inasmuch as the primary goal of the measurement is to estimate the phase drift at the phase center of the antenna, it is important to distinguish between (1) round-trip phase accumulation, for which approximately half of the measured phase applies at the phase center, and (2) phase drifts in the power-amplifier train, which are one-way effects that contribute in their entirety to the phase drift at the phase center of the antenna.

This work was done by Leslie Paal, Ryan Mukai, Victor Vilnrotter, Timothy Cornish, and Dennis Lee of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-44611

Board Saver for Use With Developmental FPGAs

A printed-circuit board is protected against repeated soldering and unsoldering.

NASA's Jet Propulsion Laboratory, Pasadena, California

A device denoted a board saver has been developed as a means of reducing wear and tear of a printed-circuit board onto which an antifuse field-programmable gate array (FPGA) is to be eventually soldered permanently after a number of design iterations. The need for the board saver or a similar device arises because (1) antifuse-FPGA design iterations are common and (2) repeated soldering and unsoldering of FPGAs on the printed-circuit board to accommodate design iterations can wear out the printed-circuit board. The board saver is basically a solderable/unsolderable FPGA receptacle that is installed temporarily on the printed-circuit board.

The board saver is, more specifically, a smaller, square-ring-shaped, printed-circuit board (see figure) that contains half