

The **Signal-Distribution and Phase-Measurement Subsystems** for two antennas in an array are depicted here in greatly simplified form to illustrate the present phase-measurement method.

mitted signals. A major impediment to accurate measurement of phase drifts over time by the prior method is the fact that although DSN reference-frequency sources separate from the transmitting signal sources are stable and accurate enough for most DSN purposes, they are not stable enough for use in maintaining phase calibrations, as required, to within a few degrees over times as long as days or possibly even weeks. By eliminating reliance on the reference-frequency subsystem, the present method overcomes this impediment.

In a DSN array to which the present method applies (see figure), the microwave signals to be transmitted are generated by exciters in a signal-processing center, then distributed to the antennas via optical fibers. At each antenna, the signals are used to drive a microwave power-amplifier train, the output of

which is coupled to the antenna for transmission. A small fraction of the power-amplifier-train output is sent back to the signal-processing center along another optical fiber that is part of the same fiber-optic cable used to distribute the transmitted signal to the antenna. In the signal-processing center, the signal thus returned from each antenna is detected and its phase is compared with the phase of the signal sampled directly from the corresponding exciter. It is known, from other measurements, that the signal-propagation path length from the power-amplifier-train output port to the phase center of each antenna is sufficiently stable and, hence, that sampling the signal at the power-amplifier-train output port suffices for the purpose of characterizing the phase drift of the transmitted signal at the phase center of the antenna.

In this method, the phase comparison is performed continuously while the transmitting frequency is ramped as a known function of time. On the basis of the fundamental relationships among frequency, phase, and signal-propagation path length, it can be shown that if the sweep for a given antenna is started at frequency f and the phase-comparison measurement is found to change by an amount $\Delta\theta$ when the frequency has changed by an amount Δf , then

$$\Delta\theta = (2\pi/c)(f\Delta_d + d\Delta_f + \Delta_d\Delta_f),$$

where c is the speed of light in the fiber-optic cable or other signal-propagation medium and Δ_d is the change in the path length during the frequency-sweep interval. If the frequency is ramped over an interval just large enough to cause $\Delta\theta = 2\pi$ and the ramp is rapid enough that Δ_d is negligible during the measurement time interval, then after straightforward algebraic manipulation of the above equation for $\Delta\theta$, the electrical length can be estimated by the simple equation $d = c/\Delta_f$.

It must be recognized that the phase-comparison measurement used in this method is a round-trip phase-difference measurement: as such, it does not inherently distinguish between round-trip and one-way phase effects. Inasmuch as the primary goal of the measurement is to estimate the phase drift at the phase center of the antenna, it is important to distinguish between (1) round-trip phase accumulation, for which approximately half of the measured phase applies at the phase center, and (2) phase drifts in the power-amplifier train, which are one-way effects that contribute in their entirety to the phase drift at the phase center of the antenna.

This work was done by Leslie Paal, Ryan Mukai, Victor Vilnrotter, Timothy Cornish, and Dennis Lee of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-44611

Board Saver for Use With Developmental FPGAs

A printed-circuit board is protected against repeated soldering and unsoldering.

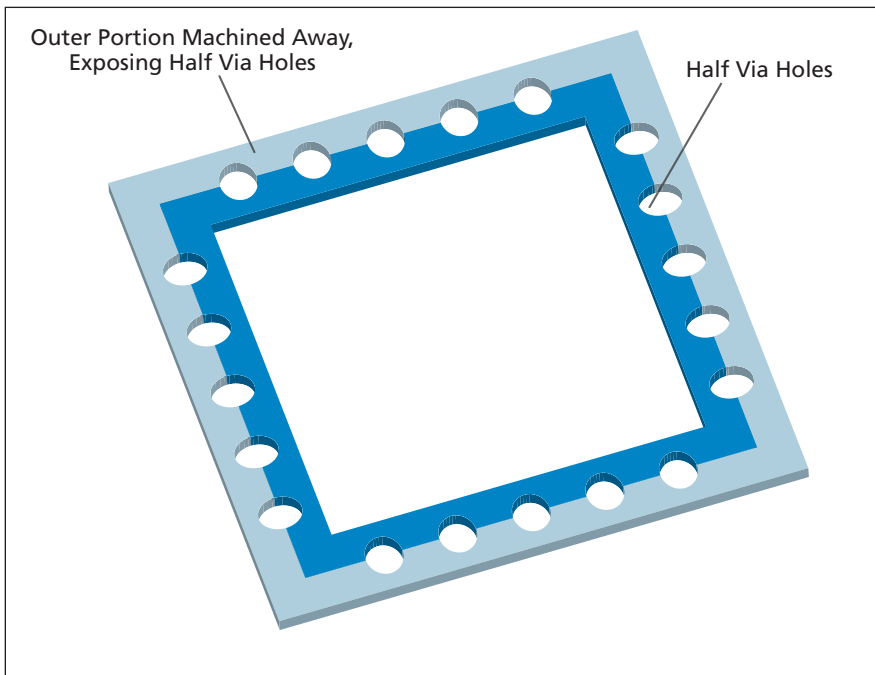
NASA's Jet Propulsion Laboratory, Pasadena, California

A device denoted a board saver has been developed as a means of reducing wear and tear of a printed-circuit board onto which an antifuse field-programmable gate array (FPGA) is to be eventually soldered permanently after a number of design iterations.

The need for the board saver or a similar device arises because (1) antifuse-FPGA design iterations are common and (2) repeated soldering and unsoldering of FPGAs on the printed-circuit board to accommodate design iterations can wear out the printed-circuit

board. The board saver is basically a solderable/unsolderable FPGA receptacle that is installed temporarily on the printed-circuit board.

The board saver is, more specifically, a smaller, square-ring-shaped, printed-circuit board (see figure) that contains half



The **Board Saver** is shown here in a simplified plan view (greatly reduced number of via holes) and not to scale, to facilitate understanding of its basic layout.

via holes — one for each contact pad — along its periphery. As initially fabricated, the board saver is a wider ring containing full via holes, but then it is milled along its outer edges, cutting the

via holes in half and laterally exposing their interiors. The board saver is positioned in registration with the designated FPGA footprint and each via hole is soldered to the outer portion of the

corresponding FPGA contact pad on the first-mentioned printed-circuit board. The via-hole/contact joints can be inspected visually and can be easily unsoldered later.

The square hole in the middle of the board saver is sized to accommodate the FPGA, and the thickness of the board saver is the same as that of the FPGA. Hence, when a non-final FPGA is placed in the square hole, the combination of the non-final FPGA and the board saver occupy no more area and thickness than would a final FPGA soldered directly into its designated position on the first-mentioned circuit board. The contact leads of a non-final FPGA are not bent and are soldered, at the top of the board saver, to the corresponding via holes. A non-final FPGA can readily be unsoldered from the board saver and replaced by another one. Once the final FPGA design has been determined, the board saver can be unsoldered from the contact pads on the first-mentioned printed-circuit board and replaced by the final FPGA.

This work was done by Andrew Berkun of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-44745

Circuit for Driving Piezoelectric Transducers

Circuits similar to this one could be useful in ultrasonic cleaners.

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The figure schematically depicts an oscillator circuit for driving a piezoelectric transducer to excite vibrations in a mechanical structure. The circuit was designed and built to satisfy application-specific requirements to drive a selected one of 16 such transducers at a regulated amplitude and frequency chosen to optimize the amount of work performed by the transducer and to compensate for both (1) temporal variations of the resonance frequency and damping time of each transducer and (2) initially unknown differences among the resonance frequencies and damping times of different transducers. In other words, the circuit is designed to adjust itself to optimize the performance of whichever transducer is selected at any given time. The basic design concept may be adaptable to other applications that involve the use of piezoelectric transducers in ultrasonic cleaners and

other apparatuses in which high-frequency mechanical drives are utilized.

This circuit includes three resistor-capacitor networks that, together with the selected piezoelectric transducer, constitute a band-pass filter having a peak response at a frequency of about 2 kHz, which is approximately the resonance frequency of the piezoelectric transducers. Gain for generating oscillations is provided by a power hybrid operational amplifier (U_1). A junction field-effect transistor (Q_1) in combination with a resistor (R_4) is used as a voltage-variable resistor to control the magnitude of the oscillation. The voltage-variable resistor is part of a feedback control loop: Part of the output of the oscillator is rectified and filtered for use as a slow negative feedback to the gate of Q_1 to keep the output amplitude constant. The response of this control loop is much slower than 2 kHz and, therefore, does

not introduce significant distortion of the oscillator output, which is a fairly clean sine wave.

The positive AC feedback needed to sustain oscillations is derived from sampling the current through the piezoelectric transducer. This positive AC feedback, in combination with the slow feedback to the voltage-variable resistors, causes the overall loop gain to be just large enough to keep the oscillator running.

The positive feedback loop includes two 16-channel multiplexers, which are not shown in the figure. One multiplexer is used to select the desired piezoelectric transducer. The other multiplexer, which is provided for use in the event that there are significant differences among the damping times of the 16 piezoelectric transducers, facilitates changing the value of one of the resistors in the positive-feedback loop to accommodate the damping time of the selected transducer.