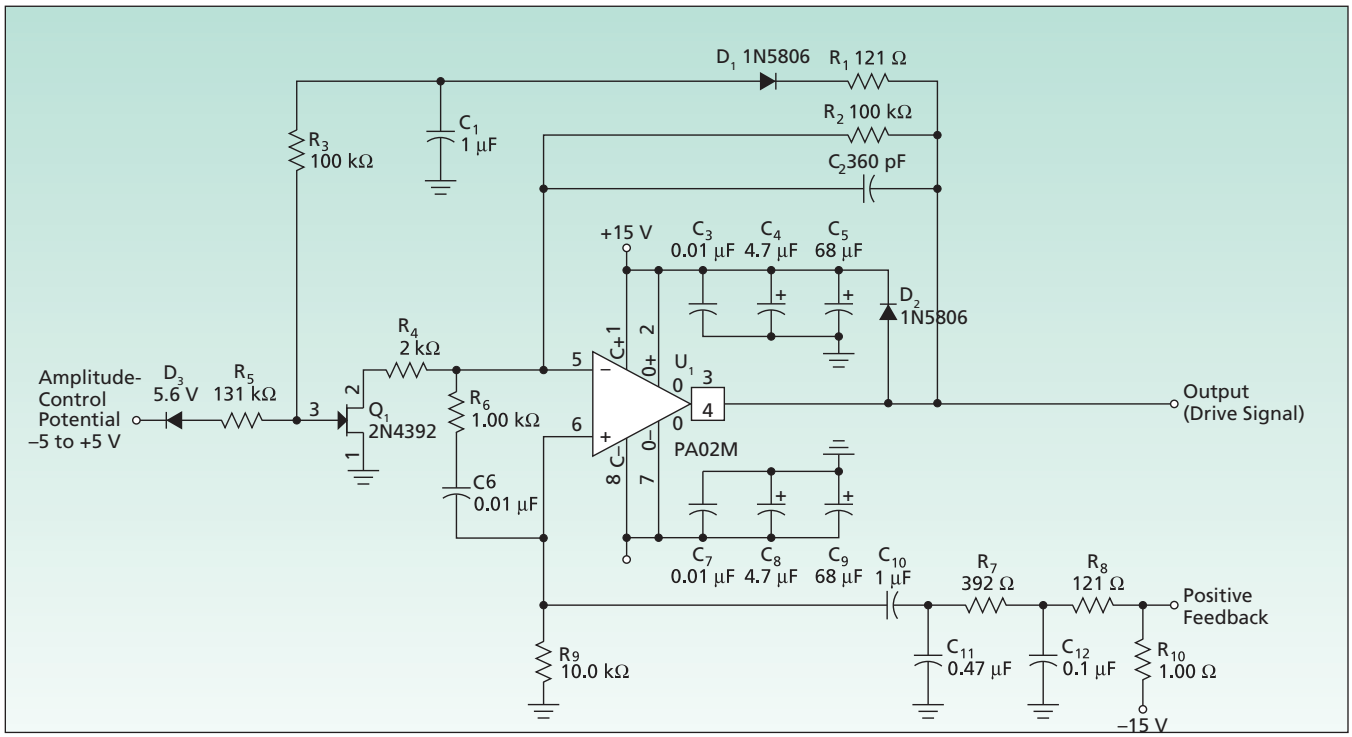

This **Oscillator Circuit** generates a nearly optimum, nearly sinusoidal output for driving a vibrational piezoelectric transducer.

The amplitude of the oscillator output is controlled by use of an externally generated potential, between –5 and +5 VDC, applied via Zener diode D_3 and resistor R_5 to the gate of Q_1: +5 VDC corresponds to an output amplitude of 25 V peak to peak; –5 VDC corresponds to an output amplitude of 9 V peak to peak.

Prior to the development of this circuit, it was common practice to excite vibrational piezoelectric transducers by use of "bang-bang" oscillators, the outputs of which contain significant proportions of harmonics. The harmonics contribute to stress and waste of power in heating the transducers. The near-sine-wave output of this circuit has much lower harmonic content and, therefore, imposes less stress on the transducers and enables them to operate at lower temperature.

Previously, it was also common practice to control the drive amplitude of oscillation by using an additional regulator circuit to control the supply potential. In this circuit, the supply potential is not varied and the amplitude of oscillation is controlled by use of a DC control potential as described above, eliminating the need for the additional regulator circuit.

This work was done by David P. Randall and Jacob Chapsky of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-45529

Digital Synchronizer Without Metastability

Lyndon B. Johnson Space Center, Houston, Texas

A proposed design for a digital synchronizing circuit would eliminate metastability that plagues flip-flop circuits in digital input/output interfaces. This metastability is associated with sampling, by use of flip-flops, of an external signal that is asynchronous with a clock signal that drives the flip-flops: it is a temporary flip-flop failure that can occur when a rising or falling edge of an asynchronous signal occurs during the setup and/or hold time of a flip-flop.

The proposed design calls for (1) use of a clock frequency greater than the frequency of the asynchronous signal, (2) use of flip-flop asynchronous preset or clear signals for the asynchronous input, (3) use of a clock asynchronous recovery delay with pulse width discriminator, and (4) tying the data inputs to constant logic levels to obtain (5) two half-rate synchronous partial signals — one for the falling and one for the rising edge. Inasmuch as the flip-flop data inputs would be permanently tied to constant logic levels, setup and hold times would not be violated. The half-rate partial signals would be recombined to construct a signal that would replicate the original asynchronous signal at its original rate but would be synchronous with the clock signal.

This work was done by Robert M. Simle and Jose A. Cavazos of Lockheed Martin Corp. for Johnson Space Center.

Title to this invention, covered by U.S. Patent No. 6,771,099 B2, has been waived under the provisions of the National Aeronautics and Space Act {42 U.S.C. 2457 (f)}. Inquiries concerning licenses for its commercial development should be addressed to:

Lockheed Martin General Counsel
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