

The **Board Saver** is shown here in a simplified plan view (greatly reduced number of via holes) and not to scale, to facilitate understanding of its basic layout.

via holes — one for each contact pad — along its periphery. As initially fabricated, the board saver is a wider ring containing full via holes, but then it is milled along its outer edges, cutting the

via holes in half and laterally exposing their interiors. The board saver is positioned in registration with the designated FPGA footprint and each via hole is soldered to the outer portion of the

corresponding FPGA contact pad on the first-mentioned printed-circuit board. The via-hole/contact joints can be inspected visually and can be easily unsoldered later.

The square hole in the middle of the board saver is sized to accommodate the FPGA, and the thickness of the board saver is the same as that of the FPGA. Hence, when a non-final FPGA is placed in the square hole, the combination of the non-final FPGA and the board saver occupy no more area and thickness than would a final FPGA soldered directly into its designated position on the first-mentioned circuit board. The contact leads of a non-final FPGA are not bent and are soldered, at the top of the board saver, to the corresponding via holes. A non-final FPGA can readily be unsoldered from the board saver and replaced by another one. Once the final FPGA design has been determined, the board saver can be unsoldered from the contact pads on the first-mentioned printed-circuit board and replaced by the final FPGA.

This work was done by Andrew Berkun of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-44745

Circuit for Driving Piezoelectric Transducers

Circuits similar to this one could be useful in ultrasonic cleaners.

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The figure schematically depicts an oscillator circuit for driving a piezoelectric transducer to excite vibrations in a mechanical structure. The circuit was designed and built to satisfy application-specific requirements to drive a selected one of 16 such transducers at a regulated amplitude and frequency chosen to optimize the amount of work performed by the transducer and to compensate for both (1) temporal variations of the resonance frequency and damping time of each transducer and (2) initially unknown differences among the resonance frequencies and damping times of different transducers. In other words, the circuit is designed to adjust itself to optimize the performance of whichever transducer is selected at any given time. The basic design concept may be adaptable to other applications that involve the use of piezoelectric transducers in ultrasonic cleaners and

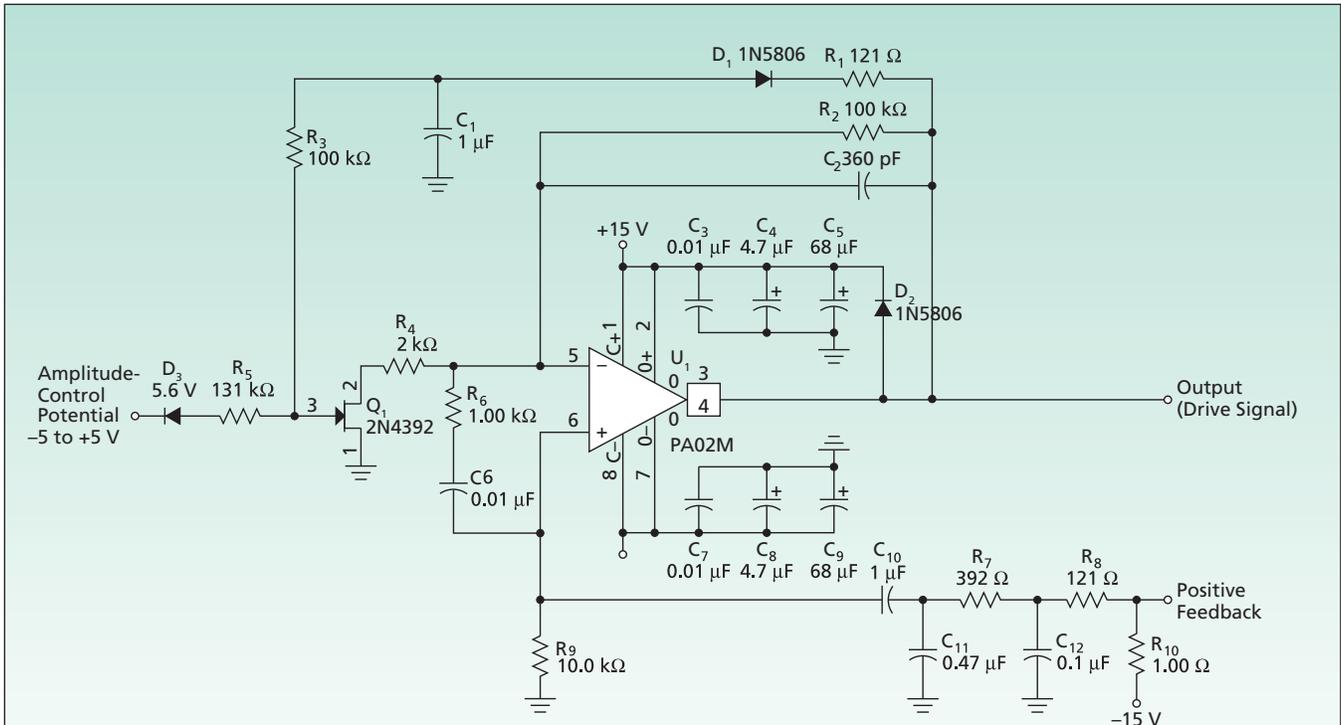
other apparatuses in which high-frequency mechanical drives are utilized.

This circuit includes three resistor-capacitor networks that, together with the selected piezoelectric transducer, constitute a band-pass filter having a peak response at a frequency of about 2 kHz, which is approximately the resonance frequency of the piezoelectric transducers. Gain for generating oscillations is provided by a power hybrid operational amplifier (U_1). A junction field-effect transistor (Q_1) in combination with a resistor (R_4) is used as a voltage-variable resistor to control the magnitude of the oscillation. The voltage-variable resistor is part of a feedback control loop: Part of the output of the oscillator is rectified and filtered for use as a slow negative feedback to the gate of Q_1 to keep the output amplitude constant. The response of this control loop is much slower than 2 kHz and, therefore, does

not introduce significant distortion of the oscillator output, which is a fairly clean sine wave.

The positive AC feedback needed to sustain oscillations is derived from sampling the current through the piezoelectric transducer. This positive AC feedback, in combination with the slow feedback to the voltage-variable resistors, causes the overall loop gain to be just large enough to keep the oscillator running.

The positive feedback loop includes two 16-channel multiplexers, which are not shown in the figure. One multiplexer is used to select the desired piezoelectric transducer. The other multiplexer, which is provided for use in the event that there are significant differences among the damping times of the 16 piezoelectric transducers, facilitates changing the value of one of the resistors in the positive-feedback loop to accommodate the damping time of the selected transducer.



This Oscillator Circuit generates a nearly optimum, nearly sinusoidal output for driving a vibrational piezoelectric transducer.

The amplitude of the oscillator output is controlled by use of an externally generated potential, between -5 and +5 VDC, applied via Zener diode D_3 and resistor R_5 to the gate of Q_1 : +5 VDC corresponds to an output amplitude of 25 V peak to peak; -5 VDC corresponds to an output amplitude of 9 V peak to peak.

Prior to the development of this circuit, it was common practice to excite vibrational piezoelectric transducers by use of

“bang-bang” oscillators, the outputs of which contain significant proportions of harmonics. The harmonics contribute to stress and waste of power in heating the transducers. The near-sine-wave output of this circuit has much lower harmonic content and, therefore, imposes less stress on the transducers and enables them to operate at lower temperature.

Previously, it was also common practice to control the drive amplitude of oscillation

by using an additional regulator circuit to control the supply potential. In this circuit, the supply potential is not varied and the amplitude of oscillation is controlled by use of a DC control potential as described above, eliminating the need for the additional regulator circuit.

This work was done by David P. Randall and Jacob Chapsky of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-45529

Digital Synchronizer Without Metastability

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A proposed design for a digital synchronizing circuit would eliminate metastability that plagues flip-flop circuits in digital input/output interfaces. This metastability is associated with sampling, by use of flip-flops, of an external signal that is asynchronous with a clock signal that drives the flip-flops: it is a temporary flip-flop failure that can occur when a rising or falling edge of an asynchronous signal occurs during the setup and/or hold time of a flip-flop.

The proposed design calls for (1) use of a clock frequency greater than the frequency of the asynchronous signal, (2) use of flip-flop asynchronous

preset or clear signals for the asynchronous input, (3) use of a clock asynchronous recovery delay with pulse width discriminator, and (4) tying the data inputs to constant logic levels to obtain (5) two half-rate synchronous partial signals — one for the falling and one for the rising edge. Inasmuch as the flip-flop data inputs would be permanently tied to constant logic levels, setup and hold times would not be violated. The half-rate partial signals would be recombined to construct a signal that would replicate the original asynchronous signal at its original rate but would be synchronous with the clock signal.

This work was done by Robert M. Simle and Jose A. Cavazos of Lockheed Martin Corp. for Johnson Space Center.

Title to this invention, covered by U.S. Patent No. 6,771,099 B2, has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)]. Inquiries concerning licenses for its commercial development should be addressed to:

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Refer to MSC-23220-1, volume and number of this NASA Tech Briefs issue, and the page number.