

of the G<sup>4</sup>FETs constitute additional terminals (that is, terminals not available in the older JFET version) to which one can apply control voltages  $V_N$  and  $V_P$ .

Circuits in which NDR devices have been used include (1) Schmitt triggers and (2) oscillators containing inductance/capacitance (LC) resonant circuits. Figure 2 depicts such circuits containing G<sup>4</sup>FET NDR devices like that of Figure 1. In the Schmitt trigger shown here, the G<sup>4</sup>FET NDR is loaded with an ordinary inversion-mode, p-channel, metal oxide/semiconductor field-effect transistor (inversion-mode PMOSFET), the  $V_N$  terminal of the G<sup>4</sup>FET NDR device is used as an input terminal, and the input terminals of the PMOSFET and the G<sup>4</sup>FET NDR device are connected.  $V_P$  can be used as an extra control volt-

age (that is, a control voltage not available in a typical prior Schmitt trigger) for adjusting the pinch-off voltage of the p-channel G<sup>4</sup>FET and thereby adjusting the trigger-voltage window.

In the oscillator, a G<sup>4</sup>FET NDR device is loaded with a conventional LC tank circuit. As in other LC NDR oscillators, oscillation occurs because the NDR counteracts the resistance in the tank circuit. The advantage of this G<sup>4</sup>FET-NDR LC oscillator over a conventional LC NDR oscillator is that one can apply a time-varying signal to one of the extra control input terminals ( $V_N$  or  $V_P$ ) to modulate the conductance of the NDR device and thereby amplitude-modulate the output signal.

*This work was done by Mohammad Mojaradi of Caltech; Suheng Chen, Ben Blalock, Chuck Britton, Ben Prothro, and James Vander-*

*sand of the University of Tennessee; Ron Schrimph of Vanderbilt University; and Sorin Cristoloveanu, Kerem Akarvardar, and P. Gentil of Grenoble University for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).*

*In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:*

*Innovative Technology Assets Management*

*JPL*

*Mail Stop 202-233*

*4800 Oak Grove Drive*

*Pasadena, CA 91109-8099*

*(818) 354-2240*

*E-mail: iaoffice@jpl.nasa.gov*

*Refer to NPO-43929, volume and number of this NASA Tech Briefs issue, and the page number.*

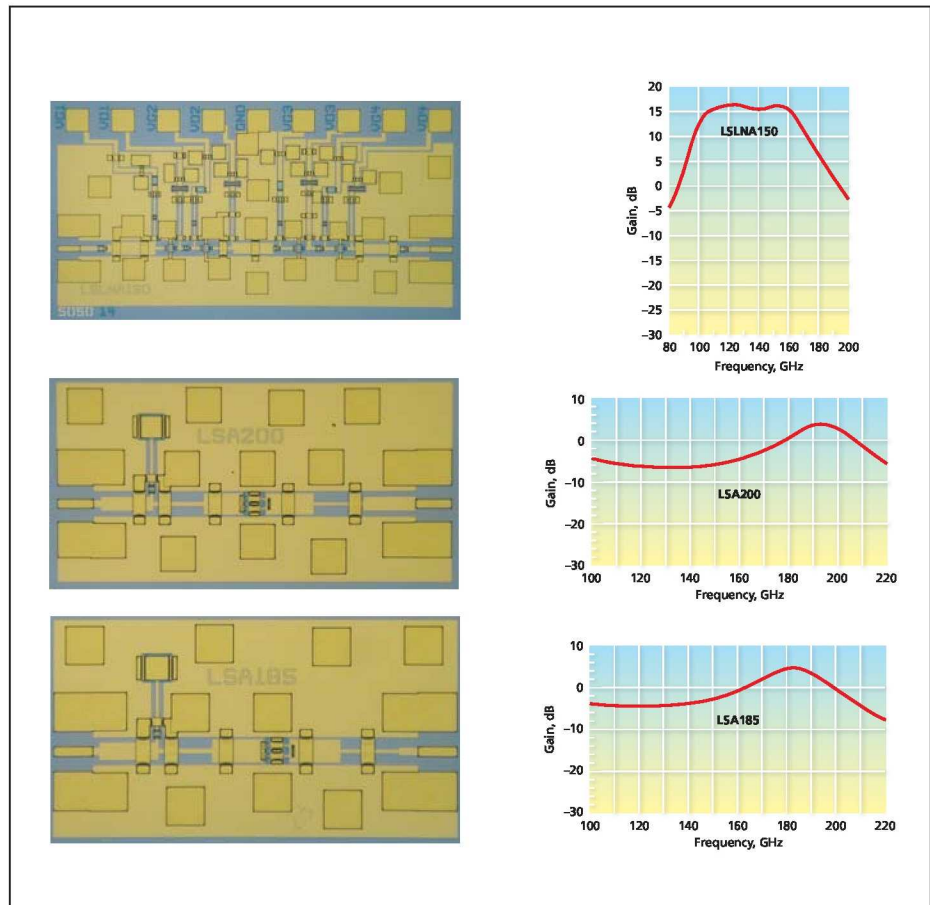
## Three MMIC Amplifiers for the 120-to-200 GHz Frequency Band

These would complement previously reported MMIC amplifiers designed for overlapping frequency bands.

NASA's Jet Propulsion Laboratory, Pasadena, California

Closely following the development reported in the immediately preceding article, three new monolithic microwave integrated circuit (MMIC) amplifiers that would operate in the 120-to-200-GHz frequency band have been designed and are under construction at this writing. The active devices in these amplifiers are InP high-electron-mobility transistors (HEMTs). These amplifiers (see figure) are denoted the LSLNA150, the LSA200, and the LSA185, respectively.

Like the amplifiers reported in the immediately preceding article, the LSLNA150 (1) is intended to be a prototype of low-noise amplifiers (LNAs) to be incorporated into spaceborne instruments for sensing cosmic microwave background radiation and (2) has potential for terrestrial use in electronic test equipment, passive millimeter-wave imaging systems, radar receivers, communication receivers, and systems for detecting hidden weapons. The HEMTs in this amplifier were fabricated according to 0.08- $\mu\text{m}$  design rules of a commercial product line of InP HEMT MMICs at HRL Laboratories, LLC, with a gate geometry of 2 fingers, each 15  $\mu\text{m}$  wide. On the basis of computational simulations, this amplifier is designed to afford at least 15



These Three MMIC Amplifiers have been designed to be suitable for a variety of applications at frequencies up to about 200 GHz.



dB of gain, with a noise figure of no more than about 6 dB, at frequencies from 120 to 160 GHz. The measured results of the amplifier are shown next to the chip photo, with a gain of 16 dB at 150 GHz. Noise figure work is ongoing.

The LSA200 and the LSA185 are intended to be prototypes of transmitting power amplifiers for use at frequencies between about 180 and about 200 GHz.

These amplifiers have also been fabricated according to rules of the aforesaid commercial product line of InP HEMT MMICs, except that the HEMTs in these amplifiers are characterized by a gate geometry of 4 fingers, each 37  $\mu\text{m}$  wide. The measured peak performance of the LSA200 is characterized by a gain of about 1.4 dB at a frequency of 190 GHz; the measured peak perform-

ance of the LSA185 is characterized by a gain of about 2.7 dB at a frequency of 181 GHz. The measured gain results of each chip are shown next to their respective photos.

*This work was done by Lorene Samoska of Caltech and Adele Schmitz of HRL Laboratories, LLC, for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-42846*

## Low-Noise MMIC Amplifiers for 120 to 180 GHz

Potential applications include radar, communications, radiometry, and millimeter-wave imaging.

NASA's Jet Propulsion Laboratory, Pasadena, California

Three-stage monolithic millimeter-wave integrated-circuit (MMIC) amplifiers capable of providing useful amounts of gain over the frequency range from 120 to 180 GHz have been developed as prototype low-noise amplifiers (LNAs) to be incorporated into instruments for sensing cosmic microwave background radiation. There are also potential uses for such LNAs in electronic test equipment, passive millimeter-wave imaging systems, radar receivers, communication receivers, and systems for detecting hidden weapons. The main advantage afforded by these MMIC LNAs, relative to prior MMIC LNAs, is that their coverage of the 120-to-180-GHz frequency band makes them suitable for reuse in a wider variety of applications without need to redesign them. Each of these MMIC amplifiers includes InP transistors and coplanar waveguide circuitry on a 50- $\mu\text{m}$ -thick chip (see Figure 1). Coplanar waveguide transmission lines are used for both applying DC bias and matching of input and output impedances of each transistor stage. Via holes are incorporated between top and bottom ground planes to suppress propagation of electromagnetic modes in the substrate.

On the basis of computational simulations, each of these amplifiers was expected to operate with a small-signal gain of 14 dB and a noise figure of 4.3 dB. At the time of writing this article, measurements of noise figures had not been reported, but on-chip measurements had shown gains approaching their simulated values (see Figure 2).

*This work was done by David Pukala, Lorene Samoska, and Alejandro Peralta of Caltech and Brian Bayuk, Ron Grundbacher, Patricia Oliver, Abdullah Cavus, and Po-Hsin Liu of Northrop Grumman Corporation for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). NPO-42783*

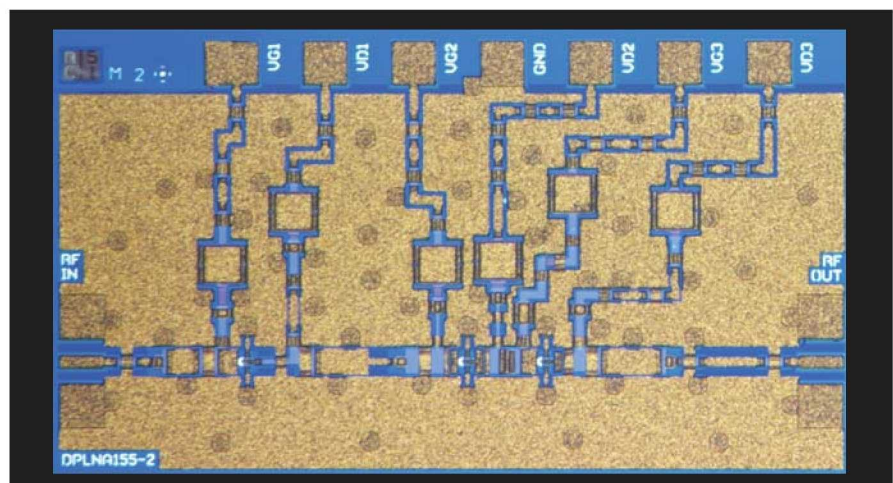


Figure 1. This MMIC contains three InP amplifier stages plus coplanar waveguide transmission lines for input and output impedance matching and DC biasing.

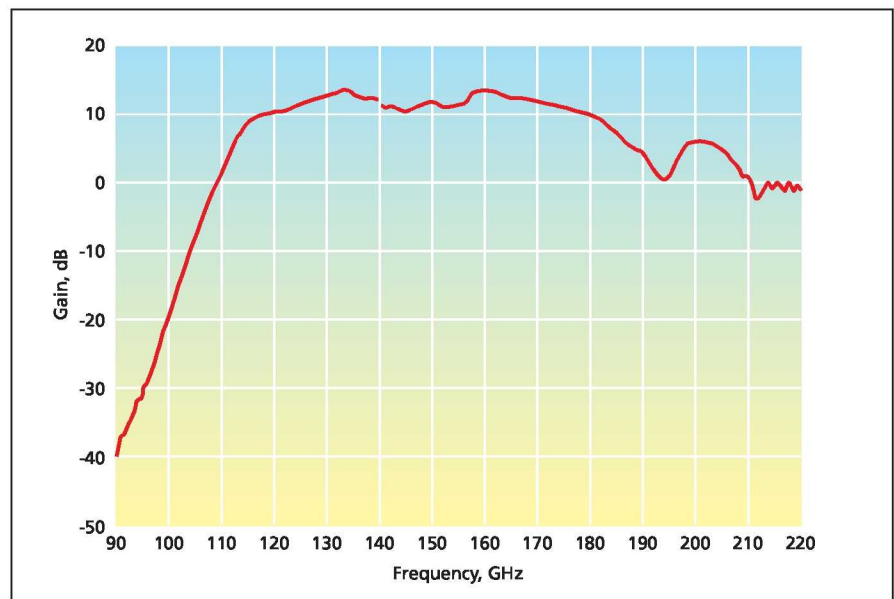


Figure 2. The Measured Gain of an amplifier like that shown in Figure 1 was found to exceed 10 dB over most of the frequency range from 120 to 180 GHz. The discontinuity in the plot at 140 GHz is an artifact of switching, at that frequency, between two waveguide bands of the instrumentation used to measure the gain.