Electronics/Computers

Integrated Spacesuit Audio System Enhances Speech Quality and Reduces Noise

This technology can also be adapted for teleconferencing, telemedicine, wireless voice communication, and other hands-free communications.

John H. Glenn Research Center, Cleveland, Ohio

A new approach has been proposed for increasing astronaut comfort and speech capture. Currently, the special design of a spacesuit forms an extreme acoustic environment making it difficult to capture clear speech without compromising comfort. The current system, called Communication-Cap-based Audio (CCA), relies on a single microphone placed close to the subject's mouth. While this results in clear audio, it also has problems: wire fatigue, blind mating, interference with food/drink, need for custom communication caps, and not being able to adjust the microphone during extravehicular activities.

The proposed Integrated Spacesuit Audio (ISA) system is to incorporate the microphones into the helmet and use software to extract voice signals from background noise. The system would rely on an array of microphones to en-hance speech quality. It will feature performance similar to the CCA system while providing comfort, ease of use, and logistical convenience. In this study, the feasibility of using microphone array beam forming or multichannel noise reduction plus a single-channel post-filter to combat a variety of in-helmet noise was validated.

The developed multichannel plus single-channel noise reduction approach can effectively enhance the intelligibility or quality of the speech from the subject. Using the acoustic data recorded inside spacesuits, it was shown that the developed multichannel noise reduction algorithm can help improve the signal-to-noise ratio (SNR) by approximately 20 dB in ideal cases, and 8–12 dB in worst cases. With four microphones, the multichannel noise reduction algorithm can yield a 4–5 dB gain in SNR with no distortion, and 12–15 dB SNR with a moderate amount of speech distortion. This new approach is more practical and more advantageous than the traditional microphone array beam-forming solutions.

This system would be applicable not only for spaceflight, but also for telecollaboration, human-machine interface, hands-free in-car phone interface, acoustic surveillance, and any kind of system where wide-area sound sensing is important.

This work was done by Yiteng (Arden) Huang, Jingdong Chen, and Shaoyan (Sharyl) Chen of WeVoice, Inc. for Glenn Research Center.

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steve Fedor, Mail Stop 4–8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18405-1.

Hardware Implementation of a Bilateral Subtraction Filter

Modules like this one are necessary for real-time stereoscopic machine vision.

NASA's Jet Propulsion Laboratory, Pasadena, California

A bilateral subtraction filter has been implemented as a hardware module in the form of a field-programmable gate array (FPGA). In general, a bilateral subtraction filter is a key subsystem of a high-quality stereoscopic machine vision system that utilizes images that are large and/or dense. Bilateral subtraction filters have been implemented in software on general-purpose computers, but the processing speeds attainable in this way — even on computers containing the fastest processors — are insufficient for real-time applications. The present FPGA bilateral subtraction filter is intended to accelerate processing to real-time speed and to be a prototype of a link in a stereoscopic-machine-vision processing chain, now under development, that would process large

and/or dense images in real time and would be implemented in an FPGA.

In terms that are necessarily oversimplified for the sake of brevity, a bilateral subtraction filter is a smoothing, edge-preserving filter for suppressing low-frequency noise. The filter operation amounts to replacing the value for each pixel with a weighted average of the values of that pixel and the neighboring pixels in a predefined neighborhood or window (e.g., a 9×9 window). The filter weights depend partly on pixel values and partly on the window size.

The present FPGA implementation of a bilateral subtraction filter utilizes a 9×9 window. This implementation was designed to take advantage of the ability to do many of the component computa-tions in parallel pipelines to enable processing of image data at the rate at which they are generated. The filter can be considered to be divided into the following parts (see figure):
- An image pixel pipeline with a 9×9-pixel window generator,
- An array of processing elements;
- An adder tree;
- A smoothing-and-delaying unit; and
- A subtraction unit.

After each 9×9 window is created, the affected pixel data are fed to the processing elements. Each processing element is fed the pixel value for its position in the window as well as the pixel value for the central pixel of the window. The absolute difference between these two pixel values is calculated and
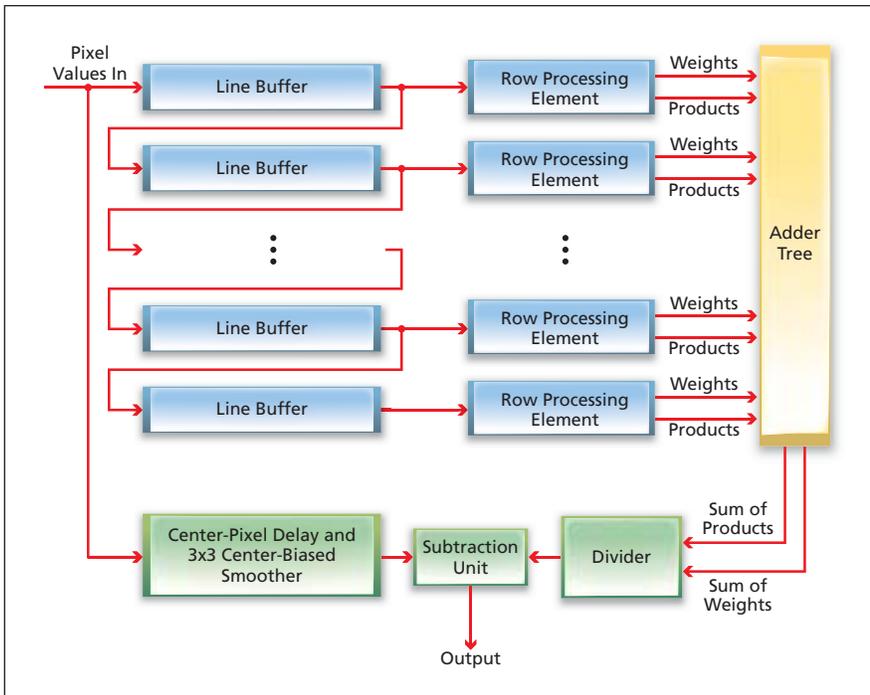
A **Bilateral Subtraction Filter** is implemented in an FPGA that performs parallel pipeline computations in a moving 9×9-pixel window.

used as an address in a lookup table. Each processing element has a lookup table, unique for its position in the window, containing the weight coefficients for the Gaussian function for that position. The pixel value is multiplied by the weight, and the outputs of the processing element are the weight and pixel-value·weight product. The products and weights are fed to the adder tree. The sum of the products and the sum of the weights are fed to the divider, which computes the sum of products ÷ the sum of weights. The output of the divider is denoted the bilateral smoothed image.

The smoothing function is a simple weighted average computed over a 3×3 subwindow centered in the 9×9 window. After smoothing, the image is delayed by an additional amount of time needed to match the processing time for computing the bilateral smoothed image. The bilateral smoothed image is then subtracted from the 3×3 smoothed image to produce the final output.

The prototype filter as implemented in a commercially available FPGA processes one pixel per clock cycle. Operation at a clock speed of 66 MHz has been demonstrated, and results of a static timing analysis have been interpreted as suggesting that the clock speed could be increased to as much as 100 MHz.

Simple Optoelectronic Feedback in Microwave Oscillators
Phase and frequency stability would be enhanced greatly.
NASA's Jet Propulsion Laboratory, Pasadena, California

A proposed method of stabilizing microwave and millimeter-wave oscillators calls for the use of feedback in optoelectronic delay lines characterized by high values of the resonance quality factor (Q). The method would extend the applicability of optoelectronic feedback beyond the previously reported class of optoelectronic oscillators that comprise two-port electronic amplifiers in closed loops with high-Q feedback circuits.

The upper part of the figure illustrates the example of a typical free-running oscillator in a conventional form stabilized with an external metal radio-frequency (RF) resonant cavity. The oscillator could be of any of a variety of types, including those based on Gunn diodes, impact avalanche transit-time (IMPATT) diodes, klystrons, backward-wave tubes, and others. The maximum Q of a typical resonant metal cavity ranges from about 10^4 at an oscillation frequency of 10 GHz down to
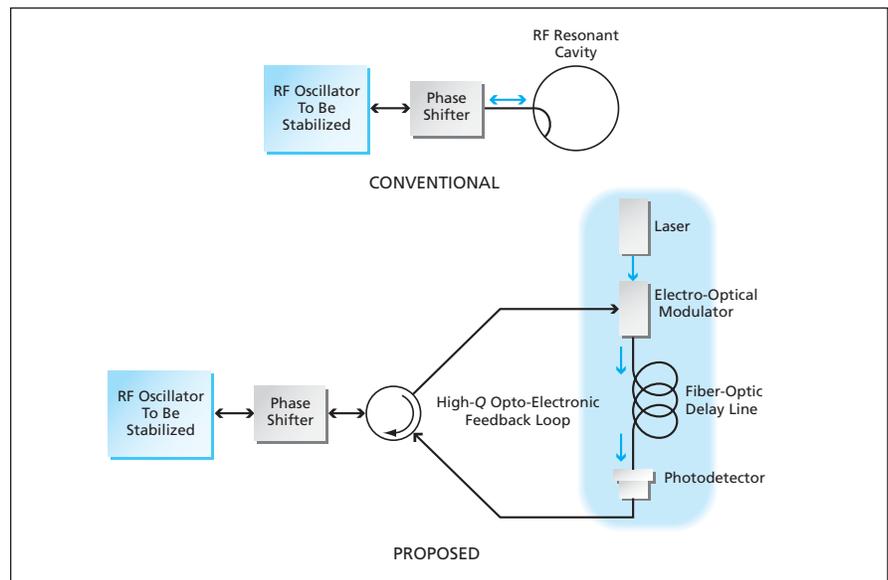
A **High-Q Optoelectronic Delay Line** would be substituted for the RF resonant cavity of a conventional free-running oscillator stabilized with an external resonator.