



Adaptation of the Camera Link Interface for Flight-Instrument Applications

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COTS (commercial-off-the-shelf) hardware using an industry-standard Camera Link interface is proposed to accomplish the task of designing, building, assembling, and testing electronics for an airborne spectrometer that would be low-cost, but sustain the required data speed and volume. The focal plane electronics were designed to support that hardware standard. Analysis was done to determine how these COTS electronics could be interfaced with space-qualified camera electronics. Interfaces available for spaceflight application do not support the industry standard Camera Link interface, but with

careful design, COTS EGSE (electronics ground support equipment), including camera interfaces and camera simulators, can still be used.

The Camera Link data path is expandable. By adding another pair of interface circuits, and five more LVDS (low-voltage differential signaling) pairs (the "medium" Camera Link interface), the data rate can be doubled (4,080 Mbps). By adding a third pair of interface circuits and five more LVDS pairs (the "full" Camera Link interface), data rates of $64 \text{ bits} \times 85 \text{ MHz} = 5,440 \text{ Mbps}$ (over 5 Gbps) can be realized. The 28-bit commercial Camera Link interface is back-

wards compatible with the 21-bit space-qualified Channel Link interface. With proper circuit design and EGSE programming, the space-qualified chip set can be used to implement a compatible Camera Link interface using COTS Camera Link EGSE. COTS EGSE in the form of instrument (camera) simulators is also readily available. This allows easy, early checkout of the EGSE and flight systems.

This work was done by David P. Randall and John C. Mahoney of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov. NPO-46991

High-Performance CCSDS Encapsulation Service Implementation in FPGA

This implementation can be used by telemetry receivers to process telemetry at high rates.

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The Consultative Committee for Space Data Systems (CCSDS) Encapsulation Service is a convergence layer between lower-layer space data link framing protocols, such as CCSDS Advanced Orbiting System (AOS), and higher-layer networking protocols, such as CFDP (CCSDS File Delivery Protocol) and Internet Protocol Extension (IPE). CCSDS Encapsulation Service is considered part of the data link layer. The CCSDS AOS implementation is described in the preceding article. Recent advancement in RF modem technology has allowed multi-megabit transmission over space links. With this increase in data rate, the CCSDS Encapsulation Service needs to be optimized to both reduce energy consumption and operate at a high rate.

CCSDS Encapsulation Service has been implemented as an intellectual property core so that the aforementioned problems are solved by way of operating the CCSDS Encapsulation Service inside an FPGA. The CCSDS

Encapsulation Service in FPGA implementation consists of both packetizing and de-packetizing features.

Packetizer features include:

- Interfaces to fixed-sized framing layers such as CCSDS AOS or variable-sized framing layers such as CCSDS Telemetry command on the egress side.
- Interfaces to any octet-aligned data source that can provide start and end data delimiter signals on the ingress side.
- Idle insertion using 1-byte encapsulation packets.
- Interoperability tested with commercial off-the-shelf telemetry receiver implementation from RT-Logic.
- Includes statistical counters at packet, frame, and byte levels to facilitate data product accounting.

De-Packetizer features include:

- Interfaces to fixed-frame-size framing layers such as CCSDS AOS and telemetry on the ingress side.

- Filters out all types of idle CCSDS encapsulation packets.
- Includes a staging buffer to re-assemble all fragments of the higher-layer protocol packets before releasing to the egress side.
- Includes the ability to discard incomplete packets that are spanned over multiple frames.
- Includes statistical counters at packet, frame, and byte levels to facilitate data product accounting.

The combination of energy and performance optimization that embodies this design makes the work novel.

This work was done by Loren P. Clare, Jordan L. Torgerson, and Jackson Pang of Caltech for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov.

The software used in this innovation is available for commercial licensing. Please contact Daniel Broderick of the California Institute of Technology at danielb@caltech.edu. NPO-47167