



Small Microprocessor for ASIC or FPGA Implementation

Goddard Space Flight Center, Greenbelt, Maryland

A small microprocessor, suitable for use in applications in which high reliability is required, was designed to be implemented in either an application-specific integrated circuit (ASIC) or a field-programmable gate array (FPGA). The design is based on commercial microprocessor architecture, making it possible to use available software development tools and thereby to implement the microprocessor at relatively low cost. The design features enhancements, including trapping during execution of il-

legal instructions. The internal structure of the design yields relatively high performance, with a significant decrease, relative to other microprocessors that perform the same functions, in the number of microcycles needed to execute macroinstructions.

The problem meant to be solved in designing this microprocessor was to provide a modest level of computational capability in a general-purpose processor while adding as little as possible to the power demand, size, and weight of a

system into which the microprocessor would be incorporated. As designed, this microprocessor consumes very little power and occupies only a small portion of a typical modern ASIC or FPGA. The microprocessor operates at a rate of about 4 million instructions per second with clock frequency of 20 MHz.

This work was done by Igor Kleyner, Richard Katz, and Hugh Blair-Smith of Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-15493-1

Source-Coupled, N-Channel, JFET-Based Digital Logic Gate Structure Using Resistive Level Shifters

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A circuit topography is used to create usable, digital logic gates using N (negatively doped) channel junction field effect transistors (JFETs), load resistors, level shifting resistors, and supply rails whose values are based on the DC parametric distributions of these JFETs. This method has direct application to the current state-of-the-art in high-temperature (300 to 500 °C and higher) silicon carbide (SiC) device production, and defines an adaptation to the logic gate described in U.S. Patent 7,688,117 in that, by removing the level shifter from the output of the gate structure described in the patent (and applying it to the input of the same gate), a source-

coupled gate topography is created. This structure allows for the construction AND/OR (sum of products) arrays that use far fewer transistors and resistors than the same array as constructed from the gates described in the aforementioned patent. This plays a central role when large multiplexer constructs are necessary; for example, as in the construction of memory.

This innovation moves the resistive level shifter from the output of the basic gate structure to the front as if the input is now configured as what would be the output of the preceding gate, wherein the output is the two level shifting resistors. The output of this innovation can

now be realized as the lone follower transistor with its source node as the gate output. Additionally, one may leave intact the resistive level shifter on the new gate topography. A source-coupled to direct-coupled logic translator will be the result.

This work was done by Michael J. Krasowski of Glenn Research Center. Further information is contained in a TSP (see page 1).

Inquiries concerning rights for the commercial use of this invention should be addressed to NASA Glenn Research Center, Innovative Partnerships Office, Attn: Steven Fedor, Mail Stop 4-8, 21000 Brookpark Road, Cleveland, Ohio 44135. Refer to LEW-18636-1.

High-Voltage-Input Level Translator Using Standard CMOS

High-voltage input circuitry would be combined with standard low-voltage CMOS circuitry.

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A proposed integrated circuit would translate (1) a pair of input signals having a low differential potential and a possibly high common-mode potential into (2) a pair of output signals having the same low differential potential and a low common-mode potential. As used

here, "low" and "high" refer to potentials that are, respectively, below or above the nominal supply potential (3.3 V) at which standard complementary metal oxide/semiconductor (CMOS) integrated circuits are designed to operate. The input common-mode potential

could lie between 0 and 10 V; the output common-mode potential would be 2 V. This translation would make it possible to process the pair of signals by use of standard 3.3-V CMOS analog and/or mixed-signal (analog and digital) circuitry on the same integrated-circuit