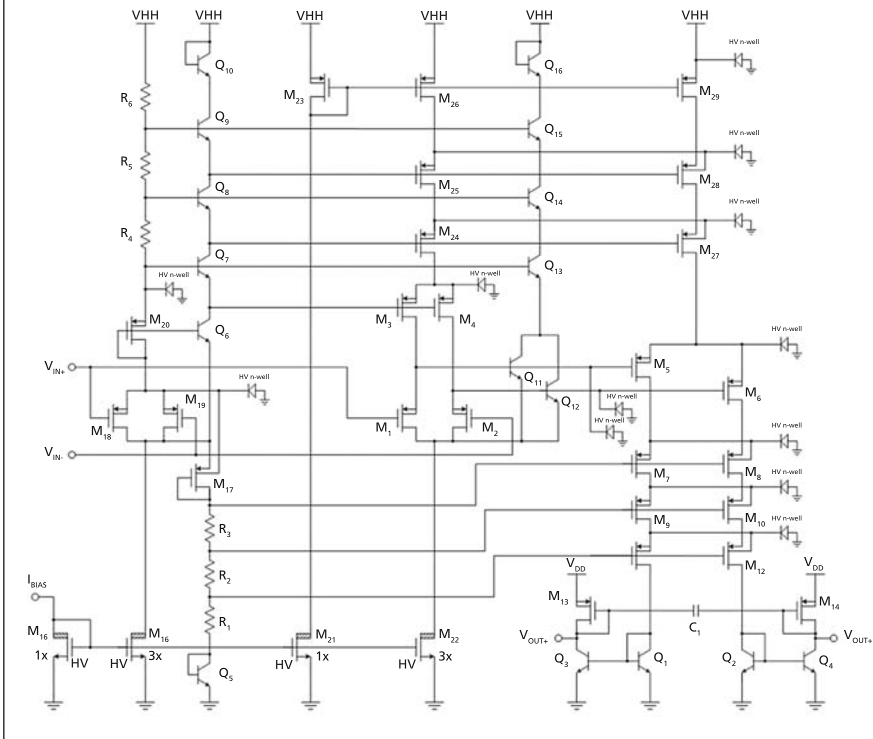
Input Common-Mode Range	0.3 to 10V
-3 dB Bandwidth	150 kHz
Common-Mode Rejection Ratio	>80 dB
Power Supply Rejection Ratio	>50 dB
Noise Characteristics MOS Flicker Noise@ 1HZ Flicker Noise Corner Broadband Noise	 $\approx$ 90 nV/$\sqrt{Hz}$ $\approx$ 800 Hz $\approx$ 55 nV/$\sqrt{Hz}$



Several Performance Parameters of the proposed level translator were extracted from results of computational simulations. The proposed circuit schematic is shown.

chip. A schematic of the circuit is shown in the figure.

Standard 3.3-V CMOS circuitry cannot withstand input potentials greater than about 4 V. However, there are many applications that involve low-differential-potential, high-common-mode-potential input signal pairs and in which standard 3.3-V CMOS circuitry, which is relatively inexpensive, would be the most appropriate circuitry for performing other functions on the integrated-circuit chip that handles the high-potential input signals. Thus, there is a need to combine high-voltage input circuitry with standard low-voltage CMOS circuitry on the same integrated-circuit chip. The proposed circuit would satisfy this need.

In the proposed circuit, the input signals would be coupled into both a level-shifting pair and a common-mode-sensing pair of CMOS transistors. The output of the level-shifting pair would be fed as input to a differential pair of transistors. The resulting differential current output would pass through six standoff transistors to be mirrored into an output branch by four heterojunction bipolar transistors. The mirrored differential current would be converted back to potential by a pair of diode-connected transistors, which, by virtue of being identical to the input transistors, would reproduce the input differential potential at the output.

The common-mode-sensing pair would be used to set the control potential for a biasing circuit that would provide the proper terminal potentials for protecting all devices against excessive excursions of potential for a common-mode potential range of 0 to 12 V. The biasing circuit would include high-voltage-drain transistors capable of withstanding the full high input potentials on their drains; the incorporation of these transistors would enable simplification of part of the bias circuit and of the circuitry associated with the input transistor pairs. High-voltage n-wells would enable floating of substrates of p-channel metal oxide/semiconductor field-effect transistors to potentials as high as tens of volts, whereas devices containing standard n-wells break down at potentials between 6 and 7 V, even though maximum gate-to-source and drain-to-source potentials remain at 3.3 V.

The expected performance of the circuit has been studied in computational simulations. The table presents values of some performance parameters determined from the results of the simulations.

This work was done by Jeremy A. Yager, Mohammad M. Mojarradi, and Tuan A. Vo of Caltech and Benjamin J. Blalock from University of Tenn., Knoxville for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1). ***NPO-45762***

Monitoring Digital Closed-Loop Feedback Systems

Designed-in test circuitry enables determination of performance margins and performance trends.

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A technique of monitoring digital closed-loop feedback systems has been conceived. The basic idea is to obtain information on the performances of closed-loop feedback circuits in such systems to aid in the determination of the functionality and integrity of the circuits and of performance margins.

The need for this technique arises as follows: Some modern digital systems include feedback circuits that enable other circuits to perform with precision and are tolerant of changes in environment and the device's parameters. For example, in a precision timing circuit, it is desirable to make the circuit insensitive to variability as a result of the manufacture of circuit components and to the effects of temperature, voltage, radiation, and aging. However, such a design can also result in masking the indications of damaged and/or deteriorating components.

The present technique incorporates test circuitry and associated engineering-

telemetry circuitry into an embedded system to monitor the closed-loop feedback circuits, using "spare gates" that are often available in field programmable gate arrays (FPGAs). This technique enables a test engineer to determine the amount of performance margin in the system, detect "out of family" circuit performance, and determine one or more trend(s) in the performance of the system.

In one system to which the technique has been applied, an ultra-stable oscillator is used as a reference for internal adjustment of 12 time-to-digital converters (TDCs). The feedback circuit produces a pulse-width-modulated signal that is fed as a control input into an amplifier, which controls the circuit's operating voltage. If the circuit's gates are determined to be operating too slowly or rapidly when their timing is compared with that of the reference signal, then the pulse width increases or decreases, respectively, thereby commanding the amplifier to increase or reduce, respectively, its output level, and "adjust" the speed of the circuits. The nominal frequency of the TDC's pulse width modulated outputs is approximately 40 kHz.

In this system, the technique is implemented by means of a monitoring circuit that includes a 20-MHz sampling circuit and a 24-bit accumulator with a gate time of 10 ms. The monitoring circuit measures the duty cycle of each of the 12 TDCs at a repetition rate of 28 Hz. The accumulator content is reset to all zeroes at the beginning of each measurement period and is then incremented or decremented based of the value of the state of the pulse width modulated signal. Positive or negative values in the accumulator correspond to duty cycles greater or less, respectively, than 50 percent.

This work was done by Richard Katz and Igor Kleyner of Goddard Space Flight Center. Further information is contained in a TSP (see page 1). *GSC-15489-1*