Multifunctional Logic Gate Controlled by Temperature

This circuit performs different logic functions at different temperatures.

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The figure is a schematic diagram of a complementary metal oxide/semiconductor (CMOS) electronic circuit that has been designed to function as a NAND gate at a temperature between 0 and 80 °C and as a NOR gate at temperatures from 120 to 200 °C. In the intermediate temperature range of 80 to 120 °C, this circuit is expected to perform a function intermediate between NAND and NOR with degraded noise margin. The process of designing the circuit and the planned fabrication and testing of the circuit are parts of demonstration of polymorphic electronics — a technological discipline that emphasizes designing the same circuit to perform different analog and/or digital functions under different conditions. In this case, the different conditions are different temperatures.

A more extensive discussion of polymorphic electronics was presented in "Polymorphic Electronic Circuits" (NPO-21213), *NASA Tech Briefs*, Vol. 28, No. 4 (April 2004), page 38. To recapitulate: The traditional approach to design is abandoned in favor of an evolutionary approach to impart the desired multiple functionality to a circuit. In the evolutionary approach, one designs, constructs, and tests a sequence of populations of circuits that function as incrementally better solutions of a given design problem through the selective, repetitive connection and/or disconnection of capacitors, transistors, amplifiers, inverters, and/or other circuit building blocks. The evolution is guided by a search-and-optimization algorithm (in particular, a genetic algorithm) that operates in the space of possible circuits to find a circuit that exhibits an acceptably close approximation of the desired functionality.

In the evolutionary approach, a circuit design can be tested by computational simulation, tested in real hardware, or tested in random sequences of computational simulation and real hardware. In the present case, the designed functionality has been tested thus far by computational simulation and also in real time. The computational simulations have included many tests to assess the robustness of the NAND and NOR gate performances in the presence of noise, for all possible sequences of positive and negative input-signal transitions, and under changes in diverse parameters that include not only temperature but also switching speed, power dissipation, power-supply voltage, transistor sizes, and changes in the transistor model between two commercial fabrication processes. These tests showed the performances to be robust, and once fabricated, the circuit performed as intended.

This work was done by Adrian Stoica and Ricardo Zebulum of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1).*
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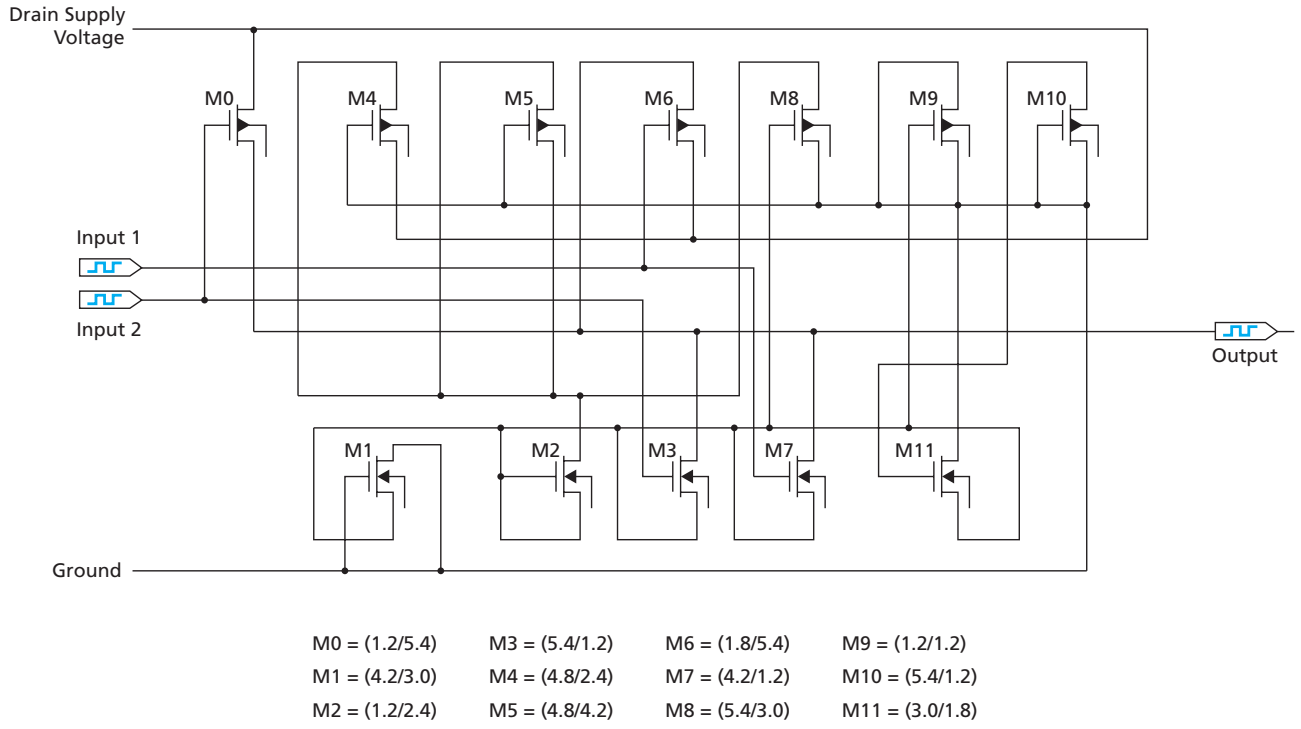

This **Circuit Performs as One of Two Logic Gates**, depending on the temperature. Between 0 and 80 °C, it is a NAND gate; between 120 and 200 °C, it is a NOR gate. The labels M0 through M11 refer to twelve transistors in this circuit. The first and second numbers in parentheses next to each label are the width and length, respectively, of the transistor in microns.