Multifunctional Logic Gate Controlled by Supply Voltage

This circuit performs different logic functions at different levels of supply voltage.

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The figure is a schematic diagram of a complementary metal oxide/semiconductor (CMOS) electronic circuit that functions as a NAND gate at a power-supply potential (V_{dd}) of 3.3 V and as NOR gate for V_{dd} = 1.8 V. In the intermediate V_{dd} range of 1.8 to 3.3 V, this circuit performs a function intermediate between NAND and NOR with degraded noise margin. Like the circuit of the immediately preceding article, this circuit serves as a demonstration of the evolutionary approach to design of polymorphic electronics — a technological discipline that emphasizes evolution of the design of a circuit to perform different analog and/or digital functions under different conditions. In this instance, the different conditions are different values of V_{dd}.

This demonstration is a step toward the development of a variety of logic gates, the functionalities of which can be changed by a single global signal — in this case, V_{dd}. The state-of-the-art logic circuits with which polymorphic logic circuits can be expected to compete are the configurable logic blocks (CLBs) of field-programmable gate arrays (FPGAs). The reconfiguration of a typical CLB involves multiplexing, switching, and downloading of thousands of bits from a lookup-table memory circuit. To configure in excess of thousands of CLBs in a larger FPGA may take even seconds; moreover, for satellite/spacecraft FPGA for which a new configuration is sent from Earth through a slow uplink communication, the time to reconfigure could be much longer. The main advantages of the type of polymorphism demonstrated here are the rapidity of the change in functionality and the simplicity of the circuitry needed to effect the change: Simply by changing V_{dd}, the functionalities of thousands of logic cells can be changed within nanoseconds, without multiplexing and without switches or lookup tables.

As in the case of the preceding article, the functionality of the present circuit has been tested by computational simulations. The simulations have tested the robustness of the circuit in the presence of input noise, for all possible sequences of positive and negative input-signal transitions, and under changes in parameters that include not only V_{dd} but, also temperature, switching speed, fanout, and power dissipation. In addition, the circuit has been fabricated on a silicon chip and verified to function substantially as intended. This is the first circuit designed by artificial evolution to be so realized.

This work was done by Adrian Stoica and Ricardo Zebulum of Caltech for **NASA's Jet Propulsion Laboratory**. *Further information is contained in a TSP (see page 1).*

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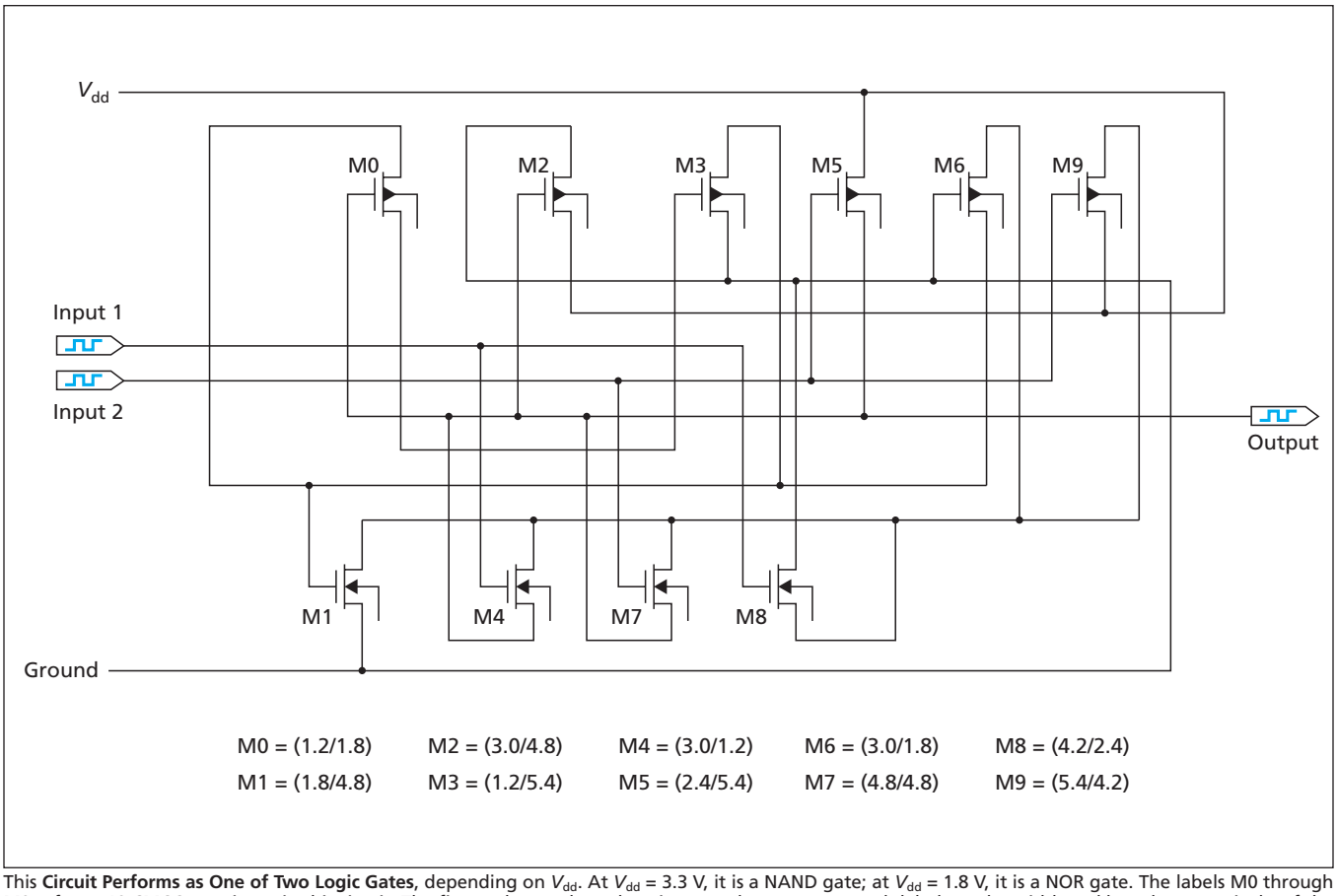

This **Circuit Performs as One of Two Logic Gates**, depending on V_{dd}. At V_{dd} = 3.3 V, it is a NAND gate; at V_{dd} = 1.8 V, it is a NOR gate. The labels M0 through M9 refer to 10 CMOS transistors in this circuit. The first and second numbers in parentheses next to each label are the width and length, respectively, of the transistor in microns.