Power Divider for Waveforms Rich in Harmonics

The power of a square-wave signal can be divided without adverse effect on either the amplitude or phase of the waveform.

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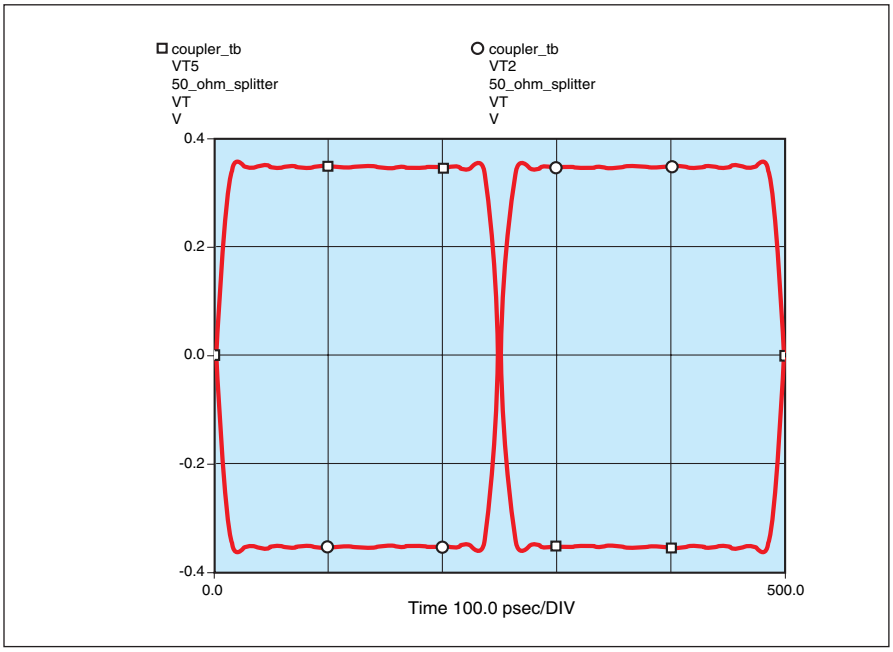
A method for dividing the power of an electronic signal rich in harmonics involves the use of an improved divider topology. A divider designed with this topology could be used, for example, to propagate a square-wave signal in an amplifier designed with a push-pull configuration to enable the generation of more power than could be generated in another configuration.

Many power-divider topologies have been conceived for application in power amplifiers operating at microwave and lower radio frequencies. Some examples are (1) the Wilkinson hybrid topology, which is restricted to division by powers of two, (2) the radial-wave power hybrid topology, which includes a lumped-element filter network, and (3) the circular-sector topology, which features a narrow usable frequency range.



These Two Waveforms at Output Ports of a 50-Ω Power Divider are 180° out of phase with each other and resemble the input waveform.

The present improved topology was developed for an application in which there is a requirement to divide the power of a square-wave radio signal and deliver the signal to an antenna. Another requirement is to maintain the relative-amplitude and phase relationship between the fundamental-frequency component and each of the harmonic-frequency components. The present improved power-divider topology satisfies these requirements. The figure presents an example of output waveforms from a power divider of this topology.

This work was done by William Herbert Sims III of **Marshall Space Flight Center**. *Further information is contained in a TSP (see page 1).*

This invention has been patented by NASA (U.S. Patent No. 6,320,478). Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to Sammy Nabors, MSFC Commercialization Assistance Lead, at (256) 544-5226 or sammy.a.nabors@nasa.gov. Refer to MFS-31186.

SCB Quantum Computers Using iSWAP and 1-Qubit Rotations

Practical implementation in the SCB context appears to be feasible.

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Units of superconducting circuitry that exploit the concept of the single-Cooper-pair box (SCB) have been built and are undergoing testing as prototypes of logic gates that could, in principle, constitute building blocks of clocked quantum computers. These units utilize quantized charge states as the quantum information-bearing degrees of freedom.

An SCB is an artificial two-level quantum system that comprises a nanoscale superconducting electrode connected to a reservoir of Cooper-pair charges via a Josephson junction. The logical quantum states of the device, $|0\rangle$ and $|1\rangle$, are implemented physically as a pair of charge-number states that differ by $2e$ (where e is the charge of an electron). Typically, some 10^9 Cooper pairs are involved. Transitions between the logical states are accomplished by tunneling of Cooper pairs through the Josephson junction. Although the two-level system contains a macroscopic number of charges, in the superconducting regime, they behave collectively, as a Bose-Einstein condensate, making possible a coherent superposition of the two logical states. This possibility makes the SCB a candidate for the physical implementation of a qubit.

A set of quantum logic operations and the gates that implement them is characterized as universal if, in principle, one can form combinations of the operations in the set to implement any desired quantum computation. To be able to design a practical quantum computer, one must first specify how to decompose any valid quantum computation into a sequence of elementary 1- and 2-qubit quantum gates that are universal and that can be realized in hardware that is feasible to fabricate. Traditionally, the set of universal gates has been taken to be the set of all 1-qubit quantum gates in conjunction with the