NASA/TM—2012-217290 AIAA–2011–5509

Small Radioisotope Power System at NASA Glenn Research Center

Gina M. Dugala
Glenn Research Center, Cleveland, Ohio

Martin Fraeman, David P. Frankford, Dennis Duven, Andrei Shamkovich, and Hollis Ambrose
The Johns Hopkins University, Applied Physics Laboratory, Laurel, Maryland

David W. Meer
Sest Inc., Middleburg Heights, Ohio

January 2012

NASA STI Program . . . in Profile

Since its founding, NASA has been dedicated to the advancement of aeronautics and space science. The NASA Scientific and Technical Information (STI) program plays a key part in helping NASA maintain this important role.

The NASA STI Program operates under the auspices of the Agency Chief Information Officer. It collects, organizes, provides for archiving, and disseminates NASA's STI. The NASA STI program provides access to the NASA Aeronautics and Space Database and its public interface, the NASA Technical Reports Server, thus providing one of the largest collections of aeronautical and space science STI in the world. Results are published in both non-NASA channels and by NASA in the NASA STI Report Series, which includes the following report types:

- TECHNICAL PUBLICATION. Reports of completed research or a major significant phase of research that present the results of NASA programs and include extensive data or theoretical analysis. Includes compilations of significant scientific and technical data and information deemed to be of continuing reference value. NASA counterpart of peer-reviewed formal professional papers but has less stringent limitations on manuscript length and extent of graphic presentations.

- TECHNICAL MEMORANDUM. Scientific and technical findings that are preliminary or of specialized interest, e.g., quick release reports, working papers, and bibliographies that contain minimal annotation. Does not contain extensive analysis.

- CONTRACTOR REPORT. Scientific and technical findings by NASA-sponsored contractors and grantees.

- CONFERENCE PUBLICATION. Collected papers from scientific and technical conferences, symposia, seminars, or other meetings sponsored or cosponsored by NASA.

- SPECIAL PUBLICATION. Scientific, technical, or historical information from NASA programs, projects, and missions, often concerned with subjects having substantial public interest.

- TECHNICAL TRANSLATION. English-language translations of foreign scientific and technical material pertinent to NASA's mission.

Specialized services also include creating custom thesauri, building customized databases, organizing and publishing research results.

For more information about the NASA STI program, see the following:

- Access the NASA STI program home page at *http://www.sti.nasa.gov*

- E-mail your question via the Internet to *help@sti.nasa.gov*

- Fax your question to the NASA STI Help Desk at 443–757–5803

- Telephone the NASA STI Help Desk at 443–757–5802

- Write to:
  NASA Center for AeroSpace Information (CASI)
  7115 Standard Drive
  Hanover, MD 21076–1320

NASA/TM—2012-217290 AIAA–2011–5509

Small Radioisotope Power System at NASA Glenn Research Center

Gina M. Dugala
Glenn Research Center, Cleveland, Ohio

Martin Fraeman, David P. Frankford, Dennis Duven, Andrei Shamkovich, and Hollis Ambrose
The Johns Hopkins University, Applied Physics Laboratory, Laurel, Maryland

David W. Meer
Sest Inc., Middleburg Heights, Ohio

Prepared for the
9th International Energy Conversion Engineering Conference (IECEC)
sponsored by the American Institute of Aeronautics and Astronautics
San Diego, California, July 31–August 3, 2011

National Aeronautics and
Space Administration

Glenn Research Center
Cleveland, Ohio 44135

January 2012

Acknowledgments

This work is funded through the NASA Science Mission Directorate. Any opinions, findings, and conclusions or recommendations expressed in this article are those of the authors and do not necessarily reflect the views of the National Aeronautics and Space Administration. A number of people provided invaluable assistance to the project. The authors wish to acknowledge personnel at the NASA Glenn Research Center including Michael Brace, Salvatore Oriti, Wayne Gerber, and Mark Bell who provided mechanical and electrical testing support and Wayne Wong who provided support for the development of ASC-L with the passive balancer, and Richard Shaltens who contributed to project development. The authors wish to acknowledge personnel at The Johns Hopkins University Applied Physics Laboratory including Ron Dennisen who was the Program Manager, John Hayes developed the microcontroller, floating point processor, and control law sequencer and wrote the initial version of the microcontroller software. Albert Hong led the mechanical effort to design and analyze the chassis structure. Joanna Mellert performed most of the remaining FPGA design, and Harry Shipley built and helped test many of the breadboard circuits, Robert Summers developed the SCC SRD, and Clayton Smith guided the development of the FMEA. The authors wish to acknowledge personnel at Sunpower, Inc. including Doug Mansfield and Yongsu Kim who assisted in development and testing of ASC-L with the passive balancer. The success of the SRPS project would not have been possible without these contributions.

Level of Review: This material has been technically reviewed by technical management.

Available from

NASA Center for Aerospace Information
7115 Standard Drive
Hanover, MD 21076–1320

National Technical Information Service
5301 Shawnee Road
Alexandria, VA 22312

Available electronically at http://www.sti.nasa.gov

Small Radioisotope Power System at NASA Glenn Research Center

Gina M. Dugala
National Aeronautics and Space Administration
Glenn Research Center
Cleveland, Ohio 44135

Martin Fraeman, David P. Frankford, Dennis Duven, Andrei Shamkovich, and Hollis Ambrose
The Johns Hopkins University
Applied Physics Laboratory
Laurel, Maryland 20723

David W. Meer
Sest Inc.
Middleburg Heights, Ohio 44130

Abstract

In April 2009, NASA Glenn Research Center (GRC) formed an integrated product team (IPT) to develop a Small Radioisotope Power System (SRPS) utilizing a single Advanced Stirling Convertor (ASC) with passive balancer for possible use by the International Lunar Network (ILN) program. The ILN program is studying the feasibility of implementing a multiple node seismometer network to investigate the internal lunar structure. A single ASC produces approximately 80 W_e and could potentially supply sufficient power for that application. The IPT consists of Sunpower, Inc., to provide the single ASC with balancer, The Johns Hopkins University Applied Physics Laboratory (JHU/APL) to design an engineering model Single Convertor Controller (SCC) for an ASC with balancer, and NASA GRC to provide technical support to these tasks and to develop a simulated lunar lander test stand. A controller maintains stable operation of an ASC. It regulates the alternating current produced by the linear alternator of the convertor, provides a specified output voltage, and maintains operation at a steady piston amplitude and hot end temperature. JHU/APL also designed an ASC dynamic engine/alternator simulator to aid in the testing and troubleshooting of the SCC. This paper describes the requirements, design, and development of the SCC, including some of the key challenges and the solutions chosen to overcome those issues. In addition, it describes the plans to analyze the effectiveness of a passive balancer to minimize vibration from the ASC, characterize the effect of ASC vibration on a lunar lander, characterize the performance of the SCC, and integrate the single ASC, SCC, and lunar lander test stand to characterize performance of the overall system.

Nomenclature

AC	alternating current
A/D	analog to digital converter
ASC–L	Advanced Stirling Convertor—lunar
CBE	current best estimate
CSAF	cold side adapter flange
D/A	digital to analog converter
DC	direct current
DDS	direct digital synthesizer
DSP	digital signal processor
E	engineering-level Stirling convertor

E2	second generation of the engineering-level Stirling convertor
EDR	engineering design review
EM	engineering model
EMF	electromotive force
EMI	electromagnetic interference
FET	field effect transistor
FPGA	field programmable gate array
GRC	Glenn Research Center
IEEE	Institute of Electrical and Electronics Engineers
ILN	International Lunar Network
IPT	Integrated Product Team
JHU/APL	The Johns Hopkins University Applied Physics Laboratory
PV	pressure vessel
PWM	pulse width modulated
SCC	Single Convertor Controller
SDM	System Dynamic Model
SRD	systems requirements document
SRL	Stirling Research Laboratory
SRPS	Small Radioisotope Power System
TID	total ionizing dose

1.0 Introduction

NASA Glenn Research Center (GRC) is the lead NASA center for the development of the Advanced Stirling Convertor (ASC) for use in space. In April 2009, NASA GRC formed an integrated product team (IPT) to develop a Small Radioisotope Power System (SRPS) utilizing a single ASC with passive balancer for possible use by the International Lunar Network (ILN) program. The ILN program is studying the feasibility of implementing a multiple-node seismometer network to investigate the internal lunar structure. A single ASC produces approximately 80 W_e and could potentially supply sufficient power for that application. The IPT consists of Sunpower, Inc., to provide an ASC with balancer, The Johns Hopkins University Applied Physics Laboratory (JHU/APL) to design an engineering model (EM) Single Convertor Controller (SCC) for the single ASC with balancer, and NASA GRC to provide technical support to these tasks and to develop a simulated lunar lander test stand. JHU/APL also designed an ASC dynamic engine/alternator simulator to aid in the testing and troubleshooting of the SCC.

The ASCs tested in the Stirling Research Laboratory (SRL) at NASA GRC are tested both as single units and dual-opposed pairs. A single ASC requires mounting to a large mass to reduce vibration produced by the convertor. A dual-opposed pair is mounted with the heater heads facing outward and the pressure vessel sections rigidly attached to each other. This configuration permits dynamically balanced operation where the piston's motions are equal but opposite in direction. However, a single ASC mounted to a large mass is impractical for spacecraft applications. Therefore, under the SRPS project, Sunpower, Inc. designed a passive balancer to replace the large mass and spring system used to absorb the vibration produced by the ASC.

The vibration produced by the ASC can affect the lander on which it is mounted. Pagnotta Engineering was tasked with designing a test stand that simulated a lunar lander. This represents the first test stand in the SRL at GRC that attempts to characterize the effect of ASC vibration on a lander.

The SCC maintains stable operation of the Stirling convertor. It regulates the alternating current (AC) produced by the linear alternator of the convertor, provides a specified direct current (DC) output voltage for the spacecraft, and maintains operation with a stable piston amplitude and hot end temperature. The controller allows adjustment of the operating point; the hot end temperature or piston amplitude may be increased or decreased. The piston amplitude is maintained by varying the load with the regulation stage

of the controller. The load presented by the controller accepts all power produced by the convertor. If the controller did not dissipate all the power, the excess would flow into the resonating piston motion, increasing amplitude, and ultimately resulting in damage to internal convertor components. Similarly, if the controller dissipated more power than produced, the balance would be extracted from the resonating piston motion, causing the piston to stall.

This paper describes an advanced ASC controller that does not require a physical tuning capacitor. Most ASC controllers in the SRL at GRC use a tuning capacitor to keep the stator current in phase with back electromotive force (EMF) voltage and piston velocity. Under these conditions, convertor operation is stable and load current flows as a response to terminal voltage. One consequence of this technique is that the tuning capacitors only cancel the alternator inductance at a single frequency. If the operating frequency deviates significantly from this value, the power factor correction is less effective. These capacitors have a large mass and volume and are unattractive for spacecraft applications.

The JHU/APL advanced controller is designed for use with one ASC whereas the others used in the SRL at GRC are intended for dual-opposed configured ASCs. The controller for a dual-opposed pair of convertors must synchronize the piston motion of the two convertors to minimize vibration as well as manage their operation. The JHU/APL controller only works with one ASC and therefore was given the name SCC. The controller was designed for flight use, but only a mechanically-equivalent, non-flight EM was built. The goal of the SCC task was to design and build a small, efficient, and reliable controller for use with a single ASC.

APL designed the controller in several stages to achieve this goal. The initial phase of the project, conceptual design, concentrated on developing the systems requirements document (SRD), conducting necessary trade studies and developing the conceptual design of the SCC. The initial phase culminated with a systems requirements review. The trade studies included desired alternator voltage, communication protocol, and controller location. The next phase of the project developed a preliminary design and led to a preliminary design review. The third phase of the project, final design, consisted of the completion and testing of breadboards of the SCC identified in the preliminary design phase, further refinements to the SCC design and parts procurement for the final EM SCC. The breadboard testing occurred at APL with GRC providing the ASC and ground support equipment. An engineering design review (EDR) was held at the end of this phase. The final phase of the project, build and test, produced an EM SCC based on the final design agreed upon at the EDR. This phase included testing of the SCC with an ASC. Further testing at GRC will include evaluation of the controller when the ASC is undergoing vibration that simulates realistic launch environments.

To aid in the testing of the breadboard and SCC versions, JHU/APL developed a dynamic engine/alternator simulator. A dynamic engine/alternator simulator refers to a combination of hardware and software to simulate the operation and electrical behavior of the ASC in real time. Prior to the JHU/APL dynamic engine/alternator simulator, advanced controller testing was performed with a resistor and inductor or an actual ASC. The dynamic engine/alternator simulator allows the controller designer to perform tests risk free and in less time. Operating an ASC with an advanced controller throughout its design cycle can damage the ASC if the controller does not function properly. Preparing the ASC for operation as well as bringing the ASC to/from the desired operating temperature is also time consuming and slows the evaluation of the controller. Testing with a resistor and inductor to simulate the engine does not accurately represent the dynamics of an ASC. Therefore, the controller did not function on the ASCs as expected from testing with a resistor, inductor, and AC source.

The goals of the SRPS project are as follows: analyze the effectiveness of a passive balancer on minimizing vibration from the ASC, characterize the effect of ASC vibration on a lunar lander, characterize the performance of the EM SCC, and integrate the single ASC with balancer, SCC, and lunar lander test stand to characterize performance of the system. This paper discusses the design, testing, and future work of the SRPS and dynamic engine/alternator simulator.

2.0 Single ASC Test Setup

A technology development effort was initiated with Sunpower, Inc., to extend the application of an ASC for missions requiring a higher rejection temperature, lower mass and lower power requirements. To meet these needs, two updates were made to the current ASC design; existing magnets were replaced with higher temperature rated magnets and a balancer was designed to use as an interface between the ASC and mounting device.

2.1 ASC–Lunar (ASC–L)

The most recent ASC designed by Sunpower, Inc., is the ASC–E2. The ASC–E2 is a second generation of the engineering-level advanced Stirling convertor development. As a technology effort, the current ASC–E2 design was evaluated to extend the current capabilities by investigating the adaptation of the technology to environments demanding higher rejection temperatures and higher alternator temperatures. Sunpower, Inc. built an ASC–L, shown in Figure 1, to demonstrate these capabilities. The ASC–L design is based on an ASC–E2 with limited changes and is intended for single-convertor configuration. The performance characteristics and temperature limits of the alternator were evaluated.

The ASC–L differs from an ASC–E2 in four ways. First, higher temperature magnets were installed for an expanded cold-side adapter flange (CSAF) temperature range of 47 to 147 °C and a pressure vessel (PV) temperature range of 55 to 155 °C. In contrast, the ASC–E2s operated at a CSAF temperature range of 17 to 125 °C and a PV temperature range of 21 to 132 °C. The rejection temperature range is based on simulations of expected lunar day/night temperatures. PV temperatures were assumed to be approximately 8 °C higher than the rejection temperature based on analysis performed by Sunpower, Inc. The ASC–L will operate at high-rejection temperatures for performance mapping only. Nominal operation is 850 °C hot-end and 90 °C rejection temperatures. A tradeoff of the higher temperature magnets is a 1.7 percent decrease in alternator efficiency. Second, the epoxy used to bond the magnets is rated at a higher temperature than that on the ASC–E2. Third, the ASC-L includes a passive balancer and

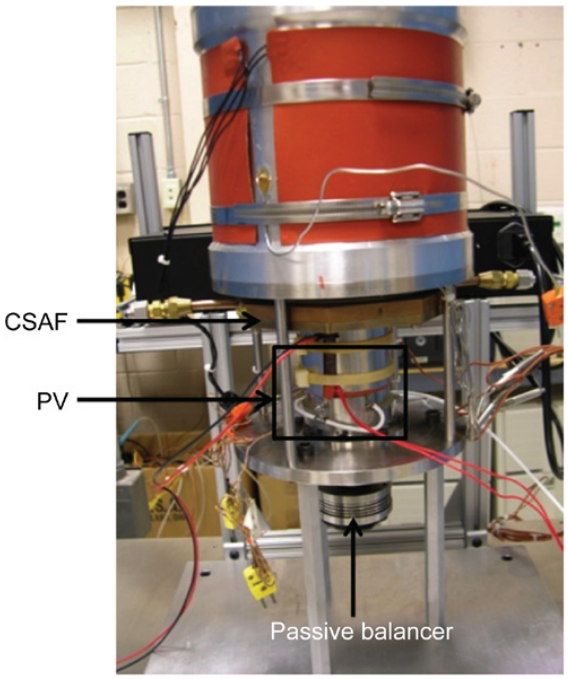

Figure 1.—ASC–L with passive balancer.

does not require an interconnect tube or external mass for operation. Passive balancers are simple, under-damped, spring mass oscillators, harmonically tuned for sympathetic resonance. Fourth, the ASC–L is considered a developmental convertor since the same quality system used on the ASCE2s was not implemented due to time and budget constraints.

Limited design changes were made to the convertor to accommodate higher rejection temperature operation. The organics and materials for the internal limit sensor and piston were not changed for higher temperature operation but were deemed acceptable for short-term operation for 100 hr or less at a PV temperature of 155 °C. The ASC–L will undergo various tests at NASA GRC as described in Section 8.0.

2.2 Lunar Lander Test Stand

To characterize the dynamic effect of a single, operating ASC on a landing platform, a test stand was designed to simulate the dynamics of a potential lander and measure the force at the interface between the ASC and the lander and at the interface between the lander and the planetary surface. Figure 2 depicts a conceptual design for an ILN lander.

The test stand was designed to replicate the dynamic behavior of the conceptual lunar lander while avoiding the fundamental frequency of the ASC, 102.2 Hz, as well as the first two harmonics, with significant frequency separation, mimic the total mass of the lander of 150 kg, and provide isolation up to 20 Hz for the potential seismometer instrumentation. Providing adjustable stiffness and damping at both the interface between the ASC housing and the simulated lander and between the simulated lander and the planetary surface was also desirable to have the capability to simulate various landers.

Figure 3 shows the final design for the lunar lander simulator test stand. It has a total estimated mass of 175 kg, a first mode at 30.36 Hz, a second mode at 320.2 Hz, and allows for adjustment of the stiffness and damping at both the interface between the ASC housing and lander simulator and between the lander simulator and ground. The test stand includes load cells at both of these interfaces for force measurement. While the ASC flexure utilizes a stainless steel plate in bending, the load fingers use a sorbothane pad to provide both stiffness and damping.

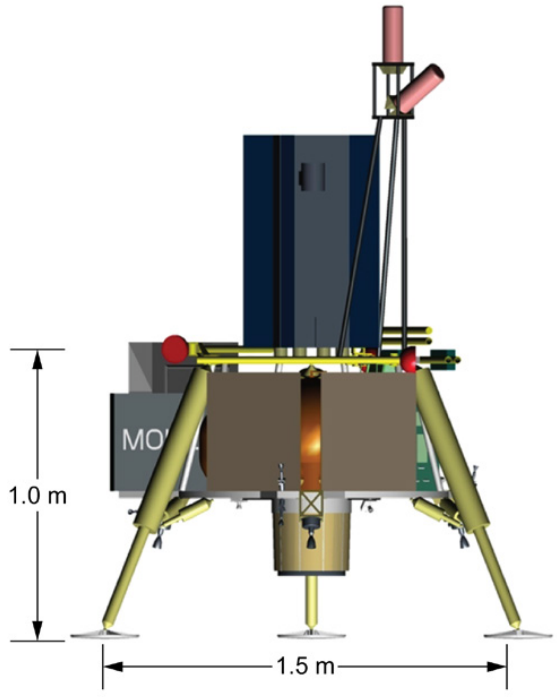

Figure 2.—Conceptual design for ILN lander.

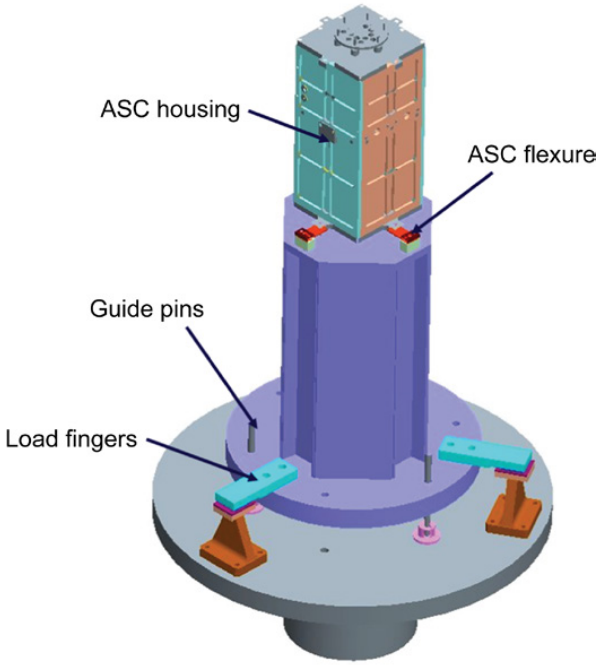

Figure 3.—Final design for lunar lander simulator test stand.

3.0 Single Convertor Controller Requirements

The SCC was designed to interface with the currently available sensors on the ASC. Thus, the SCC used measurements of the convertor's alternator electrical output; no internal piston or displacer position sensors were used. Since the ASC is designed to operate at a fixed frequency, the controller must maintain operation at that frequency. In addition, the controller was required to control convertor operation during startup (when physically connecting the thermal source to the convertor at fueling) and shutdown (at the completion of initial functional testing prior to fueling) as well as under normal operating conditions. The convertor operates continuously after integration with the heat source. Hence, the controller must support continuous operation both prior to and during integration of the SRPS with the spacecraft. The controller must operate for a 6-yr mission and for an additional 3 yr after fueling prior to the start of the mission. The fault detection and correction mechanisms in the controller protect the convertor and spacecraft from damage while recovering from a fault.

Spacecraft power needs may briefly exceed the capacity of the SRPS power source. There are many causes of such events; examples include activating thruster valves, sudden momentum wheel speed changes, telemetry downlink transmission, in-rush current surges when activating loads, and bursts of science data collection are among many such possibilities. If auxiliary power is not supplied from another source, the power bus voltage may be pulled too low and trigger a spacecraft fault. A battery frequently acts as the auxiliary power source to ensure that an adequate bus voltage is maintained during these power transients. Alternatively, a large capacitor may provide backup power if the expected power transients are short and the energy storage capacity of the capacitor is adequate. For example, the New Horizons satellite (on a flyby mission past Pluto) used a 33.6 mF capacitor bank to supply excess power during load switching events (Ref. 1). Thus, the SCC was required to support either a battery or capacitive power bus spacecraft architecture.

Missions that use the SRPS are likely to share some common characteristics, including lifetime and radiation tolerance requirements. Consumable power sources, such as a primary battery or fuel cell, are limited to short-duration missions. Solar arrays are suitable for long durations, but are limited to missions that see suitable levels of illumination and that can use a suitable backup power source, typically a rechargeable battery, during eclipse periods. Inadequate illumination in deep space or long-duration eclipses (about 2 wk) on the lunar surface makes solar array/battery power sources impractical for those missions. The SCC adapted a 9-yr lifetime (3-yr prelaunch and 6-yr mission) requirement based on the ILN notational lunar surface seismometer application. Given the fault tolerant SCC design described in this paper and the use of flight-qualified components, the SCC likely far exceeds that lifetime requirement although that analysis has not been done. Deep space missions to a planet like Jupiter with a trapped radiation belt can expose electronics to high radiation total ionizing dose (TID) even when heavily shielded. All electronic parts used in the SCC design can be obtained in versions that tolerate greater than 100 krad TID.

As with any spacecraft subsystem, the SCC was also required to minimize mass and volume while maximizing power delivered to the load. In addition, temperature and vibration requirements representative of typical spacecraft environments were defined for the mechanical design of the SCC.

4.0 SCC Architecture

A block diagram of the SCC connected to a convertor and a typical redundant spacecraft is shown in Figure 4. The SCC consists of two identical controller boards packaged in separate chassis. One unit is actively in control of the convertor at all times, while the other is not powered unless needed to recover from a fault.

Each controller board contains the power handling, data acquisition, signal processing, and secondary voltage conditioning circuits needed to control a convertor and deliver DC power to the spacecraft. A block diagram of the controller board is shown in Figure 5.

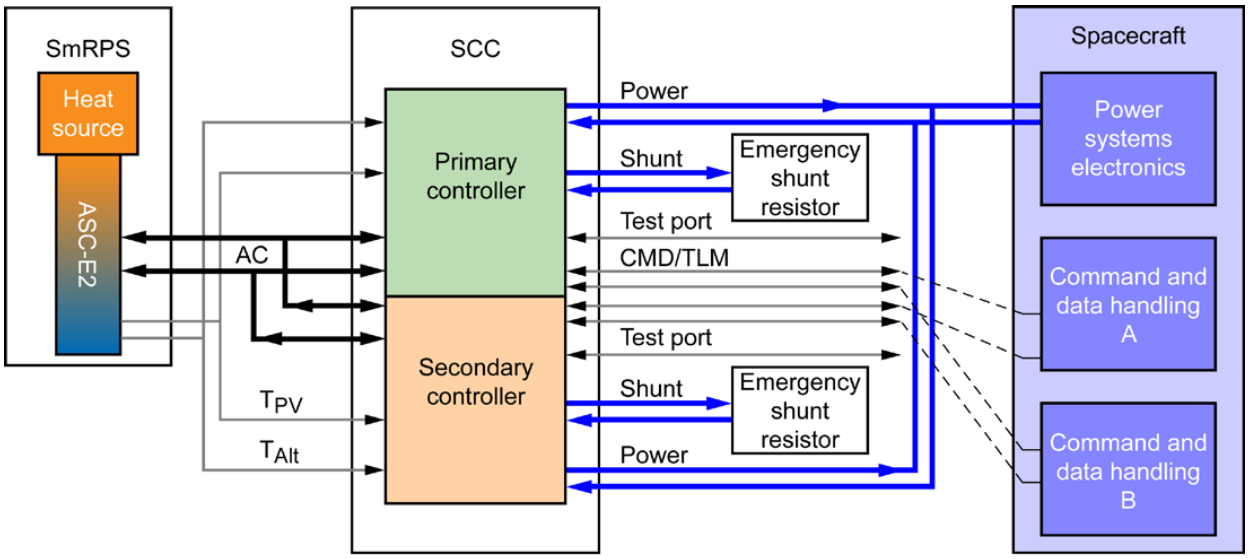

Figure 4.—Block diagram of a typical SCC redundant spacecraft application.

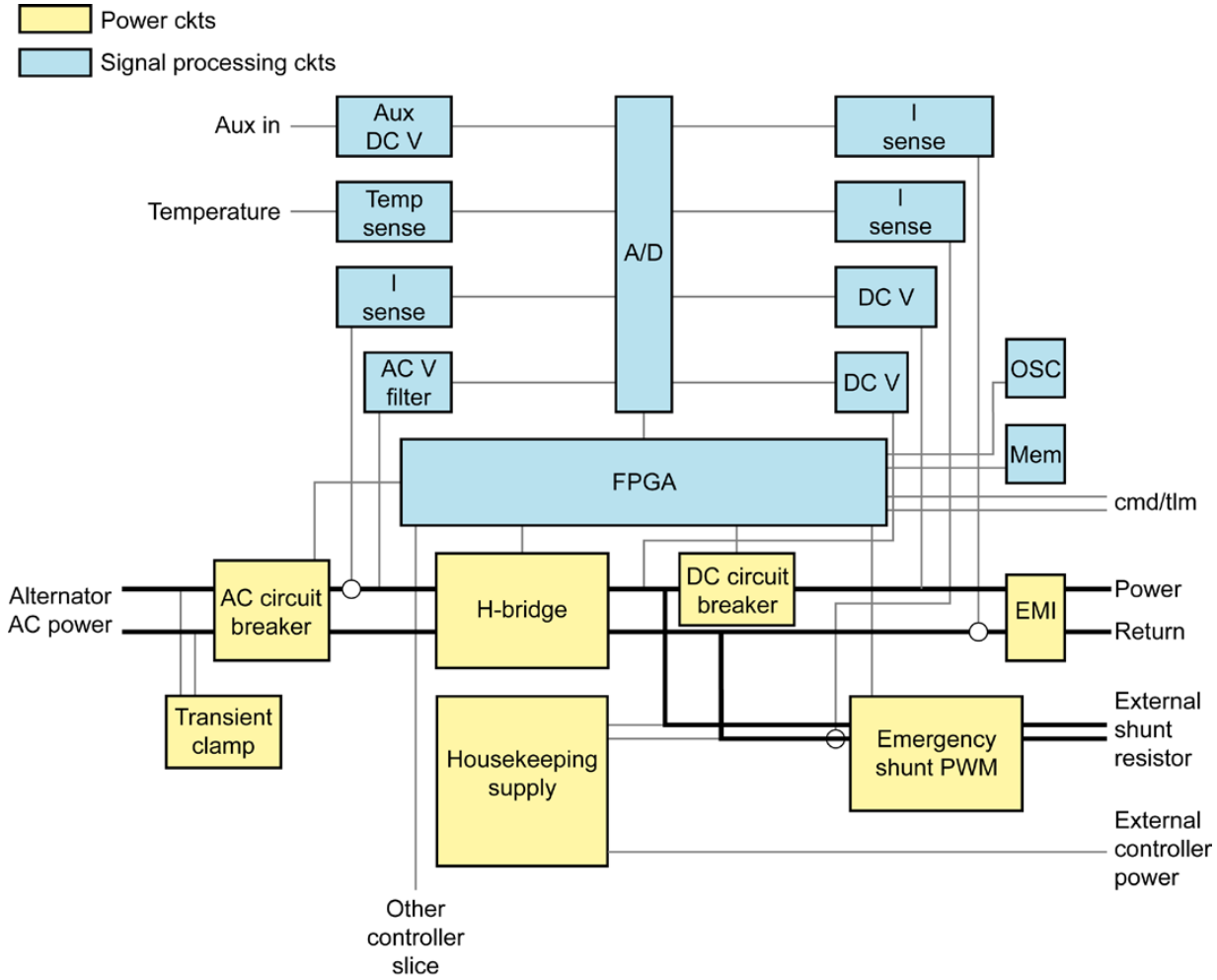

Figure 5.—Controller board block diagram.

Power flows from the convertor through an electronic switch that acts as an AC circuit breaker. The AC circuit breaker is opened in the event of a fault to isolate the convertor from the failure and allow the redundant board to initiate control. Transient suppression devices on each controller board clamp voltage spikes that may occur when the AC breaker is opened. A field effect transistor (FET) H-bridge is pulse width modulated (PWM) as determined by the control law implemented in the field programmable gate array (FPGA). An electronic DC circuit breaker utilizing two FET switches will isolate the controller board from a spacecraft fault and isolate the spacecraft from an internal controller fault. The DC breaker also has the capability to reconnect to the spacecraft while limiting in-rush current. While the DC breaker is open, convertor power flows to an external shunt resistor controlled using PWM to maintain a fixed H-bridge output voltage. An electromagnetic interference (EMI) filter on the board limits switching noise propagating from the controller to the spacecraft load.

The control law inputs and key status analog voltages are digitized by a 12-bit analog to digital converter (A/D) and processed by logic in the FPGA. The control law calculations and command and telemetry interface are implemented in the FPGA. A co-processor, consisting of an Institute of Electrical and Electronics Engineers (IEEE) single precision compliant data path controlled by a finite state machine sequencer, implements the control law algorithm. A 16-bit microcontroller implemented in the FPGA adjusts control law parameters, accepts user commands, and produces status telemetry. A combination of analog circuits, FPGA logic, and microcontroller software monitor SCC operation and detect and correct potential faults. A custom-designed DC/DC converter accepts input power from the spacecraft bus or external source and provides secondary voltages to board circuitry.

5.0 Development Approach

A mathematical model of the heat source, convertor, control algorithm, and circuits was developed to evaluate performance of the SCC design. A dynamic engine/alternator simulator was designed to support testing of the SCC. Breadboards of key circuits (H-bridge, electronic circuit breakers, current sensors, DC/DC converters, and FPGA control logic) were developed and tested with the dynamic engine/alternator simulator and an ASC. Both test methods produced similar results thereby validating the functionality of the dynamic engine/alternator simulator. In addition, a form, fit, and function flight equivalent EM of the SCC was built and tested with the dynamic engine/alternator simulator and ASC. Both test methods produced similar results.

5.1 Mathematical Model and Control Algorithm

A mathematical model of the Stirling convertor is essential when designing a convertor controller. A complex model called the System Dynamic Model (SDM) was developed by NASA GRC (Refs. 2 and 3). This model contains submodels for Stirling-cycle thermodynamics, gas dynamics, piston and displacer dynamics, alternator electromagnetics, and external thermal effects. The solution time for the complex model would significantly impact control system simulation times. Therefore, an ASC linear model was developed at NASA GRC that is simpler and more appropriate for control system design(Refs. 4 and 5) This model describes the (a 4 by 4 set of first-order linear differential equations) motions of the piston and displacer. The equations include terms called pressure factors, which approximate the forces acting on the piston and displacer due to interactions with the working gas. In some circumstances, one or two additional states are added to account for interactions of the piston with the electrical load. Nonlinear equations that approximately describe the relationship between the pressure factors and amplitudes of oscillation of the piston and displacer, as well as hot and cold end temperatures, are also provided. The linear model was used in the analysis and design of the SCC.

The linear model describes piston and displacer dynamics of the Stirling convertor as a fourth-order system with alternator current as the input and back EMF voltage as the output. The input-to-output transfer function is a complex impedance with a negative real part that implies the convertor supplies power to the alternator circuit. The eigenvalues of the system consist of two complex conjugate pairs with

one pair in the right half of the s-plane and the other in the left, indicating that operation is inherently unstable. The SCC manipulates the alternator output to keep piston and displacer amplitudes within acceptable bounds. One load option is to absorb convertor output power through a coupling capacitor and an AC voltage source, as shown in Figure 6.

The AC voltage source shown in Figure 6 influences the convertor mechanical piston oscillation amplitude and drives all of the eigenvalues into the left half s-plane. The system, therefore, does not self-oscillate but instead responds as a normal tuned-circuit to the driving function stimulus provided by the AC voltage source, and the frequency of operation will be controlled by the frequency of the AC voltage source. A controller that directly implements this circuit is feasible and is frequently used in the GRC SRL. However, the volume and mass of the tuning capacitor, C_T, are impractical for satellite applications. In addition, this controller circuit does not convert the AC alternator power to DC as required by spacecraft loads.

Instead, a controller using a more complex circuit, shown in Figure 7, duplicates the mathematical behavior of the ideal circuit while simultaneously supplying DC power to the spacecraft. An active H-bridge circuit is used to (a) simulate the voltage/current relationships of a tuning capacitor and (b) provide AC to DC conversion. The spacecraft load is represented as resistor, R_L, in parallel with either a battery or

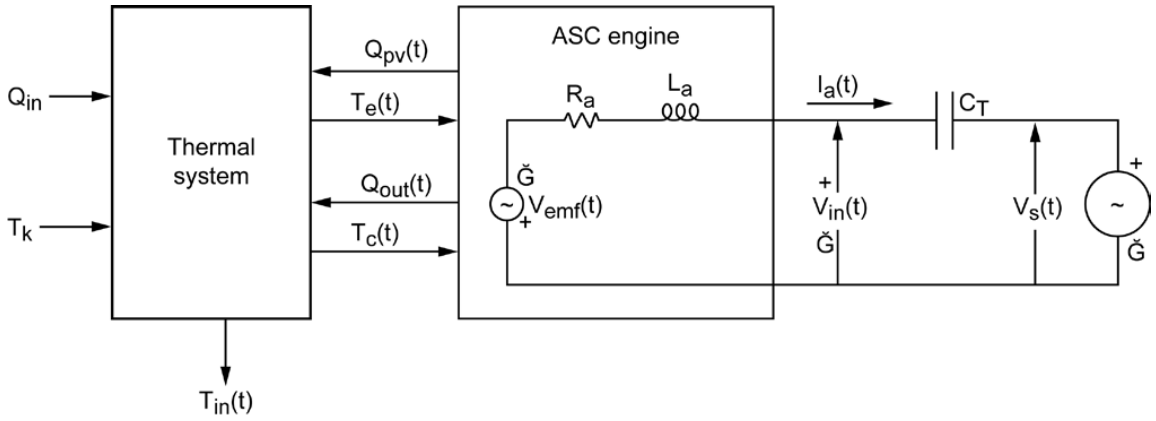

Figure 6.—Stirling convertor model including output alternator and load.

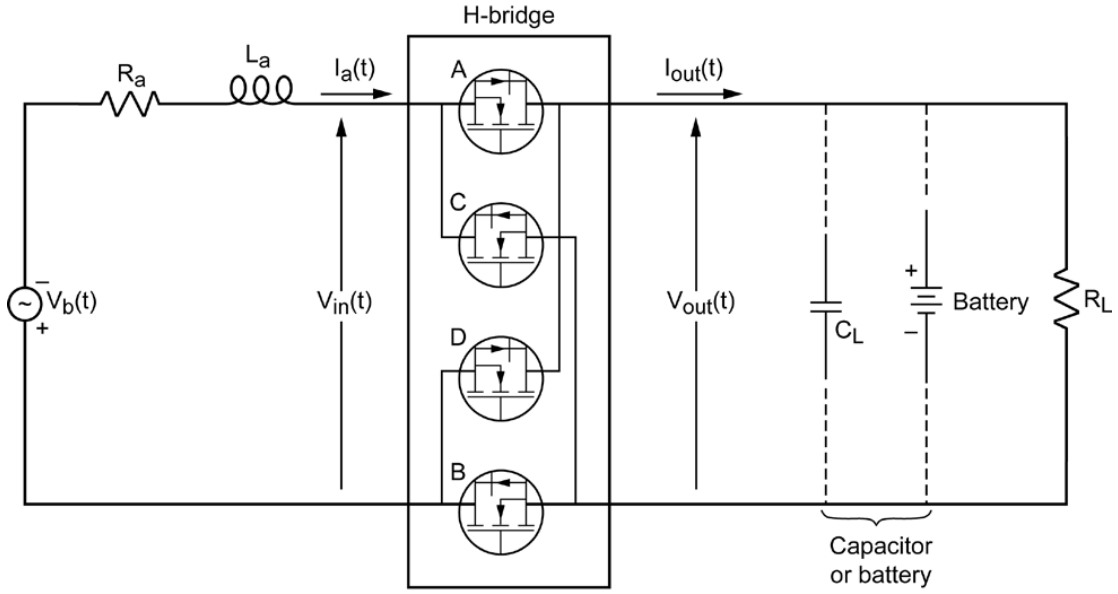

Figure 7.—Alternator circuit with an active H-bridge as the load.

capacitor, C_L. The H-bridge has four FETs that switch on and off in pairs. If FET switching is phased properly relative to alternator current, the average current delivered to R_L is positive when averaged over a full convertor operating cycle, as long as the load voltage, V_{out}, is maintained at a higher voltage than the peak value of the input voltage, $V_{in}(t)$.

Since one of the requirements was to operate at a fixed frequency, the H-bridge control algorithm was designed so that the AC load seen by the engine would appear to be an AC voltage source in series with a tuning capacitor. The $V_{in}(t)$ voltage for the active H-bridge controller of Figure 7 is the same as for the ideal controller of Figure 6 so that

$$V_{\text{in}}(t) = V_m \sin(\omega t + \theta) + V_c(0) + \frac{1}{C_T}\int_0^t I_a(u)du \,,$$

where V_m is the amplitude and θ is a possible phase bias of the AC voltage source, $V_c(0)$ is the initial voltage across the tuning capacitor, and the third term is the change in tuning capacitor voltage from t=0 to current time. A control algorithm that causes the H-bridge to mimic this behavior is specified as follows:

- Input $I_a^*(k)$ = measured alternator current and $V_{\text{out}}^*(k)$ = measured output voltage at time t_k (the beginning of the k^{th} switching cycle).
- Calculate $V_s(k) = V_m \sin(\omega t_k + \theta)$
- Take $V_c(k)$ from the $V_c(k+1)$ value calculated in the previous iteration or a specified initial value if this is the first iteration.
- Calculate $V_{\text{in}}(k|d) = V_s(k) + V_c(k)$.
- Calculate $\tau_k = \frac{1}{2}\left[1 + \frac{V_{\text{in}}(k|d)}{V_{\text{out}}^*(k)}\right]$.
- Calculate $V_c(k+1) = V_C(k) + (T/C_T)I_a^*(k)$
- Repeat indefinitely.

5.2 Dynamic Engine/Alternator Simulator

A dynamic engine/alternator simulator was developed using custom-designed circuits, commercial equipment, the linear model, and an off-the-shelf digital signal processor (DSP) development system as seen in Figure 8. Alternator inductance and resistance are modeled with physical components with electrical properties similar to the actual alternator in series with a back EMF voltage source. The voltage across the series resistor is proportional to the alternator current and is amplified by a custom-designed analog circuit and digitized by an A/D that is part of the DSP development system. The DSP is programmed to use the input current to calculate and produce an output voltage through a digital to analog converter (D/A), also part of the DSP, proportional to the ideal converter back EMF voltage. The back EMF voltage passes though an electrical isolator and then a high output commercial power amplifier. The power amplifier output is the equivalent of the back EMF output of the convertor. The dynamic engine/alternator simulator includes the linear model of the ASC and therefore, includes dynamics of the convertor mechanisms beyond the alternator electrical inductance and resistance. The dynamic engine/alternator simulator can be reprogrammed to mimic other types of ASCs by changing the linear model implemented in the DSP and the physical alternator inductance and resistance components.

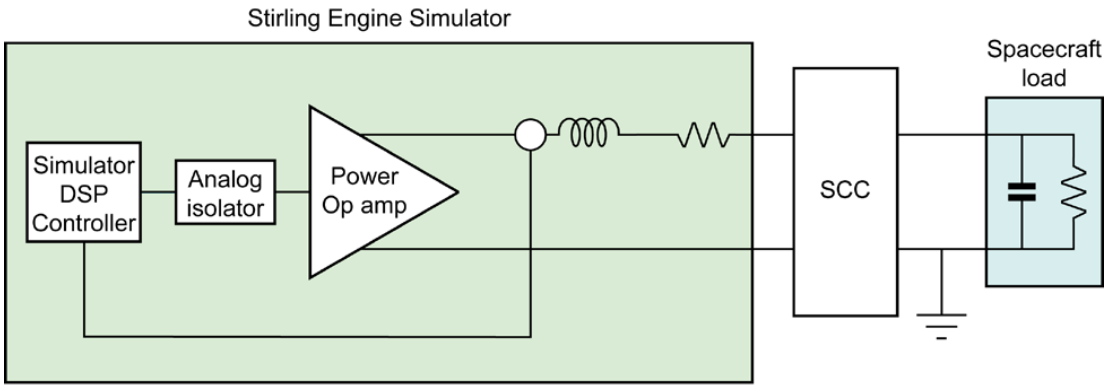

Figure 8.—Stirling dynamic engine simulator block diagram.

Previous engine simulator designs used an AC source, resistor, and inductor and only modeled electrical performance with no consideration of convertor mechanical behavior. Designers frequently found that their controllers did not function the same with an ASC as with their engine simulator. The impact of controller problems like AC input current sampling noise or spacecraft bus voltage changes on mechanical parameters like piston amplitude could only be investigated using time-consuming testing with a real ASC. In addition, damage to the ASC might occur during such evaluations.

The dynamic engine/alternator simulator was used to test the SCC breadboards and EM prior to operating with an actual ASC. The dynamic engine/alternator simulator helped solve numerous nonlinearity and noise-related problems in sensing the alternator current. Overcoming those issues reduced output power fluctuations at the load, resulting in smaller peak-to-peak variations in piston amplitude and improved operating efficiency. The effectiveness of the dynamic engine/alternator simulator was shown when the ASC was successfully controlled, at full power, on the first attempt by both the breadboard and EM controllers. If SCC testing was only performed with an ASC, the success of the controller design and its 2-yr time to full-power ASC demonstration would not have been possible. The same behavior observed while testing with the ASC was also seen while testing with the dynamic engine/alternator simulator including piston amplitude noise and controller efficiency sensitivity to load changes. The dynamic engine/alternator simulator also provides an easy-to-use environment for debugging and testing fault detection and recovery of the SCC without risk of damage to a real ASC.

6.0 Fault Detection and Recovery

The SCC not only provides power to the spacecraft but it also must regulate ASC operation to avoid damage to internal components and maintain safe thermal conditions after fueling. The controller was designed with full redundancy to avoid potential over-heating or damage to the internal structure.

During SCC development, a functional failure mode effects analysis (FMEA) listed possible functional failures in the circuits. The impact of such failures and mechanisms to detect and correct them were identified and implemented in the detailed design. Examples of the design impact of the FMEA include the addition of input and output electronic circuit breakers to isolate faults, transient suppression diodes to clamp alternator voltage during corrective actions that involve changing from one controller card to the other, and analog and digital signal processing circuits that monitor controller operation and help detect faults. The scope of potential issues were not limited to internal controller failures but extended outside to include impacts from the spacecraft and the engine. This tool will continue to be refined and assist in determining test scenarios, built-in test requirements, and evaluation of design enhancements.

Recovery from a fault is based on switching from the controller board that detected the fault to the backup board. A study was conducted to determine the time available to switch between controller boards without damage to the convertor. Simulations based on the linear model of the convertor combined with SCC electrical circuits were performed. Developing a safe response to a short or open fault across the

H-bridge resulting in an open or short applied to the convertor and potentially a short across the spacecraft battery was particularly challenging. Electronic circuit breakers were added to the design to isolate both the convertor input to the SCC and the connection to the spacecraft power bus. After detecting the H-bridge fault and isolating the failed controller, the model showed that the backup controller had less than 20 ms to reestablish proper operation of the convertor. The model also showed that the open/short must be removed in less than 5 ms to avoid internal damage to convertor components. The backup controller startup procedure applies the equivalent of a parallel resistive/capacitive load within 2 ms after startup and then switches to the standard control algorithm at the next current zero crossing. The impact on internal piston position of a controller board switchover in the SCC is shown in Figure 9.

Analysis was completed to determine methods for achieving hot swap functionality. Hot swap refers to changing a failed controller card while the active controller card maintains operation of a convertor operating at full power. Due to hot swap capability, each controller card requires its own set of harnessing. This functionality is being implemented in the SCC and will be tested in the near future.

7.0 Circuit Development

7.1 Breadboard Model

Breadboards of SCC circuits were developed to better characterize performance prior to design of the EM controller board. Circuits for AC and DC current sensing, circuit breakers, secondary voltage generation, and the H-bridge were built and separately evaluated. Current sensing was one of the most challenging tasks. Breadboards were developed to explore current sensing techniques including using transformer coupling for AC, transformer saturation for DC, Hall effect, and series resistor. A sense-resistor-based approach was selected due to saturation problems with the transformers and the lack of known rad-hard Hall effect sensors. Testing of the H-bridge breadboard revealed the importance of using a low equivalent series resistance capacitor between the H-bridge and DC breaker. The initial capacitor selection provided proper filtering at 100 Hz, but the much higher H-bridge switching frequency led to excessive power dissipation in the capacitor and reduced efficiency. The elevated temperature of the filter capacitor may also have compromised the operating lifetime.

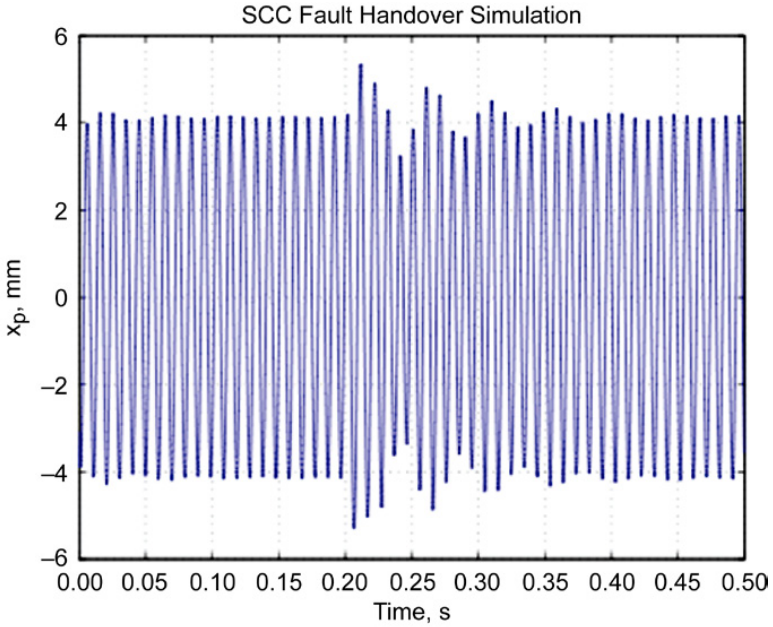

Figure 9.—Simulation of piston position during switchover. The fault triggering the switchover occurs at 0.2 s.

Preliminary versions of the SCC digital logic included an embedded microcontroller and floating point processor implemented on a commercial FPGA development board. The FPGA board was connected to the H-bridge breadboard and used to control FET switching. The H-bridge breadboard contained two D/A converters driven by the FPGA in addition to the switching FETs and drivers. Manipulation of the FPGA microcontroller software internal points in the control law calculation enabled through the D/As. That debugging tool detected several minor problems. For example, a direct digital synthesizer (DDS) was implemented as the reference frequency source in the FPGA. The initial version of the DDS loaded a microcontroller readable register with the current value of phase as a nine-bit two's-complement number (+511 and –512). The one-half-bit offset inherent to this encoding caused the control algorithm integrator output to slowly drift. So, the DDS encoding of its nine-bit two's-complement number was changed to a 10-bit number with the least significant bit always set. Hence, the range fed into the control algorithm was symmetric and zero centered (+1023 and –1023) and did not contribute to integrator output drift.

After independent debugging, the breadboards were interconnected on the lab bench and tested as a system. First, the SCC's breadboard system was used to control the dynamic engine/alternator simulator. That testing showed that the control algorithm and the circuits operated as expected. The breadboard SCC system was then used to control an ASC. The breadboard testing provided a performance baseline to evaluate the EM operation.

7.1.1 Engineering Model

An EM SCC was designed, built, and tested with both the dynamic engine/alternator simulator and the ASC. The EM schematic and physical design is compatible with radiation-hardened and flight-quality electrical components. Initially, EM operation was much less efficient than the breadboard system. Comparisons between the EM and breadboard performance led to several FET driver changes on the EM, PWM logic changes, and reduced FET switching noise. These changes improved the EM efficiency beyond the breadboard, and also reduced variations in the convertor piston amplitude. A custom-designed, flyback topology DC/DC converter generated all internal secondary voltages used by the SCC circuits. The converter reduced the size and mass of the SCC. At ASC startup, power to the SCC is supplied from an external source. When the ASC produces positive power and the H-bridge DC output voltage is high enough, the external supply can be removed. Ten secondary voltages are generated including seven independent floating sources for powering non-ground referenced circuits, such as the alternator current sense amplifier and some FET gate drivers. The DC/DC converter can supply up to 5 W but the remaining SCC circuits draw less than 2 W. Start-up time for the converter was less than 1 ms because of the fast fault switchover requirement. EM testing revealed that switching noise from the DC/DC converter injected noise into the alternator current sense circuit. Snubber networks added to the supply reduced that noise but some was still present. The supply was modified to use an independent clock during startup and then switch to a clock generated by the FPGA that was synchronized so that the DC/DC FETs never changed state while alternator current was being sampled. The FPGA is currently at 54 percent of its flight-targeted RTAX2000 capacity, so there is space to implement a considerable amount of logic to improve and extend SCC functionality.

Both alternator current and H-bridge output voltage A/D channels were also affected by PWM switching noise in the H-bridge. As with the DC/DC converter, snubber networks in the H-bridge FET drive circuits were helpful in reducing noise on these channels.

Common-mode response of the current sampling circuit was studied during testing of the EM. The H-bridge switches the alternator voltage and hence current sense resistor common-mode voltage between the spacecraft bus voltage and return. An operational amplifier configured as a difference amplifier (powered by a floating supply referenced to the alternator) was used to amplify the small voltage drop across the sense resistor. A relatively large transient response was observed on the amplifier output when the H-bridge switched, particularly at a high DC output voltage. Adjusting dynamics of the difference circuit reduced the transient. In addition, the performance was improved by synchronizing A/D sampling to H-bridge switching and to sample current when the H-bridge FET configuration held the sense resistor near

ground. The combination of these noise reductions—DC/DC and H-bridge drive snubbers, difference amplifier filtering, and sampling synchronization—resulted in less than a few counts of noise in the alternator current sense A/D channel. Amplitude variation of the alternator current and ASC power output level were reduced by these improvements.

The mechanical design of the EM satisfies flight requirements. The EM SCC was not built to meet vibration requirements, but analysis shows that the design would pass normal flight assembly practice. A fault-tolerant SCC consists of two identical boxes, each containing a copy of the same circuit. In typical operation, one box is actively controlling the convertor, while the other is available as a backup in the event of a fault. The mass of both boxes, without the interconnecting harness, is 2.27 kg (current best estimate (CBE)) using an Al–6061–T651 chassis and 2.00 kg (analysis) if Mg-ZK60A-T5 material is used. A mechanical model of the SCC and a picture of the EM circuit card in an assembly fixture are shown in Table 1 and Figure 10.

TABLE 1.—SCC MECHANICAL PROPERTIES

Property	Requirements	SCC Design (CBE)
Mass	Minimized	1.135 kg per box (CBE) using Al-6061-T651 chassis
Dimensions	Minimized	8.67 by 5.45 by 2.57 in. including mounting tabs Four no. 6, 32 mount feet
First fundamental modal frequency	>150 Hz	433 Hz in accordance with SCC structural analysis
Random vibration environments	Maximum 12.4 grms	Positive board deflection margins EEE parts vib fatigue life greater than 10^7 cycles per analysis Positive minimum dynamic clearance
Strength	Positive margins of safety per General Environmental Verification Requirements (GEVS), NASA–GSFC–STD–7000.	Positive of safety stress margins per analysis Random vibration load response greater than quasi-static limit load
Thermal environments	Base plate temp at 50 °C (max.) and 0 °C (min.)	Each box designed to dissipate 6.79 W (CBE) All EEE parts meet EEE–INST–002 derating requirements per SCC thermal analysis Temperature margins are positive
Venting environment	EELV-class (Atlas V or Delta IV)	Four (4) Ø0.050 in. vent holes under maximum pressure rate change of 1.0 psi/sec
EMC	Tongue and groove EMI gaskets	SCC uses D-sub connectors and backshells with EMI shields Tongues and grooves included in box design

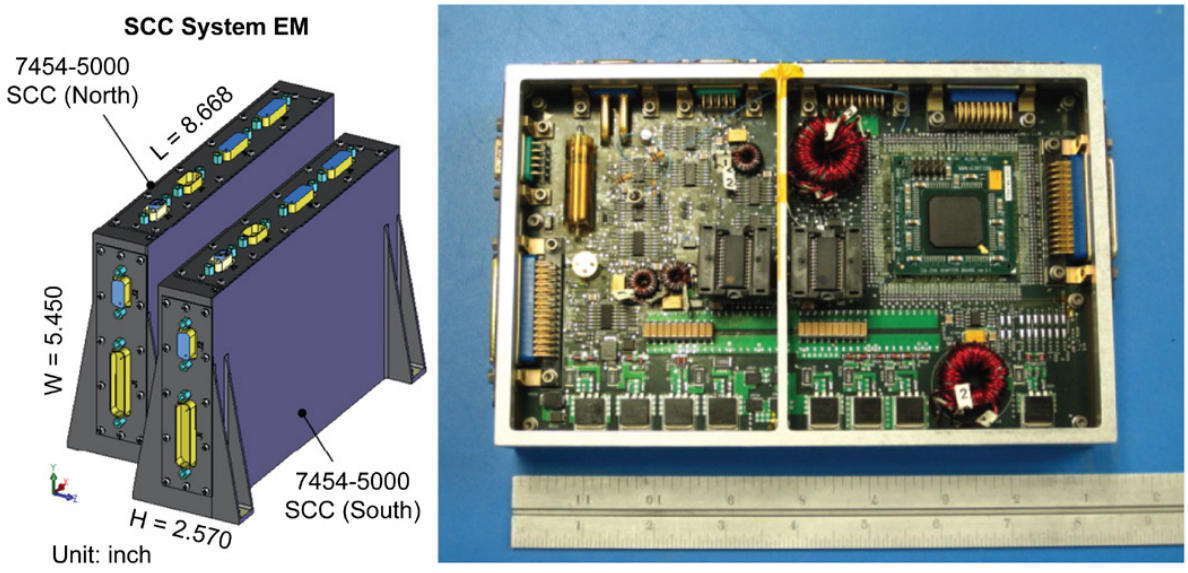

Figure 10.—Redundant SCC (left) and SCC EM circuit card in assembly fixture (right).

8.0 Integration Testing

The integration test has several goals: first, characterize the operation of the EM SCC with an ASC; second, characterize the effect of ASC operation on a lunar lander test stand; third, quantify the effect of a passive balancer on minimizing the vibration produced by an ASC; fourth, characterize the performance of the ASC–L during EMI and vibration testing, and fifth, characterize the SCC's ability to control the ASC–L during the vibration test.

A test rack (Ref. 6) was designed and built to support these tests. The data system utilizes National Instruments LabVIEW-based data acquisition hardware and software to acquire data and monitor the test. It displays and records data on a computer, collects and saves data in various timeframes, calculates parameters with received data, provides safety to the convertor, and can control the support systems without user intervention. The test rack provides two hot end temperature-control systems and two convertor-control systems: constant heater temperature and fixed-heat input for temperature control, and AC bus and EM SCC for convertor control. AC bus control dissipates power in resistors. SCC control relies on a DC electronic load to sink power. The test rack receives signals from accelerometer processors, load cells, thermistors, and thermocouples. A Yokogawa power meter measures alternator and heater voltage, current, and power. Several panels were designed to provide a means to interface the convertor, SCC, and instrumentation in the test rack.

8.1 ASC–L Testing

Before delivering the ASC–L convertor to GRC, Sunpower, Inc. completed the temperature performance map show in Table 2. The performance map test points and results produced at Sunpower, Inc., are replicated at GRC.

TABLE 2.—ASC–L TEMPERATURE PERFORMANCE MAP

Mission phase	Hot end temperature +0/–2 °C	CSAF temperature ±2 °C	PV temperature ±2 °C
BOM, *Min.*	842.7	56.9	59.5
BOM, *Max.*	843.9	86.9	97.7
EOM, *Max.*	844.4	86.4	96.0
Low Reject	839.0	46.3	54.3
High Reject	841.3	143.2	153.1

The ASC–L was delivered to GRC with the Sunpower, Inc., mechanical hardware design, which includes an insulation package, heater assembly, CSAF cooling jacket, and housing. This hardware was designed to allow for higher rejection temperature operation up to 147 °C. High rejection temperature operation will only be performed for the temperature performance map; nominal convertor rejection temperature operation is 90 °C. The ASC–L will first undergo this test while operated with the AC bus power supply since this is the type of controller used by Sunpower, Inc. Next, ASC–L will undergo a second performance map with the SCC. This test will characterize the SCC's ability to control the ASC–L over a range of temperatures. Upon completion of the temperature performance map, the Sunpower, Inc., mechanical hardware will be removed and ASC–L will be integrated with GRC-designed mechanical hardware for extended operation.

8.2 SCC Testing

Several tests were executed on the SCC prior to delivery to GRC on May 27, 2011. The breadboard version of the SCC operated with the dynamic engine/alternator simulator to confirm SCC functionality prior to integration with ASC–1 no. 4. This convertor was used at APL prior to delivery of ASC–L. The ASC–L operates at a frequency of 102.2 Hz and ASC–1 no. 4 at 103 Hz. The SCC can be modified to allow for various operating frequencies from 99.07 to 104.7 Hz. The breadboard SCC operated ASC–1

no. 4 at full power on its first attempt. Convertor power output fluctuations up to 10 W were observed. Modifications were made to the SCC as described in Section 7.0 to eliminate these fluctuations. These power fluctuations were expected since they were also observed during testing with the dynamic engine/alternator simulator.

The two EM boards were manufactured and tested with the dynamic engine/alternator simulator to confirm SCC functionality prior to integration with ASC–1 no. 4. Each EM board successfully operated ASC–1 no. 4 at full power on its first attempt. Three tests were performed with each of the EM boards. First, the DC bus voltage was varied, which confirmed the SCC's ability to maintain convertor power output stability over a range of DC bus voltages. Second, the SCC operated ASC–1 no. 4 at full power with power dissipation in the shunt. This simulates the fueled configuration. The third test verified ability of the SCC to maintain convertor control while going over and under the acceptable DC bus voltage range. The third test also demonstrated successful power transfer from the spacecraft to the shunt and recovery from the fault. The SCC attempts to reconnect to the spacecraft and connects when the spacecraft voltage reaches an acceptable range. Next, the two EM boards were each integrated in their individual chassis. Once completed, the first EM board was delivered to GRC, and was tested with ASC–1 no. 4 through the same test sequence as before. In addition to completing this test sequence, the SCC efficiency was measured while ASC–1 no. 4 operated at full power and providing power to the spacecraft load. The measured efficiency was approximately 92 percent. Efficiency is defined as power out of the SCC divided by power into the SCC.

The SCC will be tested at GRC with ASC–1 no. 3, which is the same design as ASC–1 no. 4, while ASC–1 no. 4 remains at APL for continued SCC development. The dynamic engine/alternator simulator will be used to verify SCC operation after delivery to GRC and confirm the GRC SCC harnessing, DC load, and shunt. Testing at APL used a different set of harnessing, DC load, and shunt. Next, the SCC will operate with ASC–1 no. 3 and undergo the same test sequence as done with ASC–1 no. 4 at APL. Upon completion of these tests, the SCC will operate at full power with ASC–L. Then, the SCC will operate with ASC–L for temperature performance mapping. The SCC and ASC–L with passive balancer will be integrated with the simulated lunar lander test stand to test system performance.

8.3 Integration Testing

APL delivered one of two EM boards to GRC. The second EM board will remain at APL for continued SCC development, including increased fault tolerance capability and a command and telemetry interface. After completion of this development and testing, and the delivery of the second EM board to GRC, the two EM boards will be integrated with ASC–L and undergo EMI and vibration testing. Next, the two EM boards, the ASC–L with passive balancer, and lunar lander test stand will be integrated and operated as a system for continuous unattended operation. This will quantify the SCC's ability to maintain performance of the ASC–L over an extended period of time.

The plans for the characterization of the lunar lander test stand include a tap test. During this test, several accelerometers mounted on the various components of the test stand, including the ASC–L housing, the lunar lander mass simulator, and the floor, will record the accelerations resulting from taps imparted to the structure at different locations. This test will verify that the frequencies and shapes of the system modes match those predicted in the design analysis. After integration with the ASC–L, the load cells mounted at the base of the test stand and between the simulated lander and the ASC–L housing will provide data on the vibration emitted by the convertor to the lander and lunar surface.

The ASC–L will go through a sequence of vibration testing, which include both qualification and flight acceptance testing up to levels of 12.3 grms. This level of testing is based on the standard RPS profile developed by the Jet Propulsion Laboratory. The ASC–L will operate at anticipated launch power and amplitude conditions during the vibration testing. The SCC will control the convertor during the vibration test but will not be exposed to vibration itself. This will confirm the SCC's ability to control the ASC–L during launch. The EMI test will characterize the magnetic (both AC and DC) and electric field emitted by the integrated system, the SCC and ASC–L.

9.0 Discussion

An approach throughout the SCC development was to understand how something should work before it was tested. Then, if the results did not meet expectations, the cause of the discrepancy was investigated and fixed or the model was refined to better match the data. This approach proved fruitful in developing the EM SCC. Initial testing of the EM showed a much higher power loss than expected and a several percent variation in convertor output power. As described in Section 7.0, noise from a variety of sources injected into the current sense channel strongly affected controller performance. Extensive debugging was required to eliminate the noise sources one at a time, with improved performance after each adjustment. Applying an external calibration signal independently to each channel of the A/D converter was another technique that was helpful. Initially, microcontroller sequenced sampling of the A/D channels showed surprisingly nonlinear behavior in response to a slow DC ramp input. Subsequent debugging showed that some unused A/D channel inputs were out of the part's input range and effected measurements on all channels. Conditioning circuits on some channels were also oscillating due to operational amplifier high-feedback resistance interacting with input capacitance. Finally, improved resistor matching, particularly on the differential current sense amplifiers, improved the common mode rejection of that circuit, and hence, current sensing linearity.

Another example of the importance of understanding the system was the extensive simulation work used to model system behavior in normal conditions, in response to various controller faults, and while correcting a fault. Developing these simulations was initially motivated by trying to understand the effectiveness of the control algorithm. Determining the requirement for how long the convertor could be left uncontrolled as the backup board was activated, required the addition of more details to the simulation to study actions during switchover. The switchover simulation then became a useful tool to design and evaluate the backup controller startup procedure. The results of these simulations influenced detailed circuit design, especially the DC/DC converter startup time and controller input transient protection. But, the simulation also proved useful in determining the H-bridge output- filtering circuit, in exploring and selecting the backup controller startup algorithm, and in determining a particularly effective fault detection mechanism. Most surprising to the controller designers was the realization that many possible faults can be detected in a fraction of a cycle of oscillation of the convertor piston by observing a large difference between observed and predicted alternator output voltage. An analog filter was added to remove the H-bridge PWM signal from the alternator voltage. An A/D channel digitized the filtered result and then the control law calculation engine in the FPGA computed the error signal. Logic in the FPGA digitally compared the error to a programmable threshold and if the threshold is exceeded, logic initiates the switchover to the backup controller.

A conscientious effort was made by the SCC designers to maximize efficiency throughout the controller development. The 92 percent efficiency of the SCC was achieved for several reasons; this work included but was not limited to careful debugging of the circuit, reduced noise in sampling AC current, two FETs in parallel on each switch to reduce effective on-resistance, compensation for diode shoot, and H-bridge switching technique. The use of a single precision floating point for control law calculations could also add to the efficiency of the SCC. The designers intend to investigate other methods to further improve the SCC efficiency, which will include studying the on-resistance of the FET to determine if this can be minimized further and measuring the resistance of the power traces on the printed circuit board. It was recognized throughout the SCC development that some changes made to improve efficiency of the SCC may have only resulted in saving milliwatt of power, but the philosophy that every milliwatt makes a difference was adopted.

10.0 Conclusion

The SRPS is compatible with lunar missions that require a single ASC and have a low vibration requirement due to instrumentation. The SRPS has the potential to be adapted for other planetary missions, as well. The project resulted in delivery of an ASC–L with passive balancer, simulated lunar

lander test stand and SCC. Initial testing of these items has been completed with plans to perform more extensive testing at the component and system level. The project produced a low mass and volume, high efficiency, and reliable SCC. As a result of the project, an invaluable controller development tool was designed that was not previously available to controller designers: the dynamic engine/alternator simulator. This tool not only aids in SCC controller testing but in future controller development efforts as well. It reduces the risk and time involved in operating an ASC during controller development. The project can be adapted for other missions that require even less vibration than that of an ASC with passive balancer through use of an active balancer. Initial analysis shows that an active balancer can potentially decrease vibration levels beyond that of a passive balancer.

References

1. Ottman, G. K., and Hersman, C. B. (2006). The Pluto-New Horizons RTG and Power System Early Mission Performance. *4th IECEC*, AIAA 2006–4029.
2. E. J. Lewandowski and T. F. Regan: "Overview of the GRC Stirling Converter System Dynamic Model, AIAA paper 2004, *2nd International Energy Conversion Engineering Conference*, Providence, Rhode Island, 16-19 August 2004.
3. T. F. Regan and E. J. Lewandowski: "Development of a Stirling System Dynamic Model with Enhanced Thermodynamics," CP746, Space Technology and Applications International Forum—STAIF 2005, edited by M. S. El-Genk, 2005 American Institute of Physics 0-7354-0230-2/05/$22.50.
4. T. F. Regan and E. J. Lewandowski: "Development of a Linear Stirling System Model with Varying Heat Inputs," AIAA paper.
5. T. F Regan, E. J. Lewandowski, and J. G. Schreiber: "Stirling System Modeling for Linear Dynamics Analysis," AIAA paper
6. G.M. Dugala: "Test Rack Development for Extended Operation of Advanced Stirling Convertors at NASA Glenn Research Center," AIAA paper 2009, *7th International Energy Conversion Engineering Conference*, Denver, Colorado, 2-5 August 2009.

REPORT DOCUMENTATION PAGE	Form Approved OMB No. 0704-0188

1. REPORT DATE *(DD-MM-YYYY)*	2. REPORT TYPE	3. DATES COVERED *(From - To)*
01-01-2012	Technical Memorandum	

4. TITLE AND SUBTITLE
Small Radioisotope Power System at NASA Glenn Research Center

5a. CONTRACT NUMBER

5b. GRANT NUMBER

5c. PROGRAM ELEMENT NUMBER

6. AUTHOR(S)
Dugala, Gina, M.; Fraeman, Martin; Frankford, David, P.; Duven, Dennis; Shamkovich, Andrei; Ambrose, Hollis; Meer, David, W.

5d. PROJECT NUMBER

5e. TASK NUMBER

5f. WORK UNIT NUMBER
WBS 138494.03.03.02

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
National Aeronautics and Space Administration
John H. Glenn Research Center at Lewis Field
Cleveland, Ohio 44135-3191

8. PERFORMING ORGANIZATION REPORT NUMBER
E-17825

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
National Aeronautics and Space Administration
Washington, DC 20546-0001

10. SPONSORING/MONITOR'S ACRONYM(S)
NASA

11. SPONSORING/MONITORING REPORT NUMBER
NASA/TM-2012-217290

12. DISTRIBUTION/AVAILABILITY STATEMENT
Unclassified-Unlimited
Subject Category: 20
Available electronically at http://www.sti.nasa.gov
This publication is available from the NASA Center for AeroSpace Information, 443-757-5802

13. SUPPLEMENTARY NOTES

14. ABSTRACT
In April 2009, NASA Glenn Research Center (GRC) formed an integrated product team (IPT) to develop a Small Radioisotope Power System (SRPS) utilizing a single Advanced Stirling Convertor (ASC) with passive balancer for possible use by the International Lunar Network (ILN) program. The ILN program is studying the feasibility of implementing a multiple node seismometer network to investigate the internal lunar structure. A single ASC produces approximately 80 W_e and could potentially supply sufficient power for that application. The IPT consists of Sunpower, Inc., to provide the single ASC with balancer, The Johns Hopkins University Applied Physics Laboratory (JHU/APL) to design an engineering model Single Convertor Controller (SCC) for an ASC with balancer, and NASA GRC to provide technical support to these tasks and to develop a simulated lunar lander test stand. A controller maintains stable operation of an ASC. It regulates the alternating current produced by the linear alternator of the convertor, provides a specified output voltage, and maintains operation at a steady piston amplitude and hot end temperature. JHU/APL also designed an ASC dynamic engine/alternator simulator to aid in the testing and troubleshooting of the SCC. This paper describes the requirements, design, and development of the SCC, including some of the key challenges and the solutions chosen to overcome those issues. In addition, it describes the plans to analyze the effectiveness of a passive balancer to minimize vibration from the ASC, characterize the effect of ASC vibration on a lunar lander, characterize the performance of the SCC, and integrate the single ASC, SCC, and lunar lander test stand to characterize performance of the overall system.

15. SUBJECT TERMS
Controller; Stirling; Lunar; Stirling convertor simulator; Stirling convertor modeling; Lunar test stand

16. SECURITY CLASSIFICATION OF:			17. LIMITATION OF ABSTRACT	18. NUMBER OF PAGES	19a. NAME OF RESPONSIBLE PERSON
a. REPORT	b. ABSTRACT	c. THIS PAGE			STI Help Desk (email:help@sti.nasa.gov)
U	U	U	UU	26	19b. TELEPHONE NUMBER *(include area code)* 443-757-5802