ducing leakage power). When the feature size of the transistor is reduced, supply voltage (V_{dd}) and threshold voltage (V_{th}) are also reduced accordingly; then, the leakage current becomes a bigger factor of the total power consumption. To maintain low power consumption, operation of electronics at sub-threshold levels can be a potentially strong contender; however, there are two obstacles to be faced: more leakage current per transistor will cause more leakage power consumption, and slow response time when the transistor is operated in weak inversion region.

To enable low power consumption and yet obtain high performance, the CMOS (complementary metal oxide semiconductor) transistor as a basic element is viewed and controlled as a four-terminal device: source, drain, gate, and body, as differentiated from the traditional approach with three terminals: i.e., source and body, drain, and gate.

This technique features multiple voltage sources to supply the dynamic control, and uses dynamic control to enable low-threshold voltage when the channel (N or P) is active, for speed response enhancement and high threshold voltage, and when the transistor channel (N or P) is inactive, to reduce the leakage current for low-leakage power consumption.

This work was done by Tuan A. Duong of Caltech for NASA's Jet Propulsion Laboratory. Further information is contained in a TSP (see page 1).

In accordance with Public Law 96-517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

Innovative Technology Assets Management
JPL
Mail Stop 202-233
4800 Oak Grove Drive
Pasadena, CA 91109-8099
E-mail: iaoffice@jpl.nasa.gov

Refer to NPO-47337, volume and number of this NASA Tech Briefs *issue, and the page number.*

Hardware for Accelerating N-Modular Redundant Systems for High-Reliability Computing

Goddard Space Flight Center, Greenbelt, Maryland

A hardware unit has been designed that reduces the cost, in terms of performance and power consumption, for implementing N-modular redundancy (NMR) in a multiprocessor device. The innovation monitors transactions to memory, and calculates a form of sumcheck on-the-fly, thereby relieving the processors of calculating the sumcheck in software.

This sumcheck could be calculated using addition operations, or CRC-type (cyclic redundancy check) operations — whichever is most economical in terms of die area and power consumption. In each of the NMR systems, the sumcheck logic is initialized at the start of a task (a well-defined unit of work that will be performed by each of the NMR systems), then captured and transmitted to the vote-taker at the end of the task. The vote-taker compares the sumchecks, determines if errors have occurred, and what action, if any, should be taken to correct the errors.

The advantage over existing techniques is that minimal logic is required to implement the sumcheck unit, minimal power is consumed by the sumcheck unit when active, and the unit can have a reduced power sleep mode when inactive. Calculating a sumcheck for a task using the sumcheck unit requires no additional cycles, and so has lower latency than calculating it as a post-task in the processing unit.

This work was done by Keith Bindloss and Carl Dobbs, Sr. of Coherent Logix for Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-16324-1