A RADIATION HARDENED BY DESIGN CMOS ASIC FOR THERMOPILE READOUTS. G. Quilligan[1] S. Aslam[2], and J. DuMonthier[1], [1]Instrument Electronics Development Branch, NASA Goddard Space Flight Center, Greenbelt, MD 20771, [2]Solar System Exploration Division, NASA Goddard Space Flight Center, Greenbelt, MD 20771.

Introduction: A radiation hardened by design (RHBD) mixed-signal application specific integrated circuit (ASIC) has been designed for a thermopile readout for operation in the harsh Jovian orbital environment. The multi-channel digitizer (MCD) ASIC (shown in Figure 1) includes 18 low noise amplifier channels which have tunable gain/filtering coefficients, a 16-bit sigma-delta analog-digital converter (SDADC) and an on-chip controller. The 18 channels, SDADC and controller were designed to operate with immunity to single event latchup (SEL) and to at least 10 Mrad total ionizing dose (TID). The ASIC also contains a radiation tolerant 16-bit 20 MHz Nyquist ADC for general purpose instrumentation digitizer needs. The ASIC is currently undergoing fabrication in a commercial 180 nm CMOS process. Although this ASIC was designed specifically for the harsh radiation environment of the NASA led JEO mission it is suitable for integration into instrumentation payloads on the ESA JUICE mission where the radiation hardness requirements are slightly less stringent.

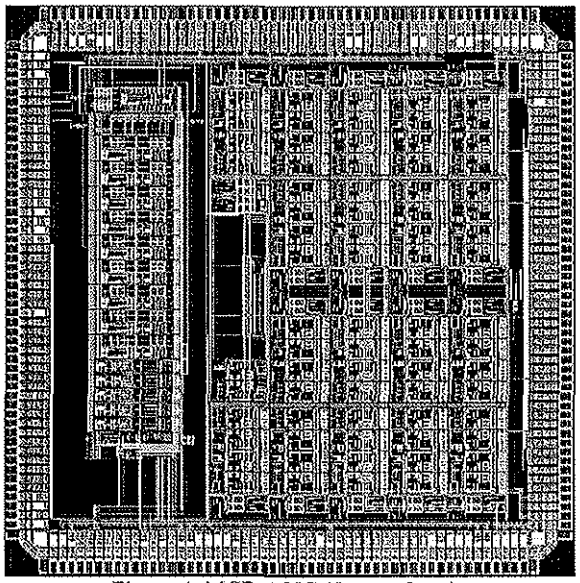

Figure 1. MCD ASIC (5mm x 5mm)

Radiometry Application: Mapping the surface temperature anomalies and thermal inertia of a cold moon like Europa or Ganymede, from a space borne platform, requires the accurate measurement of the infrared spectral radiance [1]. One sensitive measurement technique employs a filter radiometer operating in the nadir pointing, push-broom mode that uses several thermopile linear arrays, with each array integrated with infra-red filters that have appropriate wavelength pass bands [2]. The tiny thermopile pixel voltage outputs must be amplified, filtered and digitized with minimum noise. Commercial 64-pixel linear arrays are available [e.g. thermopile array TPL640, www.micro-hybrid.de] while custom made 2D-arrays with as many as 640 pixels can be fabricated. Each pixel must be processed by a dedicated amplifier channel while one ADC can be used to sequentially digitize the multiplexed channel outputs. The high channel count dictates the use of an ASIC (see Figure 2) to minimize the mass-volume-power (MVP) product. The ASIC needs to operate under extremely high levels of radiation as well as at relatively low temperatures in the 170 K range: the expected temperature range of the instrument housing in thermal equilibrium with its space environment.

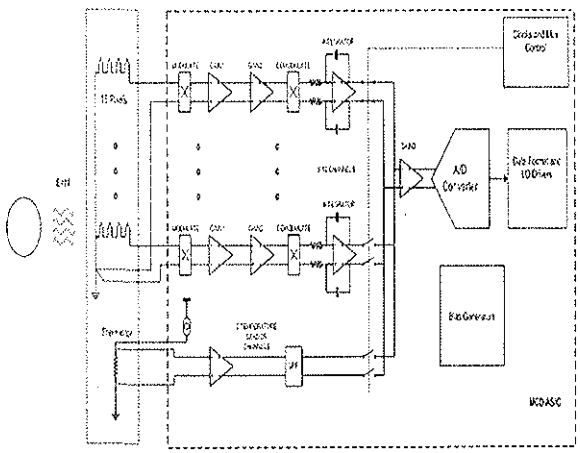

Figure 2. MCD block schematic

Thermopile Arrays: Thermopiles based on Bi-Sb thermoelectric materials [3] are thermal detectors of choice for long duration planetary missions because they (i) generate an output voltage that is proportional to the incoming radiation within the spectral range being mapped; (ii) do not require an electrical bias or an optical chopper; (iii) have negligible 1/f noise, (iv) do not require active cooling and (v) show radiation hardness to 10 Mrad (Si) TID [4]. Furthermore, Bi-Sb thermoelectric materials show better efficiency in the range 150 K to 200 K. The thermal instrument (TI) observation cycle consists of 110 ms signal integration

intervals, interspersed with instrument views of an internal blackbody. This corresponds to a 10 Hz frequency range. Thus low 1/f noise in both the detectors and the readout circuitry is essential. Thermopile detectors intrinsically have low 1/f noise when read out with high-input-impedance voltage amplifiers. Thermopile pixel elements, of size 240 x 480 μm^2, have a typical electrical resistance of 14 kΩ at 300 K and are therefore dominated by Johnson noise, i.e. $\approx$ 15 nV/$\sqrt{Hz}$. The TI thermopiles demonstrate a specific detectivity, D*, value of $\approx 8 \times 10^8$ cm$\sqrt{Hz}$/W at 10 Hz. The MCD ASIC has an input-referred noise of < 50 nV/$\sqrt{Hz}$ and is the dominant focal plane noise source.

The MCD ASIC: The thermopile pixels are read out in parallel with the custom MCD ASIC comprising signal conditioning, multiplexing and 16-bit digitization functions. The roughly dc signal from each pixel is modulated by an electronic chopping circuit. The resulting AC signal is amplified, demodulated, integrated and digitized. Because amplification occurs at a high frequency rather than near dc, the 1/f noise in the CMOS amplifier is dramatically reduced. Integrated signals of each of the thermopile channel outputs are multiplexed into a single analog output stream. Mounted on the same substrate as the thermopile arrays are thermistors that monitor any temperature drift of the arrays on the focal plane assembly. The pixel and thermistor outputs connect directly to the MCD ASIC. The MCD has 16 thermopile pixel readout channels and two temperature sensor channels. Four such ASICs interface to the array and are in close proximity so as to minimize noise pick-up and parasitic thermocouple effects. One consequence of this placement is each MCD must operate in a cryogenic environment where the ambient temperature is as low as 170 K, far below the temperatures at which commercial grade chips operate, i.e. 248 K. Cryogenic ambients also impact on the radiation hardness of the MOS devices: TID induced positive charge captured in the gate oxide increases with falling temperature that does not anneal with time or bias [5].

Radiation Mitigation Strategy: In addition to meeting demanding electrical specifications, the design of the TI concept places a heavy emphasis on minimizing the MVP while maximizing longevity in Jupiter's harsh environment awash with high energy particles. Minimizing the MVP is vital to the pragmatic needs of constraining launch cost, which limits the fuel needed for the trip to Jupiter and ultimately the size of the MMRTG. In addition to ensuring that a circuit will work reliably over the mission lifetime in an extreme environment, RHBD figures very prominently in the MVP product: if a circuit can be radiation hardened, there is less of a shielding requirement which reduces the mass of the instrument significantly.

If an ASIC is not designed to be sufficiently radiation hard or adequately shielded [6] it would be vulnerable to failure when exposed to the high radiation environment within the Jovian magnetosphere. For operation in a 3Mrad TID environment, a circuit that is radiation hard to only 300 krad (Si) would need to be spot shielded with an enclosure that has 25.4 mm (1000 mils) thick aluminum walls. In order to reduce the spot shielding mass significantly, a radiation hard ASIC tolerant to at least 3 Mrad (Si) TID is required. For the same enclosure volume, the resulting aluminum shielding thickness would be significantly reduced giving nearly a 10-fold reduction in shielding mass.

Choice of Technology: The choice of technology for manufacturing the MCD ASIC was determined by the following requirements: a) inherent radiation hardness or amenable to RHBD; b) speed, bandwidth, and die area; and c) cost. Because there has been a lot of success with RHBD techniques using bulk non-hardened CMOS processes, a domestic commercial foundry was decided upon.

Commercial foundry process nodes have the following advantages: (i) stable, non-iterating processes with a heritage of proven designs; (ii) a comprehensive and robust Process Design Kit (PDK); (iii) regular tape-in schedules that are known well in advance; (iv) good support from the foundry, i.e. libraries, application notes, etc.; (v) ITAR compliant, preferably domestic source; (vi) available radiation data indicating inherent radiation tolerance and (vii) low cost. Both IBM and TowerJazz semiconductor foundries offer 180 nm CMOS nodes that are good candidate processes for an ASIC such as the MCD. If RHBD techniques, such as enclosed layout transistors (ELT), are utilized in a process node which already has some TID tolerance (defined here as at least 100 krad (Si)) then a high TID/latch-up immune ASIC can be built. So the strategy to get to at least 3 Mrad (Si) TID was to have a design which (1) exceeds the specifications before irradiation, (2) is built in an unmodified process node with some inherent hardness to TID and (3) which has been hardened with RHBD and/or SOI. RHBD here includes ELTs, guard rings and circuit techniques.

Both IBM and Towerjazz also offer silicon on insulator (SOI) variants at the 180 nm nodes. The SOI variants naturally possess single-event latch-up immunity [7], but can suffer single-event snapback in the absence of well-designed body ties [8]. Silicon dioxide insulator layers enclosing the Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) channels increase the possible exposure to TID effects [9]. Fur-

thermore, for smaller feature sizes, a single heavy ion charge track may give rise to charge accumulation under the buried oxide and in the channels of multiple MOSFETs, resulting in upsets at multiple circuit nodes [10]. However, bulk CMOS processes are also prone to this type of multiple bit upsets in addition to being susceptible to single-event latch-up (SEL).

Ultimately we settled on TowerJazz Semiconductor's CA18HD process (non SOI) which provides thick/thin oxide devices, native NMOS devices (for low Vts) and high sheet poly resistors. We chose Towerjazz because of (i) the availability of extensive measurement data indicating non-hardened radiation tolerance to at least 100 krad TID in analog/digital circuits, (ii) low cost regular multi-product wafer (MPW) runs, (iii) excellent process design kits and (iv) good support from the foundry. Since the RHBD includes guard rings around all NMOS/PMOS devices the SOI feature wasn't needed, further reducing the cost.

MCD specifications

Parameter	Value
Supply voltage	1.80 V
Supply current	70 mA
Number of TP channels	16
Number of TS channels	2
Signal to noise ratio	> 256
TP input signal amplitude	0.1 – 120 μV
Gain (variable)	1 – 10k
Chopper frequency	40 - 125 kHz
Noise	<50 nV/√Hz
Ambient temperature	150 – 300 K
SDADC resolution	16 - 20 Bits
SD modulator clock rate	1 MHz
SD Nominal OSR	256
Pipeline ADC resolution	16
Pipeline ADC clock rate	1 – 20 MHz

MCD ASIC Design: As stated above, the main function of the MCD, illustrated in Figure 2, is to amplify, integrate and digitize the outputs of a thermopile array. A summary of the specifications of the ASIC is given in the table. The amplification task is particularly challenging with respect to offset and noise as the pixel voltages generated by the thermopile range from hundreds of nanovolts to only one or two hundred microvolts. A representative plot of the thermopile pixel output voltage versus Europa scene temperature is shown for two filter bands in Figure 3. The output voltage calculation is based on a thermal instrument that has a primary telescope mirror of 80mm diameter and is in polar orbit at 100 km height from the surface. These slowly changing voltages must be greatly amplified (by as much as several thousand) and integrated before digitization, which places stringent demands on the noise and offset performance of the analog front end (AFE). Each of the 16 pixel channels is comprised of a high input impedance, auto-zeroed chopper stabilized instrumentation amplifier and an integrator. The instrumentation amplifier and integrator are tunable with respect to gain and integration period. The outputs of the 16 pixel channels and two temperature sensor channels are multiplexed into one final amplifier that drives a 16-bit ADC with fully balanced differential signals.

The channel gains have a roughly exponential relationship to the user supplied gain code. A variable gain allows the user to optimize the SNR depending on the thermopile signal amplitudes. An integrator following each demodulator (prior to the multiplexer) performs an filtering function on the amplified signals, which removes most of the chopper tones and high frequency noise.

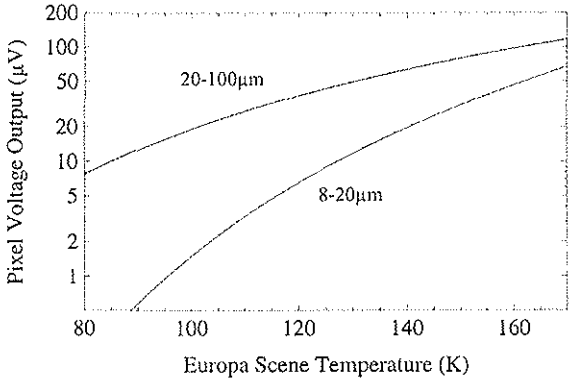

Figure 3. Typical thermopile output signal amplitudes for a thermal instrument with a 80mm diameter primary mirror observing Europa at 100km orbit.

In order to minimize the effects of 1/f noise and offsets, each channel modulates its input before amplification. The chopping is performed with "passive circuits" using switches to perform the modulation/demodulation. The chopping occurs at a rate between 40 kHz and 125 kHz. This relatively low rate of chopping minimizes the power dissipation per channel and is facilitated by auto-zeroing of the instrumentation amplifiers (which can be disabled). The demodulation is performed using a switched capacitor integrator which is also auto-zeroed. The user has the option of bypassing the integrator for some or all of the channels. The output of the integrator is held constant after the required number of integrate cycles. It may still have chop tones indirectly coupled through substrate parasitics and the supplies. Sub-sampling this (with the

appropriate multiplexer and ADC sampling) removes the chop tones.

Each channel (Figure 4) thus outputs an amplified and filtered signal, which is fed to a final buffer amplifier through a 18:1 multiplexer. Two of the channels are dedicated to the thermopile's local temperature sensor. The temperature sensor channels each supply a 5 μA bias current to the array thermistors. During a normal data collection run, the multiplexer is switching from channel to channel with a cycle time of 18 channel sampling intervals. The channel sampling interval is determined by the required frame rate, where a frame represents the digitized data for all 18 signals (pixels plus temperature sensors). The frame rate can be as high as 20 frames per second (fps). Thus all of the data associated with each of the 18 channels must be unloaded in 50 ms which is equivalent to 1 channel approximately every 2.78 ms. Thus the effective ADC conversion rate is 360 samples per second.

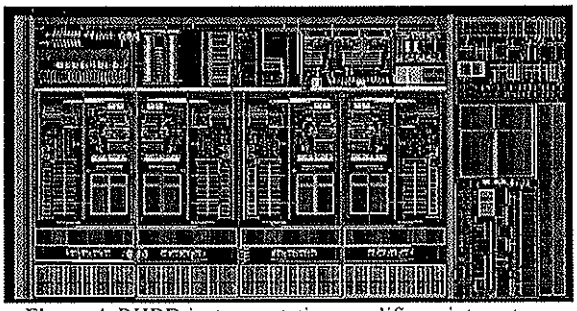

Figure 4. RHBD instrumentation amplifier – integrator.

There are two 16-bit ADCs on-chip. One of the ADCs, a sigma-delta architecture, was hardened like the gain channels and multiplexer. The SDADC uses a 2nd order modulator and outputs a 1 MHz bit stream for off-chip decimation and filtering. A single output helps minimize the backend interface requirements. The output signal can be fed into an FPGA for processing. The pipeline ADC converts at rates up to 20 MHz but is not hardened, instead relying on the inherent tolerance (100 krad TID minimum). This ADC can be powered down when the SDADC is being used and runs off a separate set of supplies from the hardened circuits. The Nyquist ADC was included for other applications (e.g. Earth Sciences) which don't require Mrad hardening.

MCD ASIC RHBD Techniques: RHBD is employed to compensate for cumulative and spontaneous radiation effects. Cumulative radiation effects caused by TID tend to increase the threshold voltages of PMOS transistors and decrease them in NMOS transistors, although this effect scales with the process node (thinner oxides provide less volume in which to capture and store the TID induced positive charge [11]). While displacement damage dose (DDD) degrades mobility [12], TID effects on NMOS leakage is the primary concern for the ASIC's reliable operation in the Jovian system. Accumulated positive charges in the thicker field oxide boundaries around each NMOS transistor can cause parasitic conduction paths from drain-source (through virtual NMOS devices in parallel with their hosts) and between adjacent NMOS devices with different drain/source potentials. This raises the off-state power dissipation, lowers the gain of the transistor through increased drain-source conductance, decreases the isolation between affected nodes and renders switches always on to some extent. Eventually, TID can cause total failure of a circuit.

TID's impact on the NMOS transistors is the main focus of hardening for cumulative radiation effects. The classic strategy to mitigate these effects is to harden the NMOS in the physical design using n+/p+ diffusion guard rings and edgeless or Enclosed Layout Transistors (ELTs). These techniques, though effective, incur area, power and performance (e.g. parasitic capacitance) penalties.

Spontaneous events are termed Single Event Effects (SEEs), which include SEL, Single Event Transients (SETs) and Single Event Upsets (SEUs). Latch-up after a single event strike is particularly hazardous, as the result can be an open circuit in the metal conductors caused by electron migration due to high induced currents. At best, SEL may just render the circuit inoperable until the power supply is switched off and back on again. SETs and SEUs affect both the analog and digital portions of an ASIC by causing voltage/current/bit changes, which perturb a signal from its correct value. Such perturbations in the analog circuit could manifest as errors picked up in the quantization or maybe temporarily destabilize an otherwise stable amplifier loop. In digital circuits, bit patterns can get corrupted which might, in the worse case, cause high current situations that ultimately shorten the life of the chip. SET and SEU errors in general, though, can either be flushed out, scrubbed (if detected) or protected against using temporal latches or triple mode redundancy.

The 180 nm bulk CMOS process node chosen for the MCD has been extensively evaluated for radiation hardness, both within NASA and externally. The thin gate oxide of the 180 nm FETs provides inherent resistance to threshold voltage shifts caused by TID [13]. The CA18 process uses STI and coupled with the lower supply voltages this helps to reduce the general sensitivity to SEL [14]. However, the STI can be a contributing element in the onset of TID induced leakage. The baseline hardness for this process node is at least 100 krad (Si) TID with no RHBD. The process

also offers a thick oxide FET variant, which allows operation at 3.3 V (nominal), which is useful for large swing signals and input/output (I/O) circuits.

The MCD ASIC takes a multi-path approach to RHBD, employing both circuit and layout enhancements to raise the tolerance to TID and single events. In the amplifier, comparator and bias current generator circuits, standard low voltage design techniques are employed with adaptive bias to compensate for threshold voltages that vary with temperature, age and radiation. Utilizing a front-to-back fully differential signal path also helps to harden the circuit against TID induced changes in the common mode (CM) levels of analog voltages. Thus all of the amplifier and ADC circuits use fully balanced differential signal paths, which also enhances linearity and noise rejection. Since the TID mechanism has a more severe effect on NMOS devices, PMOS is employed in the first instance wherever possible. For example, the input differential pair of the operational transimpedance amplifiers (OTAs) are PMOS, which facilitates the incorporation of ELT NMOS as transconductance multiplier or folded cascode loads.

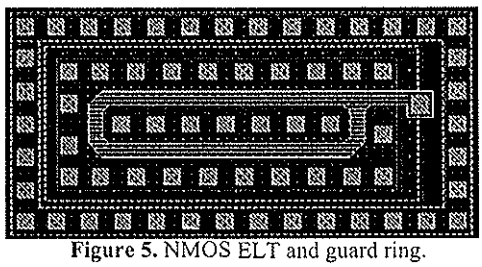

Figure 5. NMOS ELT and guard ring.

The ELT (NMOS version is shown in Figure 5), while reportedly the best hardening mechanism for an NMOS, has several caveats requiring special attention. ELTs are inherently asymmetric with a large difference in the drain and source areas, have higher gate capacitances (than their standard geometry counterparts) and occupy a larger die area for equivalent W/L ratios. Reliability and low output conductance requirements point to using an outer drain region in the layout of the device [15]. The asymmetry also results in a difference between the drain- and source-to-bulk capacitances, which has implications for switched capacitor circuit designs [15]. Since SPICE models for ELTs are not currently (in 2012) included in most, if not all, foundries' PDKs, the models are often approximations derived from standard geometry devices customized by the designer. For the MCD ASIC, a parameterized cell (p-cell) was developed for the ELT allowing customization of the gate width/length, poly chamfer, and guard ring contacting which decreased layout time. All NMOS (and PMOS) are guard ringed to prevent device-to-device leakage and SEL. Transmission gates (switches having both NMOS and PMOS devices in parallel) in the MCD's channels and analog multiplexer circuits utilize standard PMOS and ELT NMOS. In the switched capacitor circuits of the SD ADC, the switches use ELT PMOS and NMOS to minimize clock induced charge injection.

RHBD in the digital areas of the design, such as the clock signal generators, registers, control logic and input/output circuits also utilizes guard rings and ELTs. Since the system is a pipeline of analog and digital signals and no feedback loops involve digital quantities, most upsets experienced in the analog/digital sections will eventually get flushed out. There are three exceptions to this and these are in the registers containing the multiplexer channel number, channel gain and clock divider settings. An upset experienced in these areas could throw off the channel number, gain or chopper/multiplexer clock rates resulting in incorrect output data. To mitigate this, the control words for these quantities are continually refreshed.

Conclusions: An 18-channel readout ASIC has been designed to amplify/digitize the microvolt level signals from a thermopile array for use in radiometry in the Jovian orbital environment. The ASIC uses RHBD techniques in a commercial bulk silicon 180 nm CMOS process to achieve immunity to SEL and TID hardness to at least 10 Mrad.

References: [1] Hanel R. A. et al. (2003) *Exploration of the Solar System by Infrared Remote Sensing.* [2] Paige D. A. et al. (2010) *Space Sci. Rev.*, vol. 150, 125-160. [3] Dillner U. (2006) *Proc. of IRS 2006,* 295-300. [4] Gaalema S. et al, (2010) *Proc. of SPIE,* vol. 7780. [5] Citterio M. et al (2002) *IEEE Trans. Nucl. Sci.*, vol. 42-6, 2266-2270. [6] Maurer R.H. et al (2008) *JH APL Tech. Digest*, vol. 28-1, 17-29. [7] Colinge J.P. (1991) *SOI Materials for VLSI.* [8] Dodd P.E. et al (2000) *IEEE Trans. Nucl. Sci,* vol. 47 2165-2174. [9] Ferlet-Cavrois V. et al. (2000) *IEEE Trans. Nucl. Sci.*, vol. 47, 2183-2188. [10] Heidel D.F. et al. (2009) *IEEE Trans. Nucl. Sci.* vol. 56-6, 3499-3504. [11] Saks N.S. et al (1984) *IEEE Trans. Nucl. Sci.*, vol. NS-31, 1249-1255. [12] Chen L. et al (2005) *IEEE Trans. Nucl. Sci.*, vol. 52-4, 861-867. [13] Faccio F. et al (2007) *Radiation Effects on Embedded Systems.* Springer, 143-160. [14] Dodds N. and Pellish J. (2011) *"TID Test Results for CA18HA FETs & Ring Oscillators",* GSFC internal. [15] Campbell M. et al (1999) *IEEE Trans. Nucl. Sci.*, vol. 46-6, 1690-1696.