Memory Circuit Fault Simulator

A wide variety of decision structures and formalisms is represented in the matrix evaluations.

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Spacecraft are known to experience significant memory part-related failures and problems, both pre- and post-launch. These memory parts include both static and dynamic memories (SRAM and DRAM). These failures manifest themselves in a variety of ways, such as pattern-sensitive failures, timing-sensitive failures, etc. Because of the mission critical nature memory devices play in spacecraft architecture and operation, understanding their failure modes is vital to successful mission operation.

To support this need, a generic simulation tool that can model different data patterns in conjunction with variable write and read conditions was developed. This tool is a mathematical and graphical way to embed pattern, electrical, and physical information to perform what-if analysis as part of a root cause failure analysis effort.

The memory device is modeled as an $n \times m$ matrix structure that is mathematically transformed by a series of matrix defined mathematical and logical operators that represent the read and write operations. The mathematical transformation process is a multi-step process that encompasses both logical and physical information of the memory array. The flexibility of MATLAB allows elements of each operator to be a wide variety of complex structures that includes integer, floating point, or character-based conditions and decision points. The application of operators can also include additional time elements to provide for time-based degradation of memory cells. The size of matrices can be scaled to represent large statistical concerns, or truncated and reduced to focus on regions of interest.

Pattern-sensitive testing schemes can be modeled to reflect real-world testing sequences. Moving inversion, walking, and disturb-based sequences are examples of standard algorithmic patterns that can be applied. Degradations and faults can be modeled at both the logical and physical levels with this formulism. Logical to physical transformations are often at the core of modern sophisticated memory faults.

System designers often assume uniform bit/byte performance while the physical reality is represented by voltage-dependent writes and cells with varying capacitance and drive capability. The fault simulator formulism presented here allows for what-if analysis to help characterize this logical to physical transformation.

This work was done by Douglas J. Sheldon of Caltech and Tucker McClure of MathWorks for NASA's Jet Propulsion Laboratory. For more information, contact iaoffice@jpl.nasa.gov.

The software used in this innovation is available for commercial licensing. Please contact Daniel Broderick of the California Institute of Technology at danielb@caltech.edu. Refer to NPO-48591.