



DSP/FPGA Design for a High-Speed Programmable S-Band Space Transceiver

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Traditional command uplink receivers are very limited in performance capability, take a long time to acquire, cannot operate on both uplink bands (NASA & AFSCN), and only support low-rate communications. As a result, transceivers end up on many programs' critical paths, even though they should be a standard purchased spacecraft subsystem. Also, many missions are impacted by the low effective uplink throughput. In order to tackle these challenges, a transceiver was developed that will provide on-site frequency agility, support of high uplink rates, and operation on both NASA and AFSCN frequency bands.

The device is a low-power, high-reliability, and high-performance digital signal processing (DSP) demodulator for an on-orbit programmable com-

mand receiver. There are several drivers available for the modulation technique. Those drivers include receiver complexity, power consumption, spectral efficiency, and CCSDS (Consultative Committee for Space Data Systems) framework recommendations. Previous research suggests that GMSK (Gaussian Minimum Shift Keying) and BPSK (Binary Phase Shift Keying) are good choices for the uplink modulation format. This approach is supported by CCSDS and helps reduce receiver complexity.

Analysis and derived simulations were performed for power, bandwidth, clock generator, bit synchronizer, and carrier loop. At the time of this reporting, the code was not yet written, and will evolve from the existing analysis and simulation.

The demodulator operates on the two selected modes, BPSK and GMSK. The bit rate covers multiple octaves and includes a bit synchronizer function. The modulator is unique in that it operates with high Doppler, over a large bit rate range, and in a space environment. In addition, this demodulator attempts to maximize low power, small size, and ease of modification to new applications.

Novel features of the innovation include DSP logic for multiple modulation types in a low-power and rad-tolerant platform. Advantages include on-the-fly programmable low-power receive communications for spacecraft.

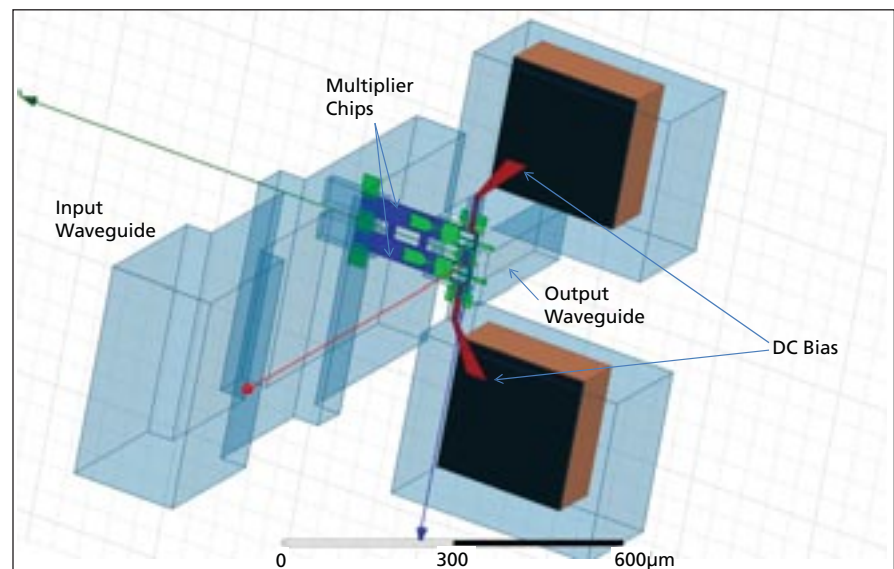
This work was done by Jeffrey Janicik and Assi Friedman of Innoflight, Inc. for Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-16030-1

On-Chip Power-Combining for High-Power Schottky Diode-Based Frequency Multipliers

High-power solid-state sources operate at terahertz frequencies.

NASA's Jet Propulsion Laboratory, Pasadena, California

A 1.6-THz power-combined Schottky frequency tripler was designed to handle approximately 30 mW input power. The design of Schottky-based triplers at this frequency range is mainly constrained by the shrinkage of the waveguide dimensions with frequency and the minimum diode mesa sizes, which limits the maximum number of diodes that can be placed on the chip to no more than two. Hence, multiple-chip power-combined schemes become necessary to increase the power-handling capabilities of high-frequency multipliers. However, the traditional power-combining topologies that are used below 1 THz present some inconvenience beyond 1 THz. The use of Y-junctions or hybrid couplers to divide/combine the input/output power at these frequency bands increases unnecessarily the electrical path of the sig-



1.9 THz On-Chip Power-Combining (2 chips).