individually packaged components for compactness. Each transceiver was designed on a single PCB with a custom enclosure providing interior walls and compartments to isolate transceiver subsystems from radiated interference. The enclosure also acts as a heat sink for the voltage regulators and power amplifiers inside the system. The PCB transceiver design produces transmit pulses of 2 W with an arbitrary duty cycle. Each transceiver is fed by an external 120-MHz signal transmit and two 1,140-MHz local oscillator signals. The received signal is amplified and downconverted to 120 MHz and is fed to the data processor. The transceiver dimensions are approximately $3.5 \times 11.5 \times 0.6$ in. ($9 \times 29 \times 1.5$ cm).

The PCB transceiver design reduces the volume and weight of the DBSAR

instrument while maintaining the functionality found in the original design. Both volume and weight are critical for airborne and flight remote sensing instrumentation.

This work was done by Matthew McLinden and Rafael Rincon of Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-16508-1

🗢 Software Defined Radio With Parallelized Software Architecture

Goddard Space Flight Center, Greenbelt, Maryland

This software implements softwaredefined radio procession over multicore, multi-CPU systems in a way that maximizes the use of CPU resources in the system. The software treats each processing step in either a communications or navigation modulator or demodulator system as an independent, threaded block. Each threaded block is defined with a programmable number of input or output buffers; these buffers are implemented using POSIX pipes. In addition, each threaded block is assigned a unique thread upon block installation. A modulator or demodulator system is built by assembly of the threaded blocks into a flow graph, which assembles the processing blocks to accomplish the desired signal processing. This software architecture allows the software to scale effortlessly between single CPU/single-core computers or multi-CPU/multi-core computers without recompilation.

NASA spaceflight and ground communications systems currently rely exclusively on ASICs or FPGAs. This software allows low- and medium-bandwidth (100 bps to \approx 50 Mbps) software defined radios to be designed and implemented solely in C/C++ software, while lowering development costs and facilitating reuse and extensibility.

This work was done by Greg Heckler of Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-16442-1