



Software Defined Radio With Parallelized Software Architecture

Goddard Space Flight Center, Greenbelt, Maryland

This software implements software-defined radio procession over multi-core, multi-CPU systems in a way that maximizes the use of CPU resources in the system. The software treats each processing step in either a communications or navigation modulator or demodulator system as an independent, threaded block. Each threaded block is defined with a programmable number of input or output buffers; these buffers are implemented using POSIX pipes. In addition, each threaded block

is assigned a unique thread upon block installation. A modulator or demodulator system is built by assembly of the threaded blocks into a flow graph, which assembles the processing blocks to accomplish the desired signal processing. This software architecture allows the software to scale effortlessly between single CPU/single-core computers or multi-CPU/multi-core computers without recompilation.

NASA spaceflight and ground communications systems currently rely ex-

clusively on ASICs or FPGAs. This software allows low- and medium-bandwidth (100 bps to ≈ 50 Mbps) software defined radios to be designed and implemented solely in C/C++ software, while lowering development costs and facilitating reuse and extensibility.

This work was done by Greg Heckler of Goddard Space Flight Center. Further information is contained in a TSP (see page 1). GSC-16442-1

Compact Radar Transceiver With Included Calibration

Volume and weight are reduced without performance penalties.

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The Digital Beamforming Synthetic Aperture Radar (DBSAR) is an eight-channel phased array radar system that employs solid-state radar transceivers, a microstrip patch antenna, and a reconfigurable waveform generator and processor unit. The original DBSAR transceiver design utilizes connectorized electronic components that tend to be physically large and heavy. To achieve increased functionality in a smaller volume, PCB (printed circuit board) transceivers were designed to replace the large connectorized transceivers.

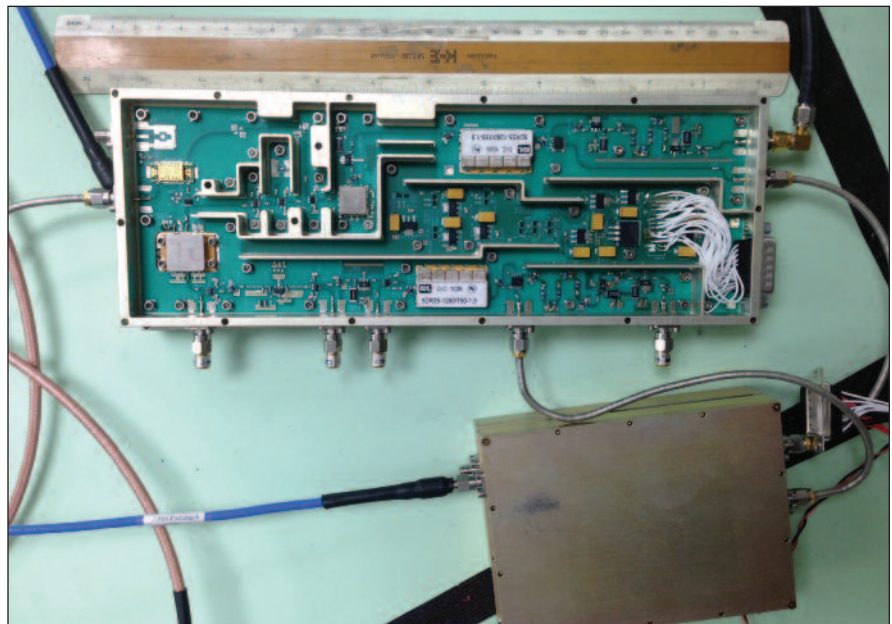
One of the most challenging problems designing the transceivers in a PCB format was achieving proper performance in the calibration path. For a radar loop-back calibration path, a portion of the transmit signal is coupled out of the antenna feed and fed back into the receiver. This is achieved using passive components for stability and repeatability. Some signal also leaks through the receive path. As these two signal paths are correlated via an unpredictable phase, the leakage through the receive path during transmit must be 30 dB below the calibration path. For DBSAR's design, this requirement called for a 100-dB isolation in the receiver path during transmit.

A total of 16 solid-state L-band transceivers on a PCB format were designed.

The transceivers include frequency conversion stages, T/R switching, and a calibration path capable of measuring the transmit power-receiver gain product during transmit for pulse-by-pulse calibration or matched filtering. In particular, this calibration path achieves 100-dB

isolation between the transmitted signal and the low-noise amplifier through the use of a switching network and a section of physical walls achieving attenuation of radiated leakage.

The transceivers were designed in microstrip PCBs with lumped elements and



DBSAR's New Transceiver Architecture will enable the implementation and demonstration of the next-generation digital beamforming synthetic aperture radar, and help advance the technology for infusion in future Earth science and planetary missions.