National Aeronautics and Space Administration

# Commercial Parts Technology Qualification Processes


Mark S. Cooper
Jet Propulsion Laboratory
Pasadena, California



Jet Propulsion Laboratory
California Institute of Technology
Pasadena, California

JPL Publication 13-6 2/13

National Aeronautics and Space Administration

# Commercial Parts Technology Qualification Processes

NASA Electronic Parts and Packaging (NEPP) Program
Office of Safety and Mission Assurance

Mark S. Cooper
Jet Propulsion Laboratory
Pasadena, California

NASA WBS: 724297
JPL Project Number: 104593
Task Number: 40.49.01.13

Jet Propulsion Laboratory
4800 Oak Grove Drive
Pasadena, CA 91109

http://nepp.nasa.gov

This research was carried out at the Jet Propulsion Laboratory, California Institute of Technology, and was sponsored by the National Aeronautics and Space Administration Electronic Parts and Packaging (NEPP) Program.

Reference herein to any specific commercial product, process, or service by trade name, trademark, manufacturer, or otherwise, does not constitute or imply its endorsement by the United States Government or the Jet Propulsion Laboratory, California Institute of Technology.

©2013. California Institute of Technology. Government sponsorship acknowledged.

## TABLE OF CONTENTS

1.0 Introduction ..... 1
- 1.1 EEE-INST-002 ..... 1
- 1.2 JPL Approach ..... 2

2.0 Qualification Approaches at Major NASA Contractors ..... 4
- 2.1 The John Hopkins University Applied Physics Laboratory (APL) ..... 4
- 2.2 Southwest Research Institute (SWRI) ..... 4
- 2.3 Northrop Grumman Space Technology (NGST, Redondo Beach) ..... 4
- 2.4 Space Exploration Technologies (SpaceX) Qualification Processes for Flight Termination Systems ..... 4
  - 2.4.1 Moisture Effects and Corrosion ..... 6
  - 2.4.2 Tin Whisker Growth from Pure Tin Plated Leads ..... 8
  - 2.4.3 Short Description of the Pinsky Algorithm ..... 9
  - 2.4.4 SpaceX Solder Replacement Stance ..... 11

3.0 Medical Electronics Parts Qualification Processes ..... 15
- 3.1 Medtronic's Electronics Parts Qualification Processes ..... 15
- 3.2 Texas Instruments (TI) Proposed Application-Based Qualification Methodology for Medical ICs ..... 20
- 3.3 Automotive Parts Qualification Processes ..... 20
- 3.4 Definition of a Qualification Family ..... 44

4.0 NEPP2012 Commercial Parts Technology Qualification Processes—Conclusions ..... 46

5.0 References ..... 48

## 1.0 INTRODUCTION

Many high-reliability systems, including space systems, use selected commercial parts (including Plastic Encapsulated Microelectronics or PEMs) for unique functionality, small size, low weight, high mechanical shock resistance, and other factors. Predominantly this usage is subjected to certain 100% tests (typically called screens) and certain destructive tests usually (but not always) performed on the flight lot (typically called qualification tests). Frequently used approaches include those documented in EEE-INST-002 and JPL DocID62212 (which are sometimes modified by the particular aerospace space systems manufacturer). In this study, approaches from these documents and several space systems manufacturers are compared to approaches from a launch systems manufacturer (SpaceX), an implantable medical electronics manufacturer (Medtronics), and a high-reliability transport system process (automotive systems).

In the conclusions section, these processes are outlined for all of these cases and presented in tabular form. Then some simple comparisons are made.

In this introduction section, the PEM technology qualification process is described, as documented in EEE-INST-002 (written by the Goddard Space Flight Center, GSFC), as well as the somewhat modified approach employed at the Jet Propulsion Laboratory (JPL). Approaches used at several major NASA contractors are also described.

### 1.1 EEE-INST-002

In this approach, screening and qualification are performed exclusively on the flight lot. Little data is requested from the part manufacturer.

The following test sequence applies to 100% screening tests:

1. External visual inspection and serialization
2. Temperature cycling (MIL-STD-883, Method 1010, Condition B (or to the manufacturer's maximum storage temperature range, whichever is less) (typically 20 cycles)
3. Radiography (topside for wire sweep)
4. CSAM (C-Mode Scanning Acoustic Microscopy) inspection (reject for any topside delamination between mold and die or more than 2/3 delamination of internal wires)
5. Initial (pre-burn-in) electrical measurements (per device specification, at 25°C and min. and max. rated operational temperatures)
6. Engineering review
7. Static (steady-state) burn-in (BI) test at 125°C or at max. operating temperature, per MIL-STD-883, Method 1015, Condition A or B (240 hr at 125°C, 445 hr at 105°C, 885 hr at 85°C, 1,560 hr at 70°C)
8. Post-static BI electrical measurements at 25°C per device specification. Calculate Delta when applicable
9. Dynamic burn-in test at 125°C or at max. operating temperature—MIL-STD-883, Method 1015, Condition D. Hours are the same as step 7
10. Final parametric and functional tests per device specification (at 25°C, max. and min. rated operating temperatures)
11. Calculate percent defective (steps 7–10). Maximum acceptable PDA is 5% for most space systems (lower risk posture) and 10% for higher risk posture
12. External visual/packing inspection

The following test sequence applies to qualification testing performed on the flight lot:

1. Visual inspection and serialization

2. Radiation analysis TID (Total Ionizing Dose) and SEE (Single Event Effects) (usually done by test)
3. Baseline C-SAM (small sample used for popcorn resistance evaluation in step 4, e.g., for variations before and after pre-conditioning)
4. Preconditioning (per JESD22-A113) (simulated solder reflow temperature with 3 passes at board assembly solder temperature) (SMT devices only)
5. Electrical measurements per device specification. Measure at 25°C, min. and max. vendor-specified operating temperatures
6. Life testing (HTOL, High Temperature Operating Life) 125°C per MIL-STD-883, Method 1005, Condition D. Minimum hours: 22 devices for 1,500 hours (low risk space mission) or 1,000 hours (medium risk mission)
7. Electrical measurement (per specification). Measure at 25°C, min. and max. vendor-specified operating temperatures
8. Temperature cycling per MIL-STD-883 Method 1010, Condition B (–55°C to +125°C). Minimum cycles: 22 devices for 500 cycles (low risk space mission) or 200 cycles (medium risk mission)
9. Electrical measurement (per specification). Measure at 25°C, min. and max. rated temperatures
10. C-SAM on 22 pieces
11. Destructive physical analysis (DPA) (MIL-STD-1580) (5 pieces)
12. Biased highly accelerated stress test (HAST) per JESD22 - A110, with continuous bias (96 hr at +130°C and 85% relative humidity, RH)
13. Unbiased HAST per JESD22-A118, Condition A (96 hr at +130°C and 85% RH)

EEE-INST-002 cautions that burn-in (and life test) design should not stress the IC junction beyond its rated capability unless supporting data is obtained from the manufacturer. In addition, the space application should be restricted to the "advertised" (datasheet) temperature range of operation.

## 1.2 JPL Approach

The JPL processes to qualify PEMs for space missions are similar to EEE-INST-002. Significant differences are described below.

JPL does not believe the temperature cycling test as a screen is effective because temperature cycling stresses package failure mechanisms that increase with number of cycles (e.g., wearout characteristic); therefore, a small number of temperature cycles does not increase the reliability of space parts. Note: JPL has test data showing no failures in early temperature cycles (less than 100 cycles).

JPL has copious data proving that X-rays (radiographic examination) of topside for wire sweep (movement of wires during the molding process) never shows a failure, or even a concern. This is not surprising in that significant wire sweep would cause wires to touch on at least a small fraction of commercial products and thus decrease yield unacceptably.

JPL uses manufacturer data to establish soldering characteristics for attachment of PEMs to the board or assembly. This precludes concern with CSAM changes before/after pre-conditioning or other stress. JPL has assessed life test data and found little correlation with CSAM results.

JPL does not perform either unbiased or biased HAST, believing that the conditions in these tests are very far from the part-level stresses found during board assembly, system assembly, or space missions. Failures in tests performed under conditions of temperature, current, or voltage very different than space mission operation conditions invalidates their significance to a situation where parts are handled properly (as they are in space systems).

JPL performs a more significant Engineering Review of burn-in test data, life test data, and extended temperature cycling data. Key electrical characteristics are plotted on probability paper (actually done by specialized software). Results show that electrical characteristics frequently follow standard distributions (typically normal distribution). Examining characteristics in this manner easily identifies statistical outliers. These outliers are culled from burn-in parts (and consequently eliminated from consideration for flight). Further, assessment of changes in electrical characteristics before/after burn-in and life test may be done without reliance on part manufacturer datasheet limits. These limits are often chosen to be wide in order to enhance yield. Changes in electrical characteristics during these stress tests may therefore be missed or underestimated and the reliability of the flight lot may be compromised.

## 2.0 QUALIFICATION APPROACHES AT MAJOR NASA CONTRACTORS

### 2.1 The John Hopkins University Applied Physics Laboratory (APL)[1]

Typically APL follows EEE-INST-002 closely since most space projects use it as a standard. Where contracts allow flexibility, APL prefers to perform 5 piece DPA first to identify issues with construction (similar to a construction analysis). APL prefers not to perform 100% CSAM since this does seem to correlate with reliability or system failures. However, engineering judgment is used so that APL may perform more CSAM with new PEM suppliers.

APL has found various problems with qualifying RF PEMs, typically related to test equipment and its programming. Often, RF parts do not have a complete set of specified electrical parameters over temperature. Therefore the CogE and parts engineer often must guess what these should be. In situations like this, after burn-in "failures" could become a matter of opinion.

Typically DPA failures are with bonds.

### 2.2 Southwest Research Institute (SWRI)[2]

SWRI has no internal standard for PEM upscreening. They develop a specification or drawing to meet customer requirements. SWRI does most upscreening for NASA projects.

SWRI follows EE-INST-002 and prefers to use initial (5 piece) DPA/Construction Analysis to identify issues. They typically perform radiation testing before—or early in—the parts qualification process.

SWRI follows EEE-INST-002 essentially.

SWRI also does radiation before or early in the parts qualification process.

SWRI prefers to not perform 100% CSAM due to difficulties in both determining failures and the lack of correlation to later failures. They note that on NASA projects, some PEM screening/qualification requirements are dropped during Parts Control Board meetings, particularly when the test lab has difficulty performing measurements or correlating with either the manufacturer or SWRI.

SWRI prefers to have PEM manufacturers upscreen to SWRI drawing due to the PEM manufacturer greater capability and lower cost, but must use an independent test lab if they are not willing, which is often the case. SWRI tries to avoid PEMs due to the high cost of complete qualification.

### 2.3 Northrop Grumman Space Technology (NGST, Redondo Beach)[3]

NGST does not have an internal PEM qualification approach or preference. They create a process to match customer requirements for each space project.

### 2.4 Space Exploration Technologies (SpaceX) Qualification Processes for Flight Termination Systems[4]

SpaceX primary Flight Termination Systems (FTS) [1] products are launch vehicles for heavy payloads to near-Earth orbits. SpaceX uses PEMs. Selection of parts for FTS is driven by mission environmental and application conditions. FTS is a harsh dynamic environment, with significant levels of mechanical shock, acceleration, and vibration.

---

1. Andrew Moor – Private Communication
2. Jessica Tumlinson and John Stone – Private Communication
3. Henry Law – Private Communication
4. V8017 Electronic Piece Parts Selection for Flight Termination Systems, Brian Julius and Andrew Ellsberry, August 30, 2011

Typical FTS mission durations vary from 8 to 10 minutes. Therefore long life or slow degradation of parts used within FTS are not issues. Both traditional military grade and PEM devices are designed to operate for many years, which is much greater (by orders of magnitude) than the FTS environment. On the other hand, mechanical and thermal robustness are very significant issues. PEMs are actually much more tolerant of this environment than traditional ceramic encapsulated microelectronics. Furthermore, PEMs typically do not have cavities, so particulate contamination is not an issue for most PEMs. The most important issues and risk factors for PEM usage in FTS are:

- Flight criticality of component
- Termination circuit vs. telemetry monitoring mass
- Thermal operating range and transition time
  - PEM operational temperature range specified may be less than for traditional military parts, but is well within the application envelope
  - PEM packages characterized for many thermal shock cycles, from 0°C to +100°CC (liquid to liquid)
- Shock levels
  - PEMs tested under mechanical shock were greater than an order of magnitude more tolerant than traditional brittle ceramic packages
- Random vibration levels
- Acceleration
- Atmosphere vs. vacuum
- Humidity exposure
  - Falcon avionics bays are environmentally controlled
- Corrosive environments
  - Chemicals used in assembly process
  - Salt fog
  - Avionics bays are environmentally controlled
- Assembly and rework methods
  - Special controls and soldering methods may be required for PEMs (popcorning and solder flux issues)
- Acceptance testing durations
- Derating
- Packaging
  - Internal cavities of traditional military grade ceramic packages are prone to intermittent electrical outputs if conductive particles are inside the cavity
  - Size of device
- Lead vs. 100% tin
  - For space missions, PEMs with lead plating of pure tin, which must be covered via solder dipping to preclude tin whisker growth, are becoming the only available lead plating
  - Tin whisker growth is very slow, mostly occurs at low or no gravity, and is substantially mitigated by solder dip
  - Several companies offer robotic solder dip processes
- Radiation
  - Historically not an issue for FTS applications
- Storage conditions
  - Selected PEMs should either be stored in dry nitrogen, packaged with desiccant, or baked out prior to soldering (popcorning issue)
- Obsolescence
  - Military-grade parts are more subject to obsolescence issues due to their much smaller market share

- Availability/lead times
    - PEMs are typically available immediately or with a short lead time

In addition to these considerations PEMs are often of lower mass (typically 1/3) and smaller footprint than traditional military hermetic packages (particularly in small surface outline or SOIC packages). High production volumes drive the part manufacturers to tighter statistical process controls, which results in more uniformity of production lots.

SpaceX identifies traditional concerns with the usage of PEMs in high-reliability applications by quoting from PEM-INST-001:

> *"1. Due to the major differences in design and construction, the standard test practices used to ensure that military devices are robust and have high reliability often cannot be applied to PEMs that have a smaller operating temperature range and are typically more frail and susceptible to moisture absorption. In contrast, high-reliability military microcircuits usually utilize large, robust, high-temperature packages that are hermetically sealed.*
>
> *2. Unlike the military high-reliability system, users of PEMs have little visibility into commercial manufacturers' proprietary design, materials, die traceability, and production processes and procedures. There is no central authority that monitors PEM commercial product for quality, and there are no controls in place that can be imposed across all commercial manufacturers to provide confidence to high-reliability users that a common acceptable level of quality exists for all PEMs manufacturers. Consequently, there is no guaranteed control over the type of reliability that is built into commercial product, and there is no guarantee that different lots from the same manufacturer are equally acceptable. And regarding application, there is no guarantee that commercial products intended for use in benign environments will provide acceptable performance and reliability in harsh space environments."*

These concerns may be summarized as:

1. Narrower operational temperature range guaranteed by part manufacturer
2. Less insight/knowledge of part manufacturer's internal designs, materials, and production processes and controls
3. No die traceability
4. No centralized agency to monitor or assess part reliability or quality controls

SpaceX asserts that they will mitigate these concerns by selecting appropriate parts for the application and through dedicated lot purchases. They assert that high-reliability PEMs that are qualified to either the Aerospace Qualified Electronic Component (AQEC) standard ANSI/GEIA-STD-0002-1 or Automotive Electronics Council (AEC) standard AEC-Q100 are qualified to similar standards as MIL-PRF-38535. Regarding harsh vs. benign environments, PEMs in general are better suited for shock and vibration environments due to their lower mass.

SpaceX mitigates against negative impacts of limited operational temperature range by selecting parts with a worst case specified operating temperature range of –40°C to +125°C. Hardware temperature range is –34°C to 71°C (AFSPC Manual 91-710), which has been verified by measurements in launch systems.

### 2.4.1 Moisture Effects and Corrosion

Both long- and short-term storage controls are used to mitigate against moisture degradation effects. The primary failure mode due to moisture intrusion is the popcorning effect, which occurs during the assembly process and bond pad interconnect galvanic corrosion (long-term effect).

Popcorning is caused by moisture that is vaporized due to the application of heat and occurs most often during soldering. This can result in delamination, internal and external cracks, and bond damage. This

effect can be easily mitigated by thoroughly baking the parts out prior to assembly. Industry standards for bake out have been established and are defined based on the device's Moisture Susceptibility Level (MSL). SpaceX will use J-STD-033B.1, Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices, as their guide.

Long-term moisture degradation requires additional factors:

> *"For galvanic corrosion to occur in PEMs, the following elements are necessary: a bimetallic couple (most often gold–aluminum, present in the gold bond wire to the aluminum metallization pad), free (mobile) ionic contamination (usually chlorine, potassium, bromine, and/or sodium), and moisture (diffused from the atmosphere), to form an electrolyte. All elements listed, except ionic contamination, are present in most PEMs."* [2]

This failure mode has essentially been eliminated in modern PEMs through the reduction of ionic contaminants and cleaner semiconductor processing [3]. Today's PEMs are designed to function in spite of moisture absorption, compared to hermetic devices that focus on preventing moisture. Numerous studies have been conducted on the long-term effects of moisture intrusion on PEMs. These studies suggest that using a controlled temperature and humidity environment, along with proper packaging and periodic replacement of desiccants, result in a shelf life of more than 15 years. Below is a summary of the referenced studies:

- Component Reliability After Long Term Storage [4]
  - 20 component types (reel or tube of each) were tested to determine the effects of long-term storage on the original manufacturer's packaging in a warehouse environment for a duration of 2–17 years
  - Packaging maintained its critical properties including tribocharging (ESD properties) , but moisture barrier bags may allow moisture to enter after extended periods of time (greater than their 32-month life)
  - The results of the solderability, microscopic visual inspection (SEM and optical), spectral analysis, MSL performance, and DPA demonstrate that device life is greater than15 years
- Reliability Assessment of Electronic Components Exposed to Long-Term Non-Operating Conditions
  - Study of several hundred microcircuits and assemblies stored in uncontrolled environments (sometimes outdoor, with temperature ranges as great as –40°C– to 55°C and 100% RH)
  - The PCBs in the assemblies investigated showed a higher propensity for corrosion (on traces) than the PEM components installed on them
  - "It is … clear that the automotive environment is at least as harsh as the field storage environment and thus the automotive data is relevant to long-term storage"
- Commercial Plastic Encapsulated Microcircuits for Naval Aviation Applications (see footnote 5)
  - Analysis of 92 commercial- grade PEMS between 2 and 28 years old through visual inspection (MIL-STD-883), solderability, electrical specifications, radiographic inspection, CSAM, and DPA
  - Significant external and cosmetic anomalies were identified (the storage conditions were uncontrolled and often unknown)
  - DPA resulted in no rejections of parts newer than 18 years, corrosion only evident in 2 components that were 28 years old. These failures may have had as much to do with the contemporary manufacturing processes than the storage duration
  - "[CSAM] revealed delaminated areas in most parts, suggesting that this technique might not be a good method for PEM screening"

While all studies show that there is significant margin in modern PEM designs and they can be used in a wide range of conditions for extended durations, the most relevant study to how SpaceX proposes to store components is Component Reliability After Long Term Storage [4]. The one significant negative finding in

this study was that the original packaging was not sufficient to keep the components dry over extended periods, as the standard packaging is only designed for 32 months without repacking. While the components were all within specifications after a bake-out per J-STD-033, the preferable storage solution is one that completely eliminates moisture and corrosive contaminants, potentially extending the storage life to the several decades enjoyed by their hermetic counterparts. In order to deal with the stockpile related issues for PEMs, representatives of the U.S. Department of Defense and the major defense contractors created GEIA-STD-0003, Long Term Storage of Electronic Components, specifically for the long term preservation of piece parts for military and high- reliability applications. This standard goes beyond J-STD-033 and looks to preclude moisture intrusion, reduce corrosive contaminates, and regulate storage temperature to allow for long term storage rather than just protecting the devices until they are used.

SpaceX proposes all components will be handled and stored in accordance components will be stored in vapor barrier antistatic packaging that meets or exceeds the requirements.

- A low-contaminant desiccant will be used to reduce the introduction of corrosive elements
- Moisture Barrier Bags (MBBs) and desiccant will be replaced every 2 years or their rated lifespan, whichever is less
- Temperature will be controlled at 25°C ± 10° to reduce temperature cycling

SpaceX proposes a 3-year storage limit from the piece parts manufacturing date, lot date code, to board level assembly. The assembly service life will then be limited to 5 years from date of assembly or as defined in the assembly specification.

### *2.4.2 Tin Whisker Growth from Pure Tin Plated Leads*

Unalloyed tin coatings have been shown to have an elevated propensity for producing metallic whiskers when compared to traditional tin/lead plating. These whiskers can grow between adjacent contacts or surfaces and cause short circuits and other electrical failures. Many PEMS are only available with pure tin coated leads.

With unalloyed tin finishes becoming more difficult to avoid, the aerospace industry along with government representatives, have produced GEIA-STD-0005-2, Standard for Mitigating the Effects of Tin Whiskers in Aerospace and High Performance Electronic Systems. This standard lays out a framework for using lead-free finishes based on the allowable risk.

The NASA Parts Policy, NPD8730.2C, allows for lead-free components with a mitigation plan that meets Level 2C of the GEIA standard. This is the most stringent category of regulation that allows any use of tin plating. When a Sn/Pb finish is not available, Level 2C of GEIA-STD-0005-2 requires the following for pure tin platings:

- A component-level mitigation plan and approval for each tin plated component (no blanket exceptions)
- 2 mitigations from different mitigation categories defined as follows:
    - Design to reduce risk (spacing, encapsulation, redundancy)
    - Use of lower risk finishes (annealed/fused, nickel underplate)
    - Partial tin finish replacement (dipping component in or soldering with SnPb)
    - Conformal coating

In addition to the mitigation requirements, the standard also supports the use of analytical methods to calculate the overall risk of a tin whisker failure. The Pinsky Method, developed by David Pinsky at Raytheon, is the current analysis tool of choice across much of the aerospace industry. The calculations produce an output based on the risk of different physical properties of the device, including metallurgy and lead spacing, and mitigation techniques employed. The results are based on a number of factors, including the predicted whisker density, whisker length, and effectiveness of mitigation techniques, and are shown on a logarithmic scale. Known failures due to whiskers were used as a calibration for the

results, with none of the whisker failures scoring below an 8.99; the accepted threshold for Level 2C is a score of 7 or lower.

SpaceX proposes to comply with this methodology by submitting, for Range approval, a mitigation report for each tin plated component that includes the part information, the two or greater risk mitigation strategies employed, and a risk calculation per the Pinsky Method.

### *2.4.3 Short Description of the Pinsky Algorithm*

The intent of the algorithm [5] is to assess the risk that for a given application of a PEM with pure tin plated leads, that tin whiskers will bridge between conductors. The term "overall mechanical risk" is used to describe this risk of whisker bridging. Experience indicates that for many applications, the risk of a whisker bridging is so negligible that further assessment of the consequences is unnecessary. Experience has also shown that in a sizable fraction of the assessments where the mechanical risk is high, the consequences of a bridge are so evident that no further risk assessment is needed.

The concept behind the algorithm is that the mechanical risk is a product of the probability that whiskers will form, and the probability of these whiskers bridging between conductors. The factors that affect whisker growth relate to the properties of both the plating and the substrate onto which it is plated. The factors that affect the bridging risk relate to the geometry of the assembly and the presence or absence of insulating coatings on the conductors.

Note: This algorithm is based upon the premise that failure only occurs if a whisker bridges the entire gap between conductors. This premise applies to most applications, but not to high voltage applications where arcing across gaps is a common failure mode.

The output of the algorithm is a numerical index of the relative risk of whisker bridging, and as the levels of risk are anticipated to range over several orders of magnitude, the numerical index will be reported on a log-10 scale. Scaling factors have been selected so that the range of the numerical factor falls between zero and ten. Higher output numbers indicate higher degrees of risk.

There are 13 inputs used for the algorithm, which represent risk and mitigation factors that affect the probability of the formation of a whisker bridging between adjacent conductors. These factors are defined below.

$r_1 = f_1$ (conductor spacing)

$r_2 = f_2$ (Pb content in plating)

$r_3 = f_3$ (Sn deposition process)

$r_4 = f_4$ (Sn deposit thickness)

$r_5 = f_5$ (composition of material directly beneath Sn deposit)

$r_6 = f_6$ (substrate controlling the CTE imposed on Sn deposit)

$r_7 = f_7$ (reflow of Sn deposit)

$r_{8a} = f_{8a}$ (type of conformal coating applied directly over Sn deposit)

$r_{8b} = f_{8b}$ (type of conformal coating applied on the surface of adjacent conductors)

$r_9 = f_9$ (use of mechanical hardware that applies stress to the surface of the Sn deposit)

$r_{10} = f_{10}$ (vulnerability of the assembly to contamination related failure, as indicated by imposed environmental controls during assembly)

$r_{11} = f_{11}$ (use of conformal coating on conductors throughout assembly)

$r_{12} = f_{12}$ (airflow within assembly)

The functions $f_x$ are as defined by the table below, and the values have been adjusted during the calibration process for the algorithm.

The scale factor has been set to K = 8.9, based upon the maximum and minimum values produced by the functions defined below, to set the range of the numerical output to range from zero to ten.

These factors are combined in accordance with the following:

Overall Mechanical risk = $R_{total}$

Total susceptibility risk factor = $R_{susceptibility}$

(The effects of geometry on the ability of a whisker to create a bridge.)

Overall whisker growth risk factor = $R_{formation}$

(The risk of forming a whisker of sufficient length to create a bridge.)

Scaling constant = K

Equation 1 $$R_{total} = K + \log_{10} (R_{susceptibility} \bullet R_{formation})$$

The susceptibility of the application to whisker induced failures is broken into two parts: primary shorts and secondary shorts. Primary shorts occur when a whisker bridges directly from its origin to an adjacent conductor. Secondary shorts occur when whiskers become dislodged and migrate through the system to a remote site with a bridge between the two other conductors. The formation factor is also broken in two parts: the density of the whisker growth and the lengths of the whiskers.

Equation 2 $$R_{total} = K + \log_{10} [(R_{primary} + R_{secondary}) (R_{density} \bullet R_{length})]$$

A simplification is made to formulate the risk that whiskers will grow by assuming that there are four independent driving mechanisms of concern:

1. Stress induced during initial tin deposition
2. Stress developed in the tin as a result of inter-diffusion with the material below during time/temperature exposure
3. Stress developed over time due to differential CTE between the tin and the controlling substrate
4. Stress induced as a result of externally applied forces

Initial stress risk factor = $R_i$

Diffusion stress risk factor = $R_d$

CTE stress risk factor = $R_{cte}$

External risk factor = $R_{ex}$

The growth of whiskers across the gap will be diminished by the presence of conformal coating directly on the tin surface. Therefore, the four factors identifying sources of stress, combined with a conformal coat factor, defined the overall

Equation 3 $$R_{density} = r8a (R_i + R_d + R_{cte} + R_{ex})$$

Investigations into the distribution of whisker lengths that grow from various deposits of tin indicate that some mitigation techniques are effective, not because they necessarily decrease the density of whisker growths, but because they seem to restrict the lengths of the whiskers that do form. Therefore, the length factor is defined as a function of the individual factors representing plating process, substrate composition, and post plate heat treatment as follows:

Equation 4 $$R_{length} = (r_3 \; r_5 \; r_7)$$

Combining equations 1-4,

Equation 5

$$R_{total} = K + \log_{10}((R_{primary} \bullet R_{secondary}) \{(r_3\ r_5\ r_7)\ [r_{8a}\ (R_i + R_d + R_{cte} + R_{ex})]\})$$

Each of the six $R_x$ remaining values in Equation 5 are calculated based upon attributes of the application.

$$R_{primary} = f\ \{r_1, r_{8b}\}$$

$$R_{secondary} = g\ (R_{length}, r_{10}, r_{11}, r_{12})$$

$$R_i = h\ \{r_2, r_3, r_4, r_5, r_7\}$$

$$R_d = l\ \{r_2, r_5, r_7\}$$

$$R_{cte} = m\ \{r_2, r_6\}$$

$$R_{ex} = n\ \{r_2, r_9\}$$

Functions are f, g, h, l, m, and n. These functions are simple products and could be redefined later if data indicates a different type of relationship applies.

The net result of the calibration process is that all of the documented failures yield a score of 8.99 or higher, while applications where the SMEs generally agreed that tin was suitable for use score below the range of 7.0–7.5.

These scores are typically compared against the threshold value that is agreed upon as appropriate for the reliability requirements of the system in question. In the context of system-level controls in accordance with GEIA-STD-0005-2, a threshold value of 7.5 is recommended for use with Tin Control Level 2B, and a threshold value of 7.0 is recommended for use with Tin Control Level 2C.

### 2.4.4 SpaceX Solder Replacement Stance

The most effective tin whisker mitigation strategy is to replace all the lead finish on a component with a Sn/Pb finish. This is done through dipping the component in molten solder with a sufficient Pb content. With coverage validation, many standards, including GEIA-STD-0005-02, consider the part to be a lead-free part susceptible to whisker growth. This is a commonly used process for hermetic components and passives that are tolerant to the solder dipping, such as ceramic capacitors. The problem with plastic encapsulated microcircuits is that the potting material will crack or melt when exposed to molten solder. For this reason, hand dipping PEMs in a solder bath is not recommended.

SpaceX considers the solder dipping of PEM components to be an unnecessary risk for FTS and other critical components as it is trading a known risk that is understood and which can be mitigated with one that is unknown and highly variable.

#### 2.4.4.1 Conformal Coating

Conformal coating provides board-level defense against tin whiskers. The coating reduces the risk of whisker failures in the following ways:

- Reduces whisker quantity
- Whiskers must break through the conformal coating at the source
- Whiskers must penetrate the conformal coating on the destination contact (effective if entire board is coated)
- Reduces the risk of detached whiskers (FOD) causing a short between contacts

SpaceX currently uses thick conformal coating as its primary whisker mitigation on all assemblies. The circuit assemblies are coated with a 2 mil (±1 mil) Urethane conformal coat. This mitigation strategy is based on the work of Panashchenko at GSFC where they have conducted a long-term (11 years) study of the effect of very thick conformal coatings on whisker growth. A 2 mil (±1 mil) urethane conformal

coating was applied to test samples comprised of tin plated brass (known to be a high whisker risk material). The control areas without conformal coating produced whiskers with a density of approximately 50 whiskers/$mm^2$ while the coated areas showed no whiskers had penetrated the conformal coating after 11 years. The thick coating is effective because the whiskers that do grow lift a small amount of the conformal coat, but reach their Euler buckling point before they can break out of the coating. The thick coatings, as well as much thinner applications, protect the destination lead from a short, because the depth any whisker can penetrate before bucking is proportional to the inverse square of the whisker length.

For the NASA COTS/CRS programs, such as the Falcon 9 launch vehicle and the Dragon spacecraft, SpaceX is utilizing thick conformal coating as the tin whisker mitigation approach.

#### *2.4.4.2 Proposed Lead-Free Mitigation Plan*

SpaceX proposes the following lead finish piece parts plan:

- When available, SpaceX will procure components that are produced with an approved low whisker risk finish. The following are proposed as low risk finishes that are appropriate for use in an FTS:
  - Tin with greater than 3% lead
  - Nickel palladium
  - Nickel palladium with a gold flash
  - Gold
  - Other finishes with specific approval
- All non-DSCC approved components, or those procured from non-DSCC approved distributors, having a Sn/Pb-based lead plating will be tested as part of lot acceptance DPA to insure that the finish contains >3% Pb
- All components that do not utilize a low-risk finish as described above, as well as any Sn/Pb finished component containing <3% Pb, will be handled in accordance with GEIA-STD-0005-2, Level 2C through the following:
  - A risk and mitigation report will be generated for each component
  - At least two mitigation techniques from two different categories will be implemented, as identified in GEIA-STD-0005-2
  - An analytical assessment of the overall risk shall be conducted by using the Pinsky Method calculation to ensure that the overall risk is less than or equal to a 7.00 on the Rev. D calibrated scale
- At the board level, the following steps will be taken for all components to reduce the risk of whisker growth as well as the risks of a whisker-induced failure:
  - Sn63Pb37 solder will be used for all components
  - Entire board will be conformal coated with a 2 mil conformal

SpaceX proposes the following screening (100% test) and qualification (lot testing) flows for launch systems (Figures 2.4.4-1 and 2.4.4-2).

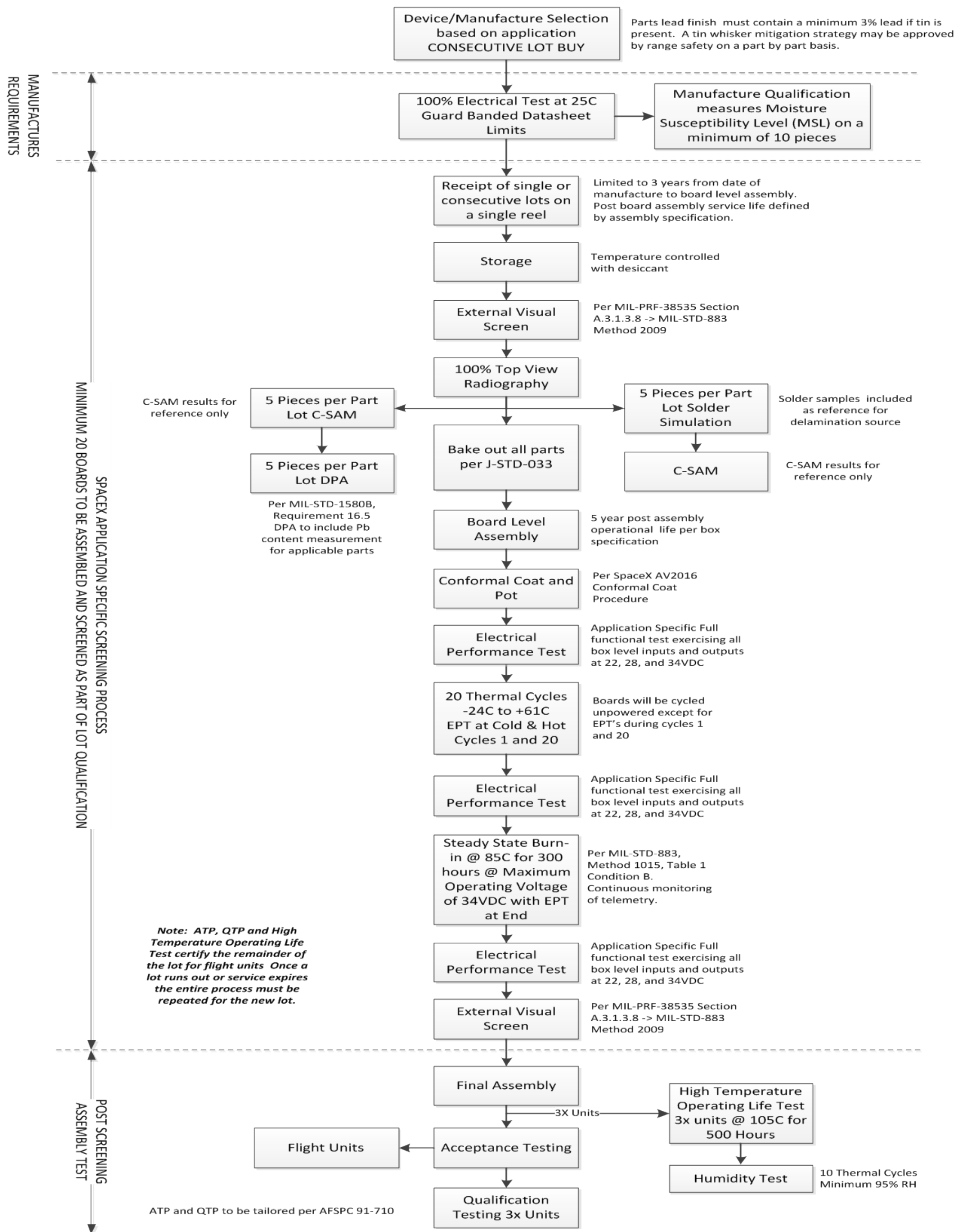


Figure 2.4.4-1. SpaceX proposed screening flow (100% test) for launch systems.

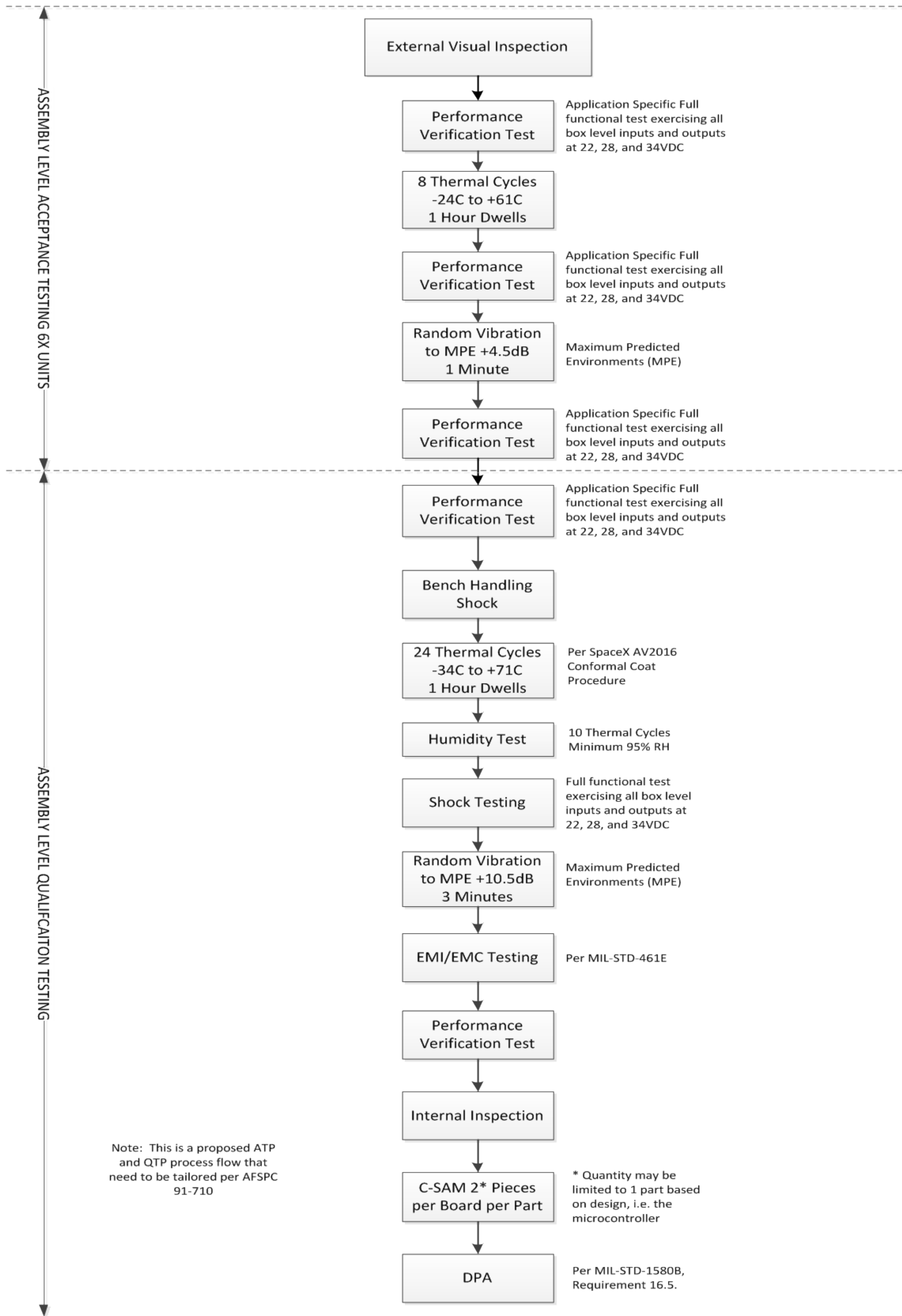


Figure 2.4.4-2. SpaceX proposed qualification flow (lot testing) for launch systems.

# 3.0 MEDICAL ELECTRONICS PARTS QUALIFICATION PROCESSES

## 3.1 Medtronic's Electronics Parts Qualification Processes [6,7,8]

Medtronic's major product base is implantable medical devices. As seen in many devices discussed in this report, the qualification approach is driven by the application market and its concerns.

Among the implantable electronics devices made by Medtronic are:

- Pacemakers (Implantable Pulse Generators-IPG)
- Implantable Cardiac Defibrillators (ICD)
- Neurological stimulators for pain and functional disorders
- Implantable drug pumps (insulin)
- Implantable pulse monitors

Among the external electronic devices made by Medtronic are:

- Automated External Defibrillators (AED)
- Glucose meters and insulin pumps
- Cardiac surgery devices

Medtronic also makes non-electronic products including:

- Coronary stents
- Heart valves
- Spinal products
- Ear, nose, and throat surgical equipment

Medical electronics infrequently use standard off the shelf electronics due to constraints such as ultra-low power, very small size, and unusual/unique functionality. Therefore the device manufacturer must often qualify internal electronic parts.

Medical devices are highly regulated according to three FDA classes:

- Class I: Devices that interact minimally with patients (tongue depressor, bandage, hearing-aid)
- Class II: Devices that have moderate interaction with patients and have a low probability of harm (X-ray machines, spinal hardware)
- Class III: Devices that interact with patients in a chronic setting or have the possibility of serious injury or death if they malfunction (pacemaker, automated external defibrillator)

Classes II and III device manufacturers must inform the regulatory agencies (e.g., the FDA) of significant changes or data (such as returns or field anomalies). Regulatory agency involvement in product qualification activities is significant.

Global regulatory requirements vary:

- U.S.A. (FDA)
- Japan (MHLW)
- Europe (TUV)

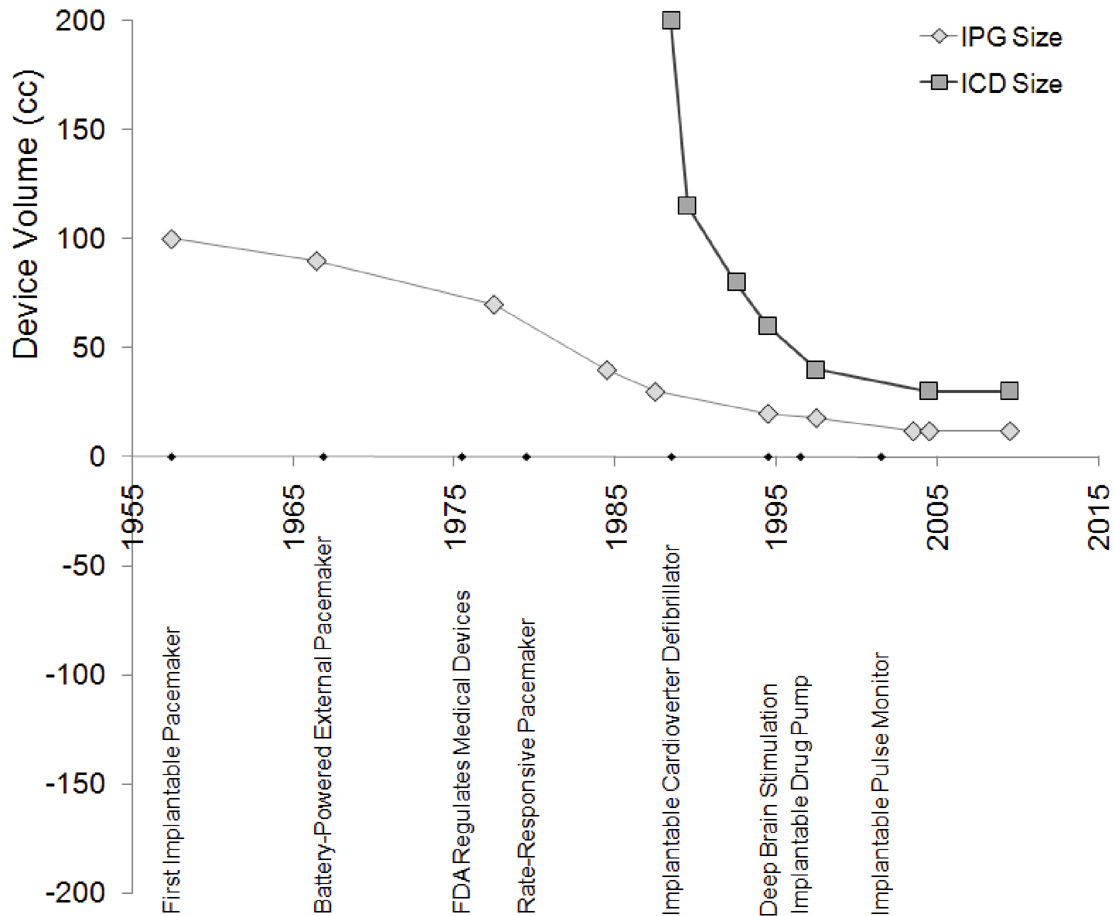


Figure 3.1-1. Size and integration of electronics has been a major driver for new technology adaption.

Medical electronics must make aggressive use of high levels of integration and CMOS scaling since greater intervention to extend useful human life and productivity is being necessitated by aging First world populations and a smaller ratio of client populations to populations “paying” for medical care [9]. More choices of medical care are being influenced by the payer (insurance) and not just the doctor. These considerations drive medical electronics that increasingly provide a wealth of internal sensor data, which must be analyzed and categorized before being made available to the medical professional for assessment. This immediately drives medical electronics into the microwatt and nanowatt power dissipation regimes. This lower power requirement also lengthens the time between procedures to implant the devices or replenish them. For these reasons, implantable medical devices frequently work in the sub-threshold CMOS regime. Furthermore, this means that reliability evaluation and qualification of such devices is qualitatively different, in that small increases in power supply current may actually be functional failures. This means that IDDQ tests/measurements/statistical evaluations have greater significance and must be more closely monitored during qualification and reliability characterization, including at the wafer and wafer foundry level.

Medtronic uses a variety of approaches to cope with the rapidly changing technology landscape:

- Integration of supplier design systems with Medtronic expertise is essential
- Internally developed requirements supplemented or modified with industry standards
- Dialog with external experts shortens learning cycles

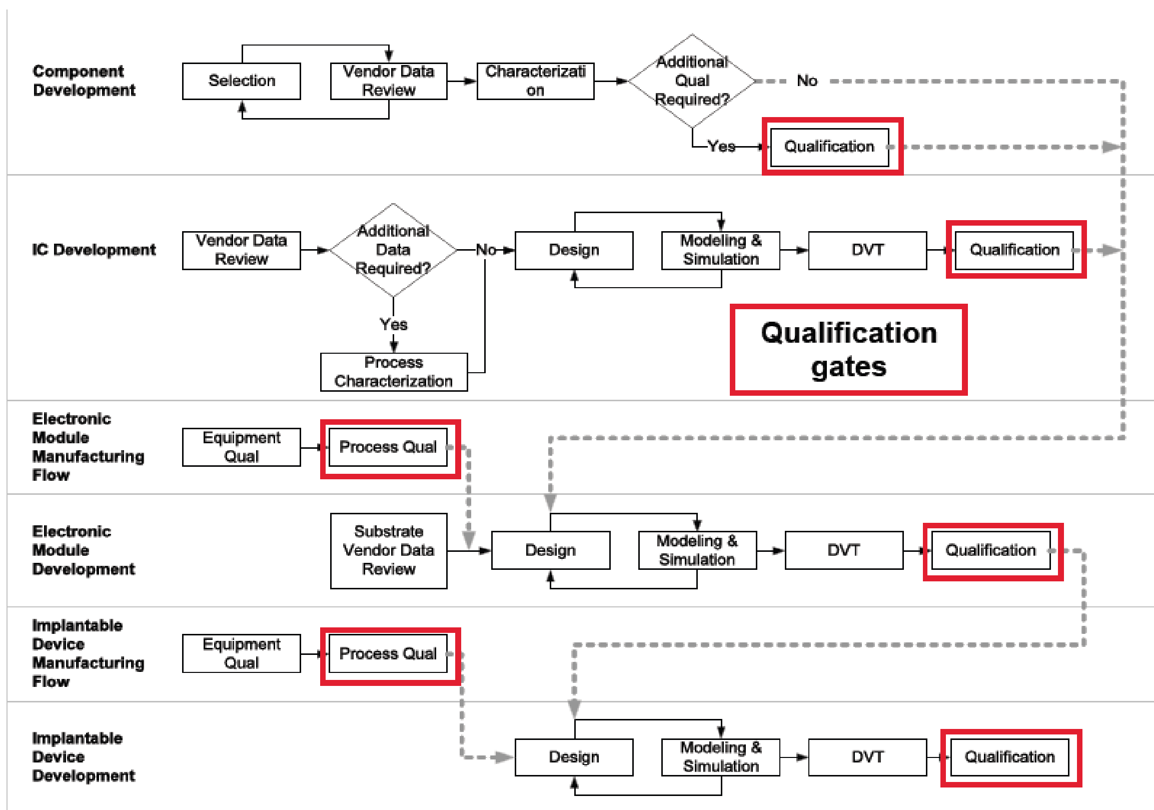


Figure 3.1-2. Qualification of manufacturing processes and components serve as gates before each successively more complex system is qualified.

**Table 3.1-1.** Qualification test protocols are based upon failure mechanisms of concern.

| Failure Mechanism | Accelerating Stresses | Qualification Test | Applicable To |
|---|---|---|---|
| Cautery/Defib Damage | Voltage | Saline tank high-voltage pulse testing | Final device |
| Ceramic Capacitor Cracking | Mechanical stress | Vibration testing, 4-point bend, drop testing | Electronic module |
| CMOS Failure Mechanisms (SILC, NBTI, TDDB) | Temperature, voltage | HTOL | CMOS-integrated circuits |
| Component Fracture Inside Final Device | Pressure | Barometric pressure testing | Final device |
| Corrosion | Temperature, RH, contaminants | Hermetic environment of implantable device makes this an insignificant failure mechanism | N/A |
| Creep | Mechanical stress, temperature | HTOL | Electronic module, final device |
| Current Leakage Increase Due to Component Degradation | Temperature, voltage, ambient environment | HTOL, bias/environmental testing | Component, electronic module |
| Delamination | Humidity, contamination, temperature cycling, mechanical stress | HTOL, temperature cycling, 85/85, vibration testing, 4-point bend | Component, electronic module, final device |

| Failure Mechanism | Accelerating Stresses | Qualification Test | Applicable To |
|---|---|---|---|
| Dendritic Growth | Temperature, voltage, differential | Hermetic environment of implantable device makes this an insignificant failure mechanism | N/A |
| Electromigration | Current density, temperature, temperature gradient | IC level conducted by foundry. This is generally not a failure mechanism of concern in implantable cardiac devices due to low current densities. Neuromodulation devices may require additional testing | Component, electronic module, final device |
| ESD Damage | Voltage | ESD testing | CMOS electronics, electronic module |
| Fatigue Cracking | Mechanical stress, strain range | Vibration testing, 4-point bend, drop testing, low frequency/low amplitude repetitive cycling | Electronic module, final device |
| High-voltage Component Failure | Temperature | Repetitive defibrillator charge/discharge cycling | Electronic module, final device |
| Intermetallic Formation (e.g., purple plague) | Temperature | HTOL | Electronic module |
| Popcorning Due to Moisture Absorption (plastic packages or epoxy overmold) | Temperature | MSL testing | Component, electronic module |
| Radiation Degradation | Radiation intensity | X-Ray radiation testing, MRI susceptibility, CT testing | Component, electronic module, final device |
| Soft Error Upset | Particle impingement rate | Alpha foil, neutron beam, proton beam, heavy ion testing | Component, electronic module |

Electrical characteristics that are important to commercial devices may or may not be significant to implantable medical devices. For example, standby current for SRAMs increases significantly at temperatures lower than about 10°C. At first one might think that standby current would therefore not be a problem in an implantable medical device. However, a battery operated pacemaker turned out to have a large fallout after shipment. This was caused by sub-zero conditions in airplane transit, which depleted the batteries inside the medical device. A counter-example would be 'popcorn' noise in precision analog electronics where commercial applications demand low noise. Medical applications also demand low noise, since popcorn noise may be on the same order of magnitude as some physiological signals. Bias currents in some low power circuits may not provide enough noise margins. These considerations emphasize that electrical testing during qualification must be more comprehensively tailored to the medical device application.

Failure mechanisms have a different significance for most medical applications, so tailoring the qualification tests used is required. The various failure mechanisms of concern and their significance for medical applications are listed here:

- Electro-migration: exponential dependence on temperature (i.e., worse at higher temperatures) and inverse square dependence on current density—lower power applications will reduce any electro-migration risk and designs are optimized for minimal junction temperature.
- Hot carrier injection: gate and substrate currents increase failure rate by power laws; temperature increases degrade time to failure by the usual Arrhenius equation—drain engineering across all technologies has made this a non-issue.

- Bias temperature instability: impacts both n- and p-channel devices; several models, including reaction-diffusion and charge trapping/detrapping; is not significant for medical devices since this effect is decreased at low power and voltage.
- Mechanical failure mechanisms: stress migration mitigated by reliability design rules, low temperature; temperature cycling concerns for large temperature swings in automotive and high-performance desktop computing are non-issues for medical electronics (Coffin–Manson model frequently used), hot spots mitigated during design process.
- Intrinsic oxide reliability (Time- Dependent Dielectric Breakdown): not a concern for medical electronics since wear-out under ultra-low power is mitigated by low voltage and low electric field.
- Ultra-thin oxide reliability: soft breakdown may be present due to current drain increase; Stress-Induced Leakage Current (SILC) may be a concern.

Since wear-out failure mechanisms are of much less concern for ultra-low powered implantable medical devices, screening and infant mortality considerations correspondingly become more important. At the wafer level, IDDQ testing—including statistical analysis of this parameter for outlier chips—becomes an important strategy. The medical electronics industry is cautious about allowing application usage of good die in bad neighborhoods. Over-voltage stress (that is, above the circuit application voltage, which will be low) may be used before IDDQ evaluation to screen out marginal chips. Components or modules (above chip level) typically use high temperature reverse bias burn-in as a screen and multiple temperature cycling screening to accelerate infant mortal defects. Repeated therapy delivery cycles is an application-related method to reduce infant mortality risks.

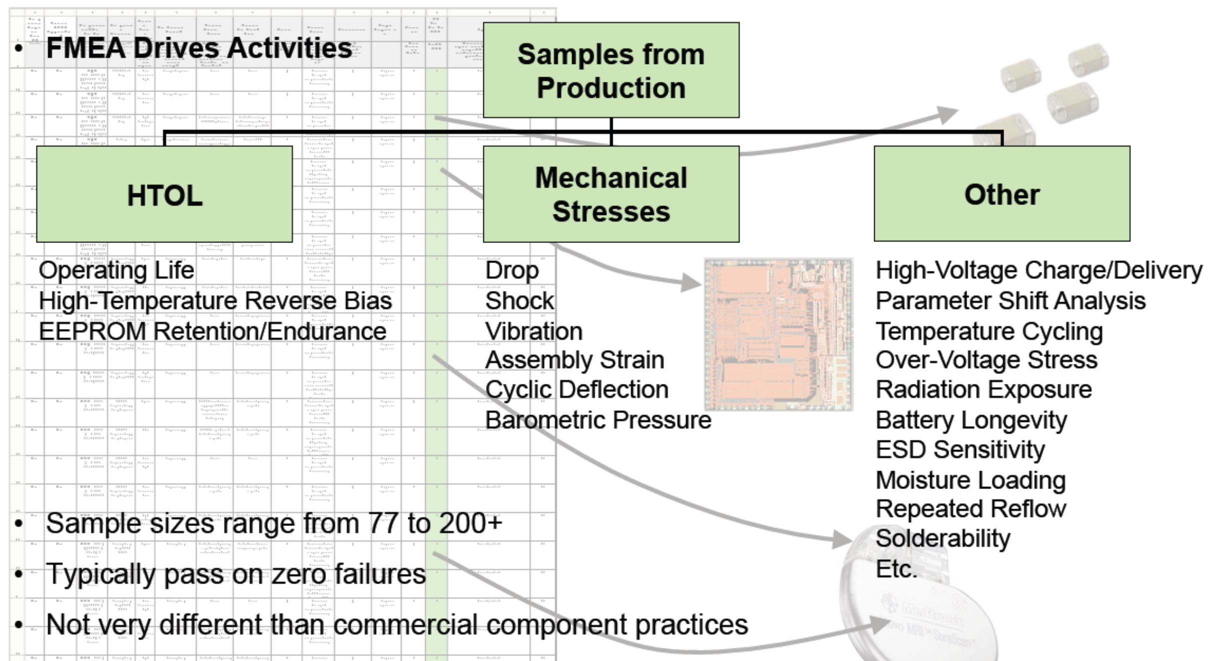


Figure 3.1-3. Qualification sequences and sample size are driven by FMEA.

Outlier IDDQ die signatures behave differently than good die signatures. Outlier value distribution may be indicative of latent defects. Intel has reported that they had order-of-magnitude higher burn-in failure rates from risky die population compared to the remainder of die.

## 3.2 Texas Instruments (TI) Proposed Application-Based Qualification Methodology for Medical ICs [10]

Traditional stress-driven qualification test programs (MIL-STD-883, Test Methods and Procedures for Microelectronics, and JEDEC JESD47, Stress-Test-Driven Qualification of Integrated Circuits) are not optimized for economical design and rapid product qualification for medical electronics. The application conditions of medical devices vary significantly and are, in general, radically different than conditions found in traditional aerospace high-reliability markets. For example, some medical applications are short duration, while chronic disease treatment monitoring systems are long duration. Few medical applications have the extremes of temperature, vibration, and mechanical shock that are typical of aerospace applications. To appropriately tailor the qualification for medical applications, a detailed analysis of the usage conditions is required early in the process. Often these usage conditions consist of a series of different environments of voltage, temperature, and frequency. TI models these conditions in the generalized form:

$$1 = \int \frac{dt}{t_{life}(V_{stress}, Temp)}$$

This equation is rewritten in a discrete form and the equivalent lifetime (teqlife) after a series of voltage and temperature stresses is expressed as

$$t_{eqlife} = \sum_{i=1}^{N} t_i = \frac{1}{\sum_{i=1}^{N} \left[ \frac{t_i}{\sum_{i=1}^{N} t_i} * \frac{1}{t_{life}(V_i, T_i)} \right]}$$

where $t_i$ is the time duration under each stress condition and $t_{life}$ is the lifetime at the stress level of Vi and Ti (voltage and temperature stresses).

This equation can be used to tailor the various test times during a qualification process provided the functional relationship of lifetime and voltage or temperature is known (for example, the familiar Arrhenius equation). In an obvious way the traditional test results of high temperature operating life test or voltage stress ramp tests may be used to qualify a medical application where the temperature, durations, and voltage stresses can be measured.

## 3.3 Automotive Parts Qualification Processes[5,6]

The automotive industry relies on an extensive qualification test program at the part level and extensive review of parts manufacturer's processes, including periodic statistical process controls such as wafer process monitors and reliability process monitors (which include sample life testing). The standards for automotive parts are maintained by the AEC.

The AEC was originally established by Chrysler, Delco Electronics and Ford to establish common part qualification and quality systems standards. It is presently an engineering committee composed of sustaining members representing end-user companies (e.g., Tier 1 or equivalent) that supplies electronics modules/systems for consumer automotive OEM's (Original Equipment Manufacturer's); technical members representing automotive market companies that use electronics in their products or

5. Automotive Engineering Council standards are maintained on the web at http://www.aecouncil.com/.
6. Testing and qualification of automotive parts is typically in accordance with either MIL-STD-883 test methods or JEDEC tests methods under JESD nomenclature and maintained at http://www.Jedec.org.

manufactured electronics components (e.g., Tier 2 or equivalent); associate members representing companies/organizations providing support and services to the electronics industries (e.g., Tier 3, sub-contractors, universities, etc.), and guest members. There is an annual reliability workshop held near Detroit, Michigan.

AEC encourages part manufacturers to use a statistically based method, called part average testing (PAT) (AEC-Q001) to remove outliers from potential use during the manufacturing process (parts with abnormal characteristics). Important characteristics are ones that could impact product quality or reliability. Critical electrical characteristics are examples. The main distribution is determined by statistical tests such as plotting the data on statistical probability paper or using analytic programs. Alternately, the robust mean may be established by the median (middle data point) of the second quartile of the ranked data. The robust sigma is established by comparing the third quartile and the first quartile. Once the main distribution is established the mean and standard deviation of this main distribution can be used to remove outliers (more than six sigma deviation from the mean or median of the main population).

AEC Test Method Q002 (Guidelines for Statistical Yield Analysis) identifies a wafer, wafer lot, or assembly lot that exhibits an unusually low yield or an unusually high bin failure rate. Experience has shown that wafer and assembly lots exhibiting these abnormal characteristics tend to have generally poor quality and can result in significant system reliability problems. The method is to collect data from at least six lots and characterize the nature of the statistical distribution for yield (good die per wafer) and for all critical failed bin units, as determined between the supplier and customer. If these distributions show a reasonable fit to a normal distribution, the mean and standard deviation are computed. Generally six months of production data and is repeated every two diffusion lots, or about every 30 days. If the distribution is not normal, the data may be transformed so that a normal distribution is applicable, or the data is fitted to another suitable distribution (Weibull, Gamma, Poisson, etc.). Upper and lower limits such as mean plus and minus, 3 sigma, and mean plus and minus 4 sigma are computed to show that the product is under acceptable statistical control.

The issue of lead-free lead plating (often pure tin or 100% matte tin) impacts various parts of many commodities used in automotive applications. Qualification and usage of these parts is discussed here for any affected commodities. AEC criteria are developed in AEC-Q005, Pb-Free Test Requirements. The purpose of this specification is to determine that a component is capable of passing the specified stress tests and thus can be expected to give a certain level of quality/reliability in the application. The science of whisker growth, including growth models and accelerated test methods, was not fully understood at the time of release of this standard. Further, the existence of tin whiskers over time does not ensure component or system failure. The environmental tests specified in this document for whisker growth evaluation require conditions of temperature, humidity and temperature cycling that are currently believed to best exacerbate whisker growth in Sn-plated leads and terminations. The user and supplier need to consider the applicable risks when using components with Sn-plated leads in sensitive applications. Tests in this specification include:

1. Solderability: Precondition the samples according to Table 3.3-1.

**Table 3.3-1.** Preconditioning requirements.

| Condition | Precondition Type | Exposure Time | Lead Finish Material |
|---|---|---|---|
| A | Steam precondition | 1 hr ± 5 min | Non-tin and non-tin alloy |
| C | | 8 hr ± 15 min | Tin and tin alloy |
| E* | 150°C dry bake | 16 hr ± 30 min | Alternative to steam precondition |

Either use the solderability dip and look method or the solderability surface mount process simulation method (per JESD22-B102 Methods 1 or 2, as applicable). A wetting balance solderability test is not required.

2. Resistance to solder heat: Perform using either the through-hole or small surface mount devices test of JESD22-B106, using lead-free solder. Soldering is performed at a higher temperature than the previously used lead tin solders.
3. Tin whisker acceptance testing: Perform in accordance with JEDEC JESD201A, Environmental Acceptance Requirements for Tin Whisker Susceptibility of Tin and Tin Alloy Surface Finishes.

The JESD201A standard is now delineated. This document is more general purpose than required by automotive applications.

Table 3.3-2 is used to determine if an acceptance characterization is needed.

Table 3.3-2. Tin and tin alloy surface finish acceptance test matrix.

| Technology or Manufacturing Process Parameter | Examples | Qual Type[1] | Acceptance Tests Req'd | | |
|---|---|---|---|---|---|
| | | | TC[2] | T & H | High/ T & H |
| **Base Metal** | | | | | |
| Base Metal Alloy[5] | Base metal, e.g., Cu alloy, FeNi42 | T | x | x | x |
| Base Metal Vendor[4] | Supplier A vs. B, same metal | S | - | - | - |
| Leadframe type | Etch vs Stamped | P | x | x | x |
| **Surface Finish Composition** | | | | | |
| Surface Finish Alloy | Sn, SnAg3.5, SnBi2-4, SnBi5-7, SnCu1, SnCu3 | T | x | x | x |
| Surface Finish Thickness | Change in thickness limits | T | x | x | x |
| Underplate Composition | Change in underplate composition | T | x | x | x |
| Underplate Thickness | Change in thickness limits | T | x | x | x |
| **Surface Finish Chemistry or Process** | | | | | |
| Surface Finish Plating Process | In-line vs. Rack vs Barrel, Bright vs. Matte tin [7] | T | x | x | x |
| Underplate Process | Change in underplate process | T | x | x | x |
| Process Chemistry | MSA, Mixed acid, etc. | T | x | x | x |
| Plating Bath Vendor | Supplier A vs. B | T | x | x | x |
| Major Plating Process Window Limits | Change beyond process window limits for additive levels, metal content, acid content, current density, temperature, impurity levels | T | x | x | x |
| Minor Plating Process Window Limits | Change within process window limits for additive levels, metal content, acid content, current density, temperature, impurity levels | S | - | - | - |
| Dip Process | Change of flux, impurity levels, immersion rate, cooling rate, etc. | T | x | x | x |
| Post Bake Process | Change in bake process parameters | T | x | x | x |
| **Assembly Process and Component Style** | | | | | |
| Lead Form | J-lead vs. gull wing | S | - | - | - |
| Lead Count | Different lead count | S | - | - | - |
| Lead Dimension | e.g., 0.25 mm wide, 0.18 mm wide | S | - | - | - |
| **Factory or Plating Process[3]** | | | | | |
| Startup New Factory | New Factory | P[6]<br>T | x<br>x | x<br>x | x<br>x |
| New Plating Line (Duplicate) | Accepted Technology/Factory/Vendor | S | - | - | - |
| New Plating Equipment | New plating line, vendor, or relocation of a line | P | x | x | x |

Surface finish acceptance test sample size is 3 lots per stress and 2 samples per lot. Temperature cycling, Temperature/Humidity Storage and High Temperature/Humidity Storage tests are all performed. Three samples per lot are used for four or less leaded parts.

Devices are placed into one of four classes based on intended applications:

- Class 3: Mission/life-critical applications such as military, aerospace and medical—Pure tin and high tin content alloys not typically acceptable
- Class 2: Business-critical applications such as telecom, high-end servers, automotive—Breaking off of a tin whisker is a concern
- Class 1: Industrial/consumer products—No major concern with tin whiskers breaking off
- Class 1A: Consumer products—Minimal concern with tin whiskers

Test flow consists of:

1. Pre-condition per JESD22A121 (similar to pre-condition for reliability testing).
2. Temperature cycling of –55°C to 85°C air to air for 3 cycles per hour and –40°C to 85°C air to air for 3 cycles per hour with an inspection every 500 cycles.
    a. For Class 1 and 2 products; 1500 cycles are required
    b. For Class 1A products; 1000 cycles.
3. Temperature humidity/storage test condition at 30°C and 60%RH with inspection every 1000 hours.
    a. Total of 4000 hours is required for Classes 1 and 2
    b. Total of 1000 hours for Class1A.
4. High temperature/humidity storage test condition of 55°C and 85%RH with inspection intervals every 1000 hours.
    a. Total of 4000 hours is required for Class 1 and 2
    b. Total of 1000 hours for Class 1A.

Acceptance criteria is by visual inspection (optical) with an allowable whisker length as indicated here:

- For Class 2: 40 micrometers during inspections after temperature/humidity storage and high temperature/humidity storage stressing; 45 micrometers after temperature cycling stress
- For Class 1: 67 micrometers for most components; 50 micrometers for high-frequency components; 100 micrometers for components with a minimum lead-to-lead gap greater than 320 micrometers
- For Class 2: 50 micrometers during inspections after temperature cycling and high temperature/humidity storage stressing; 20 micrometers after temperature/humidity storage; 75 micrometers for components with minimum lead-to-lead gap greater than 320 micrometers

The main tool for qualification of integrated circuits for high-reliability applications such as automotive is AEC-Q100 (Failure Mechanism Based Stress Test Qualification for Integrate Circuits). Since the battery of tests is very extensive and the sample sizes and number of lots required are very large, the concept of generic data to simplify the qualification test is encouraged. A qualification family for these purposes must have the same fab process (e.g., CMOS, NMOS, Bipolar, etc.) and such elements as feature size, substrate, numbers of masks, lithographic process, doping process, gate structure, polysilicon material, oxidation process, interlayer dielectric material and thickness range, metallization material and thickness range, passive material and thickness range, and die backside preparation process and metallization. The assembly process (plastic or ceramic) must share the same major process or material, including package type (DIP, SOIC, PLCC, PBGA, etc.) cross section dimensions, range of paddle (flag) size, substrate base material, leadframe base material, leadframe plating, die attach material, wire bond material, wire diameters plastic mold compound, heatsink type, etc.

The tests used to qualify integrated circuits are capable of simulating and precipitating semiconductor device and package failures in an accelerated manner compared to use conditions. Each test is designed for a particular set of failure mechanisms and may need to be revised for potential new and unique failure mechanisms. Any situation where conditions may induce failures in a particular application (including

extreme use) may be used to formulate a new test. Tests are organized in groups A through G. Not all tests are applicable to all integrated circuits.

Test Group A consists of accelerated environment stress tests. The reference standards (details of how the tests are performed) are the JEDEC JESD22** standards. In general, for surface mount devices, a pre-condition test per JEDEC J-STD_020 (JESD22-A113) is performed to simulate board-soldering process). This is done on all Group A devices. Temperature Humidity Bias or Biased HAST per JESD/22A-101 or A110, Autoclave or unbiased HAST, Temperature Cycling (JESD22-A104) (typically 500 cycles with various temperature ranges determined by the grade of part), Power temperature cycle (JESD22-A105), and High Temperature Storage Life (JESD22-A103) are done on all applicable devices). The sample size for all tests except Power Temperature Cycle and High Temperature Storage life are 3 lots of at least 77 devices per lot. The latter two tests are done with 45 parts of one lot.

Test Group B consists of accelerated lifetime simulation tests. These consist of High Temperature Operating Life test (JESD22-A108) (typically 408 hours at temperatures from 150°C to 90°C (depending on the device class) for 1000 hours); Early Life Failure rate per AEC Q100-008) on at least 3 lots of at least 800 parts per lot and Non-Volatile Memory endurance, data retention and operational life according to AEC Q100-005. The first and third tests are done on a sample size of 3 lots or more and at least 77 parts per lot.

Test Group C consists of package assembly integrity tests including Wire bond shear and wire bond pull (statistical acceptance criteria—Cpk or Ppk limits), Solderability, Physical Dimensions, Solder Ball shear, and lead integrity. Sample sizes vary depending on the test but are generally small unless necessary for the statistical success criteria.

Test Group D are die fabrication reliability tests. The intent is that these are tests performed by the part manufacturer for the industry in general. Sample size, success criteria, number of lots and test method are dependent on the part manufacturer's internal procedures but are reviewed by the AEC using membership. Among the tests are Electro-migration, Time-Dependent Dielectric Breakdown, Hot Carrier Injection, Negative Bias Temperature Instability, and Stress Migration.

Test Group E are electrical verification tests. These include the electrical tests performed in order tests in the various sequences of qualification testing before and after a stress condition. Other electrical tests include ESD tests (Human Body and Charged Device Model), Latchup, Electrical distributions, Fault Grading, Electro-thermally Induced Gate Leakage, Electromagnetic Compatibility, and Soft Error Rate. These tests are typically performed on one lot with smallish sample sizes. The exception is electrical distributions, which is performed on 3 lots of with a minimum 30 pieces per lot. Various AEC standards govern the details of the procedure/testing.

Test Group F consists of defect screening tests. These include Process Average Testing (PAT, see previous discussion) and Statistical Bin/Yield Analysis.

Test Group G consists of cavity package integrity tests. These include Mechanical Shock, Variable Frequency Vibration, Constant Acceleration, Gross/Fine Leak, Package Drop, Lid Torque, Die Shear, and Internal Water Vapor. The sample size for the stress tests is typically 3 lots of at least 39 parts per lot. The last four tests are done on 1 lot of 5 pieces.

The table below gives the process change criteria from the AEC. This gives insight into those tests that should be repeated as process changes are accomplished by the part manufacturer. It also gives insight into which tests are considered important for which automotive technologies.

Table 3.3-3. Process change qualification guidelines for the selection of tests.

**AEC - Q100 - REV-G**
**May 14, 2007**

**Automotive Electronics Council**
**Component Technical Committee**

## Table 3: Process Change Qualification Guidelines for the Selection of Tests

A2 Temperature Humidity Bias or HAST
A3 Autoclave or Unbiased HAST
A4 Temperature Cycling
A5 Power Temperature Cycling
A6 High Temperature Storage Life
B1 High Temperature Operating Life
B2 Early Life Failure Rate
B3 NVM Endurance, Data Retention
C1 Wire Bond Shear
C2 Wire Bond Pull
C3 Solderability
C4 Physical Dimensions
C5 Solder Ball Shear
C6 Lead Integrity
D1 Electromigration
D2 Time Dependent Dielectric Breakdown
D3 Hot Carrier Injection
D4 Negative Bias Temperature Instability
D5 Stress Migration
E2 Human Body / Machine Model ESD
E3 Charged Device Model ESD
E4 Latch-up
E5 Electrical Distribution
E7 Characterization
E8 Gate Leakage
E9 Electromagnetic Compatibility
E10 Short Circuit Characterization
E11 Soft Error Rate
G1-4 Mechanical Series
G5 Package Drop
G6 Lid Torque
G7 Die Shear
G8 Internal Water Vapor

**Note:** A letter or "•" indicates that performance of that stress test should be **considered** for the appropriate process change

| **Table 2 Test #** | A2 | A3 | A4 | A5 | A6 | B1 | B2 | B3 | C1 | C2 | C3 | C4 | C5 | C6 | D1 | D2 | D3 | D4 | D5 | E2 | E3 | E4 | E5 | E7 | E8 | E9 | E10 | E11 | G1-G4 | G5 | G6 | G7 | G8 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Test Abbreviation** | THB | AC | TC | PTC | HTSL | HTOL | ELFR | EDR | WBS | WBP | SD | PD | SBS | LI | EM | TDDB | HCI | NBTI | SM | HBM / MM | CDM | LU | ED | CHAR | GL | EMC | SC | SER | MECH | DROP | LT | DS | IWV |
| **DESIGN** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Active Element Design | | • | • | M | | • | • | DJ | | | | | | | D | D | D | D | D | • | • | • | • | • | S | • | • | • | | F | | | |
| Circuit Rerouting | | | A | M | | | | | | | | | | | | | | | | • | • | • | • | • | S | • | • | | | | | | |
| Wafer Dimension / Thickness | | | E | M | | • | • | | E | E | | | | | | | | • | | E | E | E | • | | | | | | | | | | |
| **WAFER FAB** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Lithography | • | | • | M | | • | G | | • | • | | | | | | | | • | | | | | • | | | | | | | | | | |
| Die Shrink | • | • | | M | | • | • | DJ | | | | | | | • | • | • | • | • | • | • | • | • | • | S | • | • | • | | | | | |
| Diffusion/Doping | | | | M | | • | G | | | | | | | | | | | • | | • | • | • | • | • | S | | | | | | | | |
| Polysilicon | | | • | M | | • | | DJ | | | | | | | | | | • | | • | • | • | • | • | S | | | | | | | | |
| Metallization / Vias / Contacts | • | • | • | M | | • | | | • | • | | | | | • | | | | • | | | | • | • | S | | • | | | | | | |
| Passivation / Oxide / Interlevel Dielectric | K | K | • | M | | • | GN | DJ | K | • | | | | | | • | • | • | • | • | • | • | • | • | PS | | | | | | | | |
| Backside Operation | | | • | M | | • | | | | | | | | | | | | | | M | M | • | | • | | | | | H | | | H | |
| FAB Site Transfer | • | • | • | M | | • | • | J | • | • | | | | | • | • | • | • | • | • | • | • | • | | S | | | | H | | | H | |
| **ASSEMBLY** | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Die Overcoat / Underfill | • | • | • | M | • | • | | | | | | | | | | | | | | | | | | | S | | | • | | | | | H |
| Leadframe Plating | • | • | • | M | • | | | | | C | • | | | • | | | | | | | | | | | | | | | | | | H | |
| Bump Material / Metal System | • | • | • | M | • | • | | | | | | • | • | | | | | | | | | | | | | | | • | | | | | |
| Leadframe Material | | • | • | M | • | | | | | • | • | • | | • | | | | | | | | | | | | | • | | H | | | H | |
| Leadframe Dimension | | • | • | M | | | | | | | • | • | | • | | | | | | | | | | | | | • | | H | | | | |
| Wire Bonding | | • | • | Q | • | | | | • | • | | | | | | | | | | | | | M | | | | • | | H | | | | |
| Die Scribe/Separate | • | • | • | M | | | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Die Preparation / Clean | • | • | | M | | • | | | • | • | | | | | | | | | | | | | | | | | | | | | | H | |
| Package Marking | | | | | | | | | | | B | | | | | | | | | | | | | | | | | | | | | | |
| Die Attach | • | • | • | M | | • | | | | | | | | | | | | | | | | | • | | | | • | | H | | | H | H |
| Molding Compound | • | • | • | M | • | • | • | | | | • | • | | • | | | | | | | | | | | S | | | • | | | | | |
| Molding Process | • | • | • | M | • | • | | | | | • | • | | • | | | | | | | | | | | S | | | | | | | | |
| Hermetic Sealing | | H | H | | H | | | | | | | H | | H | | | | | | | | | | | | | | | H | | H | | H |
| New Package | • | • | • | M | • | • | • | | • | • | • | • | T | • | | | | | | • | • | | • | | S | | • | | H | | | H | H |
| Substrate / Interposer | • | • | • | M | • | • | | | • | • | | | T | | | | | | | | | | | | S | | | | H | | | H | H |
| Assembly Site Transfer | • | • | • | M | | • | • | | • | • | • | • | T | • | | | | | | | | | • | | S | | | | H | | | H | H |

A Only for peripheral routing
B For symbol rework, new cure time, temp
C If bond to leadfinger
D Design rule change
E Thickness only
F MEMS element only
G Only from non-100% burned-in parts
H Hermetic only
J EPROM or $E^2$PROM
K Passivation only
M For devices requiring PTC
N Passivation and gate oxide
P Passivation and interlevel dielectric
Q Wire diameter decrease
S For plastic SMD only
T For Solder Ball SMD only

The attachments to AEC Q100 delineate the test methods for the strength to stress measurements, such as ESD measurements, and are similar to those from MIL-STD-883. The following discusses test methods unique to the AEC standards.

The electro-thermally induced gate leakage test (AEC Q100-006) investigates the phenomena of some devices (usually CMOS) where the gate leakage changes if 400 volts is applied to a base plate (devices resting on the base plate). A failure criterion is the device not performing to either data sheet or procurement specifications. This condition frequently occurs in automotive applications.

Fault simulation and fault grading (AEC-Q100-007) is an evaluation and acceptance method and applies to digital devices or the digital portion of mixed signal devices. This test method considers the following types of faults: blocked (propagation path to observed node is blocked), collapsed (single stuck at fault for each fault equivalent grouping), redundant, tied, untestable, stuck at, and detected. Fault grading and test coverage follow the industry standard definitions. Statistical sampling of modeled faults is not allowed. Success criteria:

- Analog circuits or analog circuit block of mixed mode circuits – 100% specification coverage
- Digital circuits or digital portion of mixed mode circuits – stuck at test coverage must be greater than or equal to 98%
- Digital circuits or digital portion of mixed mode circuits with IDDQ or ISSQ – the stuck at coverage of the production test set to be used for all parts delivered for production must be greater than or equal to 97% test coverage

Early life failure rate test (AEC-Q100-008) is an evaluation of early life failure characteristics on parts that are utilizing new or unproven processing technology or design rules, where generic is not available. In general, generic data on existing technology is strongly preferred. Unsatisfactory results indicate that corrective action is required and the parts may require processing changes, design changes, burn-in, more aggressive burn-in or application of statistical part test limits (AEC-Q001). Sample size shall be 3 lots of at least 77 parts in each lot. The parts shall be tested per the high temperature operating life test (JESD22-A108) for 48 hours at the appropriate test temperature (70°C to 150°C), dependent on device grade. Meeting all acceptance criteria and no failures is the success criteria.

Electrical distribution assessment (AEC-Q100-009) evaluates the ability of a part to function within the specification parameters over normal process variations, time, and/or anticipated application environment (operating temperature range, voltage, etc.). Parametric drift is the change of an electrical parameter from the original value or in the statistical distribution of a group of devices. Guard bands at both the lower and upper test limits are considered. For this test method generic data is not allowed. Evaluation summary includes significant or critical parameters reviewed, sample size, the metrics used (Cpk, degree of drift, etc.), temperatures assessed, as well as minimum and maximum operating frequencies.

The main tool for qualification of discrete semiconductors (e.g., transistors and diodes) for high-reliability applications such as automotive applications is stress test qualification for automotive grade discrete semiconductors (AEC-Q101). Since the battery of tests is very extensive and the sample sizes and number of lots required are very large, the concept of generic data to simplify the qualification test is encouraged. A qualification family for these purposes must have the same fabrication process (power MOS, power bipolar, small signal bipolar, Schottky rectifier, transient voltage suppressor, Zener, etc.). More than one device may be qualified and data may be combined, provided it fits a 3-year window. A wafer fab process must have the same attributes, including process flow, layout design rules, doping material, number of masks, cell density where applicable, lithographic process (e.g., contact vs. projection, photoresist polarity), coping process (e.g., diffusion vs. ion implantation) passivation/glassivation material and thickness range, oxidation process and thickness range, font/back metallization material, thickness range and number of levels. The same wafer site is also required.

Qualification family must also include the same package type and assembly process, including leadframe base material, leadframe plating, die attach material and method, wire bond material (wire diameter and process) and plastic mold compound or other encapsulation material. The same assembly site is also required.

For each qualification, the supplier must present data for *all* of these tests, whether it is stress test results on the specific device or acceptable generic family data. A review is made of other parts in the same generic family to ensure that there are no common failure mechanisms. Passing the stress test requires zero failures.

Not all tests apply to all devices. Device-specific tests do not allow family data and include electrostatic discharge characterization and parametric verification.

Test methods are mostly governed by JESD22 test procedures. Sample size for most die stress tests is 77 parts of one lot. Package stress test sample size is mostly 30 pieces of one lot. DPA is required on two parts of one lot. Pre- and post-stress electrical test is required per supplier's standard specification (data sheet) (at all temperatures on the specification). Pre-conditioning per JESD22 method A-113 is required on all surface mount devices prior to temperature cycling, autoclave, high temperature high humidity reverse bias test, and intermittent operational life and power and temperature cycling tests only.

The following are the chief stress tests (not applicable to all device types):

- External visual (all qualification parts)
- Parametric verification (25 devices per lot)
- High temperature reverse bias (HTRB): 1000 hours at 150°C junction temperature or specified maximum junction temperature with device reverse biased to 80% of the maximum breakdown voltage specification

The following tests when applicable are performed on 77 devices in one lot.

- High temperature gate bias (HTBG): 1000 hours at 150°C junction temperature or specified maximum junction temperature with gate biased to 100% of maximum gate voltage rating, with the device biased OFF
- Temperature cycling (TC): 1000 cycles with a minimum range of –55°C to maximum rated junction temperature, not to exceed 150°C
- Autoclave (AC): 96 hours with ambient temperature 121°C, 100% relative humidity and 15 psig pressure
- High humidity high temperature, reverse bias (H3TRB): 1000 hours at ambient temperature of 85°C and 85% relative humidity with device reverse biased at 80% of rated breakdown voltage, up to a maximum of 100V or limit of chamber
- HAST: 90 hours at ambient temperature of 130°C and 85% relative humidity with device reverse biased to 80% of rated voltage, up to a voltage above which arcing in the chamber is likely to occur (typically 42 volts)
- Intermittent operational life (IOL): Devices powered to ensure delta junction temperature is more than 100°C but not to exceed absolute maximum ratings
- Power and temperature cycles (PTC): This test is performed if a delta junction temperature of more than 100°C is not achievable

The following tests are performed on 30 parts in one lot or as indicated.

- ESD characterization on 30 parts with at least two of the referenced ESD models or CDM after 2006.
- DPA performed on two parts in one lot and on random samples from devices successfully completing H3TRB or HAST, and TC
- Physical dimension (PD)

- Terminal strength (TS): Per MIL-STD-750 Method 2036
- Resistance to solvents (RTS)
- Constant acceleration (CA): Y1 plane only, 15 KG
- Vibration variable frequency (VVF)
- Mechanical shock (MS): 1500 g's for 0.5 mS, 5 blows, 3 orientations
- Hermeticity (HER): Fine and gross leak test per user specification
- Resistance to solder heat (RSH): SMD devices shall be fully submerged during test
- Solderability (SD): Per J-STD-002, 10 parts per lot
- Thermal resistance (TR): 10 parts per lot
- Wire bond strength (WBS): 10 bonds from a minimum of 5 devices per MIL-STD-750 Method 2037
- Bond shear (BS): 10 bonds from a minimum of 5 devices
- Die shear (DS): 5 parts per lot per MIL-STD-750 Method 2017
- Unclamped inductive switching (UIS): 5 parts per lot per AEC-Q101-004 section 2
- Dielectric integrity (DI): 5 parts per AEC-Q101-004, section 3

The following additional conditions apply:

**Table 3.3-4.** Intermittent operational life (Test 10) or power temp cycling (Item 10alt) timing requirements.

| Package Type | Number of Cycles Required, **$\Delta T_J \geq 125°C$** | Number of Cycles Required, **$\Delta T_J \geq 125°C$** | Time per Cycle |
|---|---|---|---|
| Small (e.g., SMD SOTS through D-pak and all LEDs) | 15,000 | 7,500 | 2 minutes on/2 minutes off |
| Medium (e.g., TO-220, D2-pak) | 8,572 | 4,286 | 3.5 minutes on/3.5 minutes off |
| Large (e.g., TO-3, TO-247) | 6,000 | 3,000 | 5 minutes on/5 minutes off |
| Leadless<br>Not to Exceed | 60,000/(x+y)<br>15,000 cycles | 30,000/(x+y)<br>7,500 cycles | Fastest capable (min 2 minutes on/off<br>x minutes on plus y minutes off |

*Example 1: A package capable of 2 minutes on/4 minutes off would require 10,000 cycles [60,000/(2+4)] at $\Delta T_J \geq 100°C$ or 5,000 cycles at $\Delta T_J \geq 125°C$.*

*Example 2: A package capable of 1 minute on/1 minute off would require 15,000 cycles at $\Delta T_J \geq 100°C$ or 7,500 cycles at $\Delta T_J \geq 125°C$.*

**Table 3.3-5.** Solder conditions table (Test 21) requirements.

| Type | Test Method | Solder Temperature | Steam Age Category | Exception for Dry Heat |
|---|---|---|---|---|
| Leaded Through-hole | A | 235°C | 3 | — |
| SMD Standard Process | B | 235°C | 3 | — |
| SMD Low Temperature Solder | B | 215°C | — | 4 hr@155°C<br>(in lieu of steam age) |
| SMD Dissolution of Metals Test | D | 260°C | 3 | — |

The following table gives the process change criteria from the AEC. This gives insight into those tests that should be repeated as process changes are made by the part manufacturer. It also gives insight into which tests are considered important for which technologies for automotive applications:

**Table 3.3-6.** Process change guidelines for the selection of tests.

Note: A letter or "•" indicates that performance of that stress test should be <u>considered</u> for the appropriate process change

| Table 2 Test # / Test Name / Change | 3 External Visual | 4 Parametric Verification | 5 High Temp. Rev. Bias | 6 High Temp. Gate Bias | 7 Temperature Cycle | 8 Autoclave | 9 H3TRB | 9 alt High. Accel. Stress Test | 10/ alt Intermittent Oper. Life | 11 ESD Characterization | 12 Destruct. Phy. Analysis | 13 Physical Dimensions | 14 Terminal Strength | 15 Resistance to Solvents | 16 Constant Acceleration | 17 Vibration | 18 Mechanical Shock | 19 Hermeticity | 20 Resist. to Solder Heat | 21 Solderability | 22 Thermal Resistance | 23 Wire Bond Strength | 24 Wire Bond Shear | 25 Die Shear | 26 Unclamp.Induct.Switch | 27 Dielectric Integrity | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **DESIGN** | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Wafer Thickness | | • | • | | • | | | | • | | • | | | | | | | | x | | • | • | • | | | | F |
| **Wafer Diameter** | | • | • | • | | | | | | | | | | | | | | | | | | | | | | | |
| Die Size | | • | • | | • | | | | • | E | • | | | | | | | | • | | • | | | • | M | | F |
| Layout | | • | • | • | 3 | | | | • | E | 3 | | | | | | | | | | | | | | M | | |
| Field Termination | | • | • | | • | • | • | • | | E | • | | | | | | | | | | | | | | M | | |
| **WAFER FAB** | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Wafer Source | | • | • | | | | • | • | • | | | | | | | | | | | | • | | | | 9,M | | R |
| Lithography | | • | 4 | 4 | | | 6,7 | 6,7 | | | | | | | | | | | | | | 1 | | | | | P |
| Diffusion | | • | 5,6 | 5 | | 6 | 6 | 6 | | • | 6 | | | | | | | | | | | | | | M | | PR |
| Doping Profile/**Schottky Barrier** | | • | 5,0 | | | | | | | • | | | | | | | | | | | | | | | M | | R |
| Ion Implantation | | • | 5,6 | • | | 6 | 6 | 6 | | • | 6 | | | | | | | | | | | | | | M | | PR |
| Polysilicon | | • | • | • | • | | | | | E | • | | | | | | | | | | | | | | M | • | P |
| Metallization (Top side) | | • | 8 | | • | • | • | • | • | E | • | | | | | | | | • | | | • | • | | | | |
| Metallization (Back side) | | • | | | • | | • | • | • | | | | | | | | | | • | | • | | | • | | | |
| Passivation/Glassivation | | • | • | • | • | • | • | • | • | • | • | | | | | | | | | | | • | | | | | |
| Oxide | | • | | • | 7 | 6 | 6 | 6 | • | E | 6,7 | | | | | | | | | | | | | | | • | |
| Epitaxic Growth | | • | • | | | | | | | | | | | | | | | | | | | | | | M | | R |
| Etch | | • | 6 | 4 | | 6,7 | 6,7 | 6,7 | | | 6,7 | | | | | | | | | | | 1,7 | | | 8,M | 4 | |
| Backside Operation | | • | | | • | • | • | • | • | | | | | | | | | | • | | • | | | • | | | A |
| Fab Site Transfer | | • | • | • | • | • | • | • | • | E | • | | | | | | | | | | • | • | • | • | M | • | AIPRS |
| **ASSEMBLY** | | | | | | | | | | | | | | | | | | | | | | | | | | | |
| Die Overcoat | | | • | • | • | • | • | • | • | | • | | | | | | | H | | | | • | | | | | |
| Leadframe Plating/**Lead Finish** | D | | | | C | C | C | C | | | | D | | D | | | | H | | D | C | 2C | | C | | | |
| Leadframe Mat'l/Source | • | | | | • | • | • | • | • | | | • | • | | | | | H | • | • | • | 2 | | • | | | AFX |
| Package/LF Dimension | | | | | • | | • | • | • | | | • | | | | | | H | | | • | | | • | | | |
| Wire Bonding | | • | | | • | | • | • | • | | • | | | | | | | | • | | | • | • | | | | |
| Die Scribe/Separation/Saw | | • | | | • | | | | • | | | | | | | | | | | | | | | | | | |
| Die Preparation/Clean | | • | | | • | • | • | • | | | | | | | | | | | | | | • | | • | | | X |
| Die Attach | | • | | | • | • | • | • | • | | | | | | | | | H | • | | • | | | • | | | AX |
| Encapsulation Material | • | • | • | • | • | • | • | • | • | | • | • | | B | | | | H | • | • | • | | | | | • | AFG |
| Encapsulation Process | • | | • | • | • | • | • | • | • | | • | • | | B | | | | H | • | • | | | | | | | AG |
| Hermetic Sealing | H | | | | H | H | H | H | | | H | | H | | H | H | H | H | H | | | | | | | | |
| New Package | • | • | • | • | • | • | • | • | • | • | • | • | • | B | H | H | H | H | • | • | • | | | • | | • | F |
| Test Process/Sequence | | • | | | | | | | | | | | | | | | | | | | | | | | | | |
| Package Marking | | | | | | | | | | | | | | B | | | | | | | | | | | | | |
| Assembly Site Transfer | • | • | • | • | • | • | • | • | • | | • | • | • | • | | | H | H | • | • | | • | • | • | | | AGISX |

A Acoustic Microscopy
B If not laser etched
**C Only for Leadframe Plating change**
**D Only for Lead Finish change**
E If Applicable
F Finite Element Analysis
G Glass Transition Temperature

H Hermetic device only
I Infant Mortality Rate
M Power MOS/IGBT devices only
P CV Plot (MOS only)
R Spreading Resistance Profile
S Steady State Mortality Rate
X X-Ray

1 If bond pads are affected
2 Verify #2 (package) post
3 Only for changes at the periphery
4 Only for oxide etches or etches prior to oxidation
5 For source or channel region changes
6 For field termination changes

7 For passivation changes
8 For contact changes
9 For epitaxial changes
**0 Required for Schottky barrier changes.**

Only unique test methods for automotive-grade discrete semiconductors are discussed here.

Unclamped inductive switching determines the capability of a power MOSFET or IGBT to dissipate energy stores in an inductive load. Power MOSFETs have a parasitic back diode that is subjected to the

inductor stored energy when the device is turned off (if no external clamp is used). This test determines the ruggedness of the IGBTs with a clamp incorporated within its package. The DUT (MOSFET) has a specified power inductor as load and has a specified (step rising) voltage bypassed by a large capacitance (5700 microfarads). The MOSFET gate is connected to a pulse generator to provide a single pulse with the signal level at the maximum rated gate to source voltage. The gate is then turned on to allow current to ramp in the inductor to the specified value. The gate is then turned off and the drain voltage and current is monitored with an oscilloscope. This ensures the back diode clamps until the inductor energy is dissipated. The current is increased in steps of 1 ampere until failure. This test method is approximately similar to MIL-STD-750 test methods 3469, 3470, and 3490, but significant differences are apparent under examination.

Another test method applied by the AEC is the dielectric integrity test for MOS gated devices. In this test the drain and source are shorted and a stepped voltage is applied to the gate. The gate voltage is increased in 1 volt increments until failure.

Requirements for qualification of resistors, capacitors, relays, inductors, transformers, and switches, etc., are contained within stress test qualification for passive components (AEC-Q200).

Similar to other commodities, the main approach is to qualify the technology family with a heavy reliance on part manufacturer generic data, including process control data. Four corners data is examined (e.g., mid/low/hi C value, hi/low V for capacitors, case size for resistors and other large parts, etc.).

Passive components are grouped into five grades (0–4, with 4 being non-automotive). Each grade represents the maximum temperature range of application. Grade 0 is –50°C to +150°C; Grade 1 is –40°C to +125°C (underhood); Grade 2 is –40°C to +105°C (passenger compartment hot spots); and Grade 3 is –40°C to +85°C (most passenger compartment applications).

Qualification of a lead-free device is addressed by AEC-Q005. Qualification requirements depend on the particular commodity type and not all stresses are applicable for each commodity (Table 3.3-7).

**Table 3.3-7.** Qualification sample size requirements.

| Stress | Sample Size per Lot | Number of Lots | Acceptable Fail Number |
|---|---|---|---|
| High Temperature Exposure | 77[1] | 1 | 0 |
| Temperature Cycling | 77[1] | 1 | 0 |
| DPA | 10 | 1 | 0 |
| Moisture Resistance & Humidity Bias | 77 each test | 1 | 0 |
| High Temperature Operation Life | 77[1] | 1 | 0 |
| External Visual | All qualification parts | | |
| Physical Dimensions, Terminal Strength | 30 each test | 1 | 0 |
| Resistance to Solvents | 5 | 1 | 0 |
| Mechanical Shock | 30[1] | 1 | 0 |
| Vibration | 30[1] | 1 | 0 |
| Resistance to Solder Heat | 30 | 1 | 0 |
| Thermal Shock | 30 | 1 | 0 |
| ESD | 15 | 1 | 0 |
| Solderability | 15 each condition | 1 | 0 |
| Electrical Characterization | 30 | 3 | 0 |
| Board flex, Terminal Strength, Beam Load, Flame Retardance, Rotation Life, Surge Voltage, Salt Spray. Electrical Transient Conduction, Shear Strength, Short Circuit Fault Current Durability; as applicable | 30 each stress | 1 | 0 |
| End of Life Mode Verification | 30 | 1 | 0 |
| Jump Start Endurance | 30 | 1 | 0 |
| Load Dump Endurance | 30 | 1 | 0 |

*Note:*

1. *Where generic data (family) data is provided in lieu of part number specific data; 3 lots are required.*

**Table 3.3-8.** Test methods for tantalum and ceramic capacitors.

| Stress | Method (Reference) | Additional Requirements |
|---|---|---|
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| High Temperature Exposure (storage) | MIL-STD-202, Method 108 | Unpowered 1000 hours |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–55°c to +125°C) |
| Destructive Physical Analysis (DPA) | EIA-469 | Applies only to SMD Ceramics |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 85°C/85%RH |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at 125°C ambient; 2/3 rated voltage to tantalum capacitors; full rated voltage for ceramic capacitors |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | |
| Mechanical Shock | MIL-STD-202 Method 213 | |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | MLCCS only |
| Terminal Strength (SMD) | AEC-Q200-006 | |
| Beam Load Test | AEC-Q200-003 | Ceramics only |

**Table 3.3-9.** Test methods for aluminum electrolytic capacitors.

| Stress | Method (Reference) | Additional Requirements |
|---|---|---|
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| High Temperature Exposure (storage) | MIL-STD-202, Method 108 | Unpowered 1000 hours at max. rated operating temperature |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–40° to +105°C) |
| Destructive Physical Analysis (DPA) | EIA-469 | Applies only to SMD ceramics |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 85°C/85%RH |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at 105°C ambient temperature; rated voltage |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | |
| Mechanical Shock | MIL-STD-202 Method 213 | |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | MLCCS only |
| Terminal Strength (SMD) | AEC-Q200-006 | |
| Surge Voltage | JIS-C-5101-1 | |

**Table 3.3-10.** Test methods for film capacitors.

| Stress | Method (Reference) | Additional Requirements |
|---|---|---|
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| High Temperature Exposure (storage) | MIL-STD-202, Method 108 | Unpowered 1000 hours at max. rated operating temperature |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–55° to +85°C) |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 40°C/93%RH rated voltage |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at 85°C ambient temperature; rated voltage 1000 hours |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Moisture Resistance | MIL-STD-202 Method 106 | 24 hours per cycle |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | |
| Mechanical Shock | MIL-STD-202 Method 213 | |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | |
| Terminal Strength (SMD) | AEC-Q200-006 | |
| Flammability | UL-94 | |

**Table 3.3-11.** Test methods for magnetics (inductors/transformers).

| Stress | Method (Reference) | Additional Requirements |
|---|---|---|
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| High Temperature Exposure (storage) | MIL-STD-202, Method 108 | Unpowered 1000 hours at max. rated operating temperature |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–40°C to +125°C) |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 85°C/85%RH |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at 105°C ambient or maximum operating temperature |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | Add aqueous wash chemical |
| Mechanical Shock | MIL-STD-202 Method 213 | |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | |
| Terminal Strength (SMD) | AEC-Q200-006 | |
| Flammability | UL-94 | |

**Table 3.3-12.** Test methods for networks (R-C/C/R).

| Stress | Method (Reference) | Additional Requirements |
|---|---|---|
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| High Temperature Exposure (storage) | MIL-STD-202, Method 108 | Unpowered 1000 hours at max. rated operating temperature |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–55°C to +125°C) |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 85°C/85%RH rated voltage for capacitor networks; 10% rated power for resistor networks |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at 85°C ambient or maximum operating temperature and at rated voltage |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | Add aqueous wash chemical |
| Mechanical Shock | MIL-STD-202 Method 213 | |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | |
| Terminal Strength (SMD) | AEC-Q200-006 | |
| Flammability | UL-94 | |
| Salt Spray | MIL-STD-202 Method 101 | Test condition B |

**Table 3.3-13.** Test methods for resistors.

| Stress | Method (Reference) | Additional Requirements |
|---|---|---|
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| High Temperature Exposure (storage) | MIL-STD-202, Method 108 | Unpowered 1000 hours at 125°C |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–55°C to +125°C) |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 85°C/85%RH at 10% rated power |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at 125°C ambient temperature at rated power |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | Add aqueous wash chemical |
| Mechanical Shock | MIL-STD-202 Method 213 | Condition C |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | Condition B |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | |
| Terminal Strength (SMD) | AEC-Q200-006 | |
| Flame Retardance | AEC-Q200-006 | |

**Table 3.3-14.** Test methods for thermistors.

| Stress | Method (Reference) | Additional Requirements |
| --- | --- | --- |
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| High Temperature Exposure (storage) | MIL-STD-202, Method 108 | Unpowered 1000 hours at rated operating temperature |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–55°C to +125°C) |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 85°C/85%RH at 10% rated power |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at 125°C ambient temperature at rated power |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | Add aqueous wash chemical |
| Mechanical Shock | MIL-STD-202 Method 213 | Condition C |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | Condition B |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | |
| Terminal Strength (SMD) | AEC-Q200-006 | |
| Flammability | UL-94 | |

**Table 3.3-15.** Test methods for trimmer capacitors and resistors.

| Stress | Method (Reference) | Additional Requirements |
|---|---|---|
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| High Temperature Exposure (storage) | MIL-STD-202, Method 108 | Unpowered 1000 hours at rated operating temperature |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–55°C to +85°C) |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 85°C/85%RH at 10% rated power for resistor trimmers and rated voltage for trimmer capacitors |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at 85°C ambient temperature at rated power or voltage as applicable |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | Add aqueous wash chemical |
| Mechanical Shock | MIL-STD-202 Method 213 | Condition C |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | Condition B |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | |
| Terminal Strength (SMD) | AEC-Q200-006 | |
| Flammability | UL-94 | |
| Rotation Life | MIL-STD-202 Method 206 | Condition A |

**Table 3.3-16.** Test methods for varistors.

| Stress | Method (Reference) | Additional Requirements |
|---|---|---|
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| High Temperature Exposure (storage) | MIL-STD-202, Method 108 | Unpowered 1000 hours at 150°C |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–40°C to +125°C) |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 85°C/85%RH bias at 85% of rated varistor voltage |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at 125°C ambient temperature at rated power or voltage as applicable |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | Add aqueous wash chemical |
| Mechanical Shock | MIL-STD-202 Method 213 | Condition C |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | Condition B |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | |
| Terminal Strength (SMD) | AEC-Q200-006 | |
| Flammability | UL-94 | |
| Electrical Transient Conduction | ISO-7637-1 | Test pulses 1 to 3 |

**Table 3.3-17.** Test methods for quartz crystals.

| Stress | Method (Reference) | Additional Requirements |
|---|---|---|
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| High Temperature Exposure (storage) | MIL-STD-202, Method 108 | Unpowered 1000 hours at max. operating temperature |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–40°C to +125°C) |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 85°C/85%RH with rated Vdd applied with 1 megohm and inverter in parallel |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at 125°C with rated Vdd applied with 1 megohm and inverter in parallel |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | Add aqueous wash chemical |
| Mechanical Shock | MIL-STD-202 Method 213 | Condition C |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | Condition B |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | |
| Terminal Strength (SMD) | AEC-Q200-006 | |
| Flammability | UL-94 | |

**Table 3.3-18.** Test methods for ceramic resonators.

| Stress | Method (Reference) | Additional Requirements |
|---|---|---|
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| High Temperature Exposure (storage) | MIL-STD-202, Method 108 | Unpowered 1000 hours at max. operating temperature |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–55°C to +85°C) |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 85°C/85%RH with rated Vdd applied with 1 megohm and inverter in parallel |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at 125°C with rated Vdd applied with 1 megohm and inverter in parallel |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | Add aqueous wash chemical |
| Mechanical Shock | MIL-STD-202 Method 213 | Condition C |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | Condition B |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | |
| Terminal Strength (SMD) | AEC-Q200-006 | |

**Table 3.3-19.** Test methods for ferrite EMI suppressors and filters.

| Stress | Method (Reference) | Additional Requirements |
|---|---|---|
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| High Temperature Exposure (storage) | MIL-STD-202, Method 108 | Unpowered 1000 hours at max. operating temperature |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–55°C to +85°C) |
| Destructive Physical Analysis | EIA-469 | |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 85°C/85%RH with max. rated voltage and current |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at 85°C with rated load current |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | Add aqueous wash chemical |
| Mechanical Shock | MIL-STD-202 Method 213 | Condition C |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | Condition B |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | |
| Terminal Strength (SMD) | AEC-Q200-006 | |
| Flammability | UL-94 | |
| Electrical Transient Conduction | ISO-7637-1 | Test pulses 1 to 3 |
| Shear Strength | AEC-Q200-004 | |

**Table 3.3-20.** Test methods for polymeric resettable fuses.

| Stress | Method Reference | Additional Requirements |
|---|---|---|
| Pre and Post Stress Electrical Test | | Room temperature except as specified |
| Temperature Cycling | JESD22 Method 104 | 1000 cycles (–40°C to +125°C) |
| Biased Humidity | MIL-STD-202 Method 103 | 1000 hours 85°C/85%RH with max. rated voltage and current |
| Operational Life | MIL-STD-202 Method 108 | Steady state life at +125°C |
| External Visual | MIL-STD-883 Method 2009 | |
| Physical Dimension | JESD22 Method 100 | |
| Terminal Strength (leaded) | MIL-STD-202 Method 211 | |
| Resistance to Solvents | MIL-STD-202 Method 215 | Add aqueous wash chemical |
| Mechanical Shock | MIL-STD-202 Method 213 | Condition C for leaded devices; Condition F for SMD |
| Vibration | MIL-STD-202 Method 204 | 5 g's for 20 minutes; 12 cycles at each of 3 orientations |
| Resistance to Soldering Heat | MIL-STD-202 Method 210 | Condition B |
| Thermal Shock | MIL-STD-202 Method 107 | 300 cycles (–40°C to +125°C); max. transfer time is 20 seconds and dwell time is 15 minutes; air to air cycling |
| ESD | | |
| Solderability | J-STD-002 | Magnification 50X |
| Electrical Characterization | | Parametrically test per lot to show min., max., mean and standard deviation at room and min. and max. operating temperatures |
| Board Flex | AEC-Q200-005 | |
| Terminal Strength (SMD) | AEC-Q200-006 | |
| Flammability | UL-94 | |
| Short Circuit Fault Current Durability | AEC-Q200-004 | |
| Fault Current Durability | AEC-Q200-004 | |
| End of Life Mode Verification | AEC-Q200-004 | |
| Jump Start Endurance | AEC-Q200-004 | |
| Load Dump Endurance | AEC-Q200-004 | |

## 3.4 Definition of a Qualification Family

Capacitor Technology

- Aluminum electrolytic
- Tantalum
- Ceramic
- Film
- Trimmers

Resistor Technology

- Thin Film
- Thick Film

- Networks
- Trimmers
- Wirewounds
- Molded Metal Strip

Inductors:

- Fixed (axial/radial/SMD)
- Ferrite Cores
- Wirewound
- Multilayer
- Variable

Transformers:

- Pulse Transformers
- SMD (for DC to DC Converters)
- Switch mode Power Transformers
- SMD (Pulse applications)

Varistors:

- Ring Varistors (Barium Titanium Oxide)
- Disc Varistors (Zinc Oxide)
- Multilayer Surface Mounted Varistors

Thermistors:

- For motor sharing
- For Overcurrent Limiting
- For temperature compensation

Crystals:

- Metal AT cut
- Metal AT strip
- Molded surface mounted

## 4.0 NEPP2012 COMMERCIAL PARTS TECHNOLOGY QUALIFICATION PROCESSES—CONCLUSIONS

It has been found that the companies and organizations investigated use different processes to qualify similar commercial technology product for their high reliability applications. Choices have been made as to customer risk tolerance, system usage profiles, technology failure mechanisms and risk mitigation effectiveness. These choices have driven selected of the 100% testing (screening) and lot qualification (or periodic qualification) employed for these commercial part types. It is also clear that there are differences of technical judgment between different organizations that modify the approaches taken. In this section the differences in qualification flow are delineated and compared and the rationale between these differences is explored. These analyses are presented in tabular form for clarity.

**Table 4-1.** Key mission environmental characteristics.

| Missions | Temperature Range | Mechanical | Duration |
|---|---|---|---|
| Space | Narrow range; mostly below 20C | Benign except for launch | 1–20 years |
| Military (short duration) | Wide range; typically –40C to +110C | Moderate to severe | 1–-2 years |
| Military (long duration) | Wide range; typically –40C to +110C | Moderate | 1–-10years |
| Launch | Narrow | Severe dynamic vibration and shock | 10 minutes |
| Automotive | Very wide range; dependent on deployment location in vehicle | Moderate to severe; random vibration | 10 years |
| Medical | Narrow range limited by biological tolerances | Benign for almost all applications | 5–-20 years |

Another prime consideration is the perception of technology risks by the customers and the system designers and manufacturers. These are summarized for commercial PEMs in Table 4-2. Table 4-3 outlines the predominant risk mitigations selected by most OEM's.

**Table 4-2.** Key mission environmental characteristics.

| Failure Mechanisms of Concern | Risk Mitigations | Costs | Schedule | Special Considerations |
|---|---|---|---|---|
| Early Life Failures | Burn-in at part level; Burn-in at module level | Burn-in costs are significant | Electrical test development may take 3 months | Effective burn-in may not be possible at module level due to thermal limitations of the system |
| Long-term failure rate | Life testing; part manufacturer reliability monitor testing | Life test cost is tolerable depending on periodicity | No significant impact | Dependent on completeness and validity of electrical test and statistical evaluation of results |
| Mechanical shock/Vibration tolerance | Advantage of PEM over Hermetic package | No impact | No impact | PEMs preferable in automotive and some military applications |
| Manufacturing Risks: Popcorning | Dry bagging or bakeout prior to soldering | Small | Less than one week addition to manufacturing schedules | Use part manufacturer's standard characterization data to determine best approach |
| Impact of storage and moisture on long-term reliability | Part manufacturer's Autoclave and HAST Data; System qualification testing | Significant if testing done by OEM | Possible 1-3 months delay if OEM testing is deemed necessary | |

**Table 4-3.** OEM risk mitigations.

| Mission | Concern | Mitigation Selected | Notes |
|---|---|---|---|
| Space | Failure rate, short (infant mortality) and long term | 100% burn-in and flight lot life test | Part manufacturer test data usually ignored |
| Military (short duration) | Early life failure rate and mechanical (package) robustness | 100% burn-in usually at both part and module level; mechanical testing at module and system level | Part manufacturer early life failure rate data ignored and not trended |
| Military (long duration) | Early and long-term failure rate and mechanical package robustness | 100% burn-in; lot life test; mechanical testing at module and system level | Part manufacturer reliability data characteristics usually ignored |
| Launch | Package robustness | 100% Mechanical screening (temperature cycling, random vibration, mechanical shock) at module and system level | Part manufacturer reliability data examined periodically |
| Automotive | Long term failure rate and mechanical robustness; very high volume production | Process audit and qualification; review periodic part manufacturer testing closely | |
| Medical | Early life failure rate and long-term failure rate; thermal and mechanical environment usually benign; Very low power consumption essential | 100% burn-in and periodic life test; monitor power consumption frequently during burn-in and life test | |

## 5.0 REFERENCES


[1] B. Julius and Ellsberry, A., “Electronic Piece Parts Selection for Flight Termination Systems,” AV8017, August 30, 2011.

[2] Casasnovas and White, “Commercial Plastic Encapsulated Microcircuits for Naval Aviation Applications,” Johns Hopkins APL Technical Digest, Vol. 19, No.1, 1997, http://www.jhuapl.edu/techdigest/TD/td1801/casanovas.pdf.

[3] McCluskey, Hakim, Fink, Fowler, and Pecht, “Reliability Assessment of Electronic Components Exposed to Long-Term Non-Operating Conditions,” IEEE Transaction on Components, Packaging, and Manufacturing Technology–Part A, Vol. 21, No. 2, June 1998.

[4] R. R. Madsen, “Component Reliability After Long Term Storage,” Texas Instruments, Application Report SLVA304, May 2008, http://focus.ti.com/lit/wp/slva304/slva304.pdf.

[5] D. Pinsky, Lambert, E., “Tin Whisker Risk Mitigation for High-Reliability Systems Integrators and Designers,” Raytheon Company, Tewksbury, MA; https://www.reliabilityanalysislab.com/TinWhiskerRiskMitigationForHighReliability.pdf.

[6] M. Porter, “Medical Device Reliability and Qualification,” Medtronic Tempe Campus, Materials Physics & Design Reliability, 27 September, 2011; http://www.meptec.org/Resources/9%20-%20Medtronic.pdf.

[7] P. Gerrish, Herrmann, E., Tyler, L., and Walsh, K., “Challenges and Constraints in Designing Implantable Medical ICs,” IEEE Transactions On Device And Materials Reliability, Vol. 5, No. 3, September 2005.

[8] T. S. Savage, “The Implications of RoHS on Active Implantable Medical Devices,” Medtronic Tempe Campus, Tempe, Arizona, International Reliability Physics Symposium 2011.

[9] Y. Li, Poon, C. Y., and Zhang, Y.-T., “Analog Integrated Circuits Design for Processing Physiological Signals,” IEEE Reviews In Biomedical Engineering, Vol. 3, 2010.

[10] X. Zhu, Vasanth, K., Xu, X., Smyth, C., and Rhoton, B., “Application Based Reliability Assessment and Qualification Methodology for Medical ICs,” Medical/HiRel Business Group, High Performance Analog, Texas Instruments, Dallas, TX, International Reliability Physics Symposium, 2011.

# REPORT DOCUMENTATION PAGE

*Form Approved*
*OMB No. 0704-0188*

The public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Department of Defense, Washington Headquarters Services, Directorate for Information Operations and Reports (0704-0188), 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302. Respondents should be aware that notwithstanding any other provision of law, no person shall be subject to any penalty for failing to comply with a collection of information if it does not display a currently valid OMB control number.

**PLEASE DO NOT RETURN YOUR FORM TO THE ABOVE ADDRESS.**

**1. REPORT DATE** *(DD-MM-YYYY)*
03-01-13

**2. REPORT TYPE**
JPL Publication

**3. DATES COVERED** *(From - To)*
N/A

**4. TITLE AND SUBTITLE**
Commercial Parts Technology Qualification Processes

**5a. CONTRACT NUMBER**
NAS7-03001

**5b. GRANT NUMBER**

**5c. PROGRAM ELEMENT NUMBER**

**6. AUTHOR(S)**
Mark S. Cooper

**5d. PROJECT NUMBER**

**5e. TASK NUMBER**

**5f. WORK UNIT NUMBER**

**7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)**
Jet Propulsion Laboratory
California Institute of Technology
4800 Oak Grove Drive
Pasadena, CA 91009

**8. PERFORMING ORGANIZATION REPORT NUMBER**
JPL Publication 13-6

**9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)**
National Aeronautics and Space Administration
Washington, DC 20546-0001

**10. SPONSORING/MONITOR'S ACRONYM(S)**
NASA NEPP

**11. SPONSORING/MONITORING REPORT NUMBER**

**12. DISTRIBUTION/AVAILABILITY STATEMENT**
Unclassified—Unlimited
Subject Category 38 Quality Assurance and Reliability
Availability: NASA CASI (301) 621-0390 Distribution: Nonstandard

**13. SUPPLEMENTARY NOTES**

**14. ABSTRACT**
Many high-reliability systems, including space systems, use selected commercial parts (including PEMs) for unique functionality, small size, low weight, high mechanical shock resistance, and other factors. Predominantly this usage is subjected to certain 100% tests (typically called screens) and certain destructive tests usually (but not always) performed on the flight lot (typically called qualification tests). Frequently used approaches include those documented in EEE-INST-002 and JPL DocID62212 (which are sometimes modified by the particular aerospace space systems manufacturer). In this study, approaches from these documents and several space systems manufacturers are compared to approaches from a launch systems manufacturer (SpaceX), an implantable medical electronics manufacturer (Medtronics), and a high-reliability transport systems process (automotive systems).

The PEM technology qualification process is described, as documented in EEE-INST-002 (written by GSFC), as well as the somewhat modified approach employed at JPL. Approaches used at several major NASA contractors are also described.

**15. SUBJECT TERMS**
Space Qualification, Commercial Parts, Automotive Parts, Medical Parts, Launch Vehicle Parts, Plastic Encapsulated Microeletronics, PEMs

| 16. SECURITY CLASSIFICATION OF: | | | 17. LIMITATION OF ABSTRACT | 18. NUMBER OF PAGES | 19a. NAME OF RESPONSIBLE PERSON |
|---|---|---|---|---|---|
| a. REPORT | b. ABSTRACT | c. THIS PAGE | | | STI Help Desk at help@sti.nasa.gov |
| U | U | U | UU | | 19b. TELEPHONE NUMBER (Include area code) (301) 621-0390 |