

vides methods of evaluating the significance of BER (bit error rate) test results as well as techniques to characterize imbalances due to inter-symbol interference or inter-channel interference. Techniques employed in the SDA provide a means to statistically characterize receiver performance efficiently using a minimum of accumulated test results with a definable level

of error. These advanced techniques have broad application to other fields that rely on evaluation of binomial experiments (pass/fail, true/false, go/no-go), and allow evaluators to extract more information from fewer trials.

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*ther information, contact the JSC Innovation Partnerships Office at (281) 483-3809.*

*This invention is owned by NASA, and a patent application has been filed. Inquiries concerning nonexclusive or exclusive license for its commercial development should be addressed to the Patent Counsel, Johnson Space Center, (281) 483-1003. Refer to MSC-24798-1.*

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## Distributed Prognostics and Health Management With a Wireless Network Architecture

**Distributed architectures prevent total system failure during emergencies, allowing parts of the system to continue to function, and making overall system recovery faster.**

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A heterogeneous set of system components monitored by a varied suite of sensors and a particle-filtering (PF) framework, with the power and the flexibility to adapt to the different diagnostic and prognostic needs, has been developed. Both the diagnostic and prognostic tasks are formulated as a particle-filtering problem in order to explicitly represent and manage uncertainties in state estimation and remaining life estimation. Current state-of-the-art prognostic health management (PHM) systems are mostly centralized in nature, where all the processing is reliant on a single processor. This can lead to a loss in functionality in case of a crash of the central processor or monitor. Furthermore, with increases in the volume of sensor data as well as the complexity of algorithms, traditional centralized systems become — for a number of reasons — somewhat ungainly for successful deployment, and efficient distributed architectures can be more beneficial.

The distributed health management architecture is comprised of a network of smart sensor devices. These devices monitor the health of various subsystems or modules. They perform diagnostics operations and trigger prognostics operations based on user-defined thresholds and rules. The sensor devices, called computing elements (CEs), consist of a sensor, or set of sensors, and a communication device (i.e., a wireless transceiver beside an embedded processing element). The CE runs in either a diagnostic or prognostic operating mode. The diagnostic mode is the default mode where a CE monitors a given subsystem or component through a low-weight diagnostic algorithm. If a CE detects a critical condition during monitoring, it raises a flag. Depending on availability of resources, a networked local cluster of CEs is formed that then carries out prognostics and fault mitigation by efficient distribution of the tasks. It should be

noted that the CEs are expected not to suspend their previous tasks in the prognostic mode. When the prognostics task is over, and after appropriate actions have been taken, all CEs return to their original default configuration.

Wireless technology-based implementation would ensure more flexibility in terms of sensor placement. It would also allow more sensors to be deployed because the overhead related to weights of wired systems is not present. Distributed architectures are furthermore generally robust with regard to recovery from node failures.

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*Inquiries concerning rights for the commercial use of this invention should be addressed to the Ames Technology Partnerships Division at 1-855-NASA-BIZ (1-855-6272-249). Refer to ARC-16450-1.*

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## Minimal Power Latch for Single-Slope ADCs

**A CMOS implementation for remote sensing applications results in further reduction of power consumption and noise.**

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Column-parallel analog-to-digital converters (ADCs) for imagers involve simultaneous operation of many ADCs. Single-slope ADCs are well adapted to this use because of their simplicity. Each ADC contains a comparator, comparing its input signal level to an increasing reference signal (ramp). When the ramp is

equal to the input, the comparator triggers a latch that captures an encoded counter value (code). Knowing the captured code, the ramp value and hence the input signal are determined. In a column-parallel ADC, each column contains only the comparator and the latches; the ramp and code generation

are shared.

In conventional latch or flip-flop circuits, there is an input stage that tracks the input signal, and this stage consumes switching current every time the input changes. With many columns, many bits, and high code rates, this switching current can be substantial. It