All-Digital Baseband 65nm PLL/FPLL Clock Multiplier using 10-cell Library

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ABSTRACT:

- A compact portable digital library is described which can be easily ported to new processes, and can be customized to provide Radiation Hardened by Design (RHBD) and ultra low power operation.
- The library is used to construct an all-digital clock multiplier to provide high speed clocks, avoiding issues with making analog PLL loops fault tolerant and re-convergent after Single Event Transients
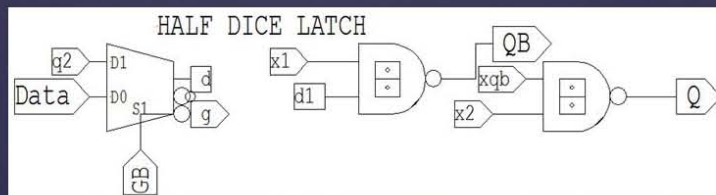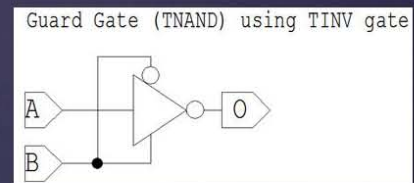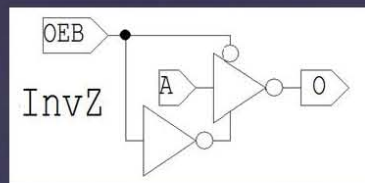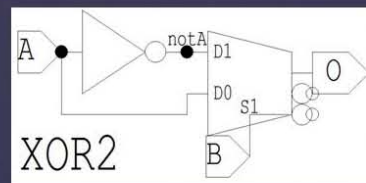
10-CELL LIBRARY:

Base cells

RHBD

65 nm layout:

INV   NAND2   NAND3   NAND4   NOR2   BUF   BUF4   MUX2b   TINVZ   TNAND0
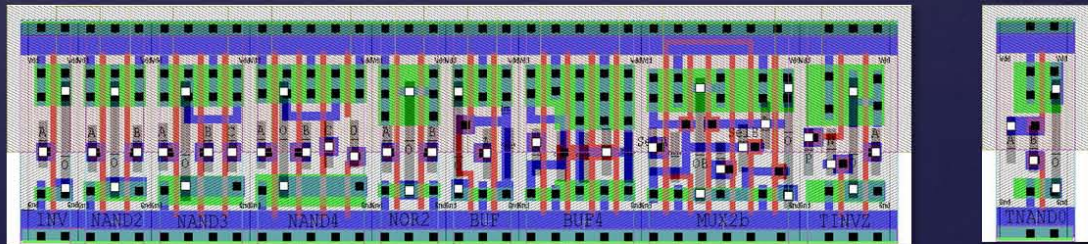
COMPOSITE GATE EXAMPLES:

LATC

DFFC

XOR2

InvZ

Guard Gate (TNAND) using TINV gate

HALF DICE LATCH
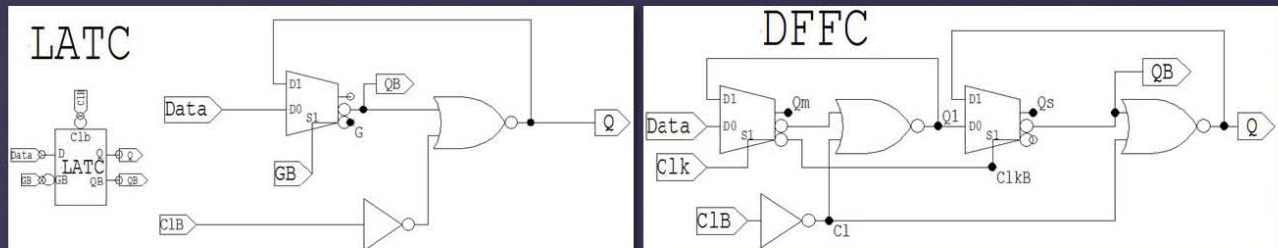
NOTES:

- Automatic over-cell 3-metal routing is reasonably efficient layout for R&D
- Custom GG & Half DICE for large RHBD designs will give production efficiency
- TINV tri-state cell more efficient for busses

IMPLEMENTATIONS:

- TSMC 65 nm for TMR ADFPLL (current project, this poster)
- XFAB 0.35 μ extensive use for low power / low voltage (1.8v) RF powered implants
- TSMC 90 nm for general radiation testing and analog PLL (Shuler, SEESYM 2010)
- TSMC 0.35 μ early version radiation testing, comparison of flip flops (Shuler, NSREC 2006, IEEE TNS)
- 10 CELLS PORTS TO NEW PROCESS – customizable for guard rails, low voltage, includes RHBD

10-CELL LIBRARY cont'd – XFAB layout with Guard Bars, XOR, ½ DICE, Schmidt Trigger:
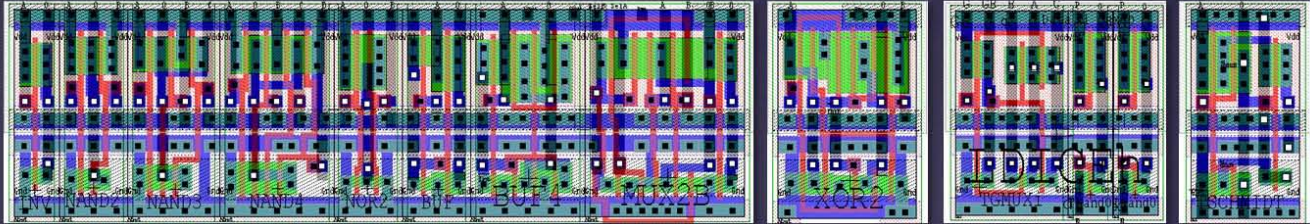

WHY AN ALL DIGITAL CLOCK MULTIPLIER?

- Clocks need to be ultra-reliable … other fault management depends on clocks
- Chips need higher speed clocks than can be brought from off chip
- Analog PLLs have difficulties managing SET/SEU, see illustration
- Existing "digital" PLL techniques are sampled data systems, not usable for highest rate clock
- New technologies may not provide analog components and may not even be CMOS
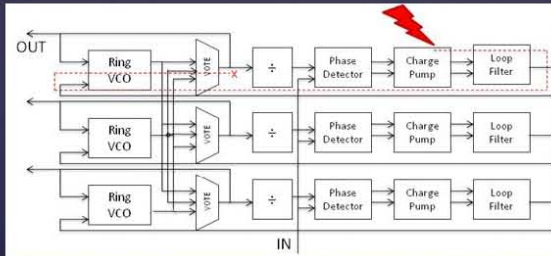
Conventional fault tolerant PLL:
- Errors removed by voters will not correct state in charge pumps or loop filters or fractional dividers
- Accumulation of invalid states may lead to susceptibility to future errors
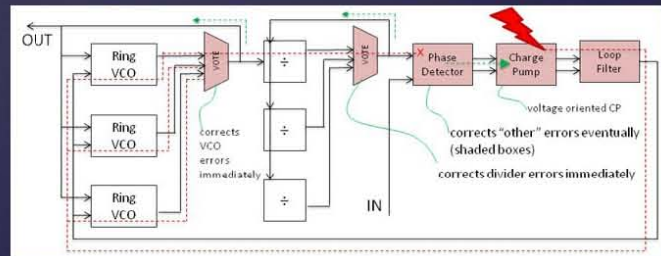
Best practices from recent literature:
- VCO and logic vote & correct errors within themselves
- Single string in rest of PLL prevents masking problem
- Natural (slow) PLL action corrects other errors eventually
- Errors reduced but significant vulnerability remains

## DIGITAL PLL / FLL / FPLL CONSIDERATIONS

- Magnitude of phase error quantized at 360° or at best 180° degrees, not continuous!
- NCO quantized frequency + quantized feedback signal $\Rightarrow$ infinite small signal gain $\Rightarrow$ instability
- Digital (ring) oscillator provides poor frequency resolution (2 gate delays period variance)
- Frequency loops are very stable & phase not needed/meaningful for fractional or high multipliers …*solutions:*
- NCO is tapped delay line with 4-phase output using delays, giving ½ gate period increment
- On-chip control provides a frequency loop + a phase loop activated when frequency is close
- Phase loop controls *phase only & for one cycle,* not accumulating via frequency change

## 128 stage NCO with 4-phase output (9 bit resolution) 74-360 MHz
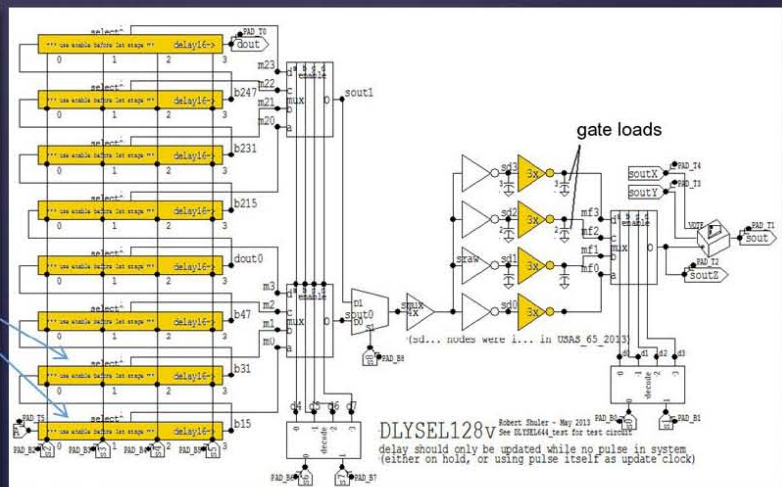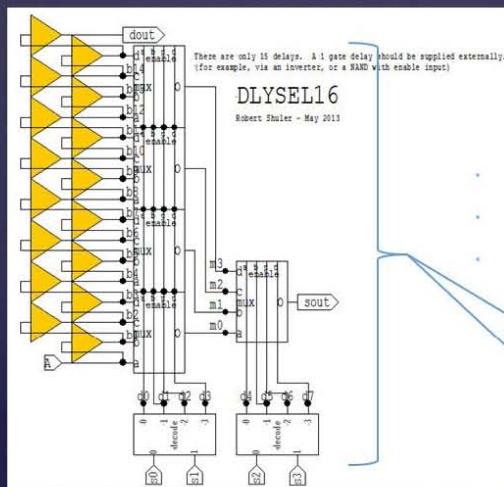
ADFPLL ON-CHIP CONTROLLER

- TMR configuration (only one string shown below)
- 9 bit up/down counter for external frequency adjustment
- Very limited I/O pin availability (10) required re-use, external adjustment requires stopping NCO
- Internal multiples of 2x, 3x, 4x & 8x ... compares edges at ever other external clock edge
- Separate frequency and phase detector (very similar, see figure)
- Coarse phase adjustment of 2 gate delays, 3 choices => poor performance at high multiples / freq.
  - Phase adjustment occurs only when frequency matches within one cycle
  - Repeats several times for high multiples
- Experimental circuit does not prevent harmonic lock (not hard to fix)
  - Simulation is very time consuming (overnight for close start frequency)
  - Need another iteration with finer phase control, no harmonic lock, more test & configuration I/O
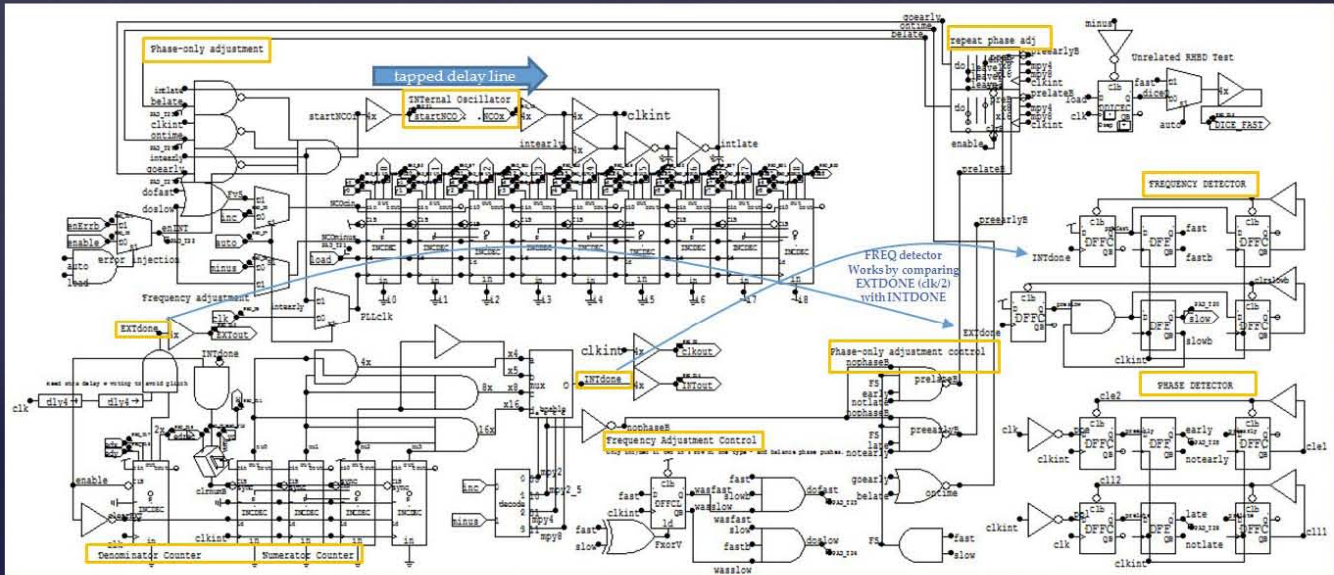
TEST RESULTS

- **3 out of 4 NCO's monotonic –4th still convergent**
  - Simulations actually performed with 130nm model file due to tools issues
  - Probably could support 8 phase selection with careful simulation
- **On 2 of 5 chips the on-chip loop control scanned without any sign of lock**
- **Very sensitive to over voltage, latchup requiring power cycle**
  - 2.5<->1.0v level shifters designed by a grad student ... exceeded bandwidth expectations but poor isolation
  - Guard bars were not used in 1.0v logic under apparently mistaken impression no latchup issue at 1.0v
- **Error checking by comparison to ref 100 MHz clock for 2x50, 4x25, and 8x12.5 combinations**
  - Several of these, particularly 2x50, very reliable & would run days without error
  - Attempted to obtain time on USAS test at TAMU, but cyclotron problems used up spare time
  - Need more test leads and additional circuits to compare single string & benchmark SEU/SET tests of logic

2 x 50 MHz good lock
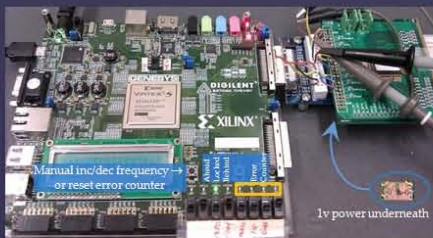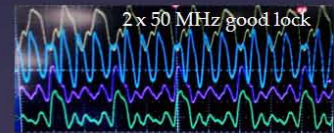
Test rig: GENESYS Virtex 5, 2v I/O, 1v core supply
(a rig w/lab power supply did not work well)

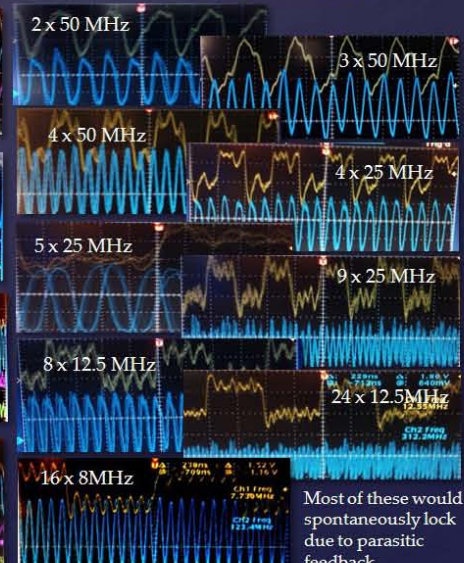Most waveform distortion due to scope lead coupling

INTERNAL LOOP w/PHASE LOCK
3 x 50 MHz good lock
4 x 25 – slowdown correction
4 x 25 – speedup correction
4 x 12.5MHz harmonic lock

EXTERNAL FREQUENCY LOOP
2 x 50 MHz
3 x 50 MHz
4 x 50 MHz
4 x 25 MHz
5 x 25 MHz
9 x 25 MHz
8 x 12.5 MHz
24 x 12.5MHz
16 x 8MHz

Most of these would spontaneously lock due to parasitic feedback