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High Current ESD Test of Advanced Triple Junction Solar Array Coupon

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***Abstract*— Testing was conducted on an Advanced Triple Junction (ATJ) coupon that was part of a risk reduction effort in the development of a high-powered solar array design by Space Systems/Loral, LLC (SSL). The ATJ coupon was a small, 4-cell, two-string configuration that has served as the basic test coupon design used in previous SSL environmental aging campaigns. The coupon has many attributes of the flight design; e.g., substrate structure with graphite face sheets, integrated by-pass diodes, cell interconnects, RTV grout, wire routing, etc. The objective of the present test was to evaluate the performance of the coupon after being subjected to induced electrostatic discharge (ESD) testing at two string voltages (100 V, 150 V) and four array currents (1.65 A, 2.0 A, 2.475 A, and 3.3 A). An ESD test circuit, unique to SSL solar array design, was built that simulates the effect of missing cells and strings in a full solar panel with special primary arc flashover circuitry. A total of 73 primary arcs were obtained that included 7 temporary sustained arcs (TSA) events. The durations of the TSAs ranged from 50 micro-seconds to 2.75 milli-seconds. All TSAs occurred at a string voltage of 150 V. Post-test Large Area Pulsed Solar Simulator (LAPSS), Dark I-V, and By-Pass Diode tests showed that no degradation occurred due to the TSA events. In addition, the post-test insulation resistance measured was > 50 G-ohms between cells and substrate. These test results indicate a robust design for application to a high-current, high-power mission.**

Keywords—Photovoltaic Cell Testing; Electro-Static Discharge Testing; High Power Solar Array

I. INTRODUCTION

In order to provide power for increased payload sophistication and/or increased number of payloads, satellite power systems are motivated to increase photovoltaic array (PVA) string voltages and string currents. These voltages and currents may exceed 100V and 1 Amp respectively. The International Space Station PVAs use 160V for power generation [1]. Recently, Cho et al. [2] report a nanosatellite test flight demonstrating 350 V operations.

When power increases on the satellite, there is an increased risk for problems, notably sustained arcs. Bodeau [3] surveyed a large amount of ground test data and compared that with a large amount of vacuum arc data to derive a safe operating region: string currents < 1A for < 200V. For future high power satellite power systems, careful consideration should be given to design and that design should be verified through adequate testing.

Space Systems/Loral, LLC (SSL) is developing a high power satellite bus system for future applications. An initial round of coupon-level tests were performed at the Marshall Space Flight Center (MSFC) to investigate PVA design robustness for voltages > 100V and currents > 1 A. SSL and MSFC have several years of partnership in combined space environment testing to qualify various aspects of SSL PVA design [4, 5, 6, 7]. The starting point for testing was to determine the robustness of the standard SSL design against voltages > 100 V and currents > 1 A in an electro-static discharge (ESD) test. The protocol for ESD testing was based on the recent ISO standard [8].

II. TEST PLAN

The objective of the ESD testing was to evaluate performance of a single coupon in configurations at two string voltages (100V, 150V) and four string currents (1.65A, 2.0A, 2.475A, and 3.3A). A cumulative total of 70 arcs were planned. See Table I for the delineation of arcs per case and the sequence of test progression. The test coupon underwent no environmental aging at MSFC. That is to say, no radiation, UV, thermal cycling, and/or ion erosion environments were applied before testing. The present test condition was ambient temperature in the inverted gradient potential case. It is noted that the coupon tested at MSFC had undergone previous ESD testing at the Kyushu Institute of Technology (KIT).

The test article was a small, four cell Advanced Triple Junction (ATJ) coupon. This coupon was from a common manufacturer that produced a series of coupons that underwent testing both at KIT and at MSFC. Each individual cell assembly contains a silicon bypass diode. Two independent "strings" of cells are formed by connecting two cells together in series to form a single string. The string layout on the coupon represents a typical string layout on a flight solar array panel. As a part of the SSL ESD mitigation design, the cell laydown included room-temperature vulcanizing (RTV) adhesive grout along the cell parallel gaps (gaps between cell strings).

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TABLE I. NUMBER OF ESD ARCS REQUIRED

String Potential (V)	String Current (A)	Number of ESD Arcs Required
100	1.65	5
150	1.65	5
100	2.0	10
150	2.0	10
100	2.475	10
150	2.275	10
100	3.3	10
150	3.3	10
Arc Summary Total		70

Figure 1 shows the coupon layout. The string on the left side of the coupon is string 1 and string 2 is on the right side of the coupon. Both strings are mounted on a Kapton sheet which is applied to a substrate structure composed of an aluminum honey-comb core with graphite face sheets. The substrate is constructed with holes in all four corners which provide a pass-through for the string wires and can be used for sample mounting. An insulating bushing is inserted in each corner hole to help isolate the pass-through wires from the grounded honey-comb structure. The size of the coupon and the limitation to a 2x2 cell format was dictated by the original 25.4 cm diameter illumination region in the MSFC radiation target chamber. A recent upgrade to the MSFC radiation target chamber allows for an illumination region of 76.2 cm in diameter.

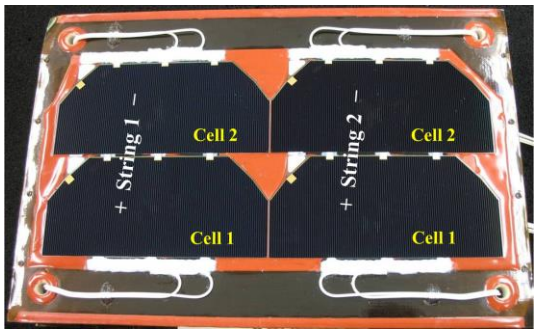


Fig. 1. Picture of test coupon. The coupon has been configured into two strings with each string composed of two cells. [4]

III. TEST SETUP

A. *Experimental Arrangement*

Testing was carried out in one of the vacuum chambers that reside in the NASA/MSFC Space Environment Effects Facility. The details of this particular vacuum chamber have been described elsewhere [4] but basic information is included here. The chamber is 2.1 m long by 1.2 m diameter with cryo-pumping capability. Base pressure reaches $\leq 1.3 \times 10^{-4}$ Pa ($\leq 1 \times 10^{-6}$ torr). A liquid nitrogen shroud of dimension 1.2 m long by 1.11 m diameter resides at one end of the chamber while a 100-keV flood gun is mounted on the other end of the chamber. All testing in this study was performed at room temperature. A 2-D stage allows movement of a Faraday Cup and Trek probe to either measure the electron beam flux or measure the coupon surface potential. An array of Tektronix oscilloscopes records diagnostic signals from the test circuit and a video camera/recording system captures visual evidence of arcs.

B. *Arc Inception Voltage*

A dedicated control rack houses a high voltage power supply to bias the coupon and several current probes (Pearson Coils) to capture movement of charge in response to an arc. A small (few nano-Farad) capacitor supplies charge for primary arc generation. The size of this capacitor is enough to allow for visual identification of the arc location. Fig. 2 shows the schematic of the arc inception voltage setup. The network of capacitors inside the chamber simulates the capacitance of missing cells and the capacitance of cells to substrate in the flight architecture. For arc inception voltage testing, these capacitors are not needed but their presence allows continuing to ESD testing without a vacuum break.

Testing was performed in the inverted gradient condition; i.e., the cell coverglass was more positive than the substrate. Initiation of the arc is caused by sequentially manipulating the electron beam flux and illumination time on the coupon. Measurement of the surface potential after each electron beam exposure allows a fairly precise way of determining the arc inception voltage. Details of the electron beam exposure method can be found in Wright et al. [4].

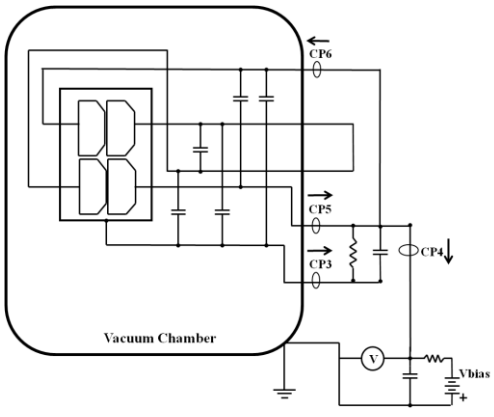


Fig. 2. Arc inception voltage test circuit. "CP" indicate location of current probe and "V" indicates location of the HV probe. [4]

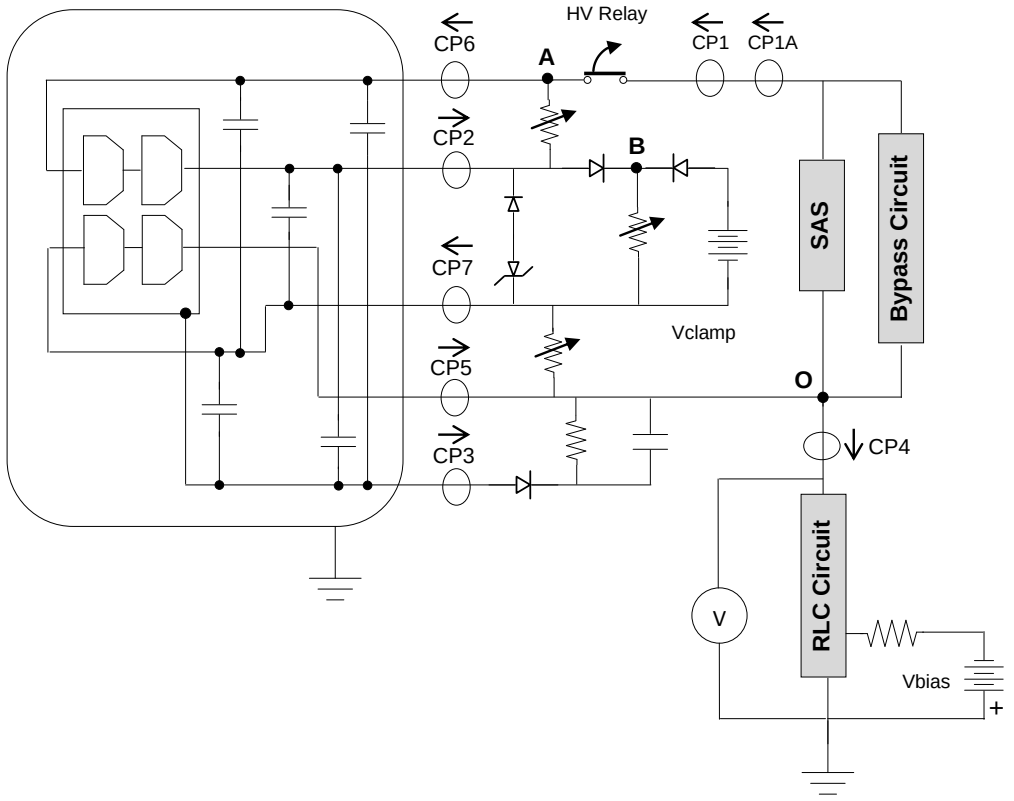


Fig. 3. ESD test circuit. "CP" indicates location of current probe and "V" indicates location of the HV probe. "A" and "B" indicate voltage measurement locations referenced to point "O." SAS is the Solar Array Simulator. [7]

C. *Electro-Static Discharge*

A separate equipment rack houses the SSL specialized ESD test circuit. Various circuit elements are present to allow simulation of the effects of a whole array panel while using only a small coupon. Key to this special setup is the primary arc pulse generation circuit. It is comprised of an RLC network to produce the amplitude (28 A) and duration (~ 190 µs) of the coverglass flashover during an arc. Discussion of the derivation of the flashover pulse can be found in Wright et al. [4].

The test circuit is shown in Fig. 3. Of special note is an arc interruption circuit that forces a HV relay to open a switch 3 milli-sec after arc initiation. This feature can prevent a sustained arc from causing ultimate coupon failure.

IV. Test Results

A. *Arc Inception Voltage*

Arc inception voltage was measured before ESD testing. A total of five arc events were acquired. The average arc inception value was ~900 V. These measurements were obtained after 3 days under vacuum and at a background pressure of 1.07×10^{-4} Pa (8×10^{-7} Torr).

During the performance of the ESD testing, the arc inception voltage increased as evidenced by the continual lowering of the electron beam energy required to induce an arc. For example, during the initial arc inception voltage testing the electron beam energy began at 6 keV and ended at ~ 5 keV (suggesting a ~ 1000 V arc inception voltage). As the final arcs were obtained in the 150 V/3.3 A case, it is inferred that the arc inception voltage was ~ 3500 V. The electron beam energy change in this case started at 6 keV and ended at < 2.5 keV (suggesting the ~ 3500 V arc inception voltage value).

It is speculated that the increase in arc inception voltage occurred as the result surface modifications due to the early high current (> 1A) arc events.

B. *Electro-static Discharge*

The ESD test sequence was performed according to Table I starting with the lowest string voltages and currents and progressing to the highest string voltages and currents. Table II shows the as-run sequence. Three additional arcs were produced: two arcs were produced while measuring the coupon Arc Inception Voltage at the end of the testing and in one case the oscilloscopes were not ready. The occurrence of Temporary Sustained Arc (TSA) events is also noted in Table II. A TSA is defined as any ESD event that extends beyond the primary ESD arc pulse of nominal 190 µs duration. Table III shows the duration beyond the primary arc for each of the seven TSA events.

TABLE II. AS-RUN ESD ARC DATA

String Potential (V)	String Current (A)	Number of ESD Arcs Acquired	Number of TSAs
100	1.65	5	0
150	1.65	5	0
100	2.0	10	0
150	2.0	10	1
100	2.475	10	0
150	2.275	10	2
100	3.3	12	0
150	3.3	11	4
Arc Summary Total		73	7

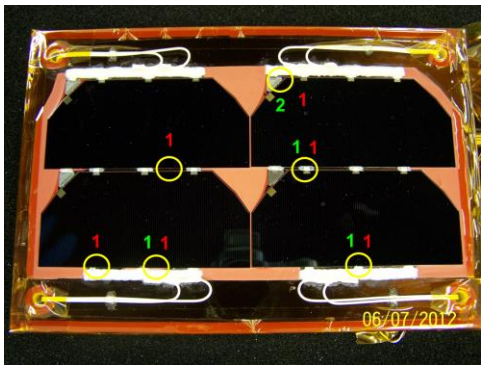
TABLE III. TSA OCCURRENCE CONDITION AND DURATION

String Potential (V)	String Current (A)	Duration (µs)
150	2	250
150	2.475	160
150	2.475	230
150	3.3	50
150	3.3	190
150	3.3	*
150	3.3	2750

* No oscilloscope data available

Figure 4 shows an arc site map for each of the four string current levels. The number of arc occurrences per location is noted on each figure and color coded as to voltage. As seen in the figure, preferential arc sites include bus bars, interconnects, and cell edges.

a.



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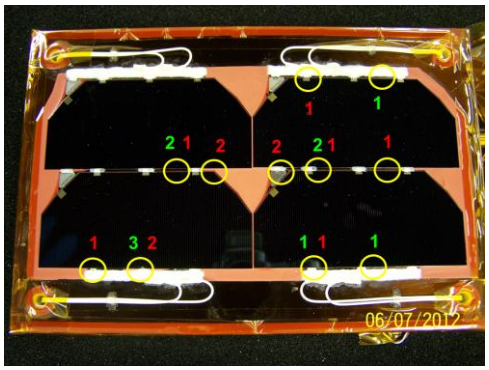
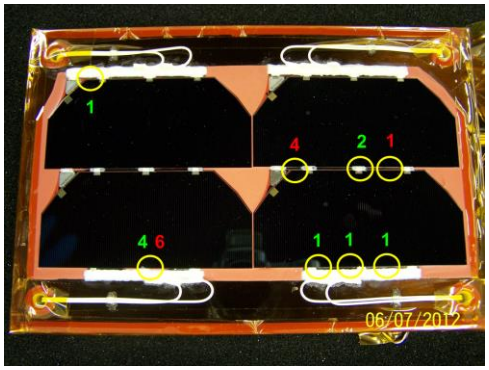


c.



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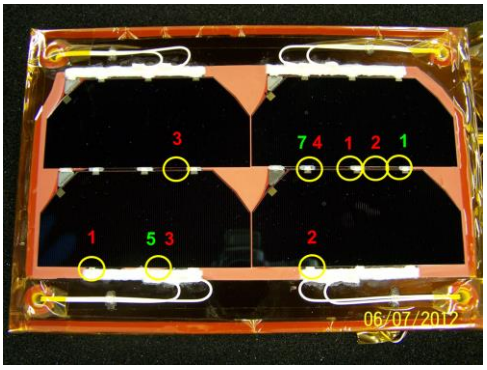


Fig. 4. Arc site locations. Each number by the circle indicates the number of events at that site. Green number is arc count at 100 V string voltage and red number is arc count at 150 V string voltage. The different sub-plots are for each string current tested: a. 1.65 A. b. 2.0 A. c. 2.475 A. d. 3.3A.

A picture of the longest duration TSA event at string voltage 150 V and string current 3.3 A is shown in Fig. 5. The current and voltage probe data for this event is shown in Fig. 6. Based on the current probe data, the path of the SAS current is overlaid in Fig. 5. The TSA ended upon the opening of the arc interruption switch – which may actually qualify this arc as a permanent sustained arc.

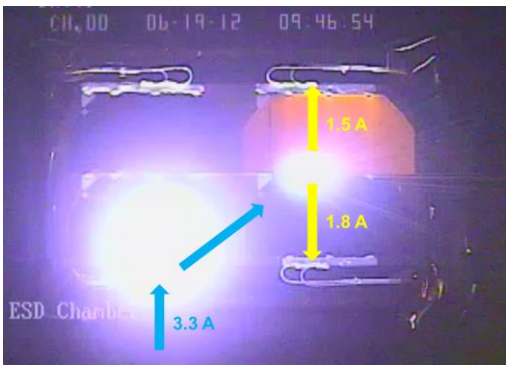
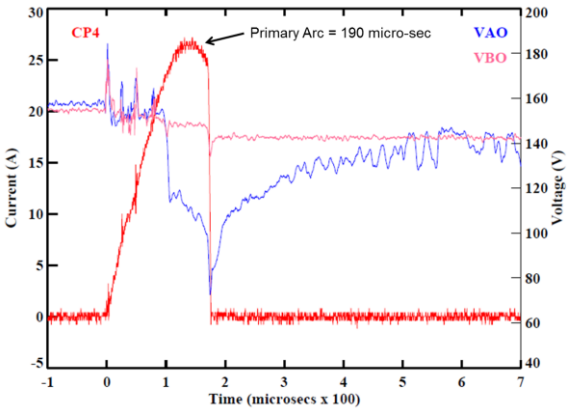


Fig. 5. Picture of the TSA event at 150 V and 3.3 A. The event duration was 2750 µs. The event may have gone longer but was stopped by the arc interruption switch opening. The path for the SAS current is also shown.

a.



b.

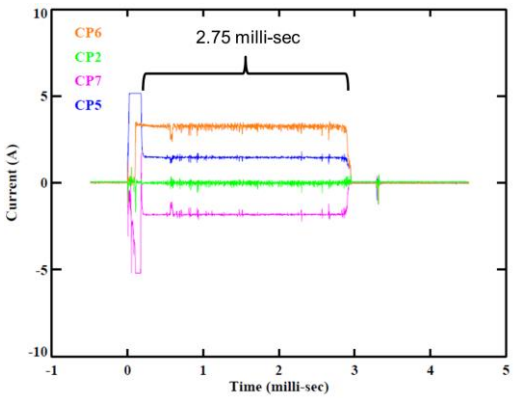
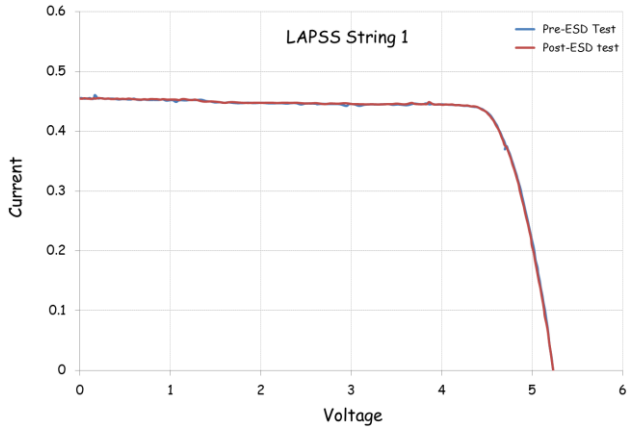


Fig. 6. Current and voltage probe data for the TSA event pictured in Fig.5. Refer back to Fig. 3 for map of CP layout. a. CP4 and voltage probe data. VAO, VBO refers to voltage difference between points A and O, B and O respectively. Refer to Fig.3. b. Current probe data for each of the four cells on the coupon.

C. Functional Tests

The functional performance of the coupon was measured both before and after ESD testing. The comparison results of Large Area Pulsed Solar Simulator (LAPSS), Dark IV, and By-Pass diode testing are shown in Fig.7. The LAPSS data provides the key performance data while Dark-IV and By-Pass diode test provide insight into subtle changes.

a.



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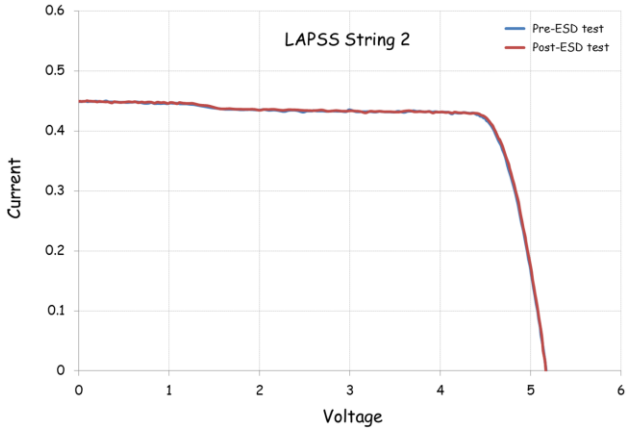

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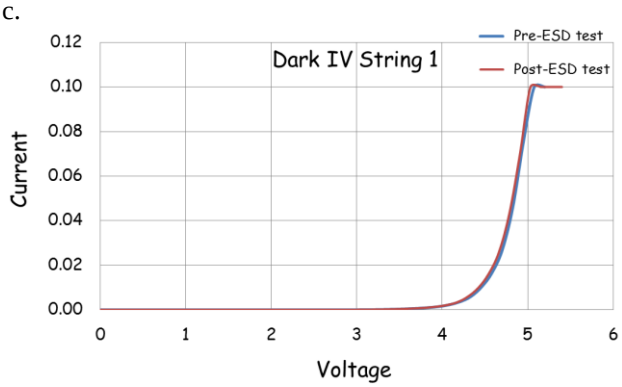

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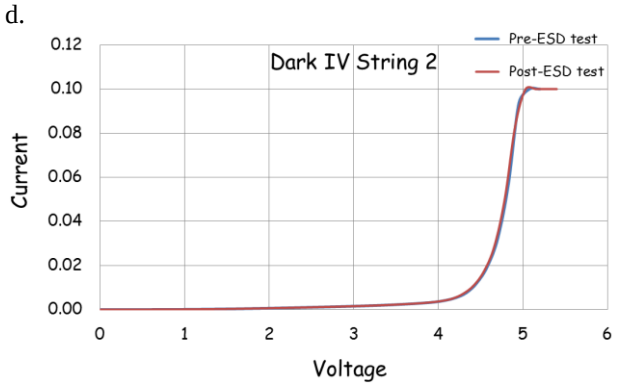
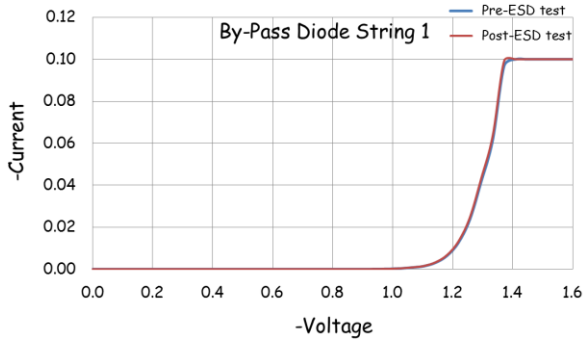


e.



f.

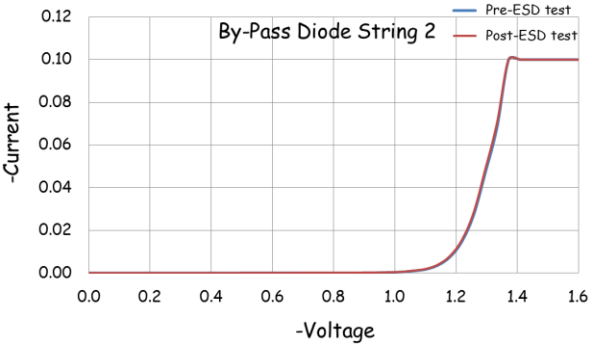


Fig. 7. Functional test data from before and after ESD testing. a. LAPSS String 1 b. LAPSS String 2 c. Dark-IV String 1 d. Dark-IV String 2 e. By-Pass Diode String 1 f. By-Pass Diode String 2

V. Summary

ESD testing was performed on a basic SSL solar array architecture that included RTV applied to interconnects, busbars, and gaps between cells. Test parameters were chosen to anticipate the array bus voltages and currents that may be used in a future SSL array design for high power application. The voltage/current test parameters used here extends those used in the previous study of Hoang et al. [9]. The purpose of this test was to examine the present design susceptibility to high power operation. A total of 73 primary arcs were induced with seven TSA events observed. All TSA events occurred at 150 V over three different string currents (2 A, 2.475 A, and 3.3 A) with the number of TSA events increasing with increasing current level. For the grouted coupons used in the Hoang et al. [9] test, a cumulative 132 primary arcs were induced on two coupons with only two TSA events observed: one at 150 V/1.0 A and one at 150 V/1.65 A. The duration of the TSA events in this test exhibit no discernible pattern. It is important to note that the longest TSA event was terminated via a pre-determined test circuit operation. Whether this event could have evolved into a sustained arc with significant damage to the coupon is uncertain. All functional test data obtained post-ESD testing indicated no degradation in cell performance. Insulation resistance measured post-ESD testing was > 50 GΩ between all cells and the substrate. In addition, microscopic examination of the coupon revealed no arc trace path between string 1 and string 2.

Based on the information published by Bodeau [3], the TSA occurrences observed in this test come as no surprise. These operational voltages and currents are in the high-risk zone as defined by Bodeau [3]. The present SSL design indicates robustness against some region of high power operation. But if power in the 150 V, 3A level is envisioned, further design and test work is needed, especially when the reality of environmental aging is considered [7].

Acknowledgment

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