6H-SiC Transistor Integrated Circuits Demonstrating Prolonged Operation at 500 °C

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Abstract

The NASA Glenn Research Center is developing very high temperature semiconductor integrated circuits (ICs) for use in the hot sections of aircraft engines and for Venus exploration where ambient temperatures are well above the ~ 300 °C effective limit of silicon-on-insulator IC technology. In order for beneficial technology insertion to occur, such transistor ICs must be capable of prolonged operation in such harsh environments. This paper reports on the fabrication and long-term 500 °C operation of 6H-SiC integrated circuits based on epitaxial 6H-SiC junction field effect transistors (JFETs). Simple analog amplifier and digital logic gate ICs have now demonstrated thousands of hours of continuous 500 °C operation in oxidizing air atmosphere with minimal changes in relevant electrical parameters. Electrical characterization and modeling of transistors and circuits at temperatures from 24 °C to 500 °C is also described. Desired analog and digital IC functionality spanning this temperature range was demonstrated without changing the input signals or power supply voltages.

Keywords: SiC, JFET, Integrated Circuit

I. Introduction

Extension of the operating temperature envelope of transistor integrated circuits (ICs) well above the effective 300 °C limit of silicon-on-insulator technology is expected to enable important improvements to aerospace, automotive, energy production, and other industrial systems [1-3]. For example, extreme temperature ICs capable of T = 500 °C operation are considered vital to realizing improved sensing and control of turbine engine combustion leading to better fuel efficiency with significantly reduced pollution. The ability to place such ICs in engine hot-sections would beneficially eliminate wires and liquid cooling plumbing performance (i.e., weight and reliability) penalties imposed when silicon ICs are used. The competitive performance benefits to large systems enabled by

extreme temperature ICs are recognized as quite substantial, even though most such systems require only a relatively small number of extreme temperature chips [1].

One critical requirement for all ICs, including extreme temperature ICs, is that they function reliably over a designed product lifetime. The emergence of wide bandgap semiconductors has facilitated transistor and small IC demonstrations at extreme ambient temperatures of 500 °C or higher over the past two decades. However, most envisioned applications require reliable IC operation over long time periods at high temperature, on the order of thousands of hours or more. Without such durability, extreme temperature semiconductor ICs will not benefit (and will not be inserted into) the vast majority of important intended applications. Many previous reports of extreme temperature transistor or IC operation have focused on current-voltage (I-V) properties and gain-frequency performance with little or no mention of how long such parts operated at high temperature. Aside from work at the NASA Glenn Research Center [4-9], we are unaware of any published reports claiming transistor operation for more than 10 hours at temperatures at or above 500 °C.

This paper reports 6H-SiC junction field effect transistors (JFETs) and small "proof of principle" digital and analog IC chips that have achieved thousands of hours of stable electrical operation at 500 °C. Longer-term 500 °C durability results, and measurements and SPICE [10] modeling as a function of temperature expand on our previous reports of prolonged 500 °C 6H-SiC JFET and simple IC testing [7-9].

II. Experimental

Driven by the primary goal to realize integrated circuits with prolonged 500 °C operational durability, a baseline IC technology using an epitaxial n-channel 6H-SiC junction field-effect transistor, which is shown in schematic cross-section in Fig. 1, was selected for development. In particular, the epitaxial SiC pn-junction gate structure (with low operating gate current) should be inherently more robust against high temperature degradation than other (insulated gate, Schottky gate, bipolar, heterojunction and/or III-N) transistor technology approaches that would otherwise offer frequency, power dissipation, and/or circuit design and performance benefits. Though it is non-planar, the mesa-etched p^+ epi-gate structure avoids defects and extreme activation temperatures associated with high-dose p-type implants in SiC [11]. Despite inferior mobility compared to 4H-SiC, 6H-SiC was selected

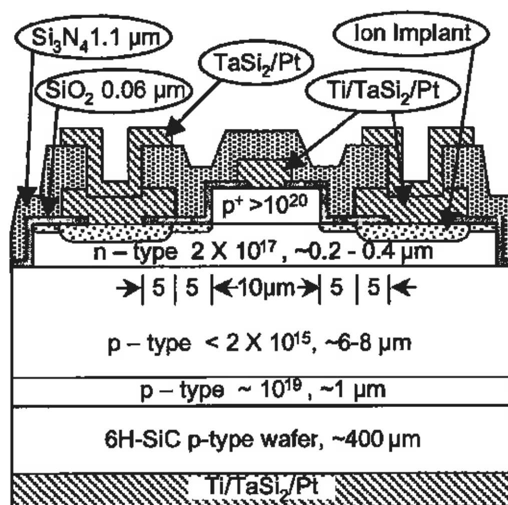

Fig. 1: Simplified cross-sectional schematic of 6H-SiC JFET.

as having demonstrated better structural stability during some thermal processing steps [12, 13]. Even though SiC is known to be chemically near-inert and diffusion resistant compared to silicon and III-V/III-N semiconductors, thermally activated degradation mechanisms at interfaces (such as metal-SiC, and/or SiC-insulator interfaces) or materials outside the semiconductor (such as metals, insulators, and/or packaging) have previously limited extreme temperature (i.e., ≥ 500 °C) stability/durability [5, 6, 14-16]. However, recently pioneered durable high temperature contacts to n-type SiC and high-temperature SiC packaging have both demonstrated prolonged 500 °C operational capability in oxidizing air atmosphere [6, 17]. The successful integration of these high temperature technologies into the epitaxial 6H-SiC JFET process is believed critical to the greatly prolonged 500 °C transistor and IC operation reported in this work.

A quarter wafer of small-signal 6H-SiC JFETs and simple ICs (configured using a single metal interconnect layer) was fabricated starting from commercially purchased [18] epilayered substrates. Most fabrication process details are described elsewhere [4, 6, 7, 15, 17, 19, 20]. On-chip resistors were formed from the JFET n-channel layer and implants/contacts with the overlying p^+ gate layer removed. Interconnects and wire bond pads were simultaneously formed by etch-patterning a layer of $TaSi_2$/Pt which was deposited on top of reactive-sputtered Si_3N_4 dielectric.

A few SiC chips from the saw-diced quarter-wafer were custom-packaged without any lids (i.e., exposed to air) and mounted onto two custom high-temperature circuit boards using the high temperature packaging approach detailed in [6]. Two 6H-SiC

JFETs (one with a 200 μm wide / 10 μm long gate and another with 100μm/10μm gate dimensions) were packaged and tested as discrete devices. Integrated circuits that were packaged and operated for thousands of hours at 500 °C included an inverting amplifier stage, a differential amplifier stage, a digital inverter (i.e., NOT logic gate) and a two-input NOR (i.e., Not OR) digital logic gate. The circuit boards with test chips were placed in two laboratory ovens with ~ 30 cm long 10 mil diameter unshielded Au wires running outside the ovens to nearby terminal strips connected to computer-controlled test instruments. The devices and circuits were operated continuously under electrical bias throughout the 500 °C test duration, with measurement data periodically stored onto computer. The atmosphere inside the oven was ordinary room air (~ 21% O_2).

III. Transistor Results

Fig. 2 illustrates the curve-tracer measured drain current (I_D) vs. drain voltage (V_D) characteristics of the packaged 100μm/10μm 6H-SiC JFET at 500 °C during the first hour (solid) of 500 °C operation and after 5000 hours (dashed) of 500 °C testing. Both Fig. 2 characteristics follow classic field-effect transistor behavior, including complete current shut-off for gate bias V_G steps more negative than -10 V. As mentioned in other reports [9, 20], the leakage causing the slight turn-up exhibited in I_D for 40 V < V_D < 50 V is effectively eliminated during the first 100 hours of 500 °C operation.

Fig. 3 more completely quantifies the measured temperature dependence of benchmark transistor parameters of drain-to-source on-state resistance (R_{DS}), transconductance ($g_m = \Delta I_D/\Delta V_G$ @ V_D = 20 V from V_G = 0V and V_G = -2V step data), and saturated drain current ($I_{DSS} = I_D$ @ V_D = 20 V, V_G = 0 V). The parameters in Fig. 3 are normalized to a transistor gate width of 1 mm. The I_{DSS} and g_m exhibit a nearly 3.5-fold decrease as temperature is increased from 25 °C to 500 °C, while R_{DS} increases by approximately the same factor. Such closely coupled behavior reflects the fact that these parameters are dominated by the same n-channel properties of decreasing mobility with increasing ionized carrier concentration as temperature is increased [21]. The threshold voltage V_T of these devices (not plotted) decreases by less than 1 V as temperature increases from 24 °C to 500 °C [20].

The dashed lines shown in Fig. 3 illustrate fits to the experimental data that can be rapidly incorporated into SPICE circuit simulation code [10, 22]. For I_{DSS} and g_m, fits proportional to $T^{-1.3}$ (in Kelvin) are shown, whereas the fits shown for R_{DS} are second order temperature polynomials (also in Kelvin). R_{DS} and n-channel resistors can be approximated by the SPICE semiconductor resistor model with SPICE parameters RSH (sheet resistance) = 8 kΩ/square, TC1 = 2.5 K^{-1} and TC2 = 5.3 x 10^{-6} K^{-2}. The basic SPICE JFET model does not include FET substrate bias body effect and temperature-dependent channel conduction. Because the NMOS LEVEL 1 SPICE transistor model does include these non-negligible effects, the NMOS model provides more accurate first-order SPICE modeling of our transistors provided that JFET gates are operated in reverse bias with low leakage relative to n-channel conduction current. This is because the

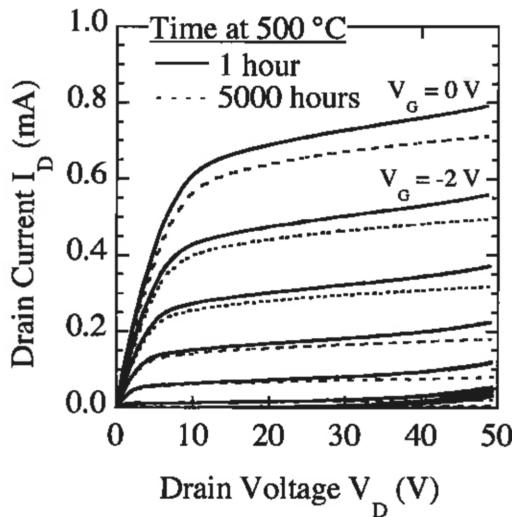

Fig. 2: Current vs. voltage (I-V) characteristics of the packaged 100μm/10μm 6H-SiC JFET measured during the 1st and 5000th hour of 500 °C operation.

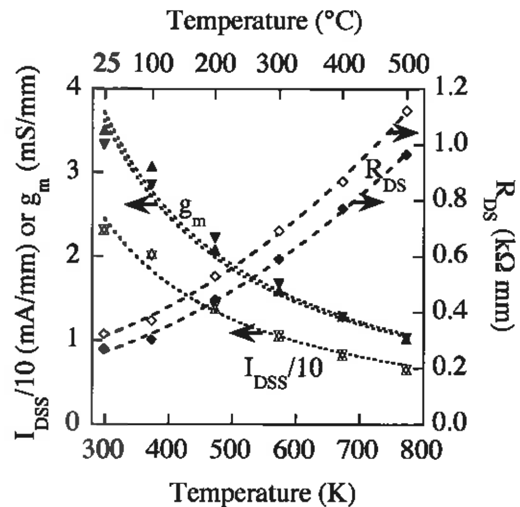

Fig. 3: Temperature dependence of device parameters (normalized to 1 mm gate width) for both packaged 6H-SiC JFETs.

drain current of both JFETs and MOSFETs (long channel, operating in the saturation on region) is approximated by [23]:

$$I_D = \frac{I_{DSS}}{V_T^2}\left(V_G - V_T\right)^2\left(1 + \lambda V_D\right) \qquad (1)$$

where λ is the saturated channel modulation parameter. For our 6H-SiC JFET devices the measured λ (SPICE LAMBDA) is ~ 0.005 V^{-1}, while the measured FET body effect coefficient (SPICE GAMMA) is ~ 0.3 $V^{-1/2}$. These two parameters exhibit negligible change between 25 °C and 500 °C.

Fig. 4 compares experimentally measured 6H-SiC JFET I-V characteristics at (top) 25 °C and (bottom) 500 °C with I-V characteristics simulated by SPICE NMOS LEVEL 1 model obtained via standard SPICE parameter fitting procedures [24, 25]. Reasonable agreement between the SPICE model and measured data is obtained at both temperatures by only changing the SPICE temperature variable TEMP. However, modifications to publicly available SPICE program source code [22] were required to obtain this result. The default MOS transistor surface potential was changed from 0.6 eV (just over half the silicon bandgap) to 1.6 eV (just over half the 6H-SiC bandgap). The temperature exponent for channel carrier mobility (BEX parameter in some versions of SPICE [24]) was set to -1.3 in agreement with the $T^{-1.3}$ data fits of Fig. 3. SPICE model parameters not extractable by I-V (such as capacitances) are first-order estimations calculated by straightforward insertion of 6H-SiC material and JFET device geometry parameters into well-known pn junction depletion approximation formulas [25, 26]. More comprehensive modifications to SPICE code, such as replacement of various silicon parameters internal to SPICE with 6H-SiC parameters, will eventually enable more accurate 6H-SiC transistor SPICE modeling.

The packaged 6H-SiC JFETs exhibited outstanding durability throughout 5000 hours of testing conducted at 500 °C. Fig. 5 shows the measured variation of I_{DSS}, g_m, R_{DS}, and V_T for both packaged JFETs as a function of 500 °C operating time. The 200μm/10μm JFET was biased at drain voltage V_D = 50 V and gate voltage V_G = -6 V and characterized using a source-measure unit (SMU). The 100μm/10μm JFET was biased and measured by a digitizing 60 Hz curve-tracer continuously operated with 50 V drain bias sweeps and -2V gate steps from V_G = 0 V to V_G = -16 V. The Fig. 5 plots are normalized to each transistor's measured value of I_{DSS0}, g_{m0}, R_{DS0}, and V_{T0} recorded at the 100 hour mark of 500 °C testing (i.e., after "burn-in") [9, 20].

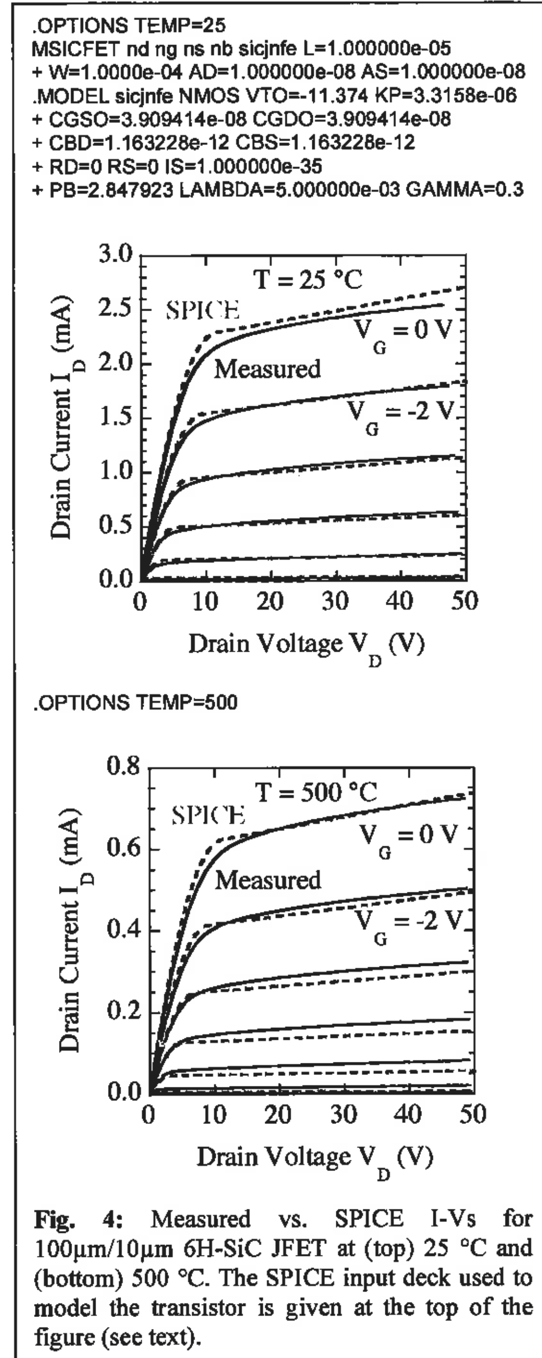

Fig. 4: Measured vs. SPICE I-Vs for 100μm/10μm 6H-SiC JFET at (top) 25 °C and (bottom) 500 °C. The SPICE input deck used to model the transistor is given at the top of the figure (see text).

With the exception of a few data points from the curve-tracer-measured 100μm/10μm JFET, the Fig. 5 data falls within a 10% parameter variation window. Fig. 5d shows the precise time variation of V_T extracted from the computer-fit x-intercept of the SMU-measured $\sqrt{I_D}$ vs. V_G of the 200μm/10μm JFET biased at V_D = 20 V [20, 24, 25]. The measured V_T changes by less than 1%. This excellent stability

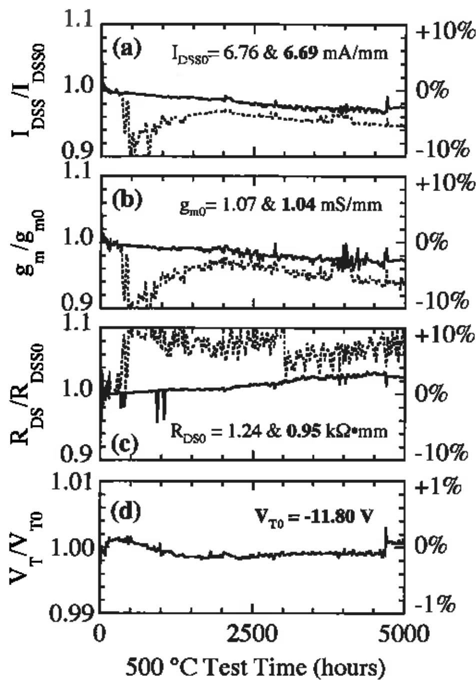

Fig. 5: Normalized (see text) JFET parameters versus 500 °C test time for packaged devices with gate dimensions of 100μm/10μm (dashed, plain text, measured by curve-tracer) and 200μm/10μm (solid, **bold text**, SMU-measured).

reflects the fact that JFET V_T is determined by the as-grown 6H-SiC epilayer structure.

IV. Integrated Circuit Results

The highly durable transistor properties summarized above enabled stable operation of prototype integrated circuits for thousands of hours at 500 °C. The operational properties of these circuits were measured as a function of temperature. Some of the circuits were also simulated with SPICE using the resistor and transistor model parameters described in the previous section, but with dimensional parameters (such as gate width W) set to reflect the accurate physical layout [10, 24, 25].

An inverting amplifier (inv-amp) IC consisting of two paralleled 40μm/10μm JFETs (simplified to a single 80μm/10μm JFET in the Fig. 6 inset) connected to a 20-square SiC load resistor was packaged for long-term 500 °C operational testing[8, 20]. A 1 V peak-to-peak sine wave test input was applied with -5 V DC bias and the V_{DD} supply voltage was 40 V with chip substrate grounded. Relatively large and temperature-independent stray capacitances are expected to arise from the oven test setup that features many long (~30 cm) unshielded Au wires running in and out of the test oven in close-proximity to each other. Using a 100 kHz capacitance meter, the effective capacitance at this particular inverting amplifier's output terminal was measured to be 55 pF with the 11 pF, 10 MΩ oscilloscope signal measurement probe connected.

Fig. 6 shows the inverting amplifier's measured (symbols) and SPICE-modeled (dashed lines) gain vs. frequency characteristics at 24 °C (black) and 500 °C (grey). Despite the large temperature difference, there is almost no difference in the low-frequency amplifier gain. Such behavior arises from the fact that the inv-amp drain resistor's value (R_{DD}) increases with temperature at about the same rate that the transistor's g_m decreases (i.e., the trends illustrated in Fig. 3). This reflects the fact that these parameters are oppositely linked to the conductivity of the 6H-SiC n-channel layer [21, 26]. Thus, the R_{DD} x g_m product that governs the amplifier circuit's low-frequency gain changes little with temperature [23]. However, the roughly 3-fold change in R_{DD} and g_m do precipitate a corresponding drop in 500 °C corner frequency evident in Fig. 6. As confirmed by SPICE simulations, the amplifier's frequency performance is primarily limited by resistive-capacitive (RC) charging time of the output terminal.

After more than 3900 hours of 500 °C operation, the inverting amplifier failed suddenly. The inv-amp chip has not yet been removed from the oven for failure analysis because other chips on the

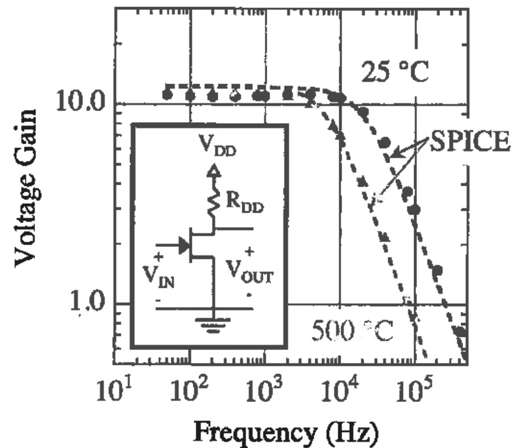

Fig. 6: Measured (points) and SPICE-modeled (dashed lines) gain-frequency characteristics of prototype 6H-SiC inverting amplifier stage at 25 °C (black) and 500 °C (grey).

same printed circuit board remain under test at 500 °C. One of the chips still being tested at 500 °C is a packaged differential amplifier (diff-amp) for which earlier results were reported in [7-9]. This diff-amp IC has now surpassed 5000 hours of 500 °C operation with less than 3% change from initial operating characteristics. Fig. 7 compares the 1 kHz test waveforms recorded during the 1st and 5000th hours of 500 °C diff-amp operation.

Digital logic gate ICs were also implemented and packaged from the same 6H-SiC wafer piece. This demonstration logic circuit family features negative logic voltage levels ($V_{High} \sim -2.5$ V and $V_{Low} \sim -7.5$ V) and two power supplies (positive $+V_{DD}$ and negative $-V_{SS}$ in the range of 20 to 25 V). Fig. 8 provides 25 °C and 500 °C results from operational testing of a packaged NOT gate that successfully operated for 3600 hours at 500 °C. For similar reasons as discussed for the inverting amplifier, this logic circuit also functions well at 25 °C without changes to signal or power supply input voltages. The successful operation of a packaged two-input NOR gate IC (from this same 6H-SiC wafer) for over 2000 hours at 500 °C was reported elsewhere [8, 9]. For a few days of this test, the setup was re-wired to demonstrate the NOT gate output successfully driving one of the NOR gate inputs. The NOR and NOT logic gates failed suddenly after 2400 and 3600 hours, respectively. The electrical failure of the NOR gate occurred in the form of an electrical near short-circuit, so failure of the insulating layer beneath a biased metal interconnect trace is suspected. However, detailed failure analysis is awaiting completion of 500 °C oven testing of other components on this board.

V. Summary Discussion

The increased 500 °C IC durability and stability demonstrated in this work is now sufficient for sensor signal conditioning circuits in jet-engine test programs. Combined with other extreme-environment technologies, such electronics might also greatly prolong the duration of data return from probes sent to explore the surface of Venus. Although only a small number of devices have been packaged and tested for thousands of hours at high temperature, this demonstration establishes the feasibility of producing SiC integrated circuits that are capable of prolonged 500 °C operation. This result was achieved through the integration of fundamental materials and/or processing advancements, including the development of high-temperature n-type ohmic contacts [17, 19] and high-temperature packaging technology [6]. We speculate that the choice of epitaxial JFET technology and its designed operation at relatively low electric fields and low current densities are also important to the demonstrated 500 °C durability. For many envisioned applications, far greater circuit complexity than the few-transistor ICs demonstrated in this initial work will be needed. Shrinkage of device dimensions and operating biases, and implementation of multilayer interconnects are obvious important further steps towards realizing durable 500 °C SiC integrated circuitry with greater complexity, higher frequency performance, and increased functionality.

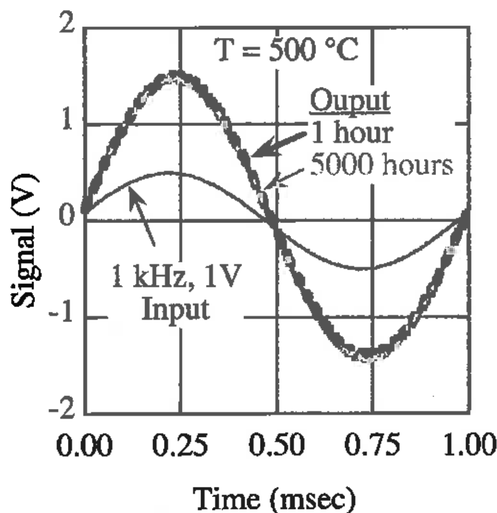

Fig. 7: Digitized test waveforms recorded from the 1st (black) and 5000th (grey) hours of differential amplifier IC operation at 500 °C.

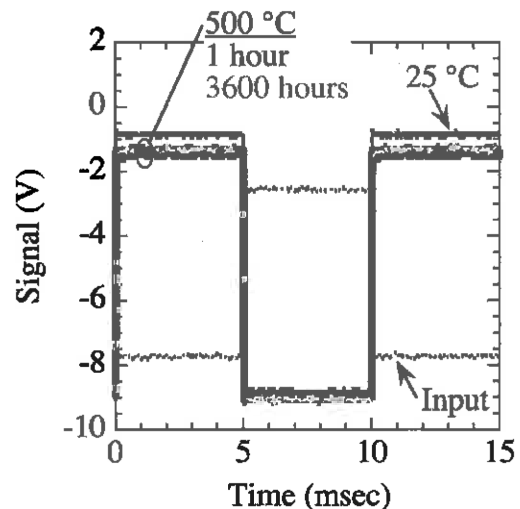

Fig. 8: Waveforms demonstrating operation of packaged digital NOT gate IC at 25 °C and at the beginning and end of prolonged 500 °C test.

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