The NASA Electronic Parts and Packaging (NEPP) Program: Overview and Roadmap for FY16

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Sundown at SCRIPPS Proton Therapy Center, Ken LaBel

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Outline

- NEPP Overview
- NEPP Tasks and Technology Selection
  - Background
  - Task “Roadmaps”
  - Other Cool Tasks
- Recent Highlights and “Concerns”
- Summary
- NEPP Electronics Technology Workshop (ETW) – June 13-16, 2016

Acronyms

Acronym	Definition
3D	Three Dimensional
3x PC	3x standard precision channel
AAIA	Automotive Aftermarket Industry Association
ACE	Absolute Contacting Encoder
ADAS	Advanced Driver Assistance Systems
ADC	Analog to Digital Converter
AEC	Automotive Electronics Council
AES	Advanced Encryption Standard
AF	Air Force
AF SMC	Air Force Space and Missile Systems Center
AFRL	Air Force Research Laboratory
AMRDEC	United States Army Aviation and Missile Research, Development and Engineering Center
AMS	Agile Mixed Signal
APL	Applied Physics Laboratory
ARC	Ames Research Center
ARM	ARM Holdings Public Limited Company
Avalanche STT	Avalanche Technology Spin Transfer Torque
BAE Systems	Marconi Electronic Systems (MES) and British Aerospace (BAe) merged to form BAE Systems
BGA	Ball Grid Array
BOK	Body of Knowledge
CAN	Controller Area Network
CAN-FD	Controller Area Network Flexible Data-Rate
CBRAM	Conductive Bridging Random Access Memory
CGA	Column Grid Array
CMOS	Complementary Metal Oxide Semiconductor
CN	Xilinx ceramic flip-chip (CF and CN) packages are ceramic column grid array (CCGA) packages
CN/Kyocera	CN Package assembled at Kyocera
Corp.	Corporation
COTS	Commercial Off The Shelf
CRC	Cyclic Redundancy Check
CSA	Canadian Space Agency
CSI2	Camera Serial Interface 2nd Generation
CU	Control Unit
Cu	Cu alloy
DDR	Double Data Rate (DDR3 = Generation 3; DDR4 = Generation 4)
DLA	Defense Logistics Agency - Land and Maritime
DMA	Direct Memory Access
DRAM	Dynamic Random Access Memory
DSP	Digital Signal Processing
dSPI	Dynamic Signal Processing Instrument
DTRA	Defense Threat Reduction Agency
Dual Ch.	Dual Channel
ECC	Error-Correcting Code
EEE	Electrical, Electronic, and Electromechanical
EMAC	Equipment Monitor And Control
ESA	European Space Agency
eTimers	Event Timers
EZSS	Air Force Components and Standardization Branch
FCCU	Fluidized Catalytic Cracking Unit
FinFET	Fin Field Effect Transistor (the conducting channel is wrapped by a thin silicon "fin")
FPGA	Field Programmable Gate Array
FY	Fiscal Year
GaN	Gallium Nitride
GAN GIT	Panasonic GaN GIT Eng Prototype Sample

Acronym	Definition
Gb	Gigabyte
GIC	Global Industry Classification
GIDEP	Government Industry Data Exchange Program
GPU	Graphics Processing Unit
GRC	Glenn Research Center
GSFC	Goddard Space Flight Center
GTH/GTY	Transceiver Type
HALT	Highly Accelerated Life Test
HAST	Highly Accelerated Stress Test
HBM	High Bandwidth Memory
HDIO	High Density Digital Input/Output
HDR	High-Dynamic-Range
HiREV	High Reliability Virtual Electronics Center
HMC	Hybrid Memory Cube
HP Labs	Hewlett-Packard Laboratories
HPIO	High Performance Input/Output
HQ	Headquarters
hr	hour
I2C	Inter-Integrated Circuit
i2MOS	Microsemi second generation of Rad-Hard MOSFET
IBM/GF	International Business Machines/Global Foundaries
IC	Integrated Circuit
IPC	IR/Convection Reflow Profile
IR	Infrared
JAXA	Japan Aerospace Exploration Agency
JEDEC	Joint Electron Device Engineering Council
JPEG	Joint Photographic Experts Group
JPL	NASA Jet Propulsion Laboratory
JSC	Johnson Space Center
KB	Kilobyte
khrs	one thousand hours
KSC	Kennedy Space Center Home
L2 Cache	independent caches organized as a hierarchy (L1, L2, etc.)
LaRC	Langley Research Center
LCMC	Air Force Life Cycle Management Center
LinFlex	Local Interconnect Network Flexible
L-mem	Long-Memory
LP	Low Power
M/L BIST	Memory/Logic Built-In Self-Test
MBSE	Model-Based Systems Engineering
MDA	Missile Defense Agency
MIPI	Mobile Industry Processor Interface
MLCC	Multi Layer Ceramic Capacitor
MPSOC	Multiprocessor System-on-Chip
MPU	Microprocessor Unit
MSFC	Marshall Space Flight Center
NAND	Negated AND or NOT AND
NASA	National Aeronautics and Space Administration
NAVSEA Crane	Naval Sea Systems Command Crane Division
Navy Crane	Naval Surface Warfare Center, Crane, Indiana
NEPAG	NASA Electronic Parts Assurance Group
NEPP	NASA Electronic Parts and Packaging
NEPP-ETW	NEPP Electronics Technology Workshop
NGSP	Next Generation Space Processor

Acronym	Definition
NOR	Not OR logic gate
NRL	Naval Research Laboratory
NRO	United States Navy National Reconnaissance Office
NY-PEMC	New York Power Electronics Manufacturing Consortium
OCM	on-chip RAM
OSMA	Office of Safety and Mission Assurance
PBGA	Plastic Ball Grid Array
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express
PCIe Gen2	Peripheral Component Interconnect Express Generation 2
PCIe Gen4	Peripheral Component Interconnect Express Generation 4
pcs	pieces
POC	Point of Contact
POF	Physics of Failure
PoP	Package on Package
PPAP	Production Part Approval Process
Proc.	Processing
QFN	Quad Flat Pack No Lead
R&D	Research and Development
R&M	Reliability and Maintainability
RAM	Random Access Memory
ReRAM	Resistive Random Access Memory
RGB	Red, Green, and Blue
RH	Radiation Hardened
RHA	Radiation Hardeness Assurance
SAE	Society of Automotive Engineers
SAR	Successive-Approximation-Register
SATA	Serial Advanced Technology Attachment
SCU	Secondary Control Unit
SD/eMMC	Secure Digital embedded MultiMediaCard
SD-HC	Secure Digital High Capacity
SDRAM	Synchronous Dynamic Random Access Memory
SEE	Single Event Effect
SEE-MAPLD	Single Event Effects Symposium and the Military and Aerospace Programmable Logic Devices
SERDES	Serializer/Deserializer
Si	Silicon
SiC	Silicon Carbide
SK Hynix	SK Hynix Semiconductor Company
SMC	Air Force Space and Missile Systems Center
SOA	Safe Operating Area
SOC	Systems on a Chip
SPI	Serial Peripheral Interface
STT	Avalanche Technology Spin Transfer Torque
TBD	To Be Determined
Temp	Temperature
TI	Texas Instruments
Tj	junction temperature
TRL	Technology Readiness Level
T-Sensor	Temperature-Sensor
TSMC	Taiwan Semiconductor Manufacturing Company
UART	Universal Asynchronous Receiver/Transmitter
USAF	United States Air Force
USB	Universal Serial Bus
VNAND	Vertical NAND
WBG	Wide Band Gap

NEPP - Frame of Reference

- **EEE (electrical, electronic, and electromechanical) parts are:**
  - **All the things that are on printed circuit boards (PCB) inside of electronics boxes.**
- **This includes:**
  - **Integrated Circuits (ICs or chips) like processors and memories as well as passives such as capacitors and resistors,**
  - **Hybrid devices or multi-chip modules: Small packages that house multiple chips internally that are placed on the PCB, and,**
  - **Connectors and wires used to send electrical or power signals between boards, boxes, or systems.**
- **This does not include:**
  - **The PCB - NASA Workmanship Program responsibility.**

PCB from Mars Rover
Image courtesy NASA

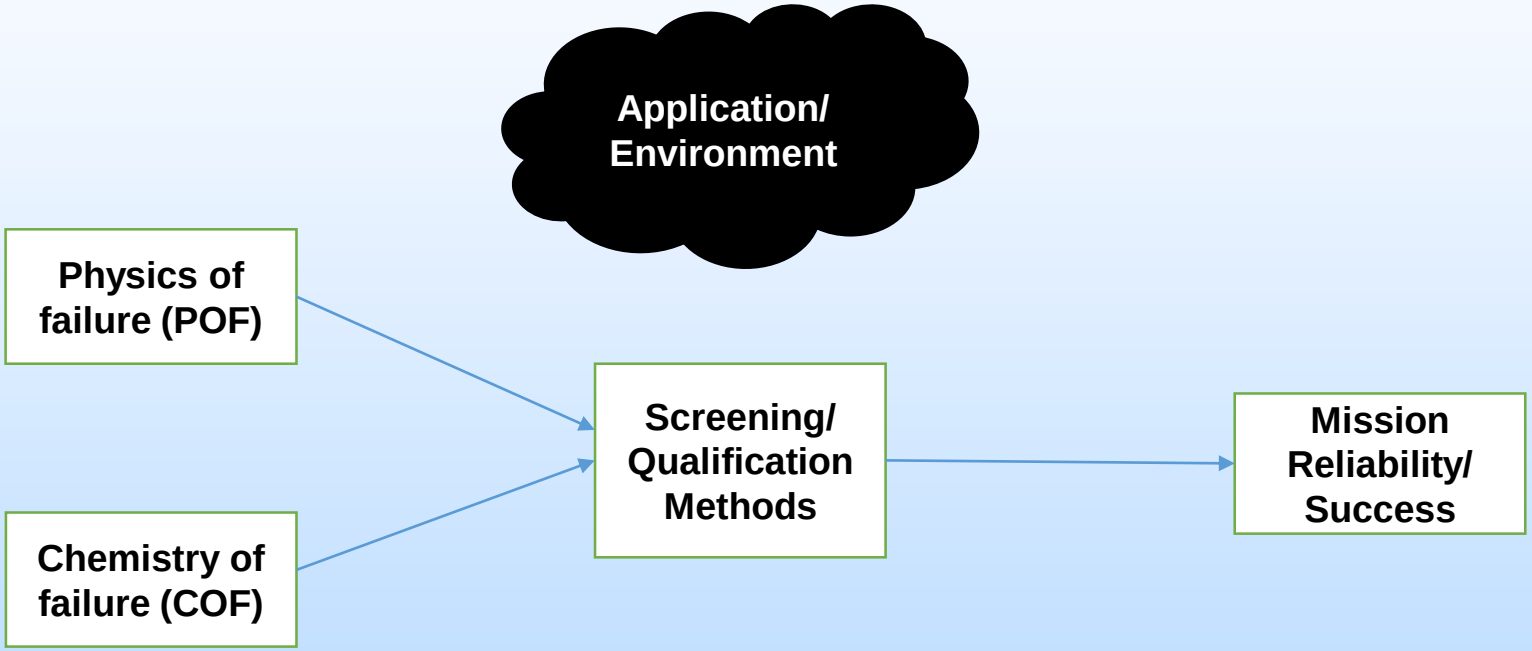
Image courtesy BAE Systems

Image courtesy NASA

NEPP

- **NEPP was chartered during the late 1980's to ensure appropriate commodities expertise existed to support the Agency.**
  - **In 2000, a subset of NEPP was created (NASA Electronic Parts Assurance Group – NEPAG) to ensure:**
    - **Appropriate sharing of information between the Centers and with other agencies, and,**
    - **Sufficient infrastructure exists to support Agency needs and to provide Agency leadership in supporting/developing EEE parts specifications, standards, guidelines, and test methods.**
- **NEPP has become a *premier* program for evaluating new EEE parts technologies and to develop insertion, test, screening, and qualification guidance.**
  - ***We do not qualify specific parts, but develop the knowledge on HOW to qualify/test the parts.***

Taking a Step Back…
A Simple View of NEPP's Perspective of What We Do



NEPP Efforts Relate to Assurance of EEE Parts –

It's not just the technology, but how to view the need for safe insertion into space programs.

NEPP Overview

NEPP provides the Agency infrastructure for assurance of EEE parts for space usage

Qualification guidance
To flight projects on how to qualify

Technology Evaluation
Determine new technology applicability and qualification guidance

Standards
Ensures NASA needs are represented

Test/Qualification Methods
Evaluate improved or more cost-effective concepts

Manufacturer Qualification
Support of audits and review of qualification plans/data

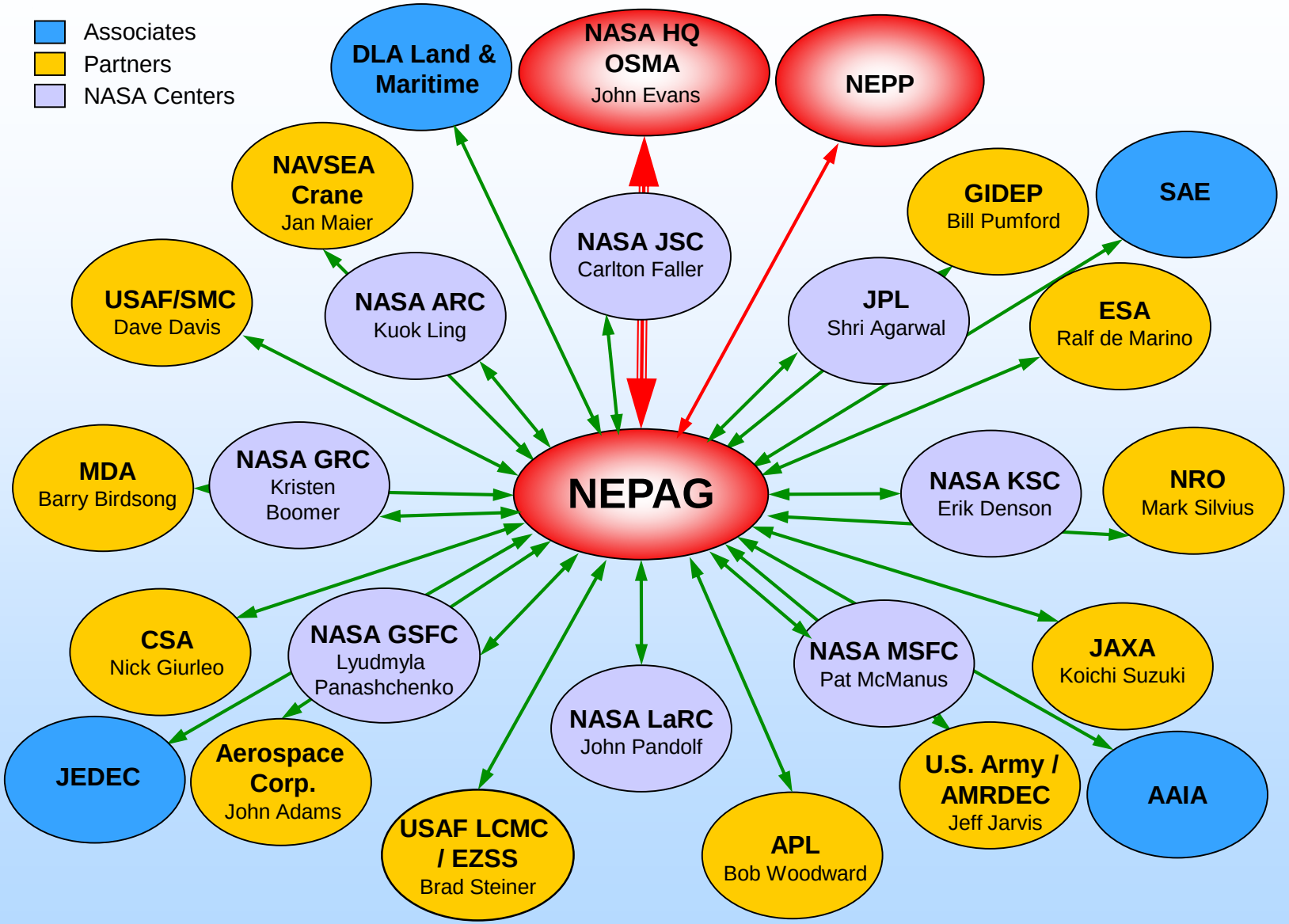
Risk Analysis
For all grades of EEE parts (commercial, automotive, military/aerospace, …)

Information Sharing
Lessons learned, working groups, website, weekly telecons

Subject Matter Experts
(SMEs) for NASA programs, other agencies, industry

NEPP and its subset (NEPAG) are the Agency's points of contact (POCs) for assurance and radiation tolerance of EEE parts and their packages.

NEPAG "Extended Family"



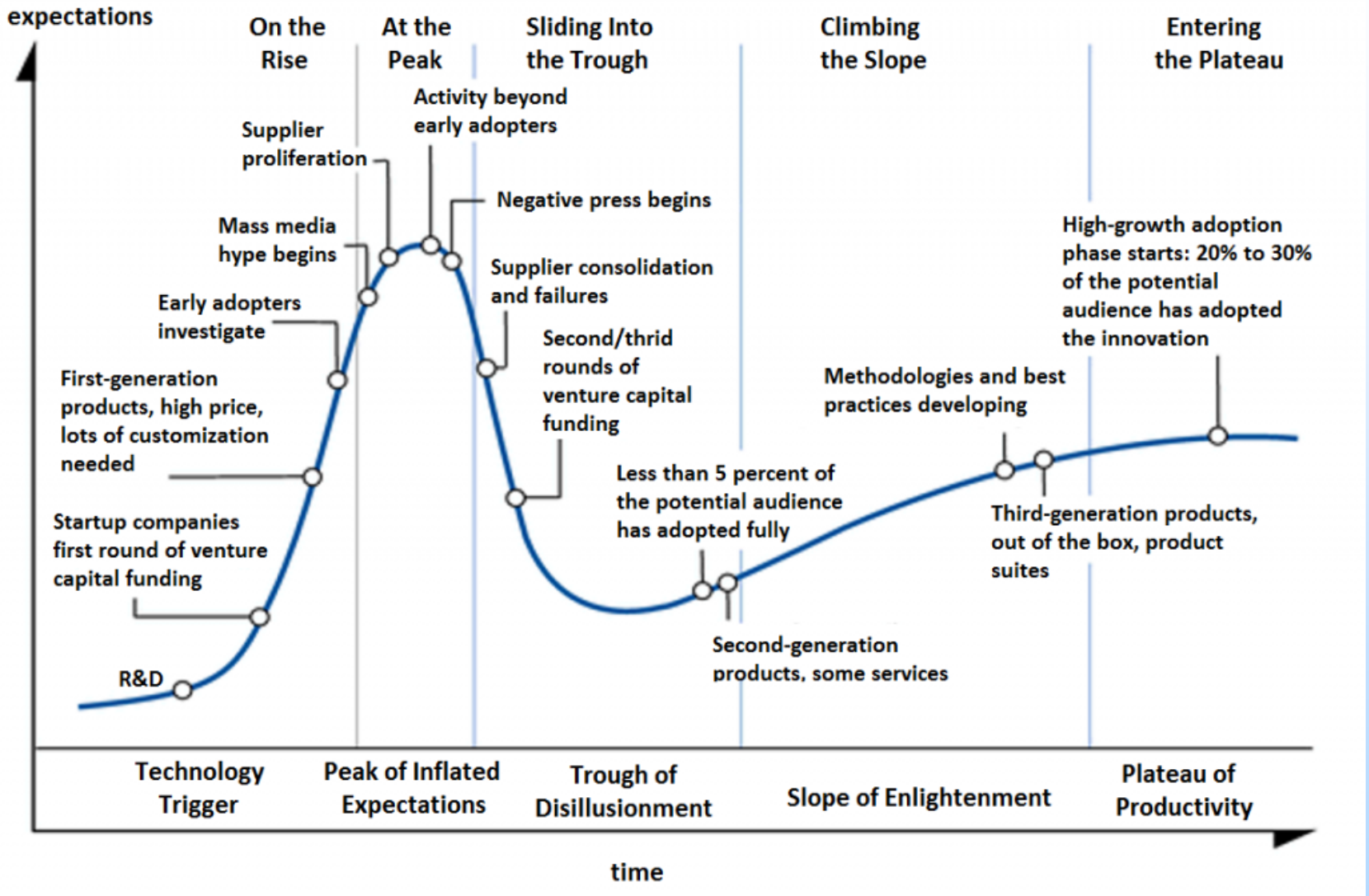
Technology Selection Criteria for NEPP Investigations

- **The technologies should satisfy all or most of the following criteria:**
  - **Wide applicability,**
  - **Product level or in productization, and,**
  - ***No distinction:*** **COTS to high-reliability aerospace.**
- **In general, we avoid:**
  - **Laboratory technologies, e.g., <TRL3,**
  - **Limited application devices with certain exceptions (critical application or NASA center specialization).**
- **Note: Partnering arrangements with other organizations preferred.**
  - **Industry examples: Microsemi, Xilinx, Altera (Intel), TI**
  - **Other U.S. Government: AF SMC, AFRL, DTRA, Navy Crane, NRO, NRL**

Technology Investigations: Sample Roadmaps Discussion

- **Caveats:**
  - ***Guidelines are often a product of technology evaluation tasks.***
  - **Only major product categories shown.**
- **Notes:**
  - **Separate CMOS roadmap not included.**
    - **NEPP leverages samples from ongoing DoD and/or commercial sources.**
    - **1xnm is current target (IBM/GF, INTEL, Samsung, TSMC).**
  - **"Reliability testing" may include product and/or package testing.**
  - **"Body of Knowledge" BOK document provides a snapshot status on a technology (manufacturing, reliability, radiation) and identifies gaps for future work.**
- **Technology areas not on NEPP Roadmap, but under consideration include:**
  - **Electro-optics (fiber optics),**
  - **Advanced analog and mixed-signal devices,**
  - **Imaging sensors,**
  - **Modeling and simulation,**
  - **High-speed communication (SERDES, fast data switches), and,**
  - **Adjunct processors (eg., graphics, signal processing).**

Gartner Hype Cycle Concept



Field Programmable Gate Arrays (FPGAs)

Trusted FPGA

- **DoD Development**

Altera

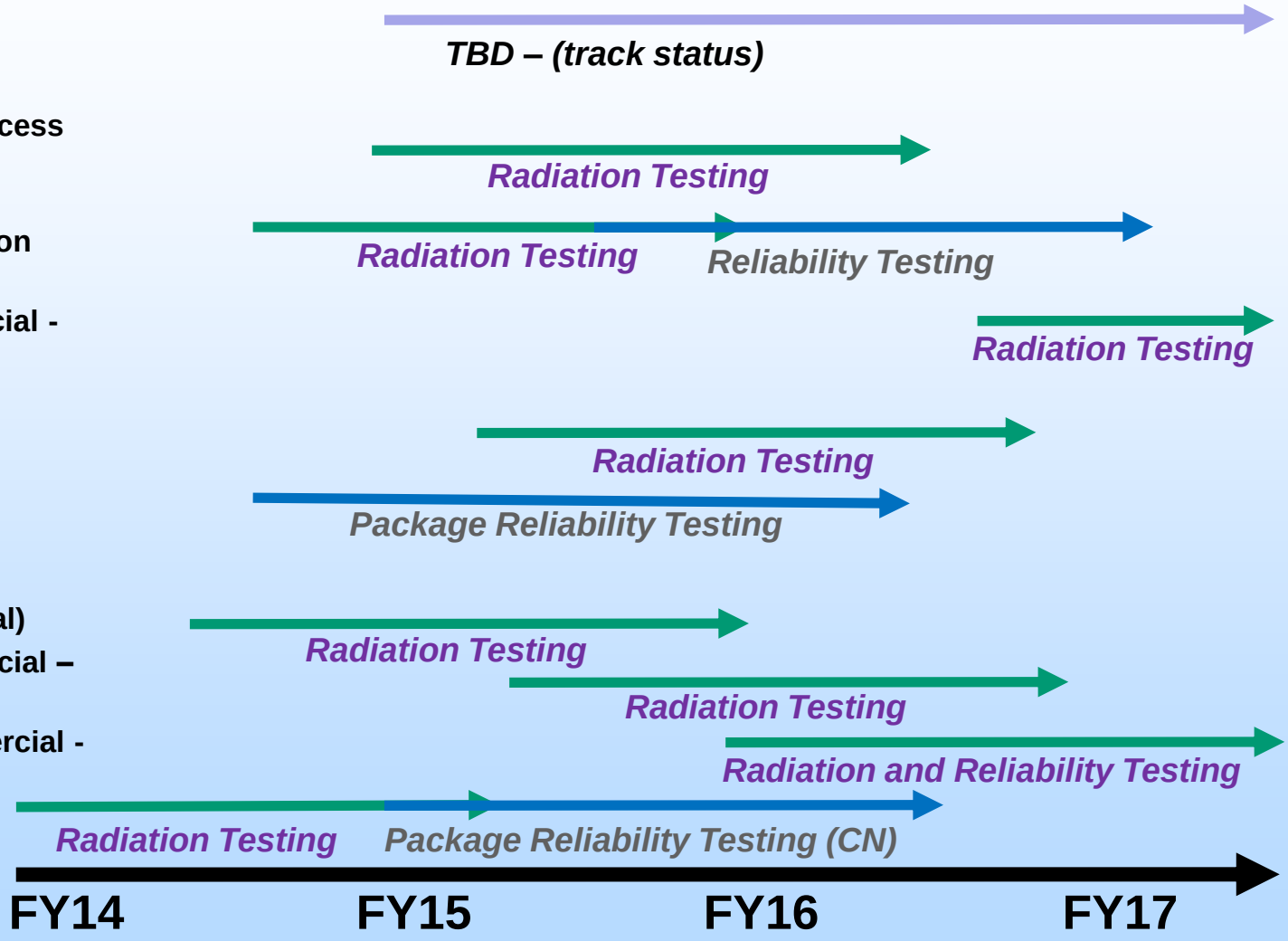
- **Stratix 5 (28nm TSMC process commercial)**
- **Max 10 (55nm NOR based commercial – small mission candidate)**
- **Stratix 10 (14nm commercial - TriGate)**

Microsemi

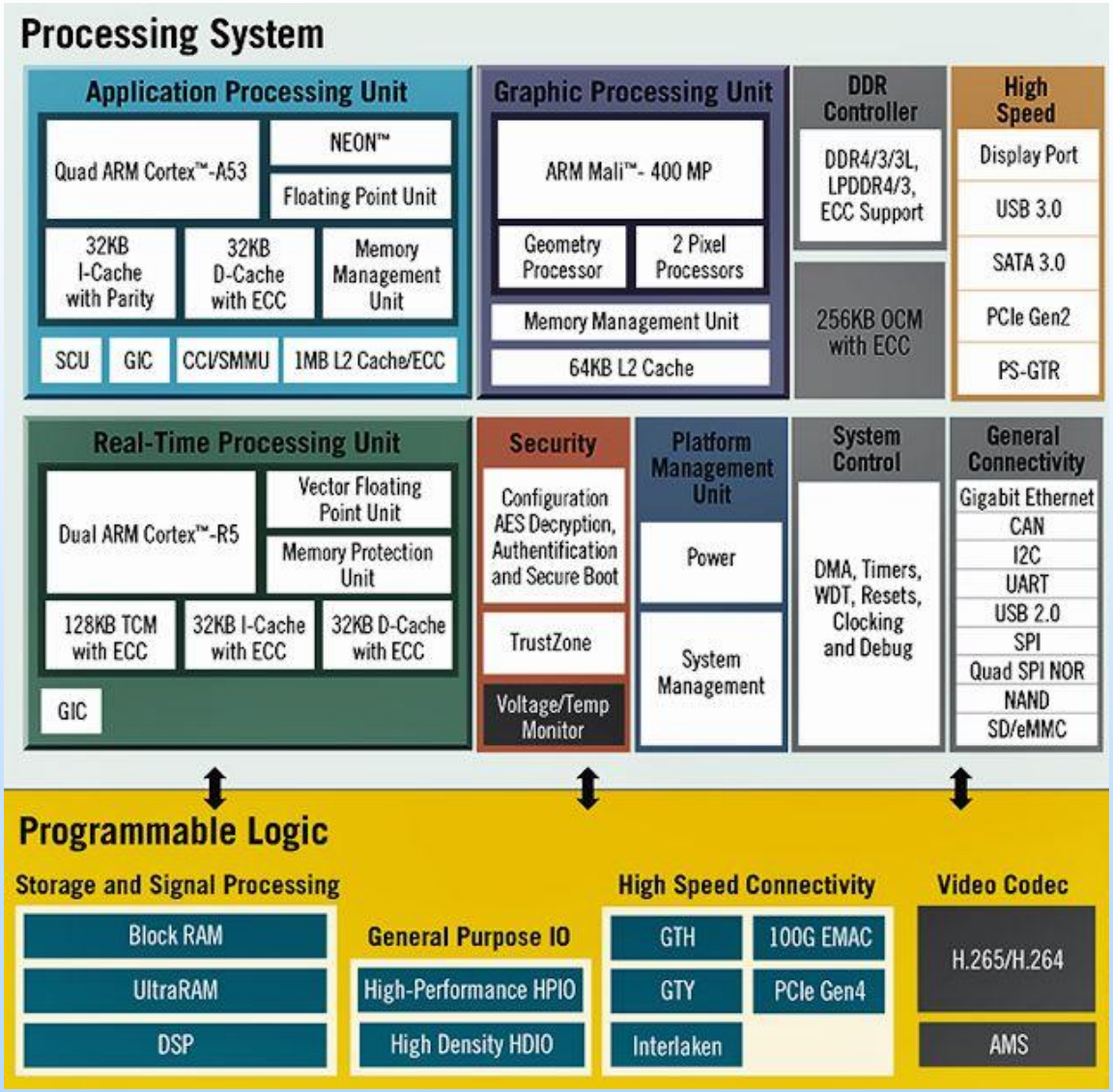
- **RTG4 (65nm RH)**

Xilinx

- **7 series (28nm commercial)**
- **Ultrascale (20nm commercial – planar)**
- **Ultrascale+ (16nm commercial - vertical)**
- **Virtex 5QV (65nm RH)**



Xilinx Zynq UltraScale+ Multi-Processor System on a Chip (MPSoC) family



From Xilinx.com

Advanced Processors

Next Generation Space Processor (NGSP)
- **Joint NASA-AFRL Program for RH multi-core processor**

TBD – (track status)

14nm CMOS Processors (w/Navy Crane)
- **Intel 14nm FinFET commercial**
  - **5th and 6th generation**
- **Samsung 14nm LP Snapdragon 820**

Radiation Testing

Radiation Testing

Freescale Processors
- **P2020 Communication Processor (w/Air Force)**
- **P5040 Network Processor**

Radiation Testing

Radiation Testing

RH Processor
- **BAE Systems RAD5510/5545**
  - **Leverages P5040 architecture**

Radiation Testing

Microcontrollers and Mobile Processors (Small Missions)

Radiation Testing

FY14 FY15 FY16 FY17

Note: Future considerations include adding Graphics Processing Units (GPUs) to NEPP Roadmap in FY17.

Commercial Memory Technology

- collaborative with Navy Crane

Other
- MRAM (Avalanche STT, other)
- FeRAM

TBD – (track status)

Resistive
- CBRAM (Adesto)
- ReRAM (Panasonic)
- ReRAM (Tezzaron)
- TBD (HP Labs, others)

Radiation and Reliability Testing → *45nm options*

Radiation and Reliability Testing

Radiation and Reliability Testing

TBD – (track status)

DDR
- Intelligent Memory (robust cell twinning)
- 1xnm DDR3, DDR4, LP (TBD)

Radiation Testing

Radiation and Reliability Testing

Hybrid or wide I/O
- HMC, HBM, Wide I/O

TBD – (track status or test)

FLASH
- Samsung VNAND (gen 1 and 2)
- Micron 16nm planar
- SK Hynix 3D, other commercial

Radiation and Reliability Testing

Radiation and Reliability Testing

Radiation and Reliability Testing

FY14 FY15 FY16 FY17

Alternate Grade Electronics: Automotive

- **NEPP has three goals for automotive electronics efforts**
  - **Determine exactly what :"automotive grade" does or does not entail.**
    - **Includes understanding:**
      - **Automotive Electronics Council (AEC) documents, and,**
      - **Manufacturer Production Part Approval Process (PPAP).**
  - **Perform "snapshot" screening and testing on representative automotive grade electronics.**
  - **Explore application of resilient automotive electronics system designs for space purposes.**

Automotive application constraints or standard compliance	To be implemented and managed at different levels			
	Audio IP	SoC	Application firmware/ software	PCB
Noisy ground(s) voltage	Common mode rejection			Passive components' accuracy
Audio perception and spatialization	THD+N, gain mismatch, Pop-up Noise	SoC routing resistance	Processing, starting and stopping sequences	Application Schematics consideration
Security	Primary diagnostic circuitry	Redundant audio interface	audio diagnostic firmware	Protection circuitry
High Temperature operation (AEC-Q100 Grade 0/1 qualification)	High performance at junction Temperature -40 °C to 125 °C	Package thermal dissipation consideration		PCB material and component soldering technology consideration

http://www.design-reuse.com/news_img/20141209_2.jpg

Small Missions/ Automotive

EEE Parts Guidelines

- **Small missions (Class D, CubeSat – 2 documents)**
- **System on a chip (SOC) single event effects (SEE) guideline**
- **Board-level proton test guideline**

Small Mission Commodities

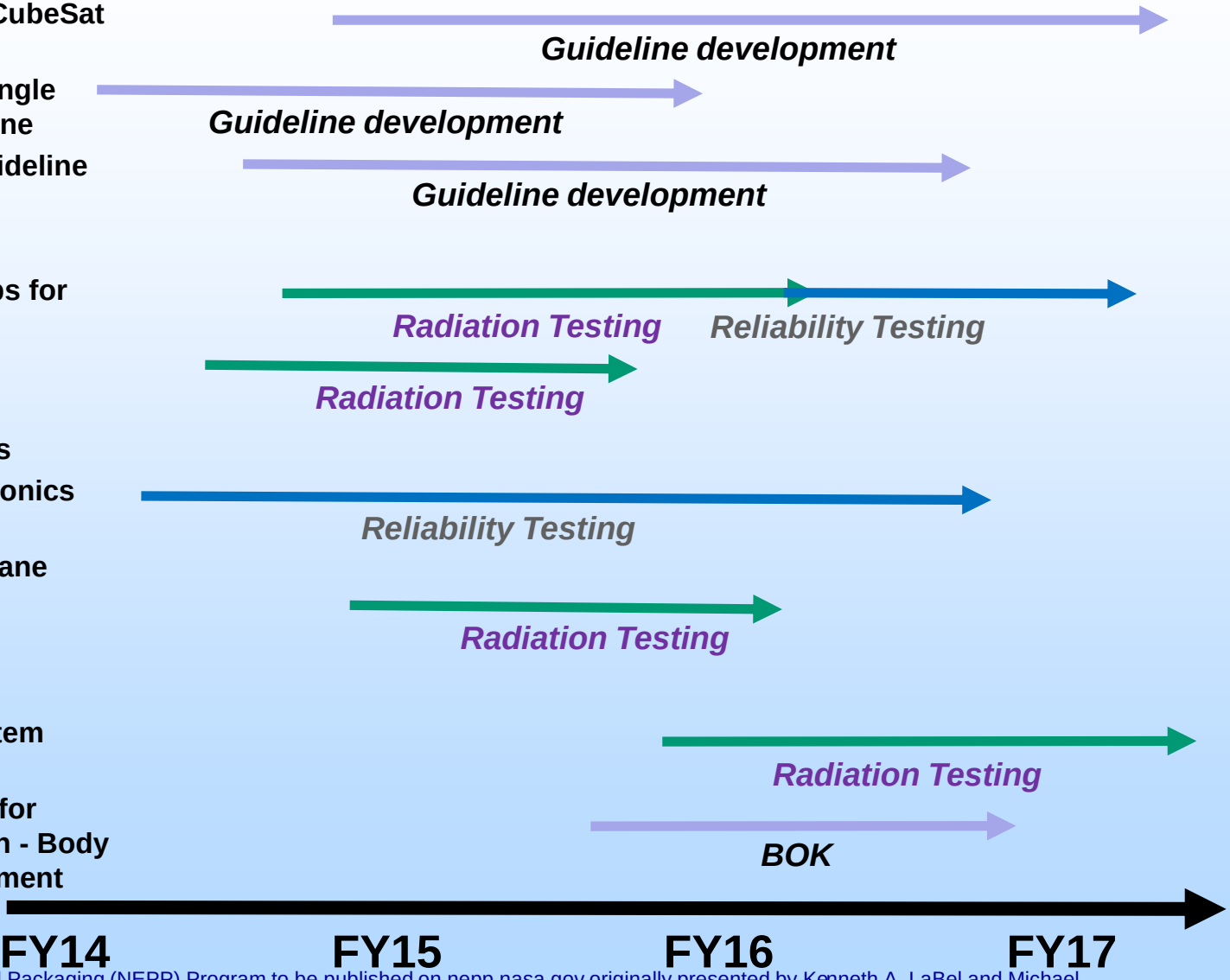
- **See commodities roadmaps for processors, power**
- **CubeSat Star Tracker**

Automotive grade electronics

- **Multiple classes of electronics (passives, actives, ICs)**
  - **NASA and Navy Crane**
- **Freescale MPC56XX**

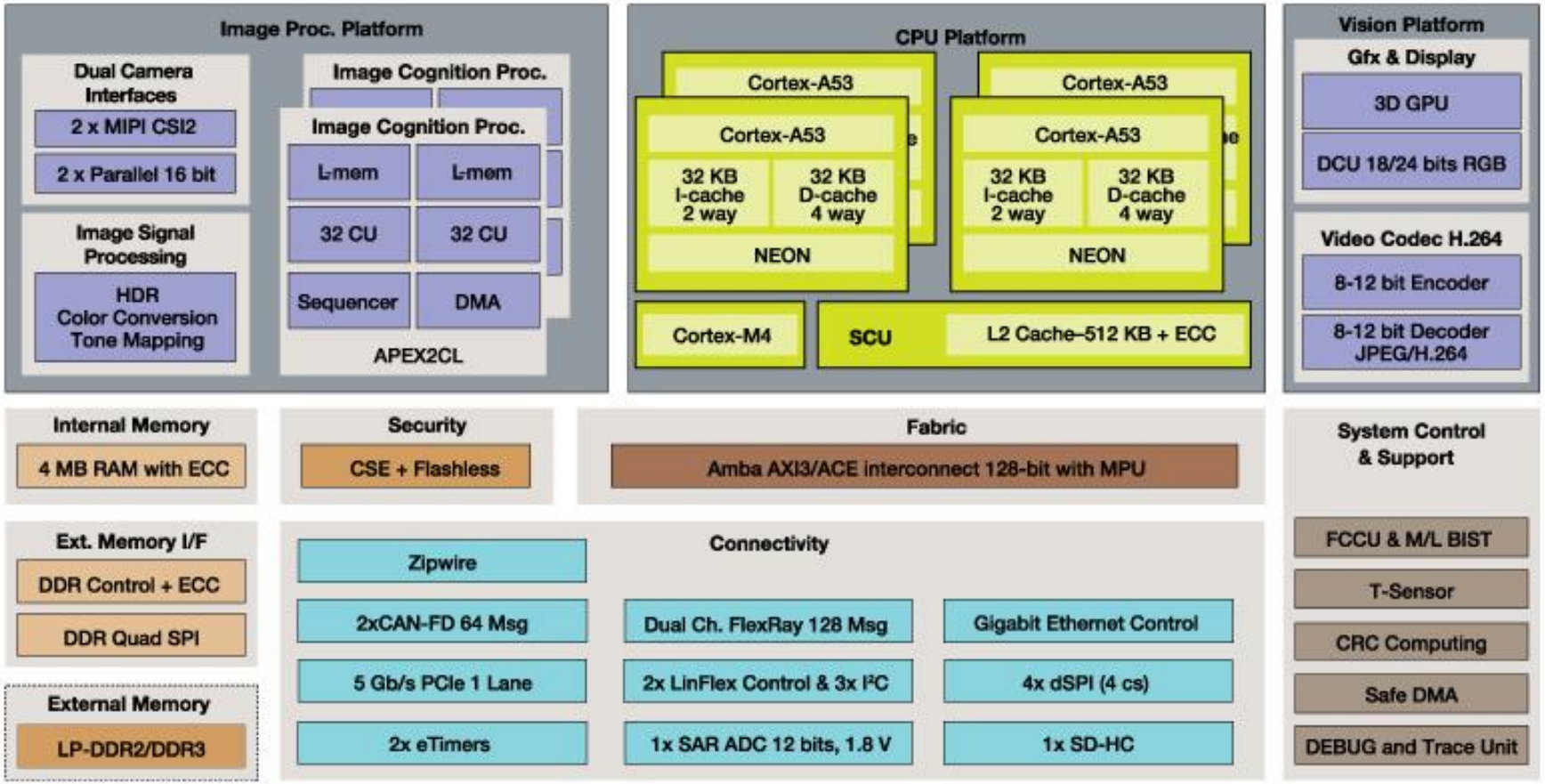
Alternate system tests

- **Automotive resilience system tests**
- **Use of board-level testing for screening and qualification - Body of Knowledge (BOK) document**



Automotive - Advanced Driver Assistance Systems (ADAS) for *Space*?

S32V234 Block Diagram



From Freescale.com

Power and Wide Band Gap (WBG) Devices

Si MOSFETs – Rad Hardened

- Microsemi i2MOS
- Infineon superjunction 100 V, 600 V (target)

Si Schottky Diodes

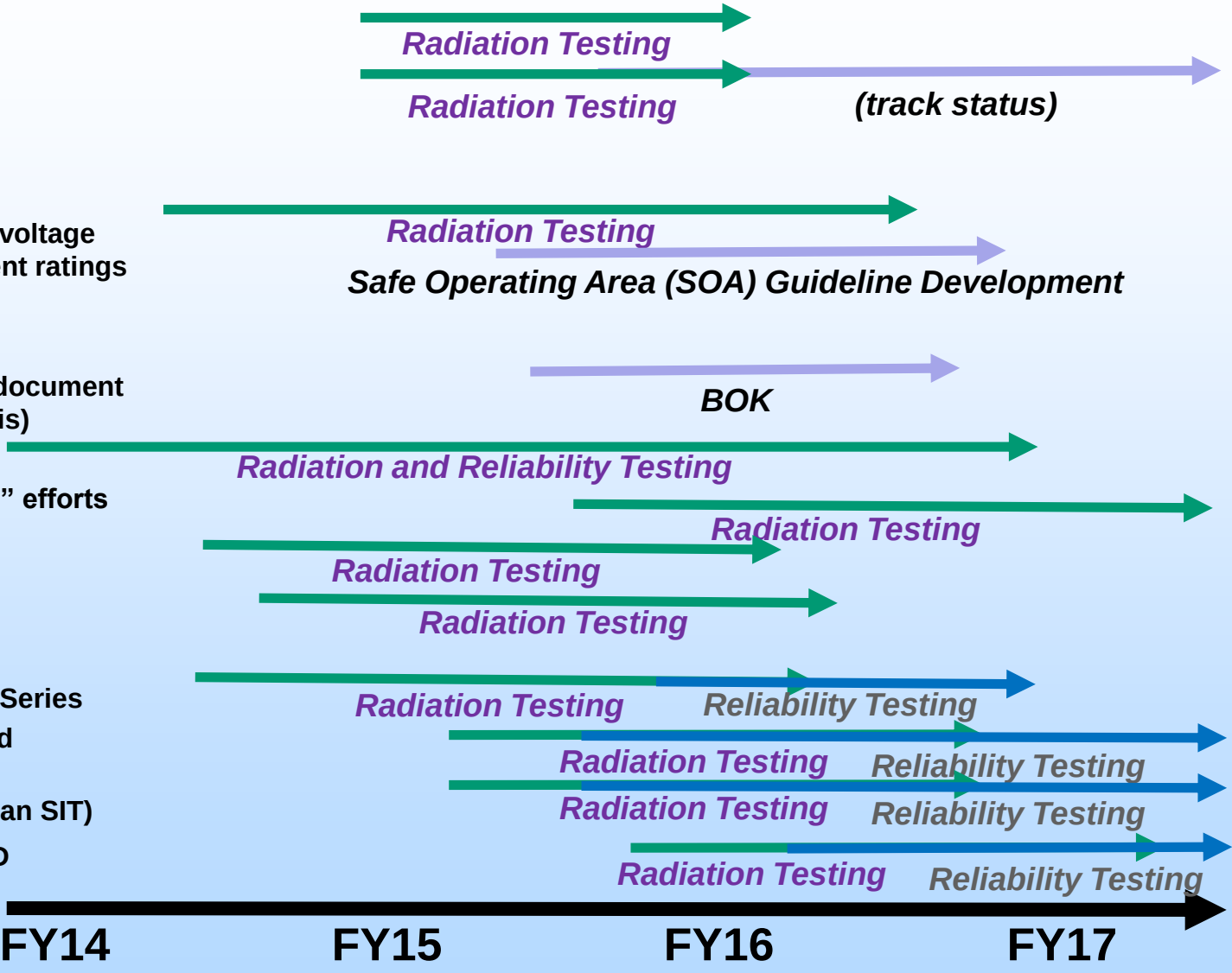
- Multiple vendors, reverse voltage ratings, and forward current ratings

SiC

- Body of Knowledge (BOK) document (knowledge and gap analysis)
- Cree Gen 1-3
- Collaboration w "hardening" efforts
- Baseline diodes
- Logic devices

GaN

- EPC 2012 (Gen3) and 8000 Series
- GaNSystems - GS61008 and GS66508 commercial
- Panasonic PGA26E19BA (Gan SIT)
- Thransphorm TPH3202PD (Cascode)



IC Packaging

High Density, Non-hermetic Column Grid Array (CGA)
- Xilinx CN/Kyocera Daisy Chain
- Microsemi Daisy Chain

Reliability Testing

Reliability Testing

HALT Methodology/Qualification
- HALT/HAST comparison
- Plastic BGA matrix

Reliability Testing

Reliability Testing

Area Array Column
- Selection guide

Guideline development

Thermal Interface Materials
- Selection guide

Guideline development

PBGA Thermal Cycle Evaluation

Reliability Testing

BOK ***Reliability Testing***

2.5/3D Packaging

QFN package reliability

Reliability Testing

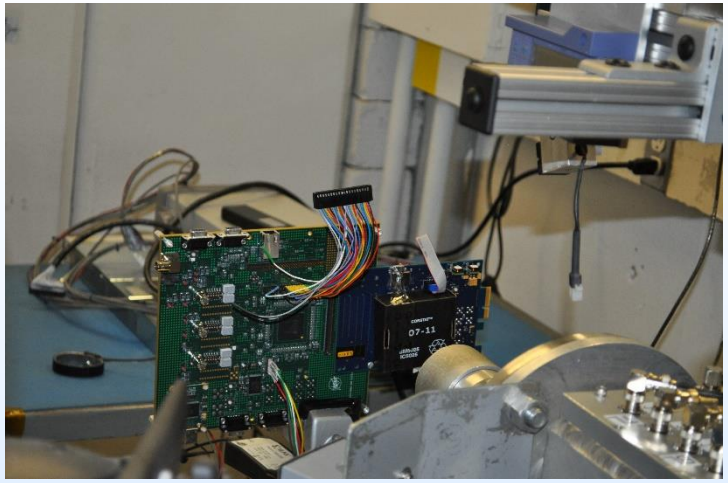
FY14 **FY15** **FY16** **FY17**

A Few Other Cool Tasks…

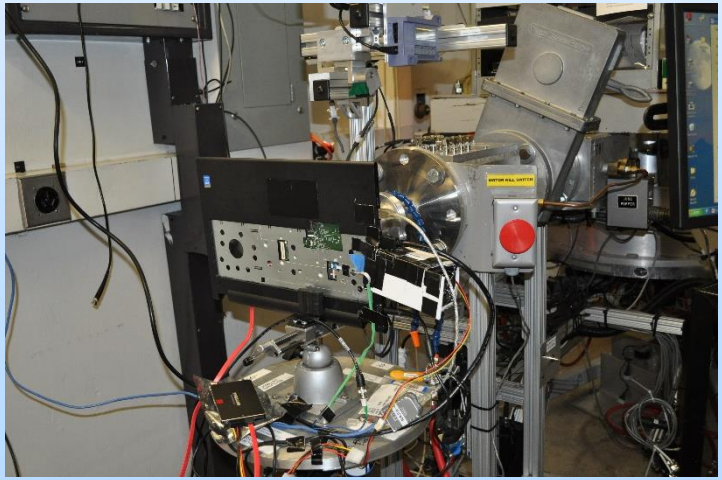
- CubeSat mission success/failure root cause analysis
  - Grant to Saint Louis University
- Using a model-based systems engineering (MBSE) approach to radiation assurance
  - Grant to Vanderbilt
  - Co-sponsored by NASA Reliability and Maintainability Program
  - Uses a tool called “Goal Structured Notation”
- Keeping the CRÈME website alive
  - Support to Vanderbilt
  - Just standard maintenance and operation, no upgrades
- Proton test facilities
  - Come to SEE-MAPLD (Single Event Effects Symposium – Military and Aerospace Programmable Logic Devices Workshop) or NEPP ETW for updates

Radiation Highlights

- Independent heavy ion testing of Microsemi RTG4 FPGA
  - Collaboration with AF/The Aerospace Corp
  - Presentations planned for SEE-MAPLD and NEPP ETW
- Heavy ion single event safe operating area (SOA) for Schottky Diodes
  - Presentations planned for SEE-MAPLD and NEPP ETW
  - Guideline planned by end of FY
- Processors
  - Collaboration with Navy Crane
  - State of the art technology (1x nm CMOS) evaluation
  - Presentations planned for NEPP ETW
- Protons
  - Board level test guideline
    - Presentations planned for SEE-MAPLD and NEPP ETW



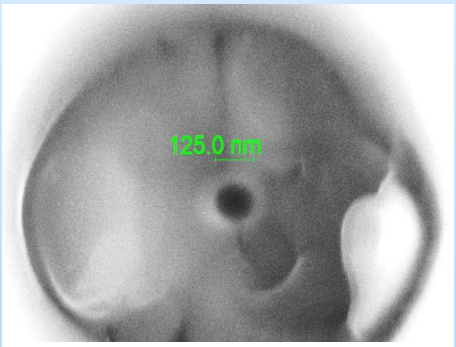
Testing of RTG4 at Texas A&M Cyclotron (TAMU), Ken LaBel



Testing of Intel Broadwell Processor at TAMU, Ken LaBel

Mike's "Highlights and Concerns"

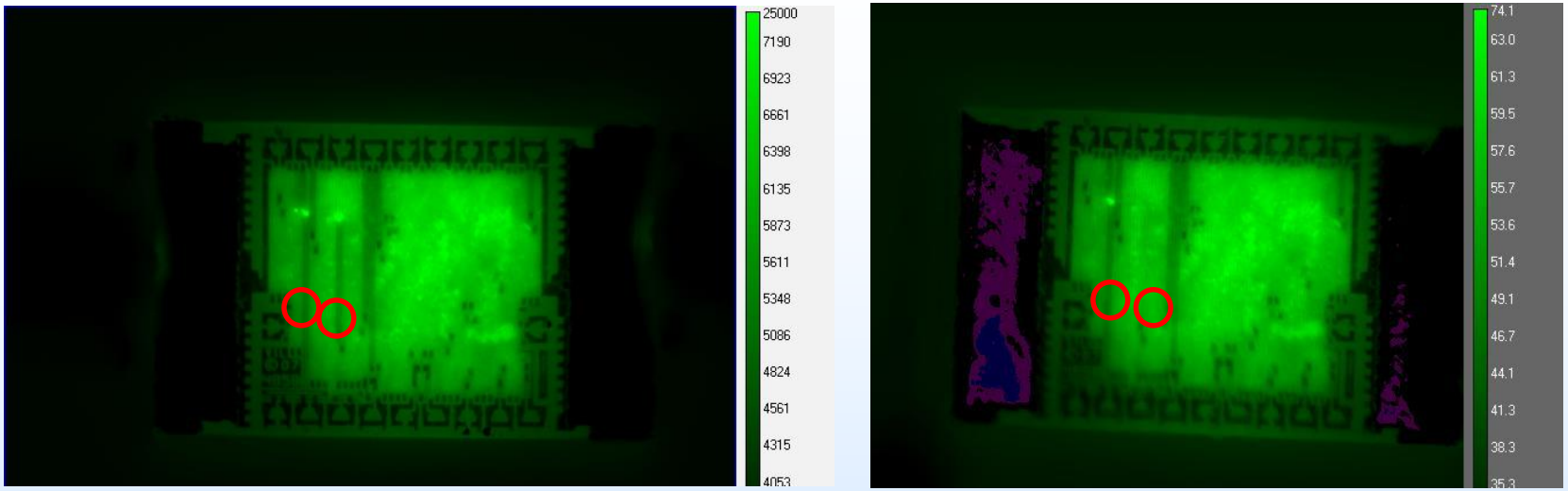
- *NEPAG celebrates 15 years of stimulating, weekly discussions and knowledge interchange that is/has been Educational, Influential, Collaborative, and Current*
- **New NASA Standard, "Electrical, Electronic, and Electromechanical (EEE) Parts Management and Control Requirements for Space Flight Hardware & Critical Ground Support Equipment" in NASA review cycle**
  - **Standardizes around current, Center- specific and shared practices**
  - **Covers selection, acquisition, traceability, testing, handling, packaging, storage, and application of EEE parts**
  - **Includes radiation, prohibited materials and counterfeit avoidance**
- **Hermeticity/ Internal Gas Analysis**
  - **NEPAG has a focus on hermeticity testing**
  - **Concerned there is no optimum test for gross leak**
  - **Gross leak escapes are riskier than fine leak ones - liquid versus gaseous contamination**
  - **NASA prototyped a gross leak standard**
- **IC Packaging Temp Cycling**
  - **Should the temp range mirror the device Tj rating or use IPC recommendation for 0 to 100C or ???**



Hole in TO-46 package

Courtesy NEPP/MSFC

Metal Foil Resistor Screening



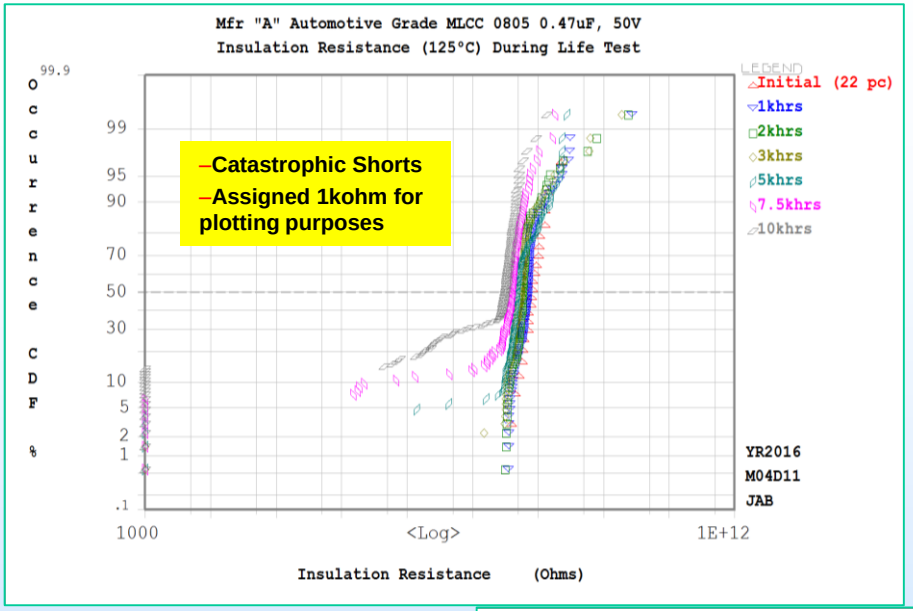
Courtesy NEPP/GSFC

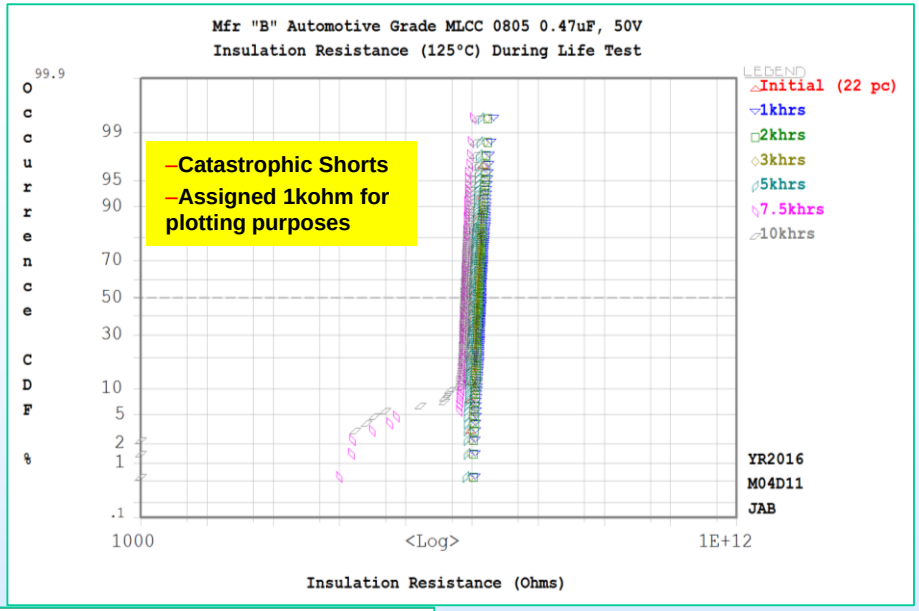
- **Thermal imaging identifies "hot spots" - defects in the resistor pattern.**
- **The hot spots can be "seen" through the coating on this chip resistor**
- **Life testing is showing the foil at these locations, can break under the stress**
- **Hot spots visible in infrared before (left) and after (right) a 2000hr life test**
- **Disappearing hot spots correspond to metal bridges opening up**
- **Was electrically verified as an ~11,000ppm shift in resistance**
- **Manufacturer participating in this evaluation**
- **Goal is for the manufacturer to adopt as a screen for space grade parts**

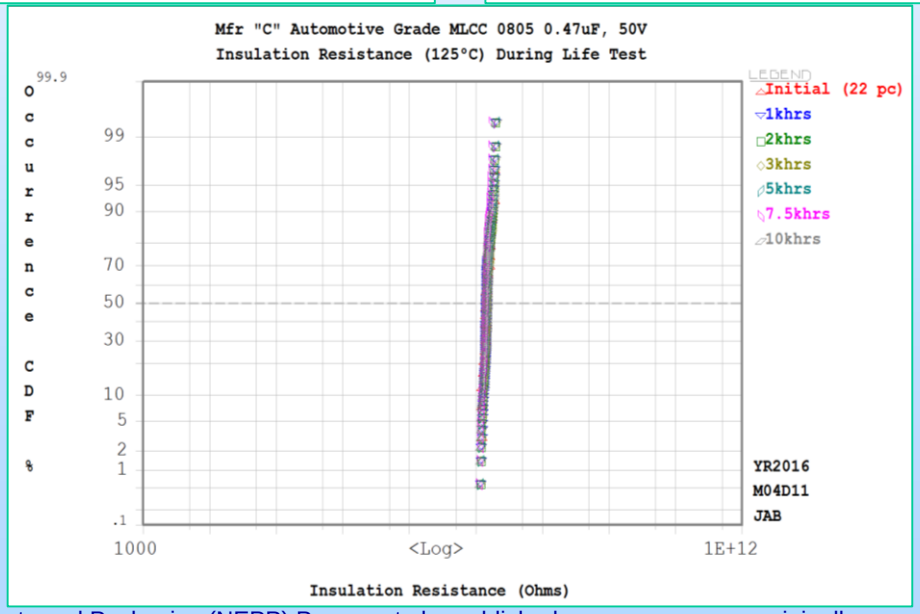
NEPP Evaluation of Automotive Grade EEE Parts

Manufacturer	Lot Code	Description	Quantity on Test	Life Testing Status	Comments
A	1302	Ceramic Chip Capacitor, 0805, 0.47uF, 50V	120	10khrs	120 pcs on test. 17 catastophic life test failures with first occurring ~3.1khrs
B	1304		120	10khrs	120 pcs on test. IR degradation noticed @7.5khrs; 3 catastrophic failures beyond 8khrs of test
C	1131		120	10khrs	120 pcs on test. No Catastrophic Life Test Failures
D	201028	Ceramic Chip Capacitor, 0402, 0.01uF, 16V	78	>2k Hrs	few devices exhibit reduced IR (non-catastrophic)
E	TBD		80	>2k Hrs	few devices exhibit reduced IR (non-catastrophic)
F	1247		79	>2k Hrs	Stable IR thus far. Note: Precious Metal Electrode
G	TBD	Microciruit, Transceiver	50	Not yet started	Initial Electricals in Progress
H	1152	Microciruit, Comparator	50	Not yet started	Initial Electricals in Progress
I	1341	Microciruit, Op Amp	50	Not yet started	Test Program in Development
J	unknown	Dual small signal NPN Bipolar transistor (similar to 2N2919 and 2N2920 MIL-PRF-19500/355)	20	>4.5k Hrs	1 failure at 1k Hrs. Failure may be handling related. Life test has completed 4.5khrs with no additional failures. Life test continuing to 5.5khrs or until a failure occurs
K	1339	Switching diode (similar to 1N4148, MIL-PRF-19500/116)	20	Not yet started	Radiography completed. Initial electrical testing completed. High Temp Reverse Bias burn-in will be starting soon
L	unknown	Transient Voltage Suppressor, 36V minimum breakdown voltage, 400 watt peak pulse power	20	Not yet started	Parts Procured. Test Plan is being reviewed at Crane. Electrical test and life test boards to be fabricated

AECQ Ceramic Chip Capacitors, Insulation Resistance at 125ºC







Upcoming NEPP Challenges

- **Complexity issues for inspection, screening, device preparation, and test**
  - **2.5/3D Packages/ICs**
  - **Package on Package (PoP) Commercial Devices**
  - **An FPGA combined with an SOC (MPSOC+ from Xilinx)**
  - **Cu Wirebonds**
- **Assurance**
  - **Automotive and catalog commercial EEE parts?**
  - **Increasing risk with a worldwide supplier base**
    - **Traceability**
    - **Change control**
    - **Screening?**
  - **Consolidation.**
    - ***What if the only source left is in an inhospitable or unauditable part of the world?***

Summary and Comments

- **NEPP Roadmaps and Tasks are constantly evolving as technology and products become available.**
  - **Like all technology roadmaps, NEPP's is limited to funding and resource availability.**
  - **Not shown are TBD passives and connector roadmaps under development.**
  - **Partnering is the key:**
    - **Government,**
    - **Industry, and,**
    - **University.**
- **We look forward to further opportunities to partner.**

https://nepp.nasa.gov

Upcoming

- **7th Annual NEPP Electronics Technology Workshop**
  - **June 13-16, 2016**
  - **NASA/GSFC (on-site) plus web access available**
    - **Registration is open!** ***https://nepp.nasa.gov/workshops/etw2016/***
    - **On-site limited to U.S. and green card only**
  - **Highlights of NEPP tasks**
  - **HiREV day**
  - **Special topics include:**
    - **Automotive electronics and SiC power devices**
    - **2.5/3D ICs and proton testing splinter groups**

Notional NEPP ETW Schedule

Mon	13-Jun	Tues	14-Jun	Wed	15-Jun	Thurs	16-Jun
Assurance		**COTS and CubeSats**		**Technology Focus Day**		**NEPP, HiREV**	
NEPP Mission		NEPP Technology Roadmap	**Ken LaBel - NASA**	Automotive Electronics - NEPP Overview	**Michael Sampson - NASA**	Invited Reliability	
NASA Parts Standard	**Peter Majewicz - NASA/LaRC**	CubeSat Success Analysis	**Prof. Michael Swartwout, St. Louis University**	Automotive Electronics - Special Session	ADAS and ECC DRAMs - **Ivan Ivanov, Micron**; Autonomous Car is the New Driver for Resilient Computing and Design-for-Test - **Nirmal Saxena - NVIDIA**	HiREV	
Thermal Signature of a Resistor - And Problems Encountered Along the Way	**Jack Shue, et al NASA/GSFC**	Cubesat COTS Efforts	CubeSat Star Tracker - **Farokh Irom - JPL**, CubeSat Processing - **Steve Guertin - JPL**, CubeSat Power Update - **Leif Scheick - JPL**		Leveraging Test Capabilities from Other Communities - **Zef Malik, Silicon Turnkey**; Automotive Electronics and PPAP - **Eli Kawam, Microchip**		
MIL/JEDEC Standards Update (includes underfill)	**Shri Agarwal - JPL**	RHA for Small Missions	**Michael Campola - NASA/GSFC**	SiC Special Session	**NY PEMC Capabilities and SiC Electronics, Alexey Vert, NY-PEMC**		
Cu Bond Wire and PEM update – Requirement Documentation and Data	**S. Ali Lilani, Integra Technologies LLC**	FPGAs			**Anant Agarwal, US Department of Energy; David Grider - Wolfspeed**		
Laser Ablation and Chemical Decapsulation for Copper Wirebonds	**Trevor Devaney, Hi-Rel Labs**			NEPP SiC Overview	**TBD - NASA**		
Future of QML Hermetic ICs	**Tim Flaherty, Golden Altos Corporation**			2.5/3D Packaging Overview and Challenges	**Robert Patti, Tezzaron**	NEPP GaN	**Leif Scheick - JPL**
Hermeticity Update	**Pat McManus - NASA/MSFC**	Processing Session	Processors - Freescale, Intel, and more - **Steve Guertin - JPL, TBD**	Proton Test Facilities and Testing	**Ken LaBel - NASA; Steve Guertin - JPL**	NEPP - HiREV Splinter	
Radiation Assurance	RHA Guideline - Michael Campola - NASA/GSFC, Board-level Proton Test Guideline - Steve Guertin - JPL, Schottky Diode SOA - Megan Casey - NASA/GSFC; Future RHA: Alternate Assurance Approach (R&M) - **TBD, Vanderbilt University**		Automotive Microcontroller - **Ted Wilcox - AS&D/NASA**	Splinter 1: 2.5/3D Packaging - future assurance challenge	Splinter 2: Proton test and facilities		