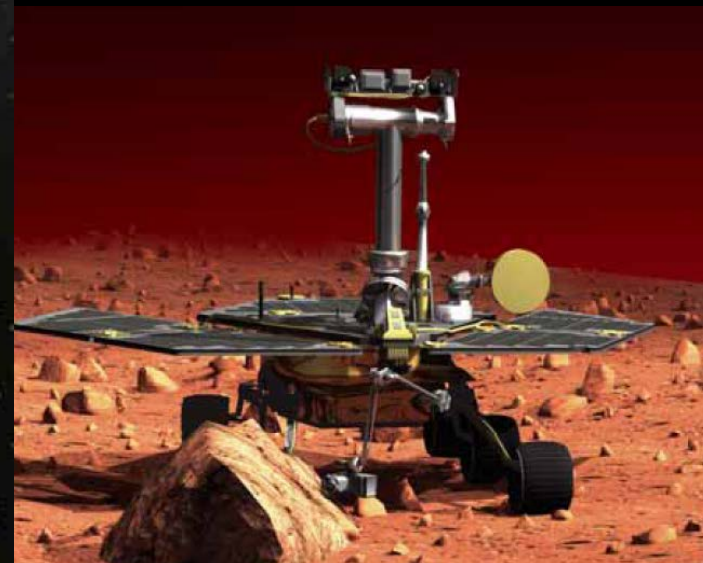
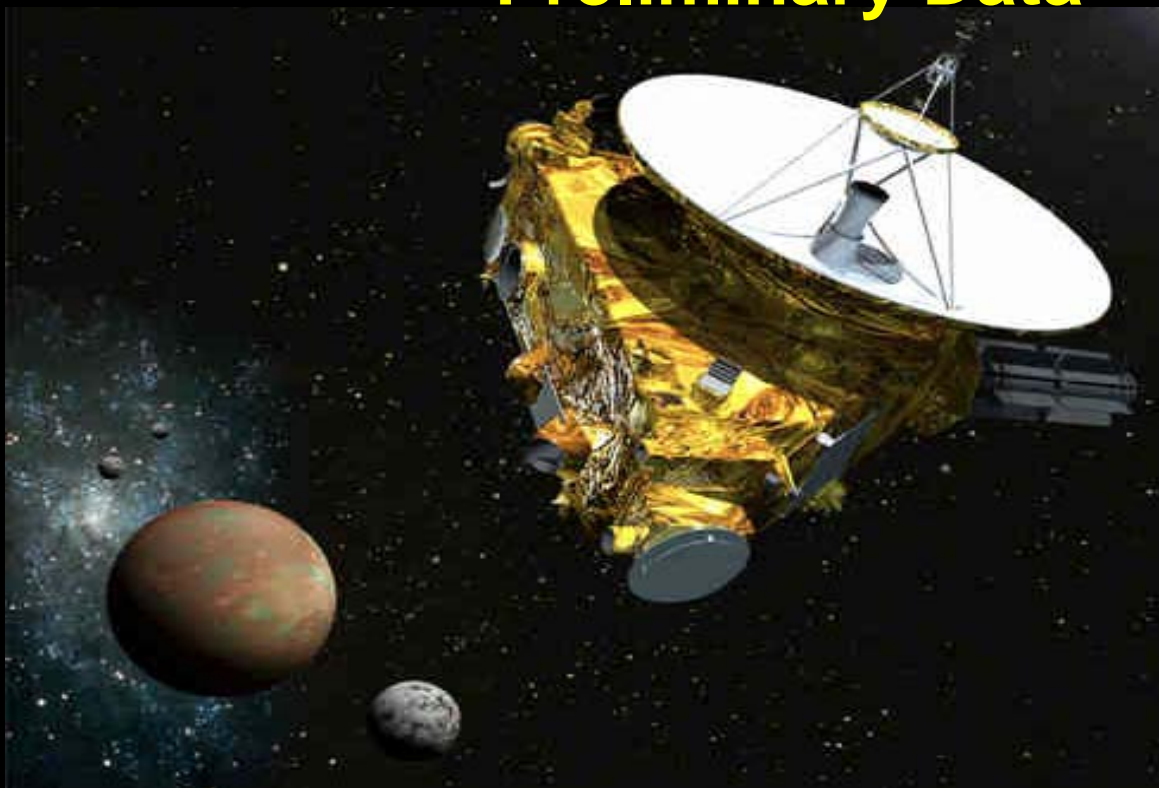


Independent Single Event Upset Testing of the Microsemi RTG4: Preliminary Data



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and Ken LaBel, NASA/GSFC**



Acronyms

- **Clock conditioning Circuit (CCC)**
- **Combinatorial logic (CL)**
- **Design under analysis (DUA)**
- **Device under test (DUT)**
- **Edge-triggered flip-flops (DFFs)**
- **Field programmable gate array (FPGA)**
- **FDDR: Double Data Rate Interface Control;**
- **Global triple modular redundancy (GTMR)**
- **Hardware description language (HDL)**
- **Input – output (I/O)**
- **Linear energy transfer (LET)**
- **Local triple modular redundancy (LTMR)**
- **Look up table (LUT)**
- **NASA Electronics Parts and Packaging (NEPP)**
- **Operational frequency (*fs*)**
- **PLL: Phase locked loop**
- **POR: Power on reset**
- **Radiation Effects and Analysis Group (REAG)**
- **SERDES: Serial-De-serializer**
- **Single Error Correct Double Error Detect**
- **Single event functional interrupt (SEFI)**
- **Single event effects (SEEs)**
- **Single event transient (SET)**
- **Single event upset (SEU)**
- **Single event upset cross-section (σ_{SEU})**
- **Static random access memory (SRAM)**
- **Static timing analysis (STA)**
- **Triple modular redundancy (TMR)**
- **Windowed shift register (WSR)**



Introduction

- **This is a NASA Electronics Parts and Packaging (NEPP) independent investigation to determine the single event destructive and transient susceptibility of the Microsemi RTG4 device (DUT).**
- **For evaluation: the DUT is configured to have various test structures that are geared to measure specific potential single event effect (SEE) susceptibilities of the device.**
- **Design/Device susceptibility is determined by monitoring the DUT for Single Event Transient (SET) and Single Event Upset (SEU) induced faults by exposing the DUT to a heavy-ion beam.**
- **Potential Single Event Latch-up (SEL) is checked throughout heavy-ion testing by monitoring device current.**

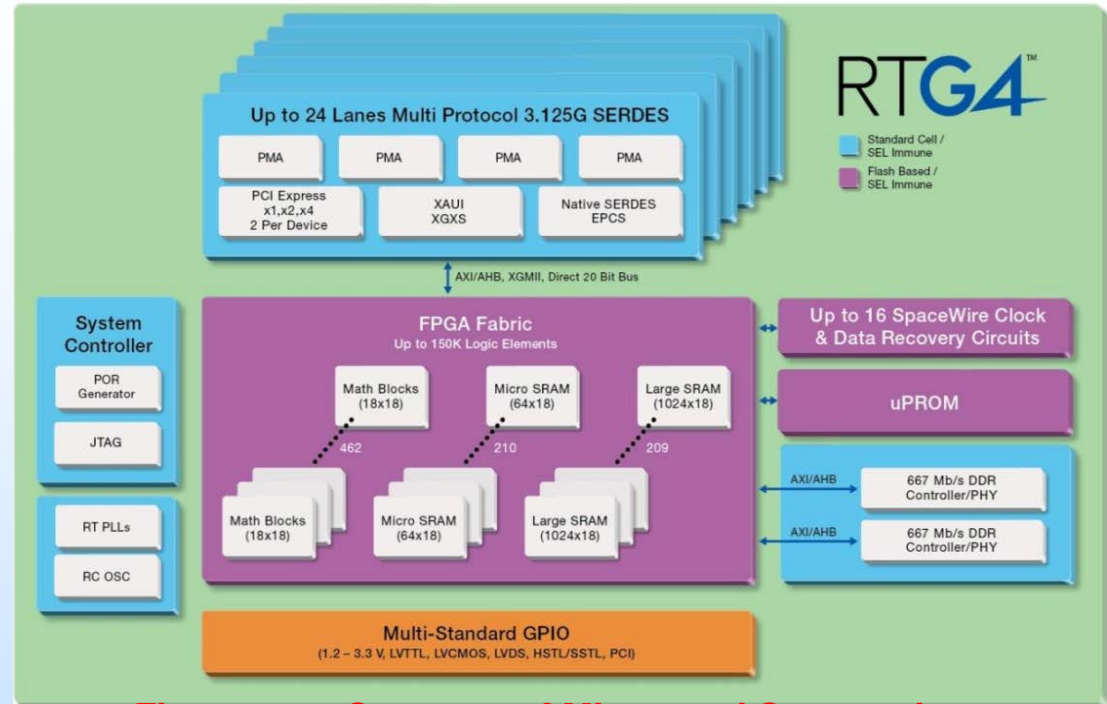
Preliminary Investigation Objective for DUT Functional SEE Response



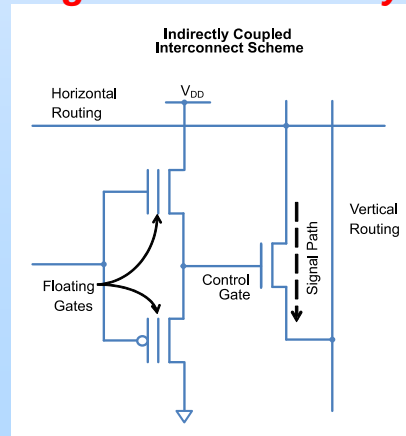
- **The preliminary objective, of this study, is to analyze operational responses while the DUT is exposed to ionizing particles.**
- **Specific analysis considerations:**
 - **Analyze flip-flop (DFF) behavior in simple designs such as shift registers.**
 - **Compare SEU behavior to more complex designs such as counters. Evaluating the data trends will help in extrapolating test data to actual project-designs.**
 - **Analyze global route behavior – clocks, resets.**
 - **Analyze configuration susceptibility. This includes configuration cell upsets and re-programmability susceptibility.**
 - **Analyze potential single event latch-up.**

Microsemi RTG4: Device Under Test (DUT)

- The DUT : RT4G150-CG1657M.
- We tested Rev B and Rev C devices.
- The DUT contains:
 - 158214 look up tables (4-input LUTs);
 - 158214 flip-flops (DFFs); 720 user I/O;
 - 210K Micro-SRAM (uSRAM) bits;
 - 209 18Kblocks of Large-SRAM (LSRAM);
 - 462 Math logic blocks (DSP Blocks);
 - 8 PLLs;
 - 48 H-chip global routes (radiation-hardened global routes);



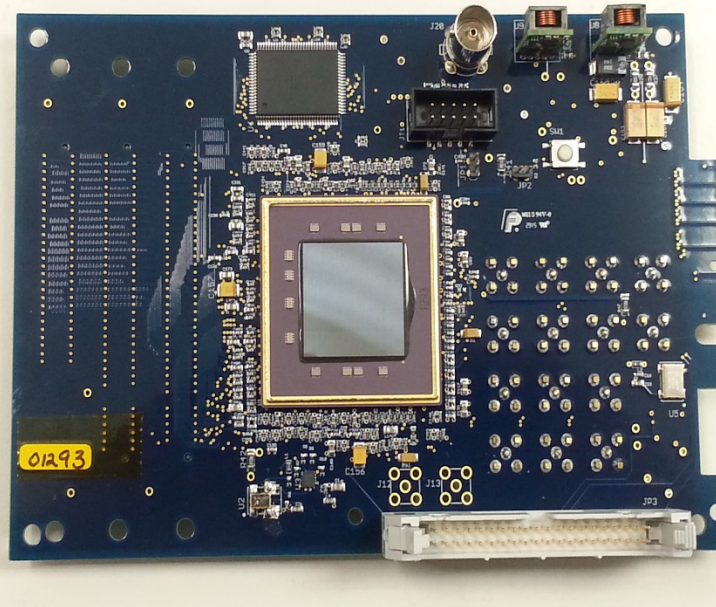
Figures are Courtesy of Microsemi Corporation.



U - Protected Flip-Flop

DUT Preparation

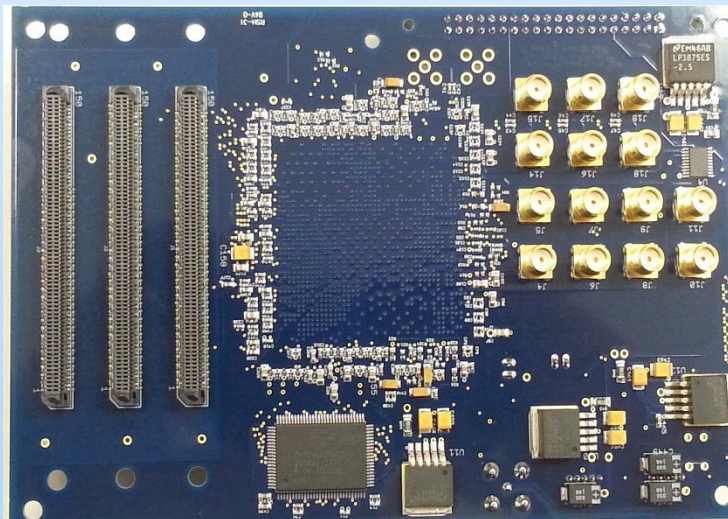
- NEPP has populated two Rev B and one populated Rev C boards with RT4G150-CG1657M devices.
- The parts (DUTs) were thinned using mechanical etching via an Ultra Tec ASAP-1 device preparation system.
- The parts have been successfully thinned to 70um – 90um.



*Top Side
of DUT*



*Ultra Tec
ASAP-1*



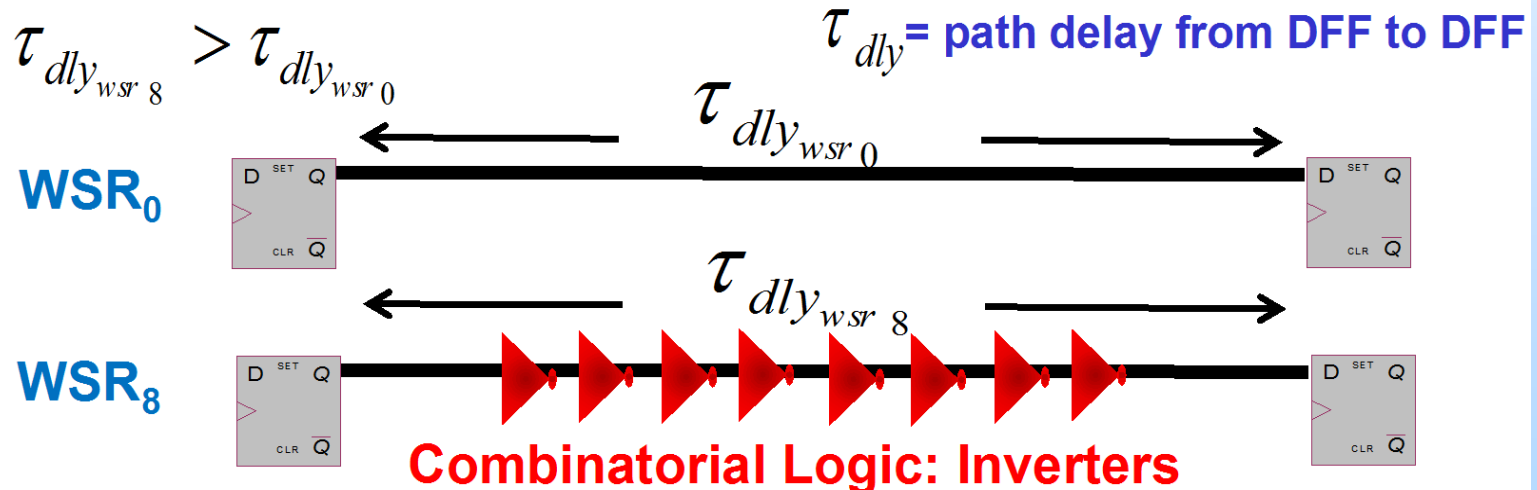
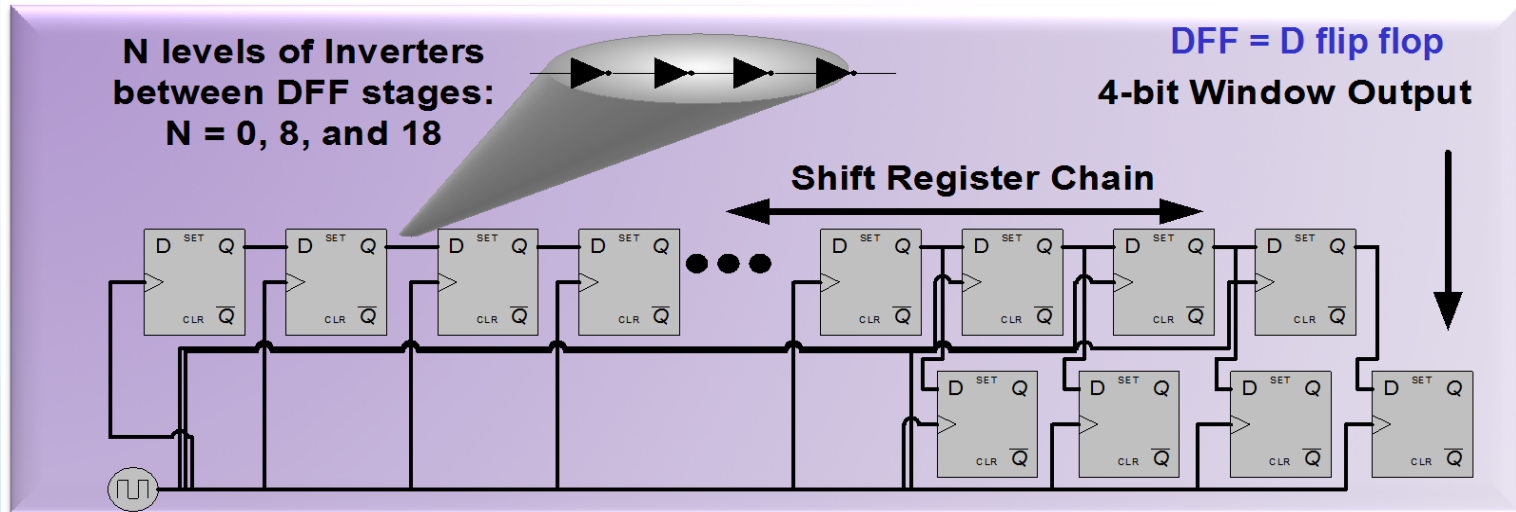
*Bottom Side of
DUT*

Summary of Test Structures and Operation

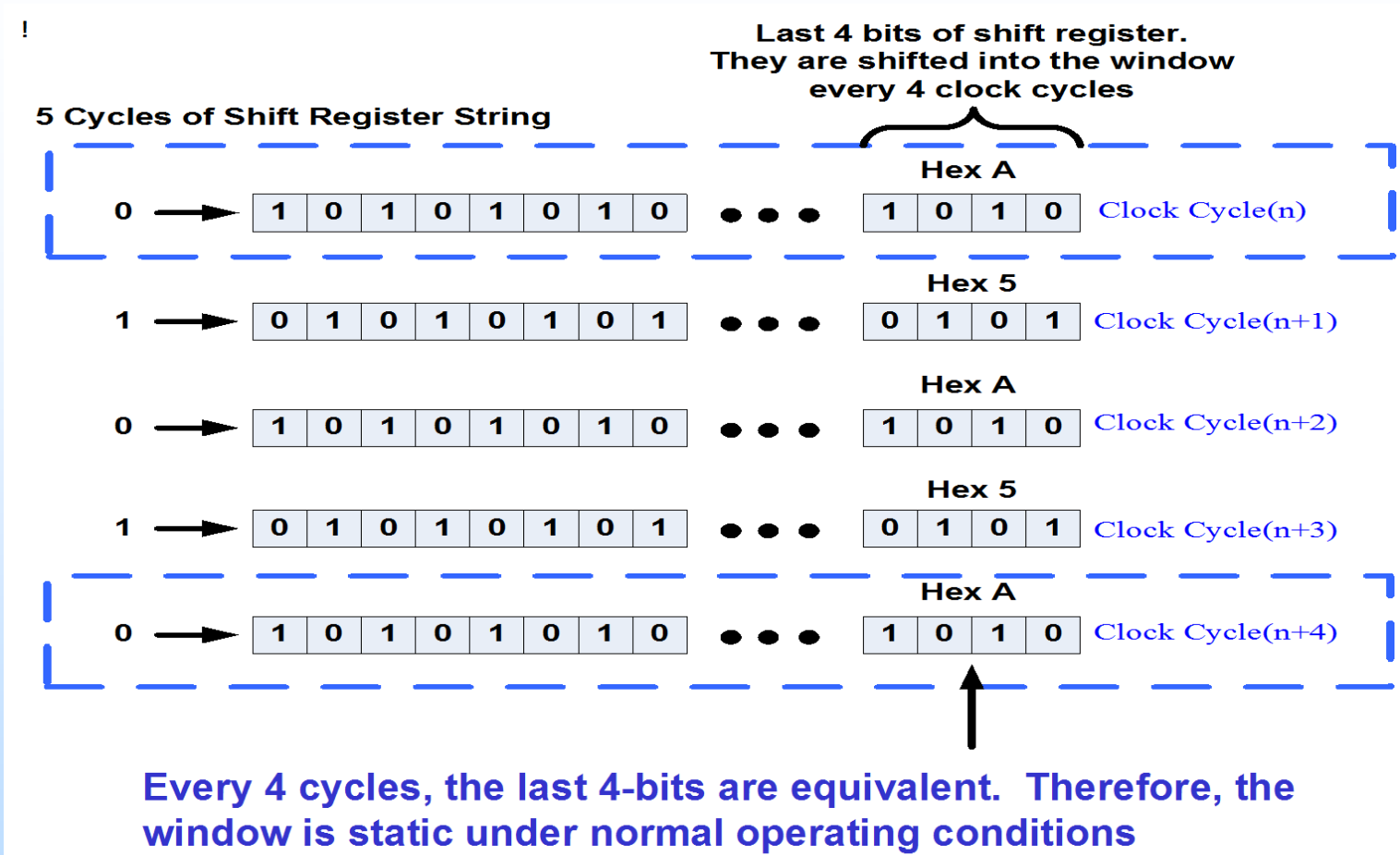


- **Windowed Shift Registers (WSRs):**
 - All designs contained four separate WSR chains.
 - Chains either had 0 inverters, 4 inverters, 8 inverters, or 16 inverters.
 - Resets were either synchronous or asynchronous.
 - Input data patterns varied: checkerboard, all 1's, and all 0's.
- **Counter Arrays (data not presented today):**
 - Resets are synchronous.
 - 200 counters in one array.
 - Two full arrays (400 counters total) in each DUT.
- **Frequency was varied for all designs.**
- **All DFFs were connected to a clock that was routed via RTG4 hard global routes (CLKINT or CLKBUF).**
 - This was verified by CAD summary output and visual schematic-output inspection.

Windowed Shift Registers (WSRs): Test Structure



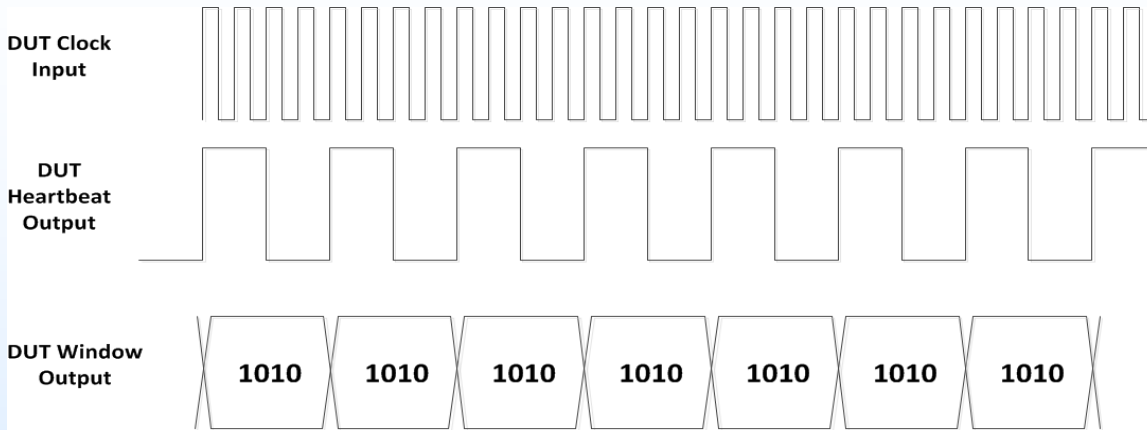
WSR Operation



Output never changes!

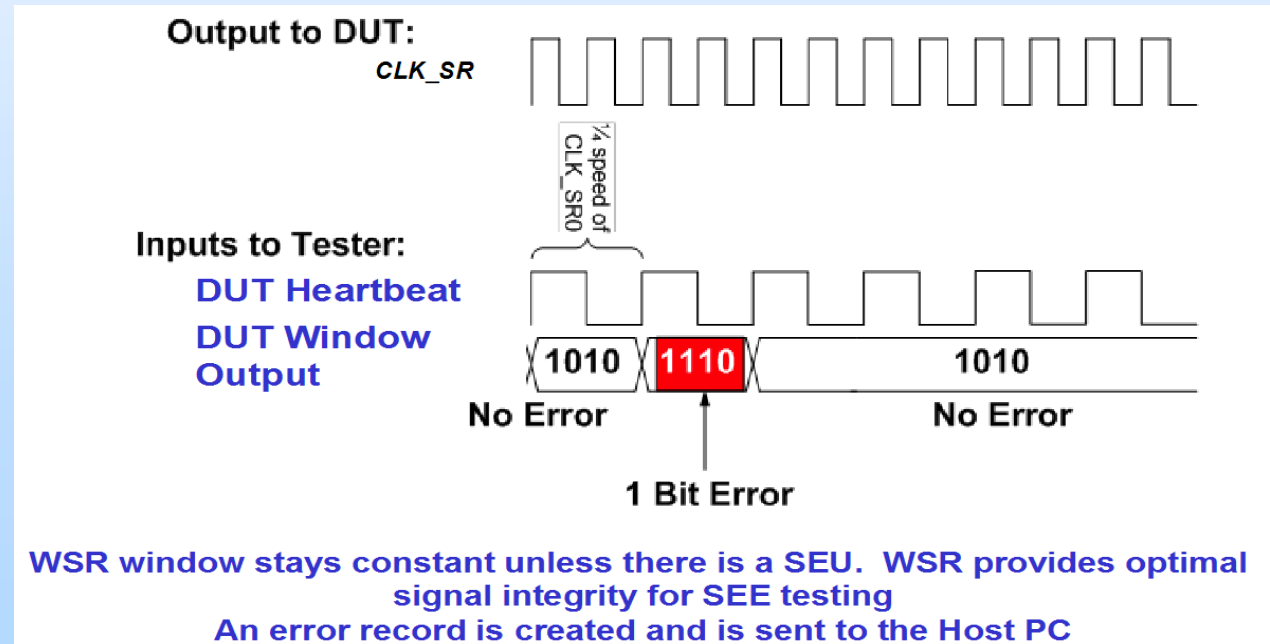
We choose WSR's over conventional shift registers because of increased signal integrity across the tester/daughter interface. Great for high speed internal DUT operation.

Errors in WSRs



No Error, output for one WSR is always “1010” or “0101”

Upon Error, output for one WSR will either: change by one bit, multiple bits, or change from “1010” to “0101”.



Microsemi RTG4 Clock Conditioning Circuit (CCC)

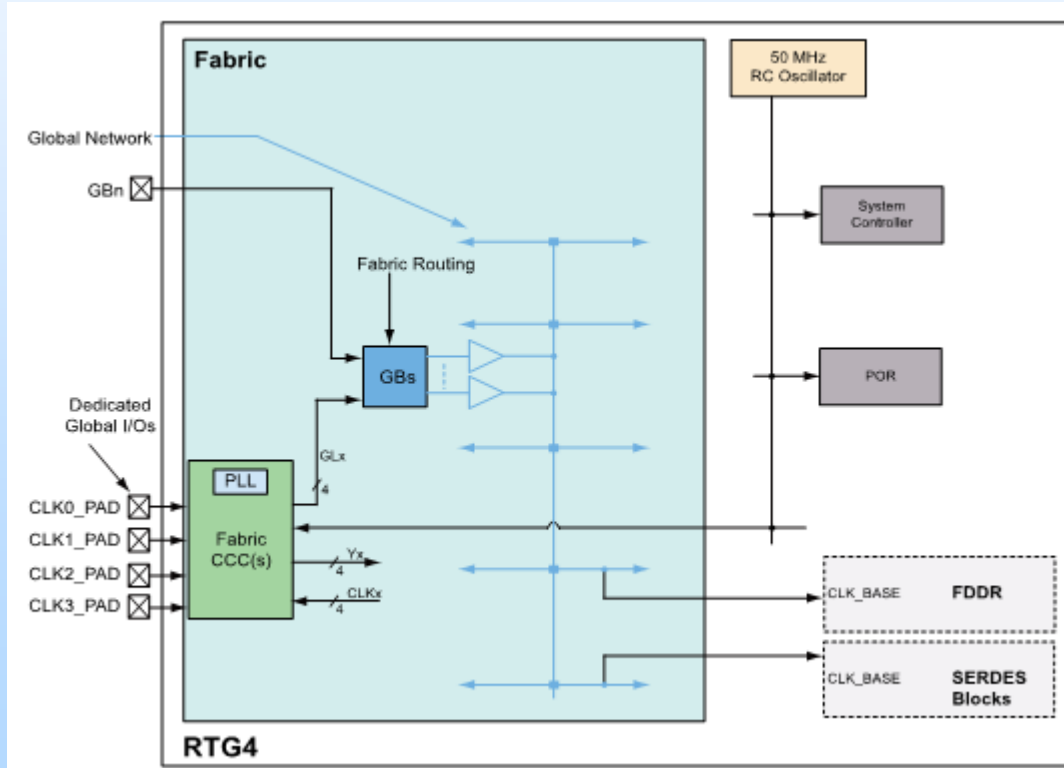


FDDR: Double Data Rate Interface Control;
SERDES: Serial-De-serializer;
POR: Power on reset;
PLL: Phase locked loop;
GBn: global network;
DGBIO: dedicated global I/O pad.

- **CLKBUF:** Hardened global route. Input can only be a DGBIO pad.
- **CLKINT:** Hardened global route. Input can come from fabric or any input.

Figure is Courtesy of Microsemi Corporation.

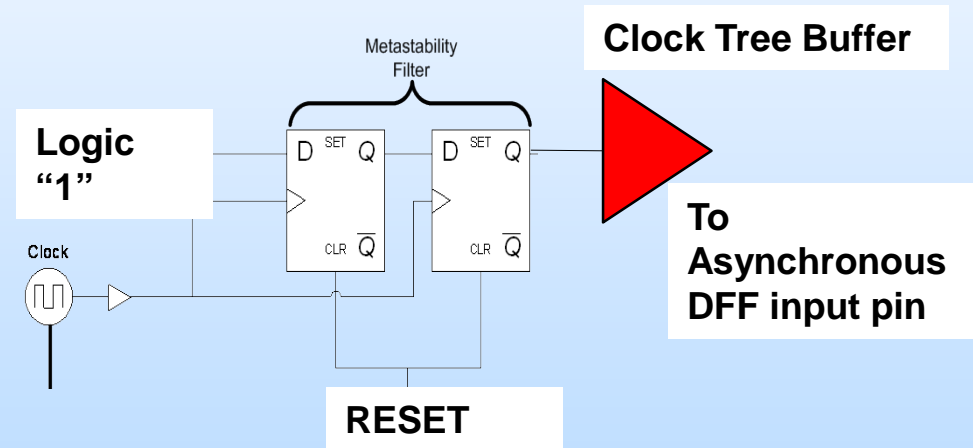
- **User can connect:**
 - From DGBIO pad to CLKINT,
 - FROM DGBIO pad to CCC-PLL to CLKINT,
 - From DGBIO pad to CLKBUF,
 - From normal input to CLKINT,
 - From normal input to CCC-PLL to CLKINT.



Asynchronous Assert Synchronous De-Assert Resets (AASD)



- AASD is the traditional method of reset implementation in NASA driven systems.
- This is a requirement for the protection of a mission in case of loss-of-clock.
- Synchronization is performed prior to clock tree connection.
- The AASD global reset is connected to the asynchronous pin of each DFF, however, it is synchronized to the clock and is hence synchronous.
- The reset synchronization is not in the data path. This allows for faster operation.





Microsemi RTG4 WSR Test Conditions

- **Temperature range: Room temperature**
- **Facility: Texas A&M.**
- **Performed December 2015, March 2016, and May 2016.**
- **NEPP Low Cost Digital Tester (LCDT) and custom DUT board.**
- **Tests pertaining to results provided in this presentation:**
 - **4 separate WSR chains with 1000 DFFs:**
 - **WSR₀: 800 DFFs with no inverters between DFF stages.**
 - **WSR₄: 800 DFFs with 4 inverters between DFF stages.**
 - **WSR₈: 800 DFFs with 8 inverters between DFF stages.**
 - **WSR₁₆: 800 DFFs with 16 inverters between DFF stages.**
 - **4 separate WSR chains with 20,000 DFFs. Each are WSR₀.**
- **LET: 1.8 MeVcm²/mg to 20.6 MeVcm²/mg.**



List of WSR Implementations (1)

- **4 clk 4 rst (800 stage WSRs):**
 - DUT that has WSR0, WSR4, WSR8, WSR16.
 - All clocks are connected to CLKINT. Only WSR0 has a DGBIO.
 - Each WSR chain has it's own synchronized AASD reset.
- **4 clk 4 rst FILTER (800 stage WSRs):**
 - DUT that has WSR0, WSR4, WSR8, WSR16.
 - All clocks are connected to **CLKINT**. Only WSR0 has a DGBIO.
 - Each WSR chain has it's own synchronized AASD reset.
 - **SET Filter is active** on every DFF in all WSR chains.
- **4 clk 4 rst Direct CLKBUF (800 stage WSRs):**
 - DUT that has WSR0, WSR4, WSR8, WSR16.
 - All clocks are connected to **CLKBUF**. All WSR chains have a DGBIO.
 - Each WSR chain has it's own synchronized AASD reset.
 - **SET Filter is active** on every DFF in all WSR chains.



List of WSR Implementations (2)

- **Large shift register (20,000 stage WSRs):**
 - DUT that has 4 WSR₀s.
 - All clocks are connected to CLKINT. Only WSR0 has a DGBIO.
- **Large shift register Filter (20,000 stage WSRs):**
 - DUT that has 4 WSR₀s.
 - All clocks are connected to CLKINT. Only WSR0 has a DGBIO.
 - SET Filter is active on every DFF in all WSR chains.
- **Large shift register CCC (20,000 stage WSRs):**
 - DUT that has 4 WSR₀s.
 - All clocks are connected to CLKBUF. All WSRs have a DGBIO.
 - SET Filter is active on every DFF in all WSR chains.
- **There are no resets in the large shift register WSRs.**
- **There are no user inserted inverters between DFF stages in the Large shift register WSRs.**

Characterizing Single Event Upsets (SEUs): Accelerated Radiation Testing and SEU Cross Sections

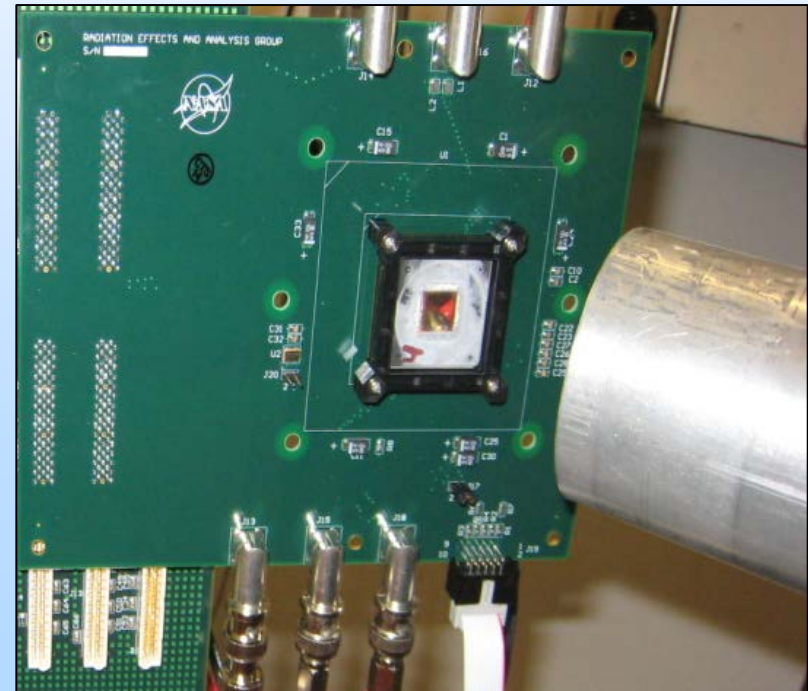
SEU Cross Sections (σ_{seu}) characterize how many upsets will occur based on the number of ionizing particles to which the device is exposed.

$$\sigma_{seu} = \frac{\#errors}{fluence}$$

Terminology:

- Flux: Particles/(sec-cm²)
- Fluence: Particles/cm²

σ_{seu} is calculated at several linear energy transfer (LET) values (particle spectrum)

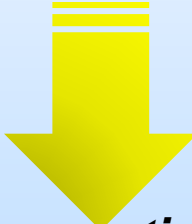


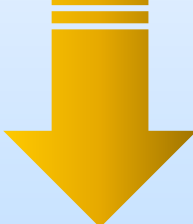
FPGA SEU Categorization as Defined by NASA Goddard REAG:



SEU cross section: σ_{SEU}

$$P(fs)_{\text{error}} \underset{\text{Design } \sigma_{SEU}}{\propto} P_{\text{Configuration}} \underset{\text{Configuration } \sigma_{SEU}}{\propto} P(fs)_{\text{functionalLogic}} \underset{\text{Functional logic } \sigma_{SEU}}{\propto} P_{SEFI} \underset{\text{SEFI } \sigma_{SEU}}{\propto}$$

 **Sequential and Combinatorial logic (CL) in data path**

 **Global Routes and Hidden Logic**

SEU Testing is required in order to characterize the σ_{SEU} s for each of FPGA categories.



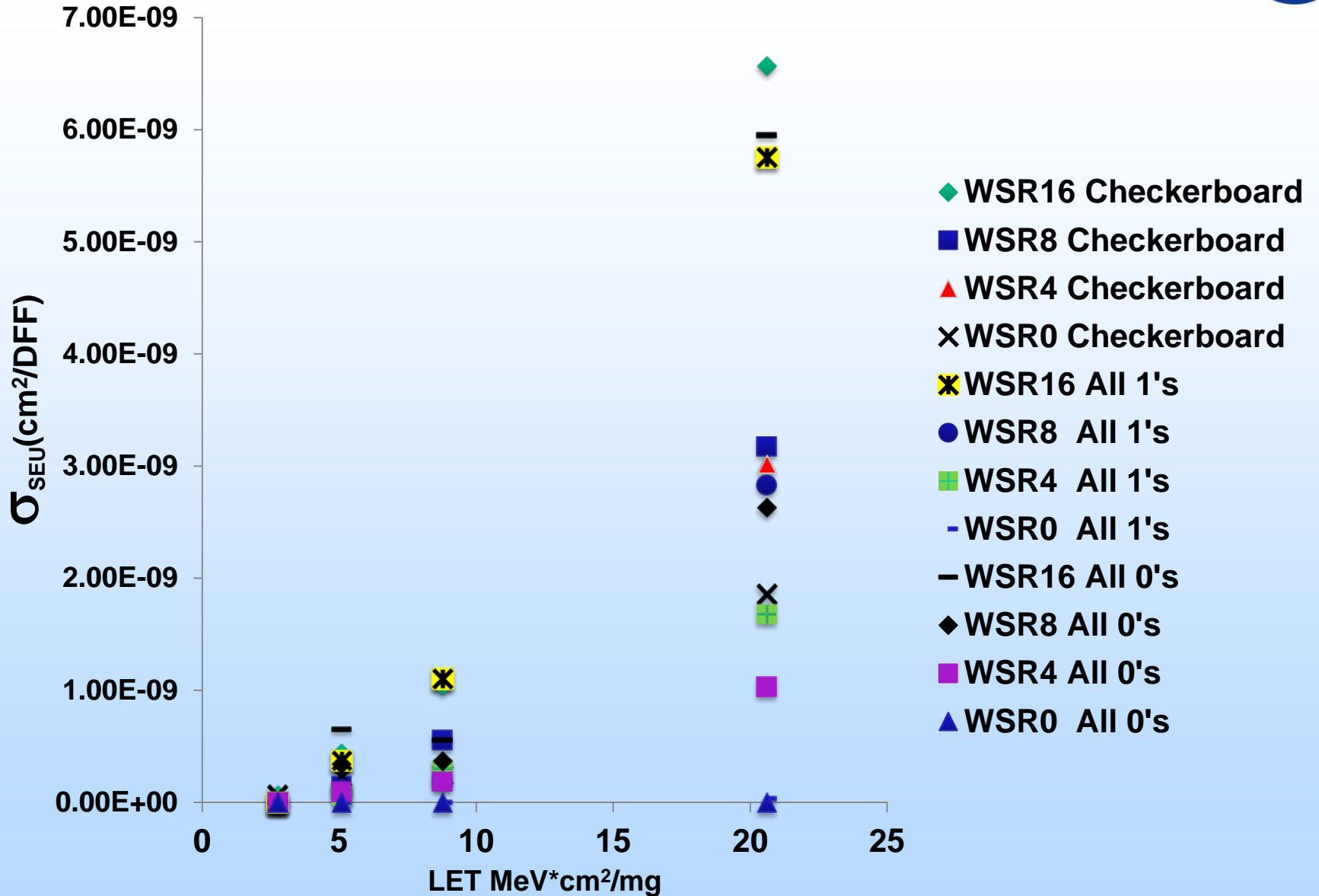
Accelerated Test Results



Configuration Re-programmability

- **During this test campaign, tests were only performed up to an LET of 20.6MeVcm²/mg.**
- **Higher LETs will be used during future testing.**
- **No re-programmability failures were observed up to an LET of 20.6MeVcm²/mg when within particle dose limits.**

4 CLK 4 RST FILTER versus LET at 100MHz

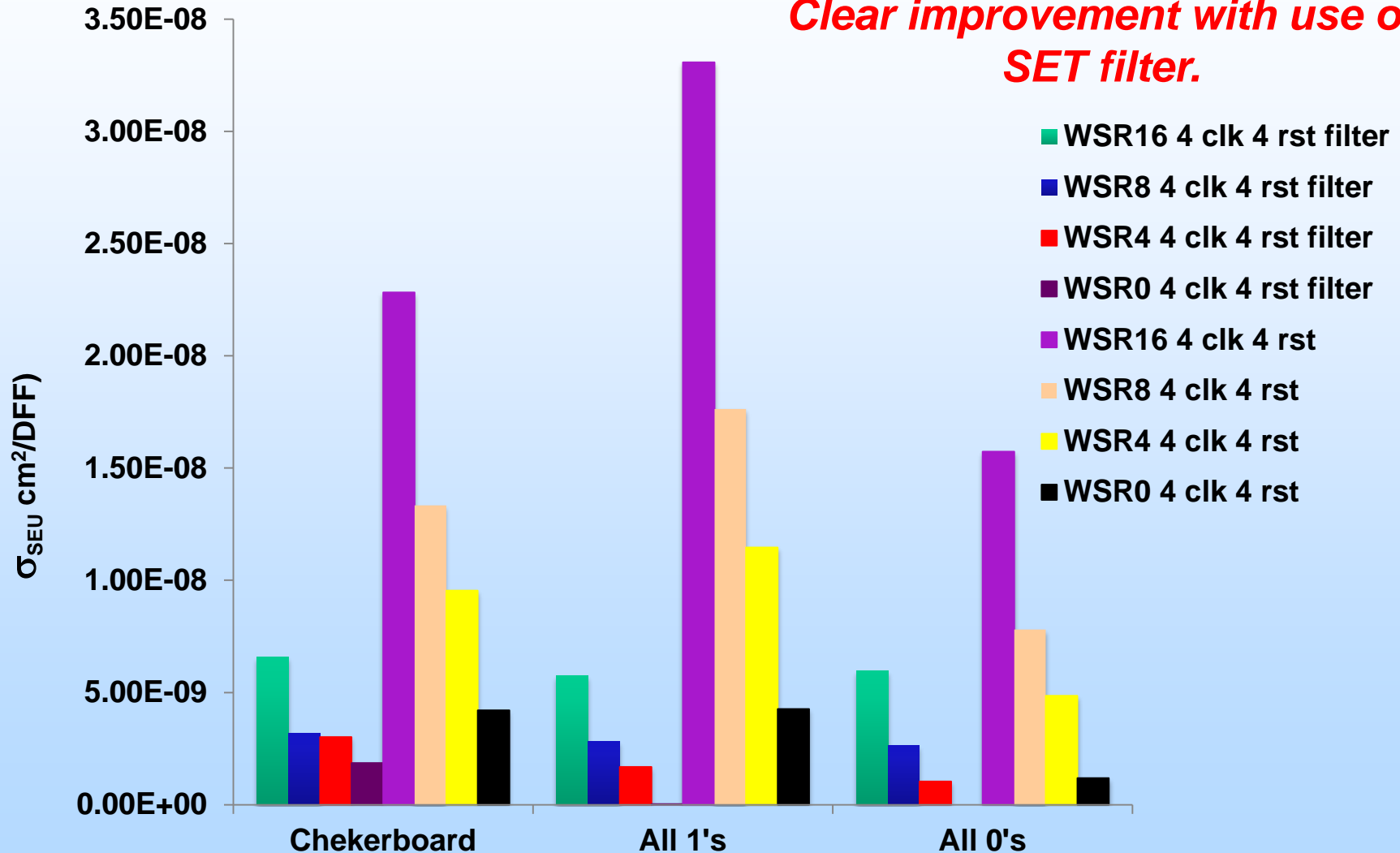




Comparing All WSR Chains:

4 clk 4 rst with Filter and 4 clk 4 rst ...100MHz with
LET = 20.6MeVcm²/mg

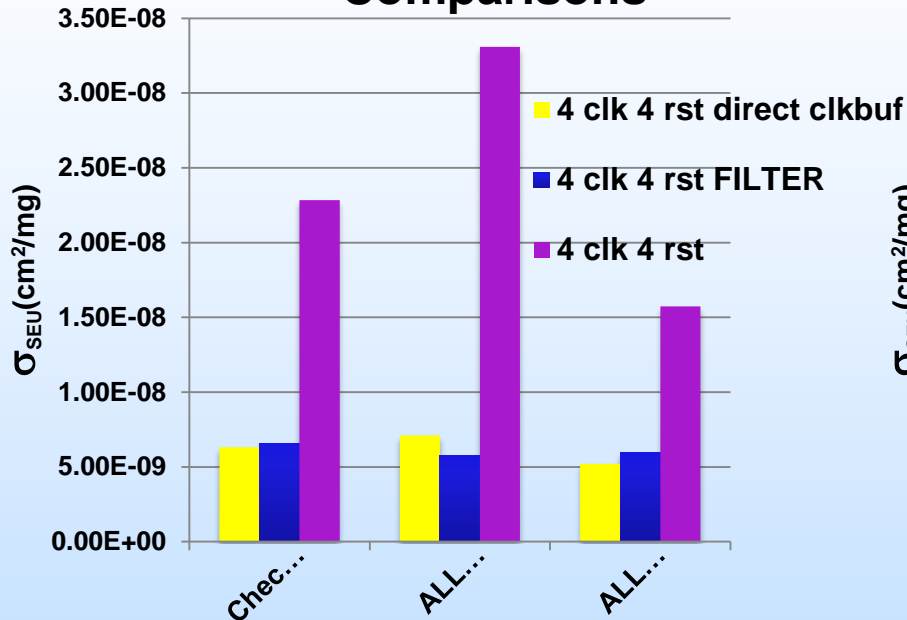
Clear improvement with use of SET filter.



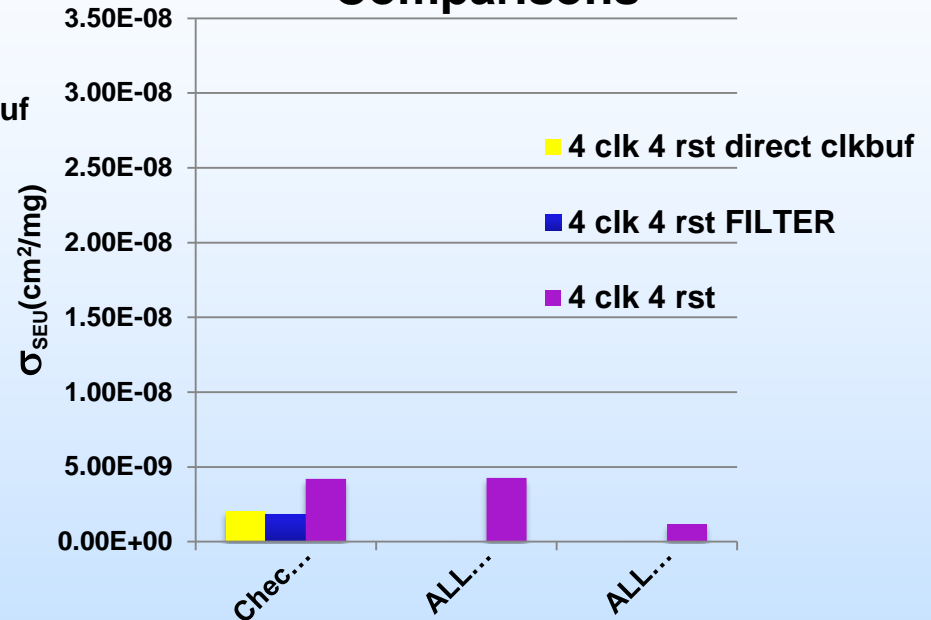
Comparing 4 clk 4 rst DUT Variations

WSR₁₆ has higher probability of data-path SET generation.

WSR16 at 100MHz LET=20.6
Comparisons



WSR0 at 100MHz LET=20.6
Comparisons



Pattern	Direct/fil ter	Direct/n o filter
Checker	0.96	0.28
All 1's	1.24	0.26
All 0's	0.88	0.33

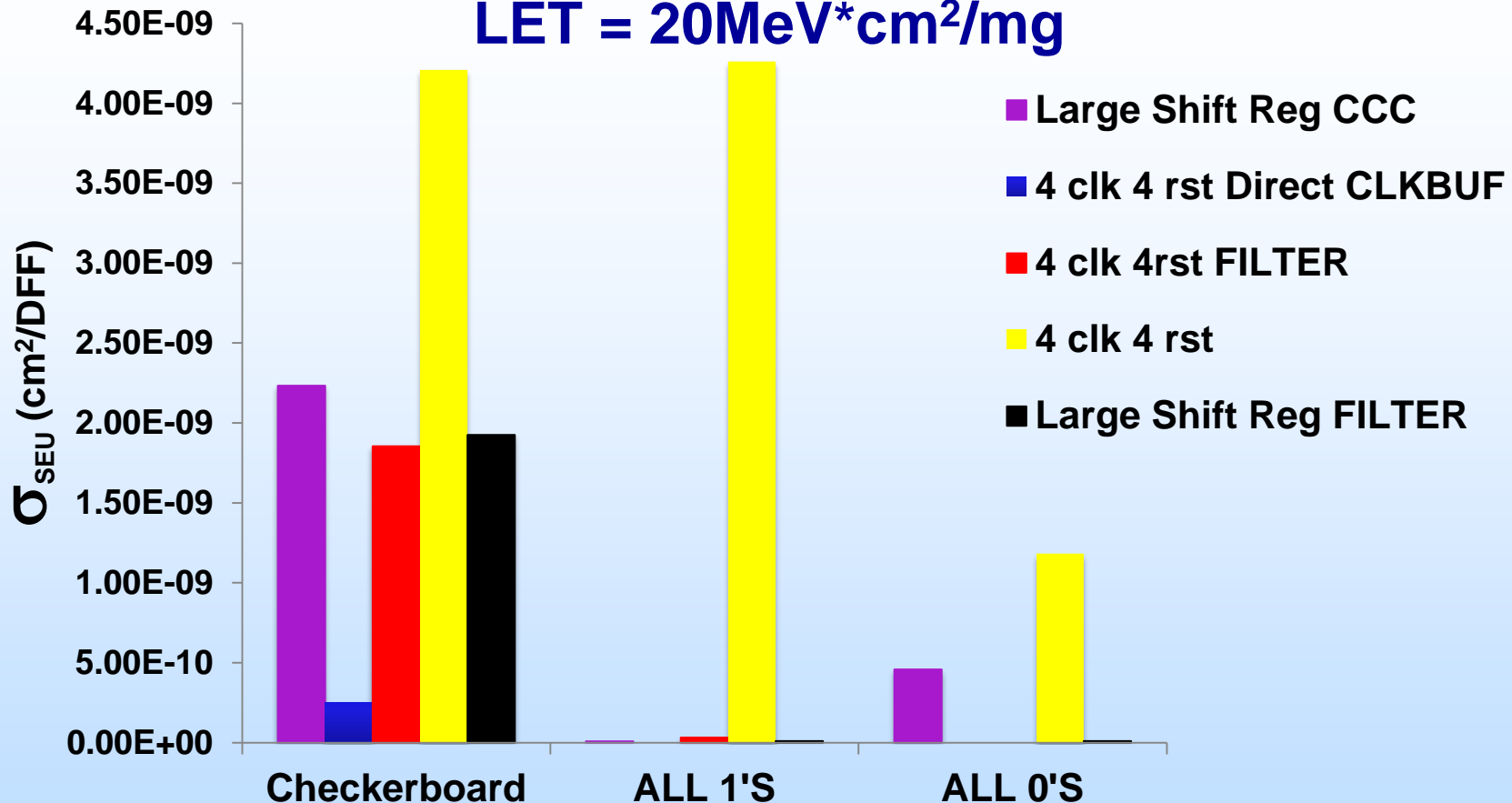
Tables represent Ratios of SEU cross sections.

Pattern	Direct/fil ter	Direct/n o filter
Checker	1.1	0.47
All 1's	1.0	0.007
All 0's	1.0	0.025



Introducing Large WSRs:

Comparison of WSR_0 SEU Cross Sections at 100MHz at LET = 20MeV*cm²/mg



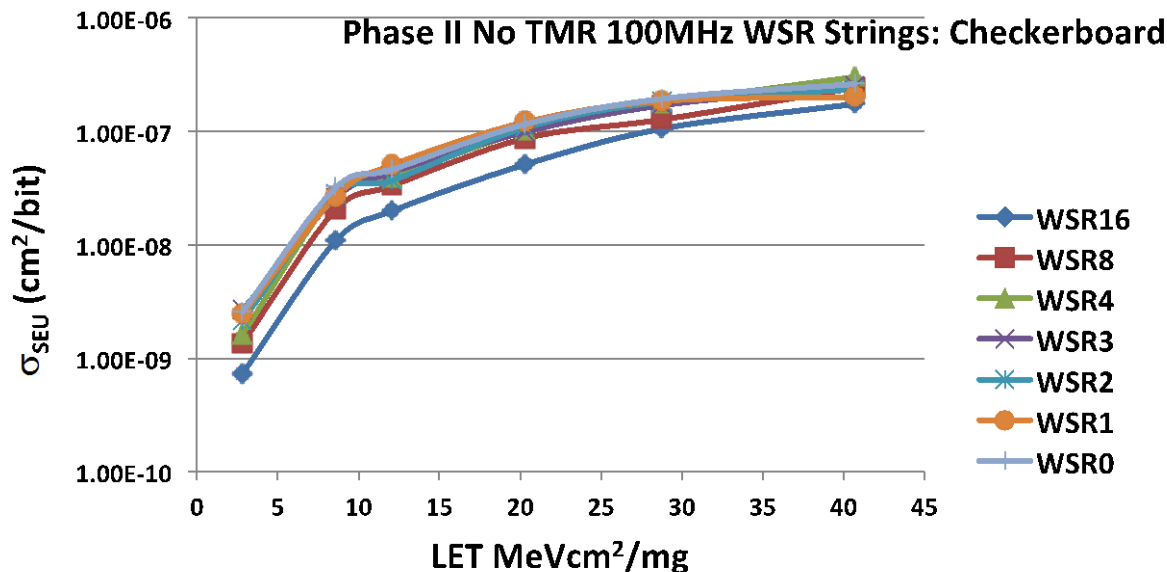
- As expected 4 clk 4 rst has the worst SEU performance. It is the only design with no SET filters.
- 4 clk 4 rst Direct CLKBUF has the best SEU performance. There is a direct connect from the DGBIO to the CLKBUF.



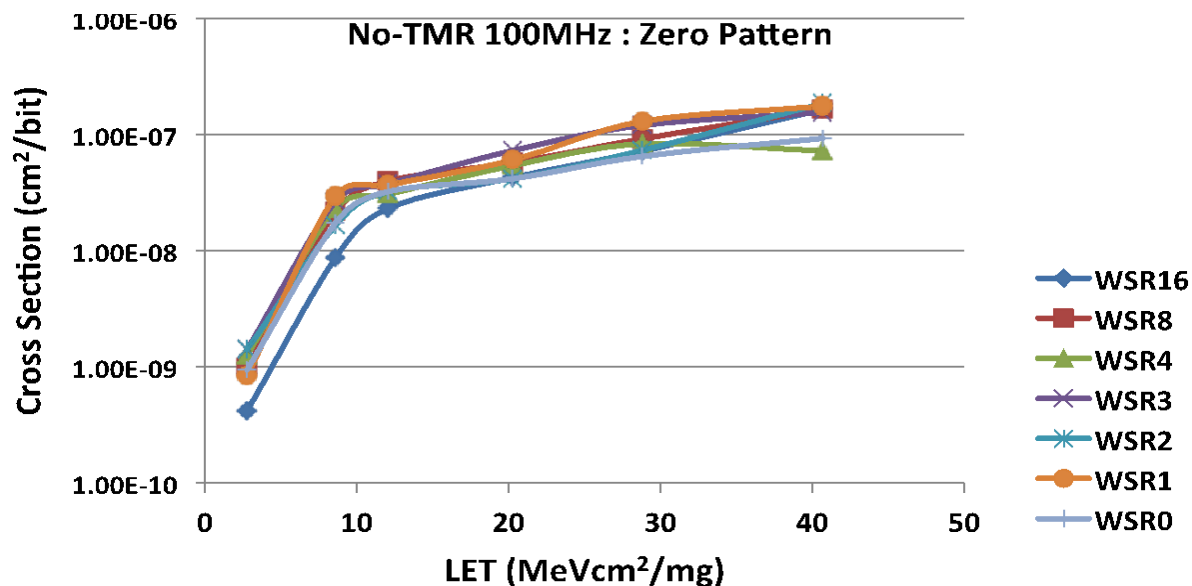
Additional Accelerated Radiation Test Data Observations

- **WSR input pattern of All 1's had greater SEU cross sections than WSR input pattern of checkerboard.**
 - This only occurred with designs that used resets. Most likely the reset was the cause.
 - **The use of resets in a synchronous design is imperative. This observation must not change the rules for reset implementation.**
- **Connecting from a DGBIO to a CLKBUF versus a normal I/O to a CLKINT did not provide significant improvement in SEU cross sections.**
- **Connect from a DGBIO to a CCC-PLL into a CLKINT did not improve SEU cross sections. It actually had higher SEU cross sections.**
 - **However, the performance is acceptable especially since there is a PLL in the path.**

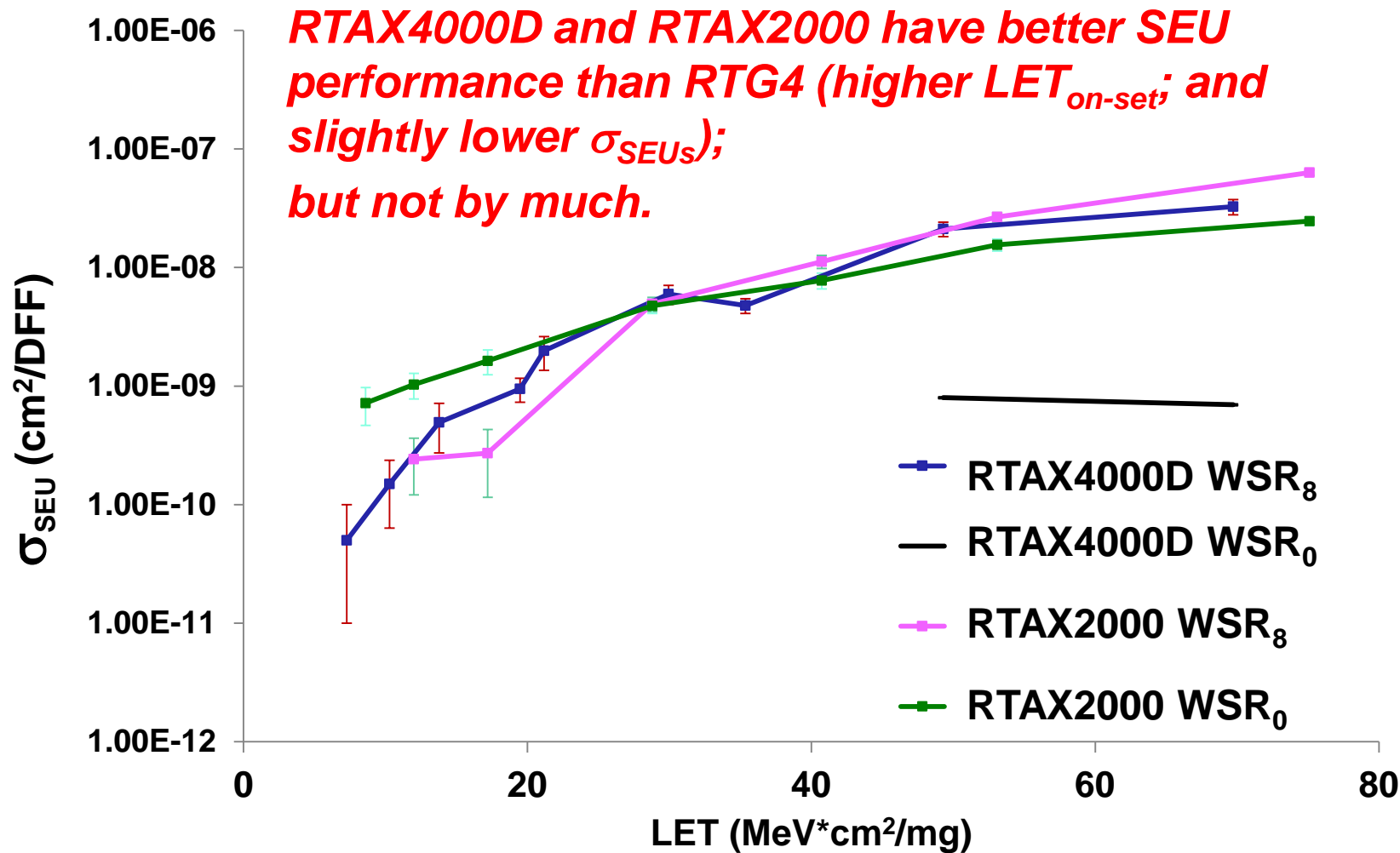
NEPP: ProASIC3 Accelerated Heavy-ion Test Results



RTG4 shows an improvement over ProASIC3 in functional data path.



RTAX4000D and RTAX2000 WSRs at 80MHz with Checkerboard Pattern





Acknowledgements

- *Some of this work has been sponsored by the NASA Electronic Parts and Packaging (NEPP) Program and the Defense Threat Reduction Agency (DTRA).*
- *NASA Goddard Radiation Effects and Analysis Group (REAG) for their technical assistance and support. REAG is led by Kenneth LaBel and Jonathan Pellish.*
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