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Final Report

INTEGRATED MICROPOWER CIRCUITS
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Table of Contents

1) Introduction 1

1.1 Scope of Program 1
1.2 Performance Requirements 2
1.3 Design Procedure 3

2) Preliminary Circuit Evaluation 6

2.1 RTL 6
2.2 RDTL 11
2.3 DTL 16
2.4 Complementary RDTL 24
2.5 T^2L 31
2.6 DCTL 36
2.7 ECTL 41
2.8 Summary 46

3) Circuit Performance Variations 49

3.1 Complementary RDTL 49
3.2 DTL 71
3.3 T^2L 85
3.4 Summary 100

4) Circuit Integration 104

4.1 Component Characteristics 104
4.2 Circuit Performance vs. Integration Techniques 108

5) Circuit Recommendations 113

5.1 Selection of Circuit 113
5.2 Circuit Fabrication 114
5.3 Final Circuit Packaging 115

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ABSTRACT

This report contains work done by Sperry Semiconductor, Division of Sperry Rand Corporation, under NASA contract NAS1-2519. The contract called for the investigations and recommendations of a group of universal digital micropower integrated circuits. The overall program was a multi-dimensioned problem where the interrelation of performance and fabrication characteristics was considered.

Initial investigations of various digital gate circuits were made using similar design conditions to determine relative performance characteristics over a wide range of power drains. Care was taken to obtain comparative performance by using the same semiconductor devices throughout the investigation. The most promising configurations were T^2L (direct coupled), DTL (single transistor gate) and complementary RDTL (two transistor complementary gate).

Each family of configurations (gates, flip-flops, etc.) were investigated in detail over the temperature range of interest to further investigate comparative performance characteristics.

Integrated component characteristics and the effect of various integration techniques on circuit performance were evaluated. Of the circuit configurations investigated, complementary RDTL offered the best overall performance characteristics. A discussion and example of the integrated techniques recommended for use in fabricating the family of complementary RDTL circuits is included in the report. AUTHOR

1. INTRODUCTION

1.1 Scope of Program

The project covered by NASA contract NAS1-2619 called for a study of Integrated Micropower Circuits for Spacecraft Electronic Systems.

The major emphasis was to reduce both the size and weight of the instrument package through reduction of both the physical size of the circuit package and the size and weight of the power supply through reductions in circuit power drain requirements.

The end result of this investigation is the recommendation of a group of universal digital circuit functions in an integrated form that present the optimum compromise between performance characteristics, low power drain, ease of fabrication and reliability.

An investigation of various digital circuit configurations was made to evaluate relative performance characteristics of each configuration. All designs incorporated worst case design procedures.

Parallel investigations of integrated circuit packaging techniques and component fabrication techniques were made in conjunction with the circuit design portion of the program. Close co-ordination was maintained between those responsible for each portion of the overall program.

It should be recognized that the overall program represents a multi-dimensioned problem, particularly in the area of circuit design and the trade-offs involved. Furthermore, the circuit performance characteristics are intimately associated with fabrication techniques used in the development of these circuits. It is well known that there are many

parasitic effects associated with integrated circuits, particularly those using I.S.C. substrate fabrication techniques. When operating circuits at low power levels, the effects of these parasitics become quite pronounced and severely limit circuit performance. It is to avoid this limitation that the major emphasis of this report was placed on separate chip integrated fabrication techniques supplemented by I.S.C. techniques where applicable.

1.2 Performance Requirements

The extent of the study program was determined by the performance characteristics required of the digital circuits. These requirements were determined by representatives of Sperry Semiconductor and NASA Langley and are outlined below.

The circuit functions required are "NAND and NOR" gates, a universal flip-flop and possibly a power driver. The flip-flop should be capable of use in either counters or shift registers. A flip-flop that may be used in a shifting accumulator is desirable if practicable.

Individual NAND and NOR gates are desired rather than the use of a single gate type and logic inversion to obtain both gating functions.

Because of radiation problems, the maximum resistance value available for consideration in circuit design must be limited to 100K Ω. Power supplies must consist of rechargeable batteries and supply levels must therefore be in multiples of 1.35 volts. It is, of course, necessary to keep supply voltage levels as low as possible to minimize power drain.

* I.S.C. - Integrated Semiconductor Circuit

Consistent with this requirement, it is desirable to limit output voltage swings to less than 3 volts.

Circuit fan-in and fan-out of five are desirable and must be larger than a minimum of three. Flip-flop repetition rates of 100KC and higher and gate transient response characteristics of less than 1μsec propagation delay per stage are required.

The circuits meeting the performance characteristics outlined above were to be investigated over the following temperature ranges:

-10°C to +85°C

-25°C to +100°C

-55°C to +25°C

1.3 Design Procedures

A preliminary evaluation of various gate circuits was completed to determine comparative performance. Power drain and propagation time were measured in identical tests for each of the configurations under investigation. For each configuration investigated, five gates were built and connected in a closed loop to form a ring oscillator. The power drain measurements were made while the circuit was operating and thus are an average transient value since the duty cycle of a ring oscillator is approximately fifty percent. The five-stage oscillator output is similar to a square wave and its period consists of the sum of five circuit turn-on times plus five turn-off times. If the period of the oscillator output is divided by ten, the resultant time is equal to the average circuit

propagation [illegible]. These two characteristics were used as the determining factors in the selection of the circuits to be more rigorously investigated.

To permit a comparative evaluation of circuit performance that is independent of semiconductor characteristics, the same transistors and diodes were used in all the initial circuit performance measurements. All configurations were worst-case designed using similar minimum and maximum specifications for semiconductor parameters. Resistor variations were assumed to be ±10% at the least favorable extreme. All power supply voltages were assumed to be battery supplied. Worst-case design normally assumes minimum and maximum values for power supply levels. Because of the voltage stability of mercury batteries and the wide variation permitted for other components, these power supply extremes were not considered in the worst case designs. The configurations investigated and performance characteristics are outlined in Section 2 of this report.

Identification of symbols used in the equations in section 2 characterizing each configuration are outlined below:

$\overline{XX}$ = Denotes maximum value

$\underline{XX}$ = Denotes minimum value

V_{AA}, V_{BB}, V_{CC} = Power supply levels

$V_{BE_{sat}}$ = Base emitter saturation voltage (turn on)

$V_{BE_{off}}$ = Base emitter turn-off voltage (+value denotes forward bias but below threshold turn-on level; -value denotes reverse bias)

$V_{CE(sat)}$ = Collector emitter saturation voltage

$V_{CE(off)}$ = Collector emitter voltage - transistor off

$I_{B(on)}$ = Transistor base current

I_{B_1} = Transistor turn on current

I_{B_2} = Transistor turn off current (transient)

I_{C} = Transistor collector current

$I_{C(BO)}$ = collector base leakage current

h_{fe} = transistor forward current transfer ratio

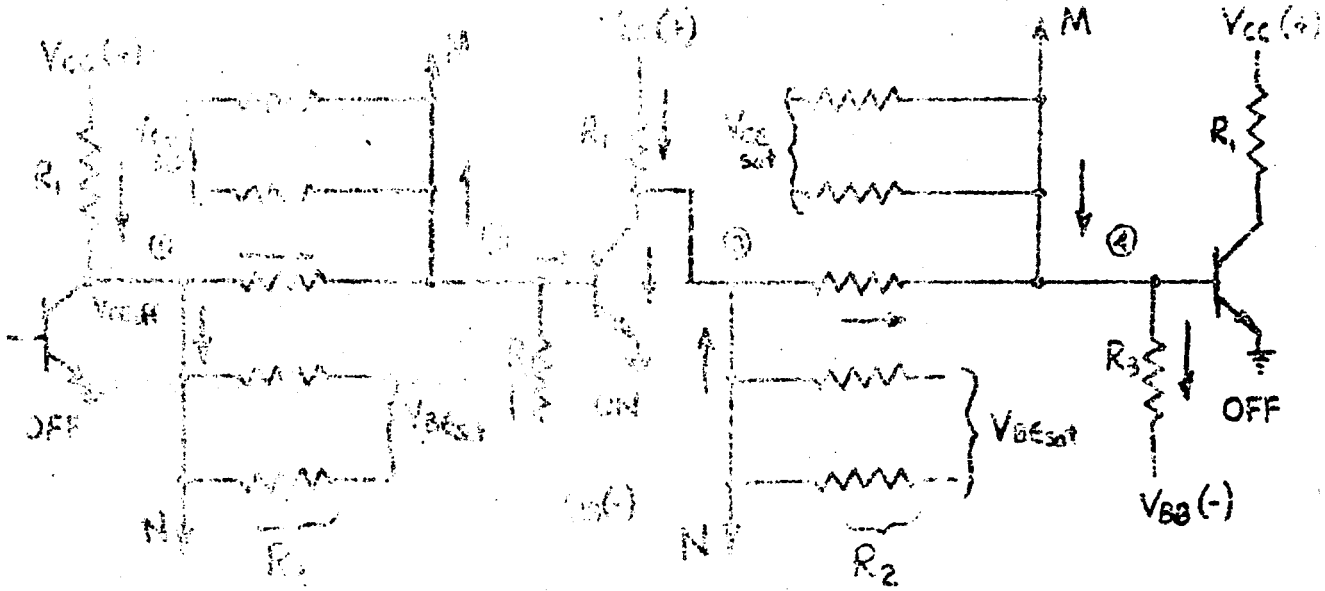
β_f = transistor forward beta = $\frac{\text{circuit collector current}}{\text{circuit base current}}$

M = fan-in

N = fan-out

[illegible]

[illegible] design equations for RTL are outlined below.



$$\frac{V_{CC} - V_{CE_{sat}}}{R_1} = \frac{V_{CE_{sat}} - V_{BE_{sat}}}{R_2} + \frac{(V_{CE_{sat}} - V_{BE_{sat}})}{R_3} \qquad (1)$$

$$\frac{V_{CE_{off}} - V_{CE_{sat}}}{R_2} = \frac{V_{BE_{sat}} - V_{CE_{sat}}}{R_2} + \frac{V_{CE_{sat}} + V_{BE_{sat}}}{R_3} + I_B \qquad (2)$$

$$V_{CE} = \frac{V_{CE} - V_{CE_{sat}}}{R_1} = \frac{V_{CE_{sat}} - V_{CE_{sat}}}{R_2} = (V_{CE_{sat}} - V_{CE_{sat}})(N - 1) \tag{3}$$

$$\frac{V_{CE} - V_{CE_{sat}}}{R_2} = \frac{V_{CE} - V_{CE_{sat}}}{R_3} = \frac{V_{CE}}{R_3} \tag{4}$$

$$\underline{\beta} = \frac{\overline{C}}{\underline{B}} \tag{5}$$

The operation of the circuit is described as follows:

When the gate transistor is turned off, all stages driven by the gate are turned on. The source of base current is supplied to the driven stages through R_1 and R_2. Thus the collector resistor must be small enough to provide turn-on current for all driven stages. The gate is switched off only when all inputs to the gate [illegible] (V_{CE}sat).

The performance characteristics of the gate are quite dependent upon fan-in and fan-out requirements. The isolation between gate outputs is dependent upon the number of input resistors (R_2) that are effectively in parallel. Crosstalk is thus quite [illegible] of small resistor values are used. Base current is proportional to [illegible] and is not constant as in most digital circuits. The collector current of each stage is determined by the [illegible] fan-out and must be held constant regardless of the fan-out [illegible]

To optimize the performance of the circuit, the following technique was used. Equations of parameters V_{BE}, V_{BES}, V_{CES}, and V_{CES} and various combinations of power supply levels were assumed. A fan-in and fan-out of 3 and a V_{BEO} of 0 volts was also used. To determine the optimum performance in terms of transistor beta requirements and output voltage swing (for possible AC coupled flip-flops) the following sequence of solution was adapted. Ten per cent resistor variations were assumed.

a. Assume $R_2 = KR_1$ where K represents the ratio of R_1 to R_2.

b. In equation 1 solve for V_{CEOff} with respect to K. (R_1's factor out)

c. Solve equation 4 assuming $R_2 = CR_2$ with $V_{BEOff} = 0V$ and evaluate C: $R_3 = CKR_1$.

d. Solve equation 2 for I_B with respect to V_{CEOff}, K, and R_1.

e. Solve equation 3 for I_C with respect to K and R_1.

f. Substitute equations 2 and 3 into equation 5 and factor out R_1. The resultant equation describes transistor beta requirements in terms of V_{CEO} and K.

g. The relationship of V_{CEO} to K is evaluated from the equation determined in Step b.

h. These results are substituted into the results of Step f to determine the relationship of h_{FE} to K.

Solution of these equations resulting in practical component values was not possible until relatively high power supply levels were used. Optimum performance with respect to fan-in, fan-out, beta requirements and turn-off voltage

and other conditions outlined above occurred when $R_1 \approx 3R_2$ and $R_3 \approx 3.5R_2$. The combination of high (greater than 5.4 volts) power supply levels and a wide range of resistor values within the same circuit ($R_3 \approx 10.5R_1$) prevent circuit operation at low power levels, particularly since the minimum resistance value (R_1) determines the collector current.

Switching speed is also limited by the relatively large input resistor (R_2). To obtain propagation times of less than 1 usec it was necessary to use circuits where power drain was well above a milliwatt. The relationship of power drain to propagation time is shown in Figure 1. These factors combine to prevent further consideration of RTL in this study program.

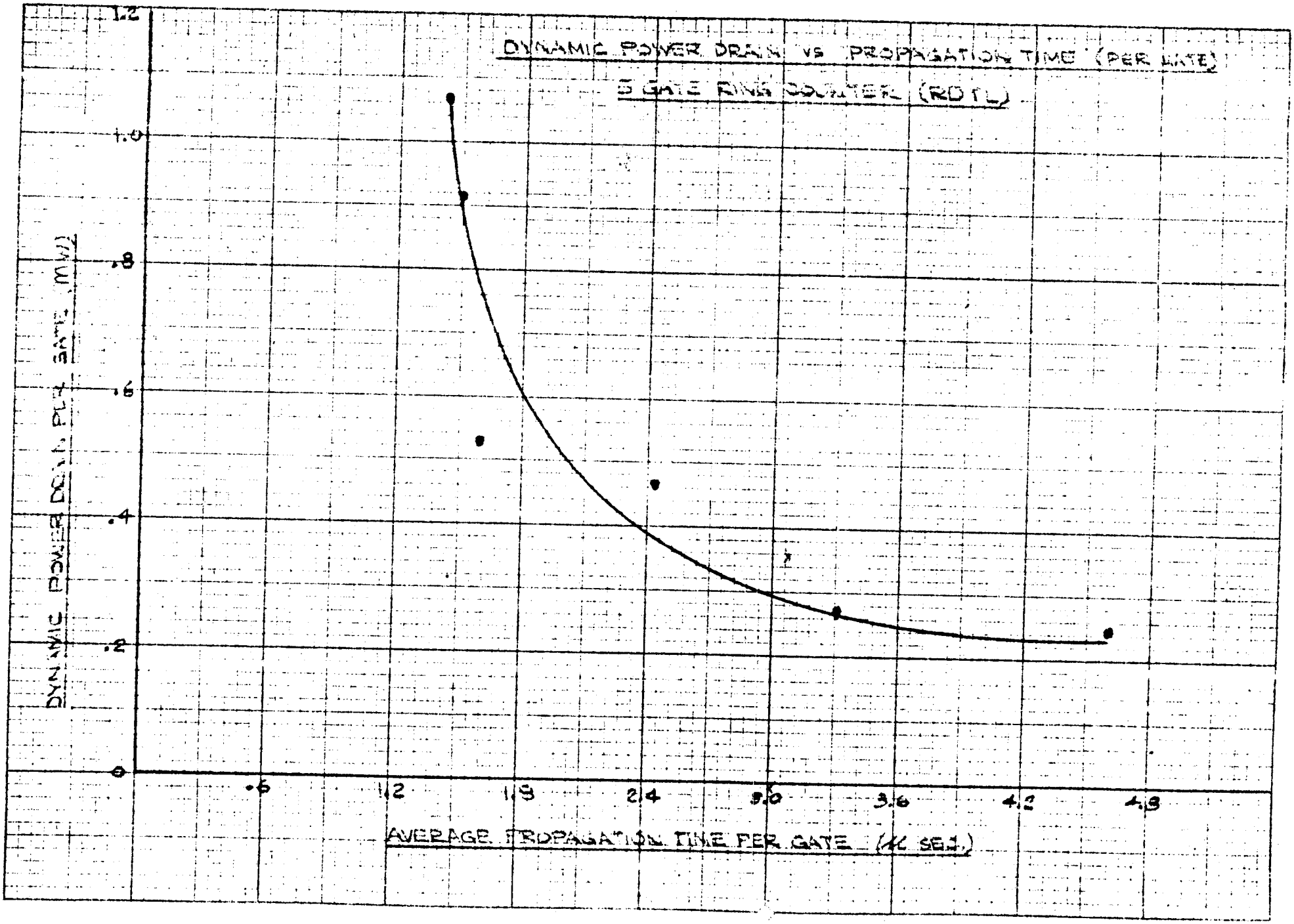
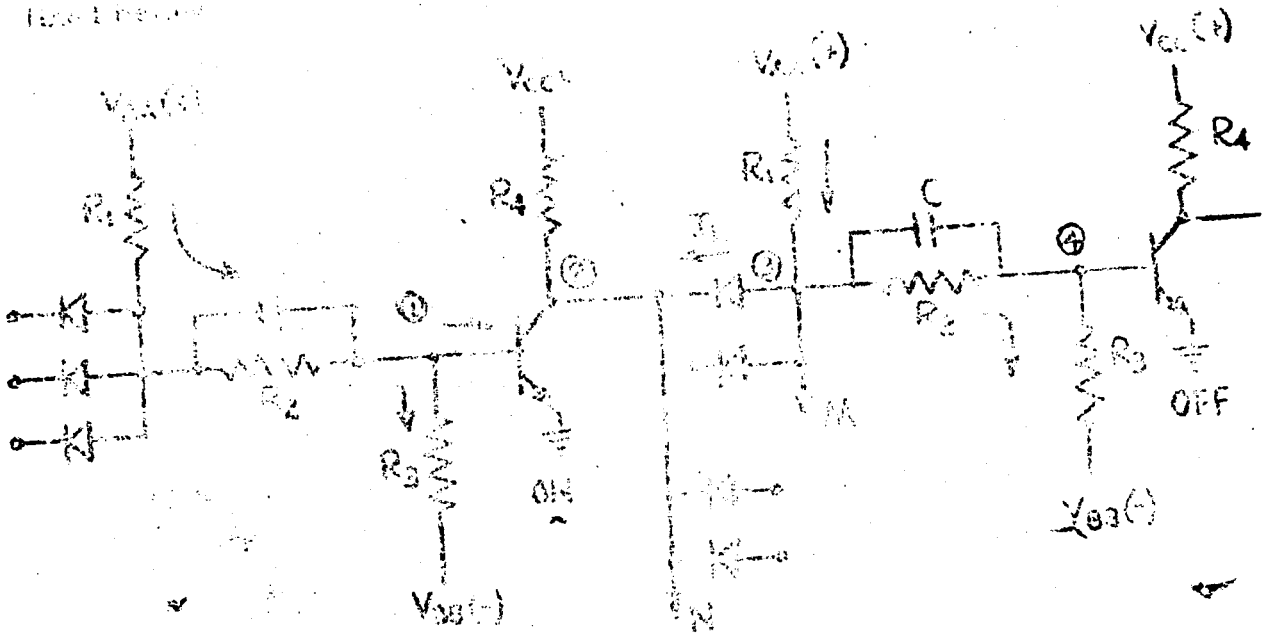

DYNAMIC POWER DRAIN VS PROPAGATION TIME (PER GATE)
5 GATE RING COUNTER (RDTL)
DYNAMIC POWER DRAIN PER GATE (MW)
1.2
1.0
.8
.6
.4
.2
0
.6
1.2
1.8
2.4
3.0
3.6
4.2
4.8
AVERAGE PROPAGATION TIME PER GATE (μ SEC.)

FIGURE 1

2.2 [illegible]

[illegible] RDTL are [illegible]

[illegible]



$$\frac{V_{AA} - V_{\overline{BE}_{sat}}}{\overline{R_1} + \overline{R_2}} = I_B + \frac{V_{BB} + V_{\overline{BE}_{sat}}}{R_3} \qquad (1)$$

$$\frac{V_{CC} - V_{CE_{sat}}}{R_4} = [illegible] = I_C \qquad (2)$$

$$\frac{V_{AA} - V_{CE_{sat}} - V_1}{R_1} = \frac{V_{CE_{sat}} + V_2 + V_3}{\overline{R_2} + \overline{R_3}} = I_L \qquad (3)$$

$$\frac{V_{CE\,sat} - V_{CC} - V_{BE}}{R_2} = 4 \quad V_{CC} = \frac{V_{CC} - V_{CE\,sat}}{R_3} \qquad (4)$$

$$\beta_F = \frac{I_C}{I_B} \qquad (5)$$

The operation of this circuit is described as follows:

The gate is turned on only if all diode inputs are reverse biased, thus allowing base current to be supplied from R_1 to the gate transistor. If any of the gate diodes are conducting, the gate transistor is turned off through the voltage divider action of R_2 and R_3.

Speed-up capacitors are used to improve both turn on and turn off time. Switching speed may also be improved by increasing the I_{B2}/I_{B1} ratio through design variations and decreasing the value of the collector resistor. RDTL, (unlike RTL), is a constant base current variable collector current digital circuit and results in a better switching speed-power drain relationship than RTL.

To evaluate the performance of the circuit, the following design procedure was used. Assumptions for parameters and supply levels V_{AA}, V_{BB}, V_{CC}, V_{BE}, $V_{CE\,Sat}$, V_{CC} and I_{CBO} were made, thus reducing the unknowns to the following: R_1, R_2, R_3, R_4, I_B, I_C, I_L, and V_{BEOff}. Solution is still impossible, so further assumptions as follows must be made:

- In equation 4 assume V_{BEOff} and a maximum value for R_3. Solve for R_2.

b. In equation 1 assume $R_1 = KR_2$ and solve for I_B.

c. In equation 3 solve for I_C.

d. In equation 5 assume a minimum h_{FE} compatible with transistor characteristics and solve for I_C.

e. In equation 2 assume a value for N and solve for R_4.

The number of possible solutions is, of course, quite large. To obtain preliminary information, the following specific values were assumed: $V_{BEO} = 0V$ and $R_1 = R_2$. These conditions limit the range of resistance values in the same circuit and result in a reasonable transistor beta requirement. Power supply voltages were as follows: $V_{AA} = +4.05$ $V_{BB} = -2.7$ $V_{CC} = +2.7$. Lower supply voltages resulted in much poorer circuit performance characteristics. A series of designs was tested to determine the relationship between propagation time and power drain. Various speed-up capacitors were used in these designs to determine the effect on switching speed improvement. The results are given in Figure 2.

Base turn-off voltage (V_{BEOff}) was varied for the above designs to determine its effect on transistor beta requirements. The relationship of V_{BEO} to forced beta required per fan-out is given in Table 3.

R_1	R_2	R_3	V_{BEOff}	β_f/N
50K	50K	125K	-.1V	19.3
50K	50K	150K	0V	11.1
50K	50K	175K	+.1V	7.7
50K	50K	215K	+.2V	5.5

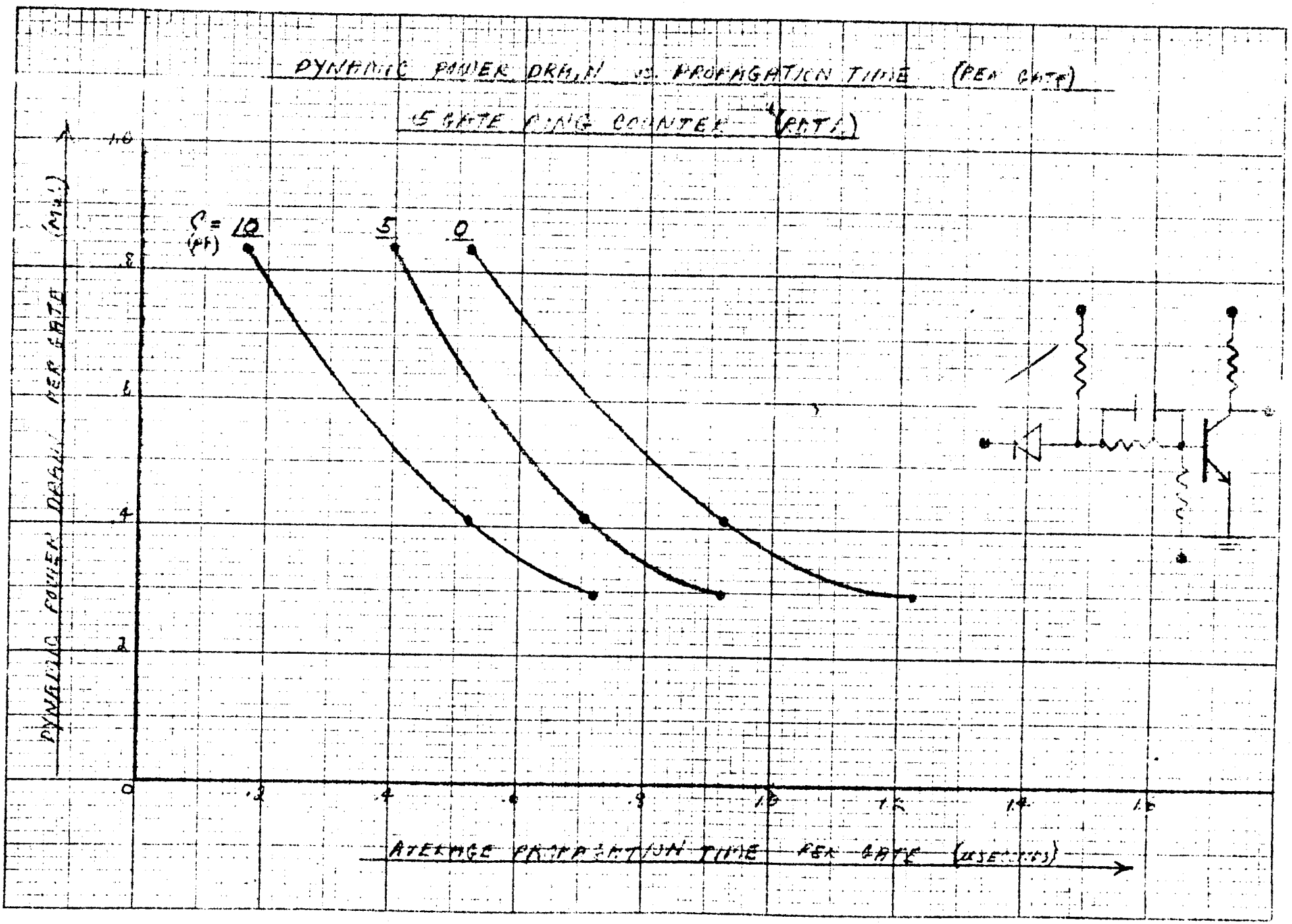
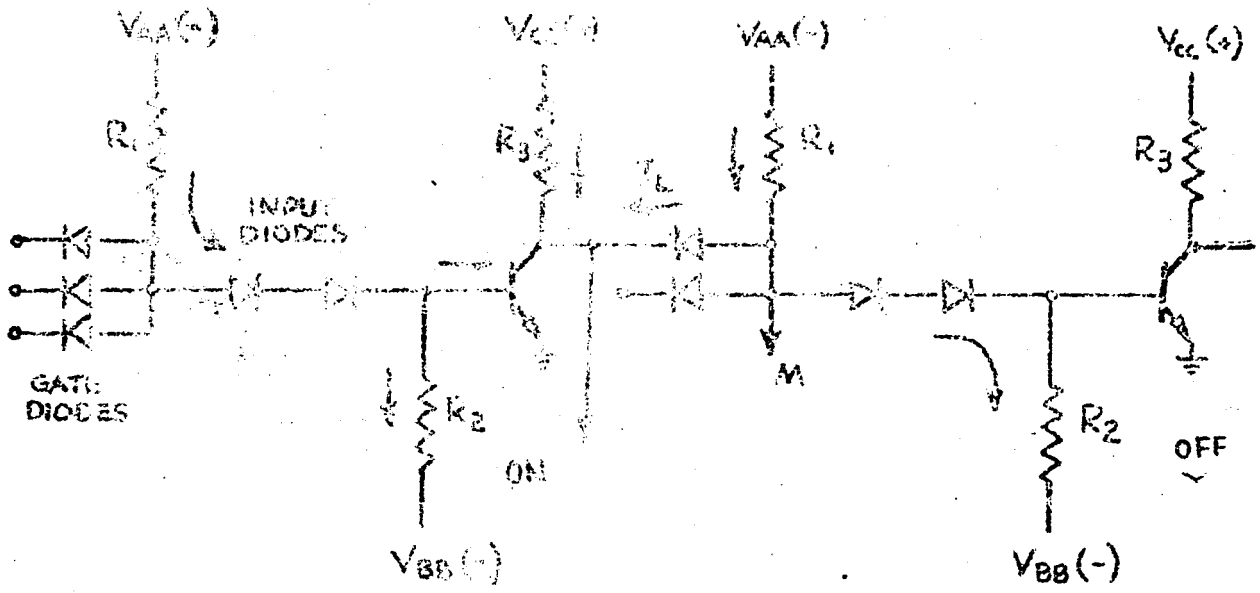

DYNAMIC POWER DRAIN vs. PROPAGATION TIME (PER GATE)
5 GATE RING COUNTER (RTL)
C = 10 (pf)
5
0
DYNAMIC POWER DRAIN PER GATE (MW)
AVERAGE PROPAGATION TIME PER GATE (μSECONDS)
0
.2
.4
.6
.8
1.0
1.2
1.4
1.6
2
4
6
8
10

FIGURE 2

The change in beta requirements is quite large for a small change in turn-off voltage because of the low voltage levels used in the design. The turn-on and turn-off requirements of the gate are such that it is desirable to make R_2 as large as possible for turn-off conditions and to make R_2 as small as possible for turn-on conditions. Any design using RDTL is a compromise between these conflicting requirements. The results obtained (see Figure 2) are, of course, not optimum, but they do indicate that the performance characteristics of this configuration are limited if lower operation is highly desirable. Other configurations discussed in this report permit operation at lower power drains at comparable switching speeds. RDTL will not be further investigated in this program.

Circuit configurations and design equations characterizing DTL are defined below.



$$\frac{V_{AA} - V_{BE_{sat}} - 2V_{\gamma} - V_{BB} + V_{CE_{sat}}}{R_1} = \frac{V_{BB} + V_{CE_{sat}}}{R_2} + I_{B_1} \tag{1}$$

$$I_C = \frac{V_{CC} - V_{CE_{sat}}}{R_3} - (I_L) \tag{2}$$

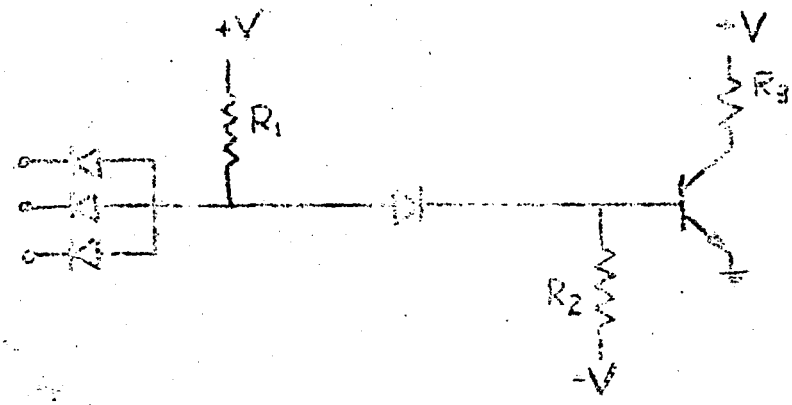
$$\frac{V_{AA} - V_{CE_{sat}} - V_{\gamma}}{R_1} = I_L + \frac{V_{BB} + V_{CE_{sat}} - I_{\gamma} - 2V_{\gamma}}{R_2} \tag{3}$$

$$V_{\overline{CE}_{sat}} = V_{\overline{C}} - \underline{W_F} - \underline{I_{BE_{off}}} \tag{4}$$

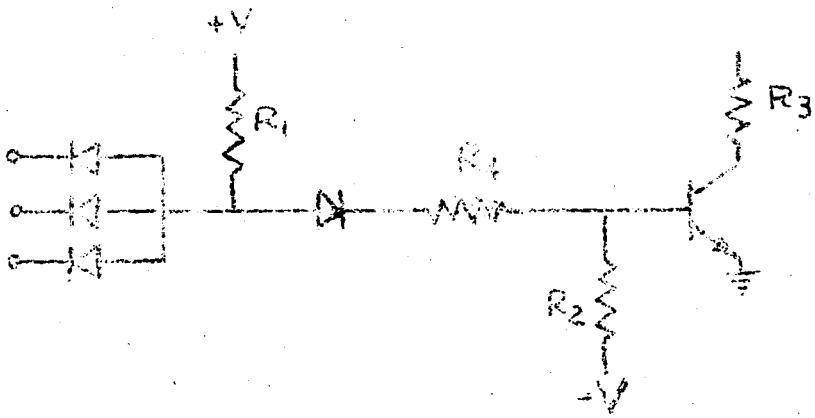
$$I_{\overline{B}_2} = \frac{V_{\overline{CE}_{sat}} + V_{BE}}{\underline{R_2}} \tag{5}$$

$$\underline{\beta_F} = \frac{\overline{I_C}}{\underline{I_B}} \tag{6}$$

Other variations of DTL that may be considered are shown below:



CIRCUIT B



CIRCUIT C

These input diodes thus act as a variable resistance constant voltage element and enhance DC performance of the gate because of these characteristics.

To optimize performance of the circuit, the following design sequence was used. Power supply levels and semiconductor characteristics were assumed as in the analysis of previously considered circuits. The remaining variables are R_1, R_2, I_C, R_3, I_L, I_{B_2} and N. To permit the solution of the equations, additional assumptions must be made as follows:

a. Solve equation 4 for $V_{B1\text{-}Off}$

b. Assume a resistance value for R_2 and solve for IB_2 in equation 6.

c. Assume $I_{B_1} = I_{B_2}$ and solve for R_1 in equation 1.

d. Solve equation 3 for I_L

e. Assume a value of N and h_{FE} and solve for I_C in equations 6.

Solve for R_3 in equation 2.

Reasonable circuit performance characteristics were obtained with minimum power supply levels (V_{AA} = +2.7V, V_{CC} = +1.35 or +2.7V, V_{BB} = -1.35V). A series of designs was tested to determine the propagation time-power drain relationship shown in Figure 4.

It should be noted that collector resistors may be varied to permit performance variations in switching speed and power drain for otherwise identical designs. A summary of one of these designs with V_{CC} = 1.35V is given in Table 5.

R_1	[illegible]	R_3	[illegible]	Power Drain/Gate	Prop. Time/Gate
30K	100K	7.5K	30	265μW	.39 μsec
30K	100K	11.0K	25	205μW	.44 μsec
30K	100K	2[illegible] K	20	181μW	.6 μsec

[illegible] 5

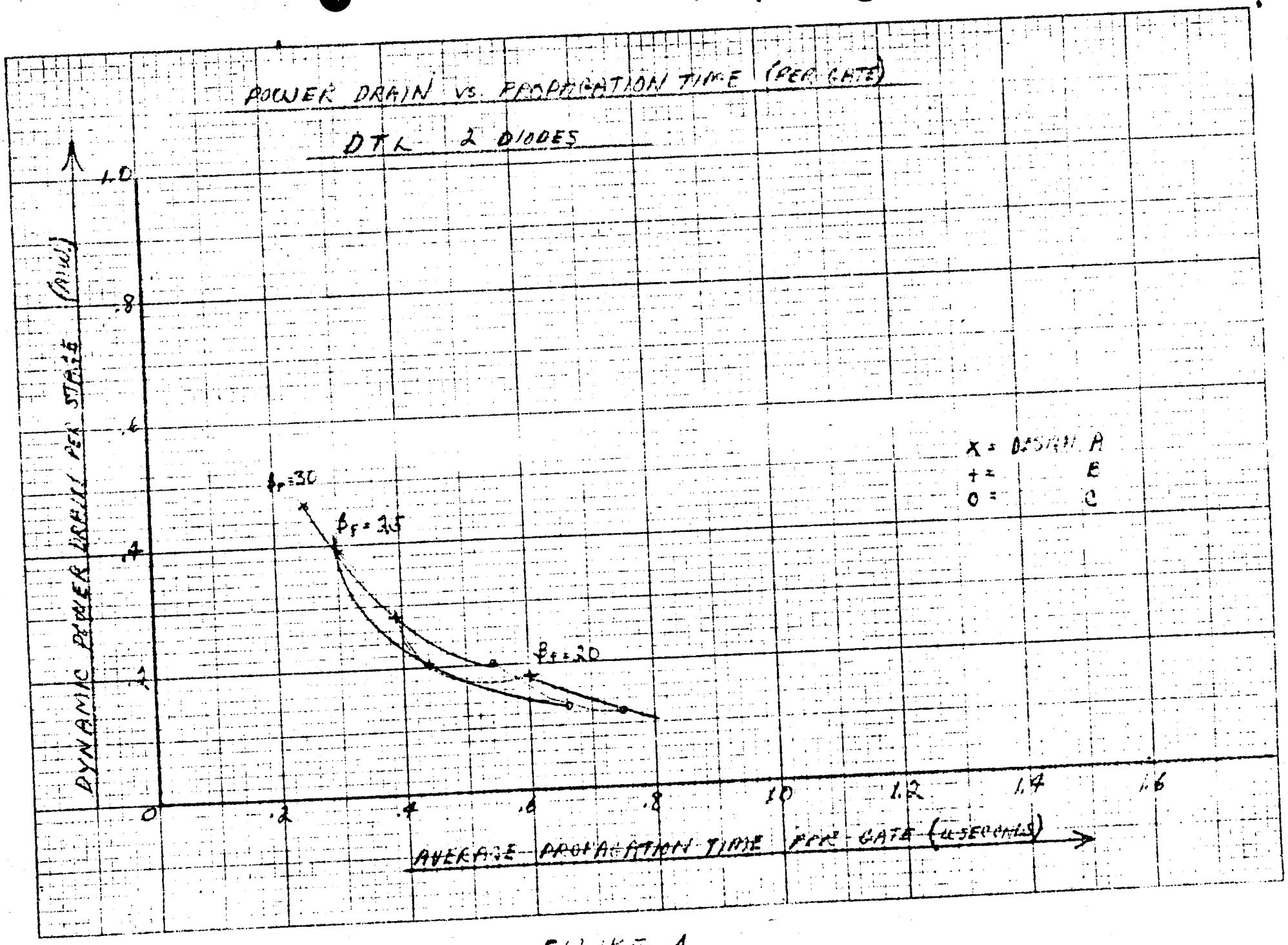

POWER DRAIN VS. PROPAGATION TIME (PER GATE)
DTL 2 DIODES
DYNAMIC POWER DRAIN PER STAGE (mW)
1.0
.8
.6
.4
.2
0
.2
.4
.6
.8
1.0
1.2
1.4
1.6
AVERAGE PROPAGATION TIME PER GATE (μSECONDS)
$\beta_F = 30$
$\beta_F = 25$
$\beta_F = 20$
X = DESIGN A
+ = B
O = C

FIGURE 4

Considerable performance variations were also obtained as various types of gate and input diodes were used in otherwise identical designs. Switching speed of the gate is inversely proportional to the reverse recovery time of the diodes used in the gate. A chart of gate switching speed (Propagation time) as a function of diode reverse recovery specifications is shown in Table 6.

R_1	R_2	[illegible]	Diode Rev. Rec. to 0V (I_F=5ma I_R=.5ma)	Propagation Time/Gate
47K	150K	30K	.1 μsec	.45 μsec
47K	150K	30K	.06 μsec	.66 μsec
47K	150K	30K	.03 μsec	4.2 μsec

TABLE 6

This relationship can be explained as follows: When the gate is switched off, the input diodes are temporarily reverse biased, causing turn-off base current to flow in the gate transistor. I_{B_2} (turn-off current) is thus provided through the input diodes as well as the base bias resistor. The duration and magnitude of I_{B_2}, which determines transistor storage time, is thus related to diode switching characteristics as indicated in Table 6.

Other variations of DTL gates (circuits B and C, (single diode and resistor and single diode) were designed and evaluated. Power drain versus propagation time characteristics are shown in Figures 7 and 8.

Design techniques are similar to those outlined for circuit A. A comparison of design results is outlined below in Table 9. V_{AA} = 2.7V V_{BB} = -1.35V V_{CC} = 1.35 V.

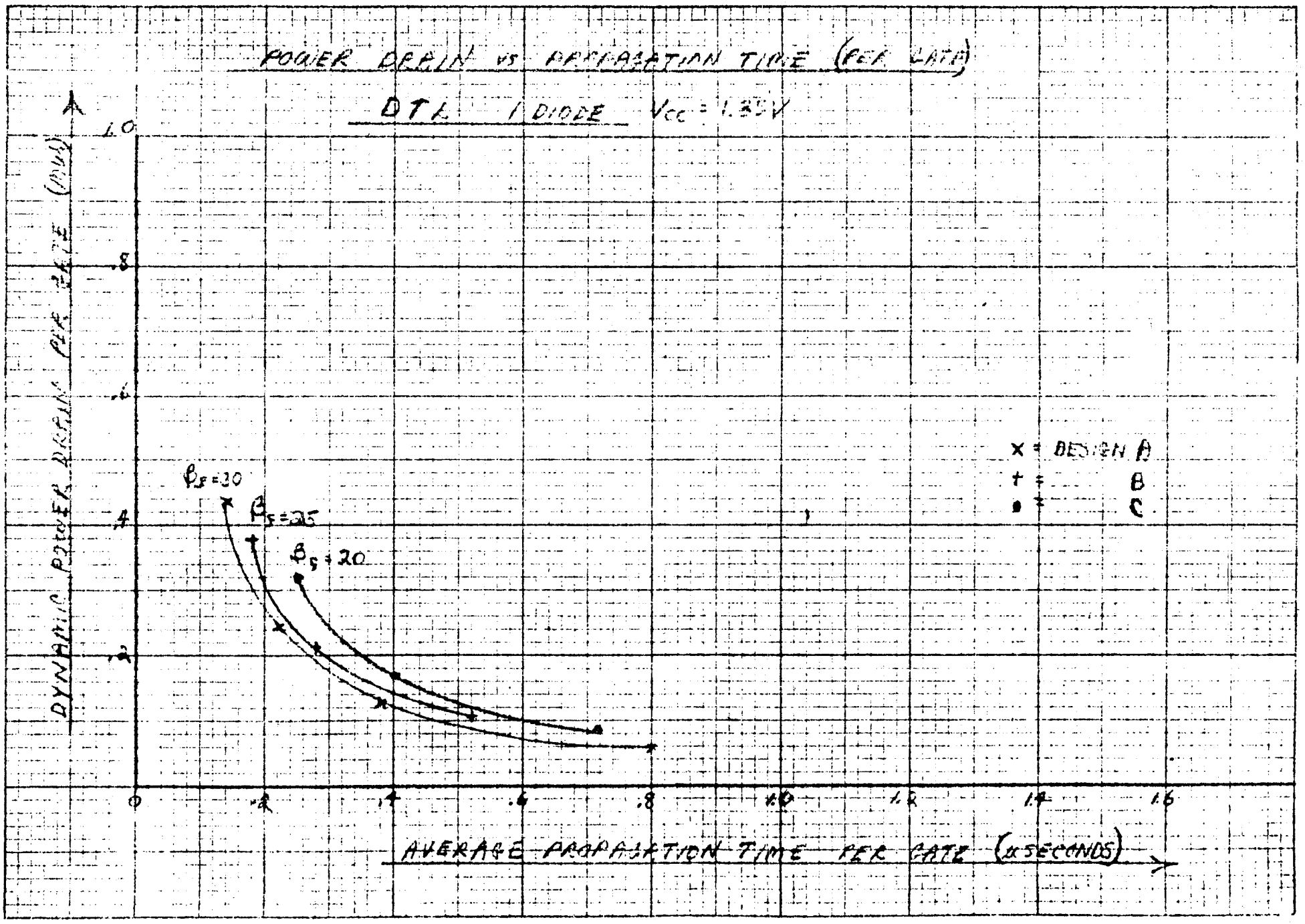

POWER DRAIN VS PROPAGATION TIME (PER GATE)
DTL 1 DIODE Vcc = 1.35V
DYNAMIC POWER DRAIN PER GATE (mW)
1.0
.8
.6
.4
.2
0
.2
.4
.6
.8
1.0
1.2
1.4
1.6
βF = 30
βF = 25
βF = 20
× = DESIGN A
+ = B
• = C
AVERAGE PROPAGATION TIME PER GATE (μSECONDS)

FIGURE 7

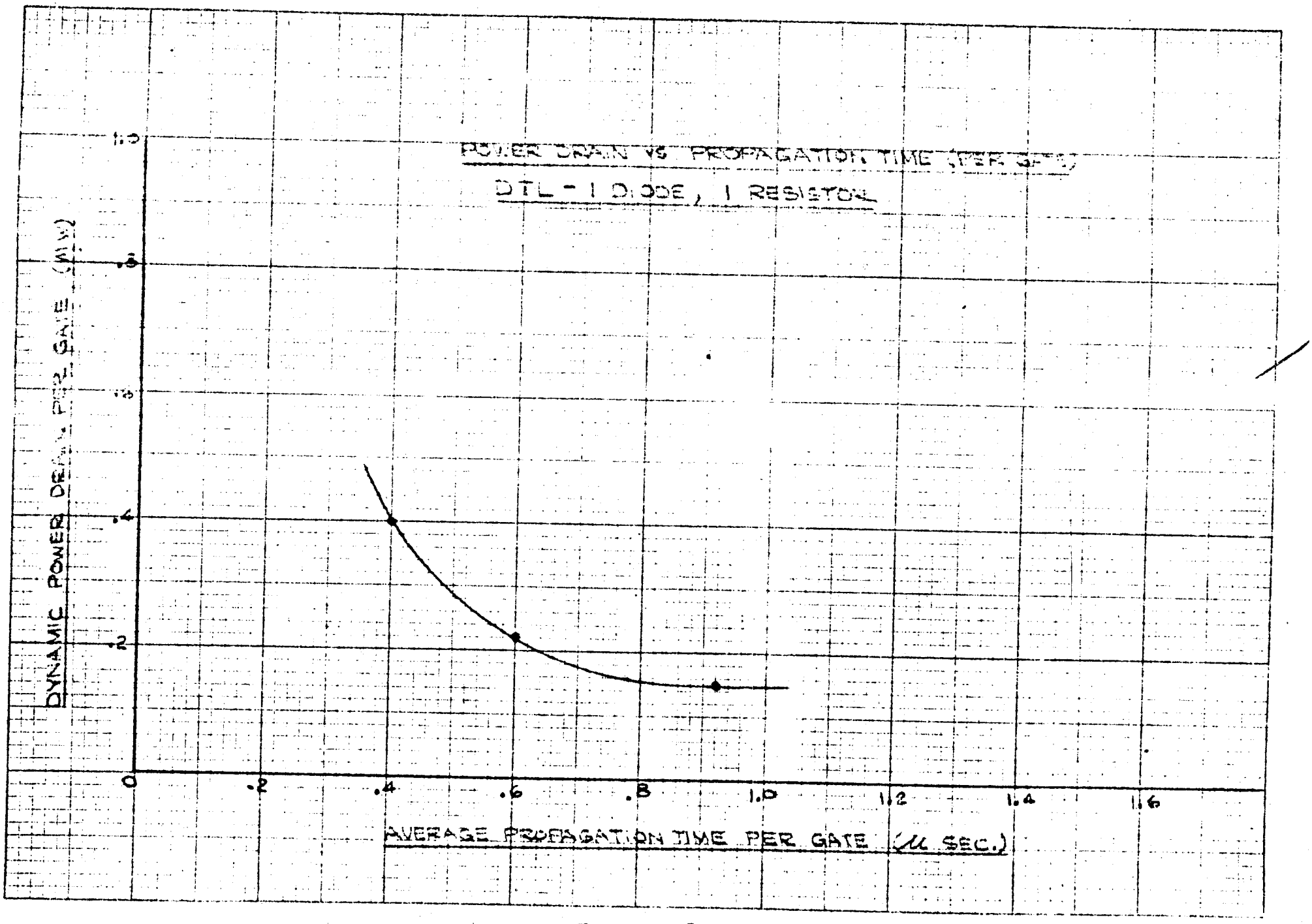

POWER DRAIN VS PROPAGATION TIME (PER GATE)
DTL - 1 DIODE, 1 RESISTOR
DYNAMIC POWER DRAIN PER GATE (MW)
1.0
.8
.6
.4
.2
0
.2
.4
.6
.8
1.0
1.2
1.4
1.6
AVERAGE PROPAGATION TIME PER GATE (μ SEC.)

FIGURE 8

Circuit	R_1	R_2	R_3	R_4	β_f	V_{bias}	Power Drain/Gate	Prop. Time/Gate
A	33K	360K	33K	----	25	-.1V	205μW	.44 μsec
B	43K	91K	36K	----		+.3V	204μW	.28 μsec
C	23K	100K	25K	10K	30	+.1V	220μW	.6 μsec

TABLE 9

It should be noted that circuit C is considerably slower in switching speed than the other configurations. This can be attributed to the limiting of transistor turn-off current by the resistor in series with the input diode.

The transient characteristics of gates A and B are similar. The major difference in DC characteristics of each circuit is the base turn-off voltages of each configuration.

The advantage of larger turn-off voltage with little sacrifice in propagation time indicates the circuit A appears to be the most promising of the DTL configurations investigated. The performance of DTL gates in general also indicates that the configuration provides good circuit performance at low power levels and will be investigated further in Section 3 of this report.

$V_{BS} - V$ [illegible]

$V_{GS} - V$ [illegible]

$V_{SE_{sat}}$ [illegible]

$V_{N_1} - V$ [illegible]

$$\frac{V_{BE_{off}}}{R_1} = \text{[illegible]} \qquad (5)$$

$$\frac{V_{BE} - V_{N}}{R_1} + \text{[illegible]} \qquad (6)$$

$$\frac{V_{BE_{off}Q_1} - V_{N_2}}{R_2} + \text{[illegible]} \qquad (7)$$

$$\beta_{f_{Q_1}} = \frac{N}{I}\frac{L}{Q_1} \qquad (8)$$

$$\beta_{f_{Q_2}} = \frac{N}{I}\frac{L}{Q_2} \qquad (9)$$

The operation of the circuit is described as follows:

When the input voltage of any gate diode is down (approximately zero volts) the diode conducts and provides a path for base current for Q_1. Q_2 is turned off by the resistor divider R_4 and R_5. When all input voltages are high (+ volts) the gate diodes are reverse biased and base drive is provided for Q_2 from R_1. The divider R_2 and R_3 turn Q_1 off. Speed-up capacitors provide transient I_{B_1} and I_{B_2} to the transistors and thus enhance switching speed. Switching speed is also improved by base a transistor base time is present at both leading and trailing [illegible] the waveform.

[illegible]

permit [illegible] for the parameters V_{CC} [illegible] V_{BE} [illegible] remaining unknowns [illegible] R_1, R_2, R_3, R_4, R_5 [illegible] $V_{BEOFFC2}$ [illegible] $V_{BEOFFC1}$, V_{N1}, V_{N2} [illegible] [illegible] performance the additional assumptions may be made: $R_1 = R_4$, $R_3 = R_5$, and $I_{BC1} \cong I_{BC2}$.

The number of unknowns now reduces to eleven for eight equations. Equations 8 and 9 can be neglected in initial calculations, since their only function is to relate transistor beta to leakage. The resulting nine unknowns for seven equations indicate that two unknowns must be assumed to solve the set of equations.

To limit the maximum resistance values in the circuit (as outlined in the design ground rules), values of R_3 and R_5 may be assumed at a maximum resistance value.

To facilitate solution of the equations, it is convenient to assume a value for I_{BC1}. The equations may now be solved in the following sequence:

a. In equation 2 assume values for R_3 and I_{BC1} and solve for R_2.

b. In equation 3 solve for $V_{BEOFFC2}$.

c. Let $V_{BEOFFC2} = V_{BEOFFC1}$ for complementary operation.

d. In equation 5 solve for V_{R_2}.

e. In equation 7 solve for R_1.

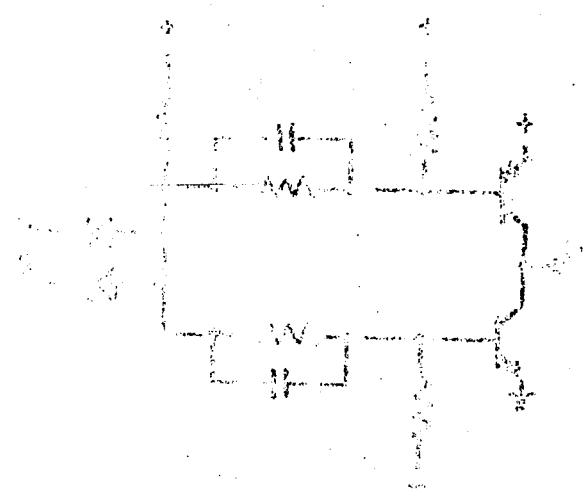
f. In equation 6 solve for actual V_{N_1}.

g. In equation 4 solve for actual I_{BC2}.

[illegible]

[illegible]

[illegible] are shown in Figure [illegible]



[illegible]	[illegible]	[illegible]
[illegible]	1	0
[illegible]	1	0
[illegible]	1	0
[illegible]	0	1

[illegible]

[illegible]	B	C
0	0	1
[illegible]	0	0
0	1	0
[illegible]	1	0

[illegible]

Initial investigations were directed to the NOR configuration. Designs at various current levels were formulated as outlined above and breadboarded in a five stage ring oscillator to determine average power drain and propagation time. The circuits were designed with two power supply conditions: (V_{AA} = -1.35, V_{BB} = 4.05, V_{CC} = 2.7) and (V_{AA} = 0V, V_{BB} = V_{CC} = 2.7V). The design results are outlined in Table II.

It should be noted that resistance values throughout the circuit are comparable in magnitude. As indicated in the design procedure R_3, R_5, and I_{B_1} were assumed at specific values. Emphasis was placed on maintaining constant turn-off voltage rather than equalizing base currents. Resistor variations were assumed to be ±10%. Power drain versus propagation time characteristics for circuits 1 through 6 are shown in Figure 12.

Investigation of propagation time versus frequency as a function of speed-up capacitors was limited by the use of the five stage ring oscillator. As larger capacitors were used, the circuit operation became too fast to properly determine propagation time through ring oscillator techniques. Propagation times became relatively small with respect to rise and fall times, thus resulting in a degeration of the normal square wave output into a semi-sinusoidal wave shape which prevented measurement of propagation time under these conditions.

It should be noted that the above information represents typical characteristics as determined through one of many design approaches. The results are, however, typical of performance obtainable from this configuration. Further investigation and performance characteristics of complementary RDTL circuits are discussed in Section 3 of this report.

Design	R_1	R_2, R_4	R_3, R_5	I_{B_1}	I_{B_2}	β_{fQ1}/N	β_{fQ2}/N	$V_{BEQ1,Q2}$	V Supply
1	270K	72K	150K	2.5uA	1.6uA	13.5	21.0	.30	[illegible]
2	115K	63K	150K	5.0uA	[illegible]	10.5	[illegible]	[illegible]	[illegible]
3	103K	46K	100K	5.0uA	7.7uA	13.4	8.7	.18	+2.7, +4.05, [illegible]
4	93K	24K	100K	[illegible]	10.4uA	[illegible]	[illegible]	[illegible]	[illegible]
5	[illegible]	25K	50K	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
6	62K	24K	50K	[illegible].5uA	11.1uA	15.5	10.5	.16	+2.[illegible], +4.[illegible]
7	71K	104K	100K	5.0uA	[illegible].4uA	9.8	9.1	.[illegible]	+2.7 only
8	32K	67K	50K	5.0uA	8.8uA	1[illegible].4	11.0	.36	+2.7 only

TABLE 12

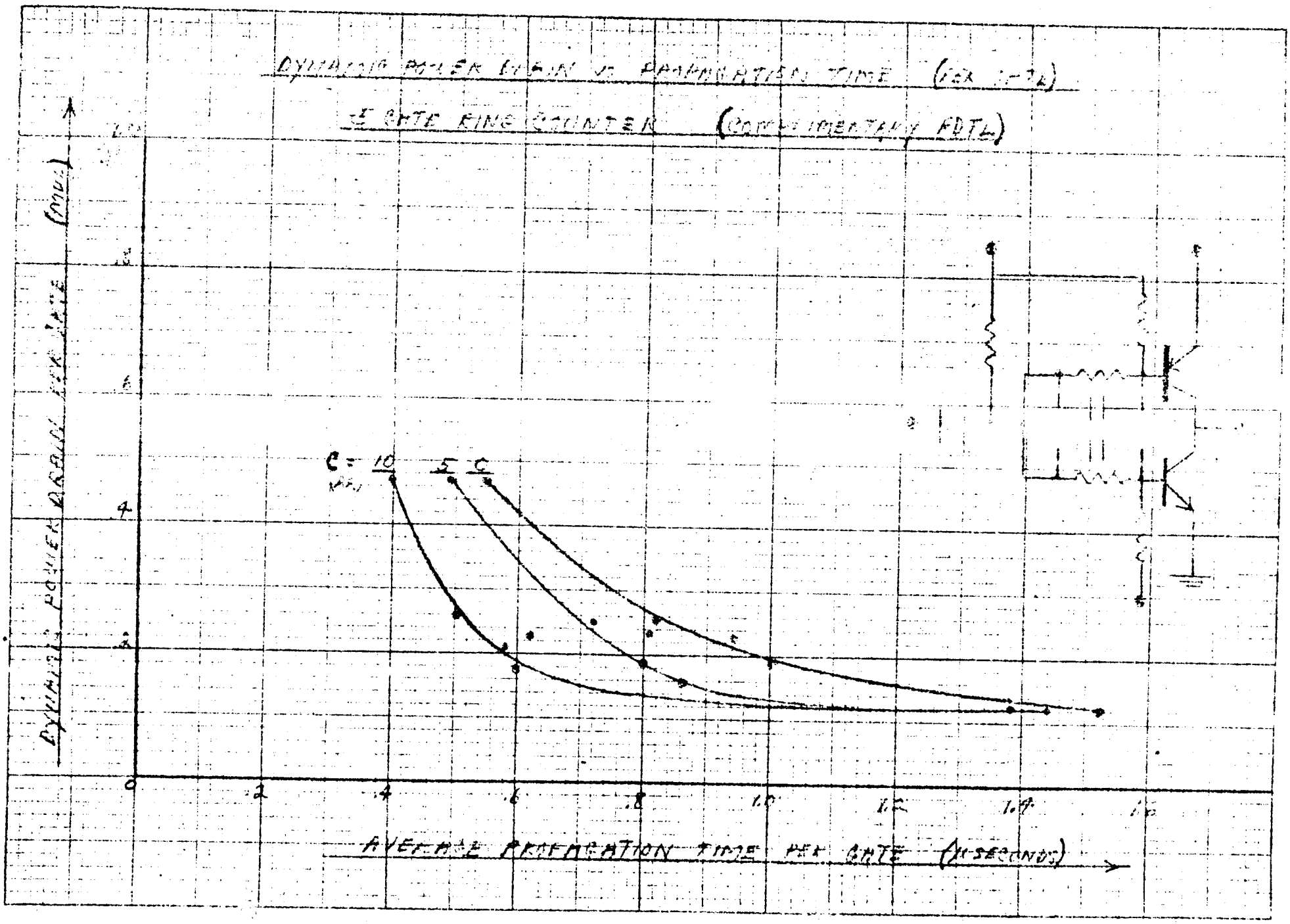
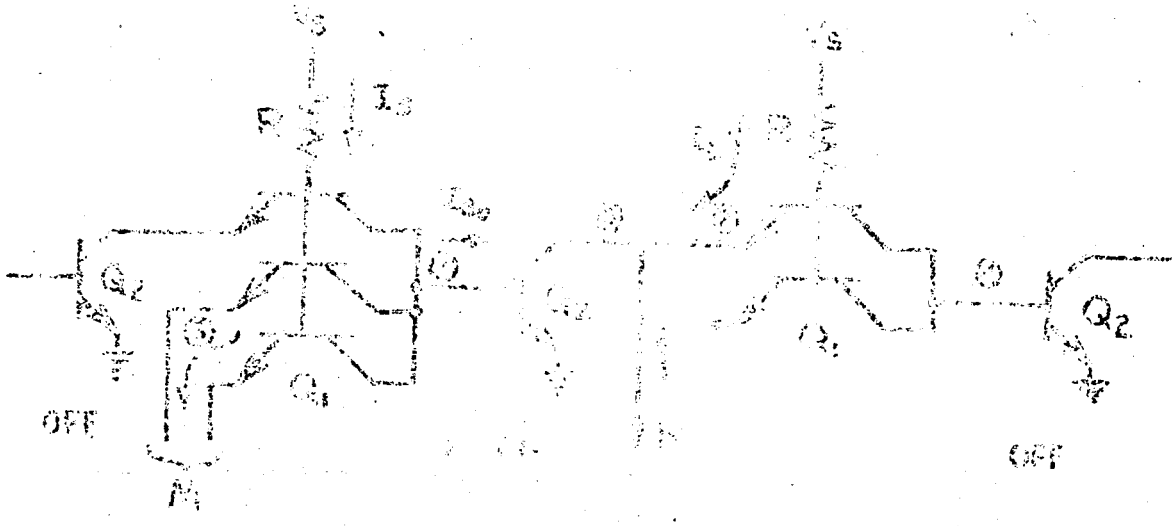

DYNAMIC POWER DRAIN VS PROPAGATION TIME (PER GATE)
5 GATE RING COUNTER (COMPLIMENTARY FDTL)
DYNAMIC POWER DRAIN PER GATE (MW)
C = 10 5 0
AVERAGE PROPAGATION TIME PER GATE (μ SECONDS)
0
.2
.4
.6
.8
1.0
1.2
1.4
1.6

FIGURE 19

[illegible]

The [illegible] configurations [illegible] equations are given below.



$$\underline{I_B} = \frac{V_S - V_{\overline{BE}_{sat}Q_2} - V_{\overline{BC}_{Q_1}}}{R} \qquad (1)$$

$$\overline{I_L} = \frac{V_S - V_{\overline{BE}_{Q_1}} - V_{\overline{CE}_{sat}Q_1}}{R} \qquad (2)$$

$$\overline{I_c} = NI_L = \beta_r \underline{I_L} \qquad (3)$$

$$V_{\underline{BE}_{off}} = V_{\underline{BE}_{Q_2}} - V_{\overline{CE}_{Q_1}} - V_{\overline{CE}_{sat}Q_2} \qquad (4)$$

$$\underline{I_{B_0}} = \underline{I_B} - (\beta_{I_{Q_1}} \underline{I_B})(N - 1)(M) \qquad (5)$$

The gate is turned off [illegible] the inputs are at a low voltage (V_{CEsat}) and [illegible] inputs are at a high enough voltage to reverse bias all the base emitter [illegible] of the gate transistor. The relatively simple [illegible] analysis of the gate can be described by equations 1 through 4. The gate transistor is alternately switched from forward operation when the gate output transistor is turned off to inverse operation when the gate output transistor is on. The relationship between base current and load current ($I_C = N I_L$) tends to optimize fan-out as the supply voltage is increased. The relationship between power drain and switching speed is shown in Figure 13 for various values of supply voltages and resistor values. Turn-off voltage, as described in [illegible] 4 varies with temperature, since V_{BE} has a negative temperature coefficient of 2-3 mV/°C while V_{CEsat} has a positive temperature coefficient of ≈ 2mV/°C. Thus, base emitter turn-off voltages are relatively independent of design variations in direct coupled circuits, such as T^2L, and tend to become smaller as ambient temperature is increased.

The least obvious problem associated with T^2L circuits are those described in equation 5. When T^2L gates are interconnected in various combinations of fan-in and fan-out conditions, it is possible for a gate transistor to switch to forward operation instead of inverse operation while driving an output transistor. This results in base current being diverted away from the gate output transistor. The major cause of this diversion of current is a mismatch in base emitter voltages of the output transistors, as shown in Figure 14.

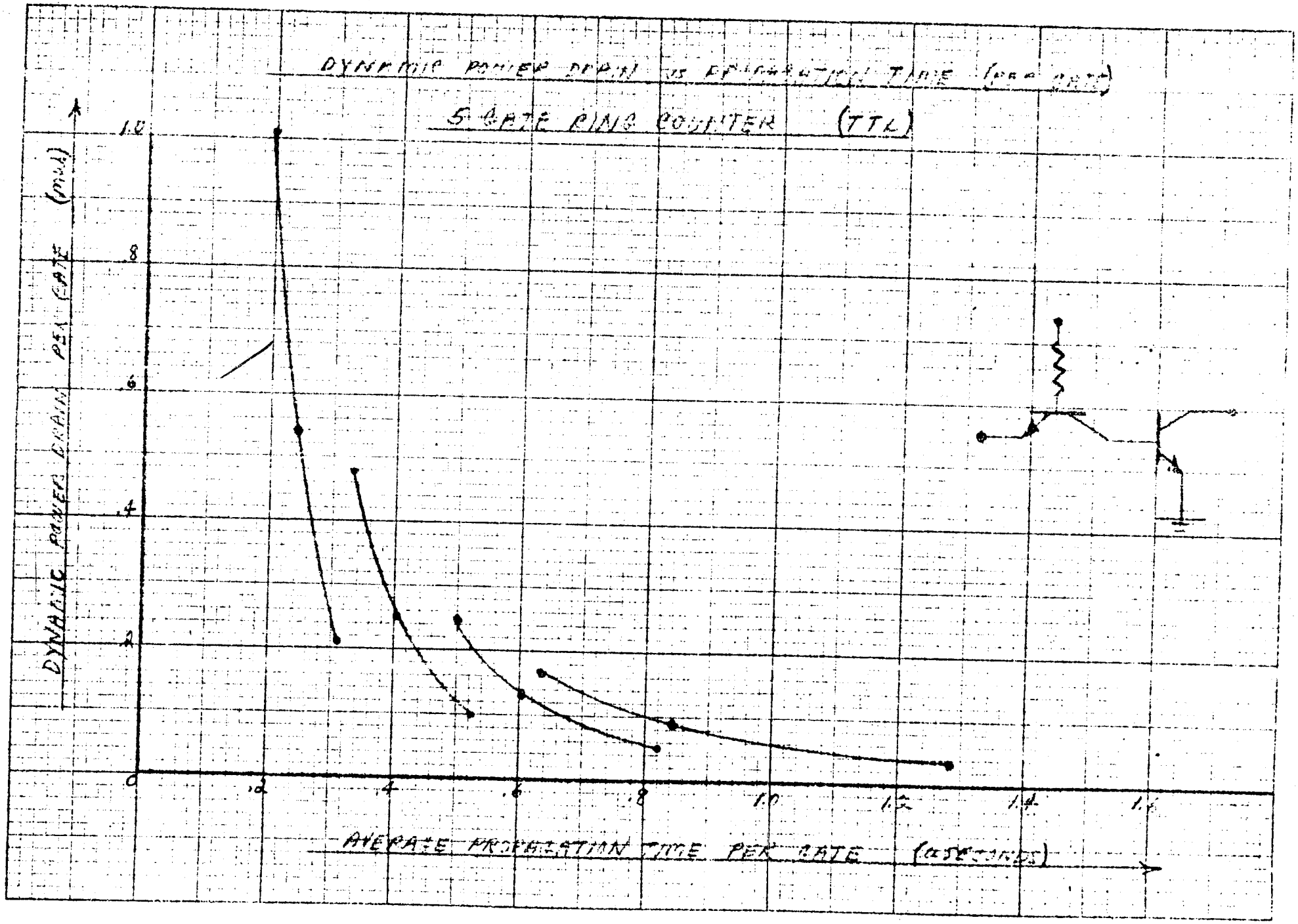

DYNAMIC POWER DRAIN VS PROPAGATION TIME (PER GATE)
5 GATE RING COUNTER (TTL)
DYNAMIC POWER DRAIN PER GATE (mW)
1.0
.8
.6
.4
.2
0
.2
.4
.6
.8
1.0
1.2
1.4
1.6
AVERAGE PROPAGATION TIME PER GATE (microseconds)

FIGURE 13

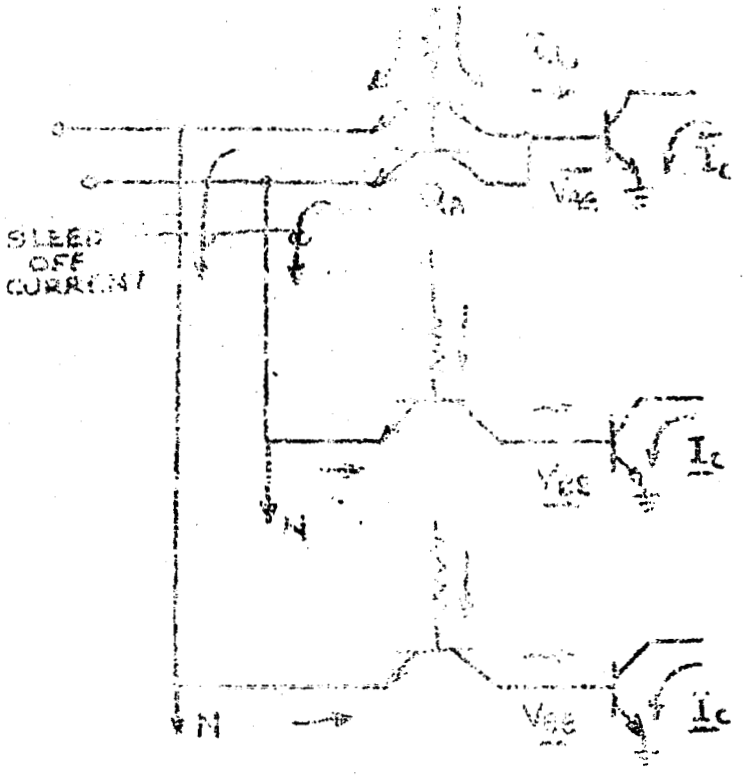


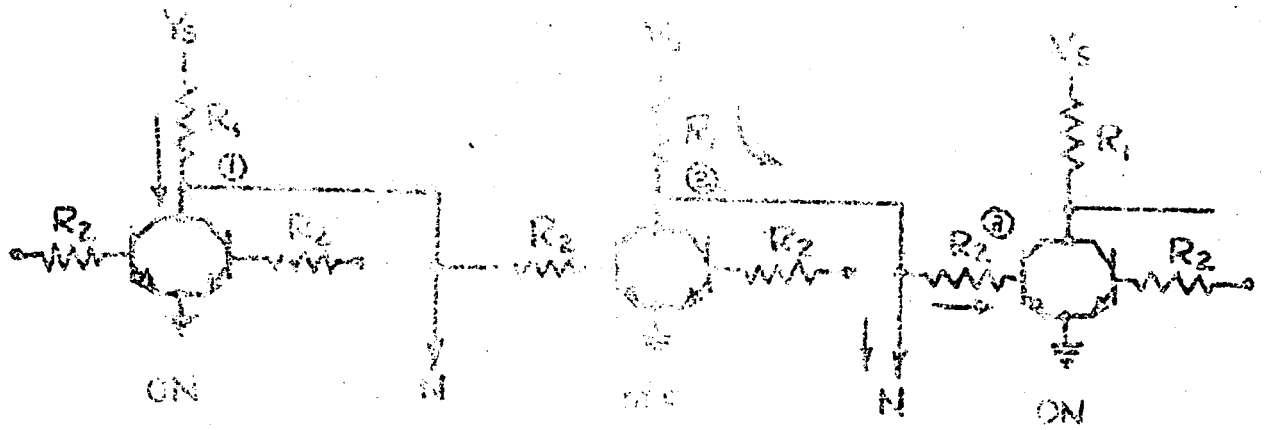
FIGURE 14

This mismatch is reflected through the gating transistor to the emitters of the gate transistors, which, if connected together because of fan-out conditions, must be at the same voltage. It is thus possible to have one gate transistor, Q_A, operating in the forward mode and supplying excess base current to other T^2L gates at the expense of base current being supplied to its own gate output transistor. The extreme case of this condition is outlined in equation 5. This equation indicates that, if a fan-in of 3 and a fan-out of 4 is required, the inverse beta of the gate transistor must be lower than .2 for the gate to be operative. In actual practice this relationship has been found to be too conservative, since the forward and inverse offset voltages of the gate transistors and variations of base-emitter voltage with varying current levels must be considered in determining whether the

gate transistor [illegible] of [illegible] which is implied in equation 5. The mismatch in V_{BE}'s of the output transistors also becomes smaller as the distribution of base current to the output transistors changes as a function of loading conditions.

The combination of fast switching speed and low power drains exhibited by the T^2L configuration indicates that it should be given further consideration in this study program. The relationship of base current to loading conditions outlined in Figure 14 will be more thoroughly investigated in subsequent sections of this report.

The [illegible] voltage [illegible] and design equations are given below:



$$\frac{V_S - V_{CE_{sat}}}{R_1} = I_C \tag{1}$$

$$\frac{V_S - V_{CE_{off}}}{R_1} = \frac{V_o - V_{BE_{sat}}}{R_2} + \frac{(N-1)(V_o - V_{BE_{sat}})}{R_2} \tag{2}$$

$$I_B = \frac{V_o - V_{BE_{sat}}}{R_2} \tag{3}$$

$$\beta_f = \frac{I_C}{I_B} \tag{4}$$

Operation of DCTL is different from the T^2L configuration previously considered, since the gate is turned off only if all of the inputs are at a low voltage (V_{CE}sat) and is turned on if any of the inputs are at a high voltage.

The [illegible] of the [illegible] described in equations 1 through 4 appears quite simple. Optimum utilization of collector current, which is determined by R_1, in driving other stages appears to result when R_2 approaches a short circuit. This relationship would be true if the input characteristics of all stages are similar. The common collector configuration of DCTL permits more than one transistor in a gate to be turned on simultaneously. If the collector-emitter saturation voltage of the transistors is very low, it is possible to forward bias the base collector junction of the gate transistors. This results in a very low base-emitter threshold turn-on voltage for all of the common collector gate transistors. [illegible] one of these gates is part of a gate fan-out that consists of gates with normal input characteristics, the low threshold gate will "rob" most of the available base current and prevent turn on of the other higher input impedance fan-outs. R_2 must be included in the circuit to make the input characteristics of both conditions less extreme. The variations in base emitter turn-on voltage were determined experimentally and solutions of the equations were made in the following sequence:

a. Assume R_1 and solve for I_C.

b. Assume R_2 and N and solve for V_o (output voltage).

c. Solve for I_B

d. Solve for h_{FE}.

A number of solutions was made with varying R_2/R_1 ratios and variable fan-outs (N). The results showing minimum transistor beta requirements and minimum output voltage swings plotted as a function of the R_2/R_1 ratio and fan-out (N) are given in Figure 15. Propagation time vs. power drain characteristics were also measured and are shown in Figure 16.

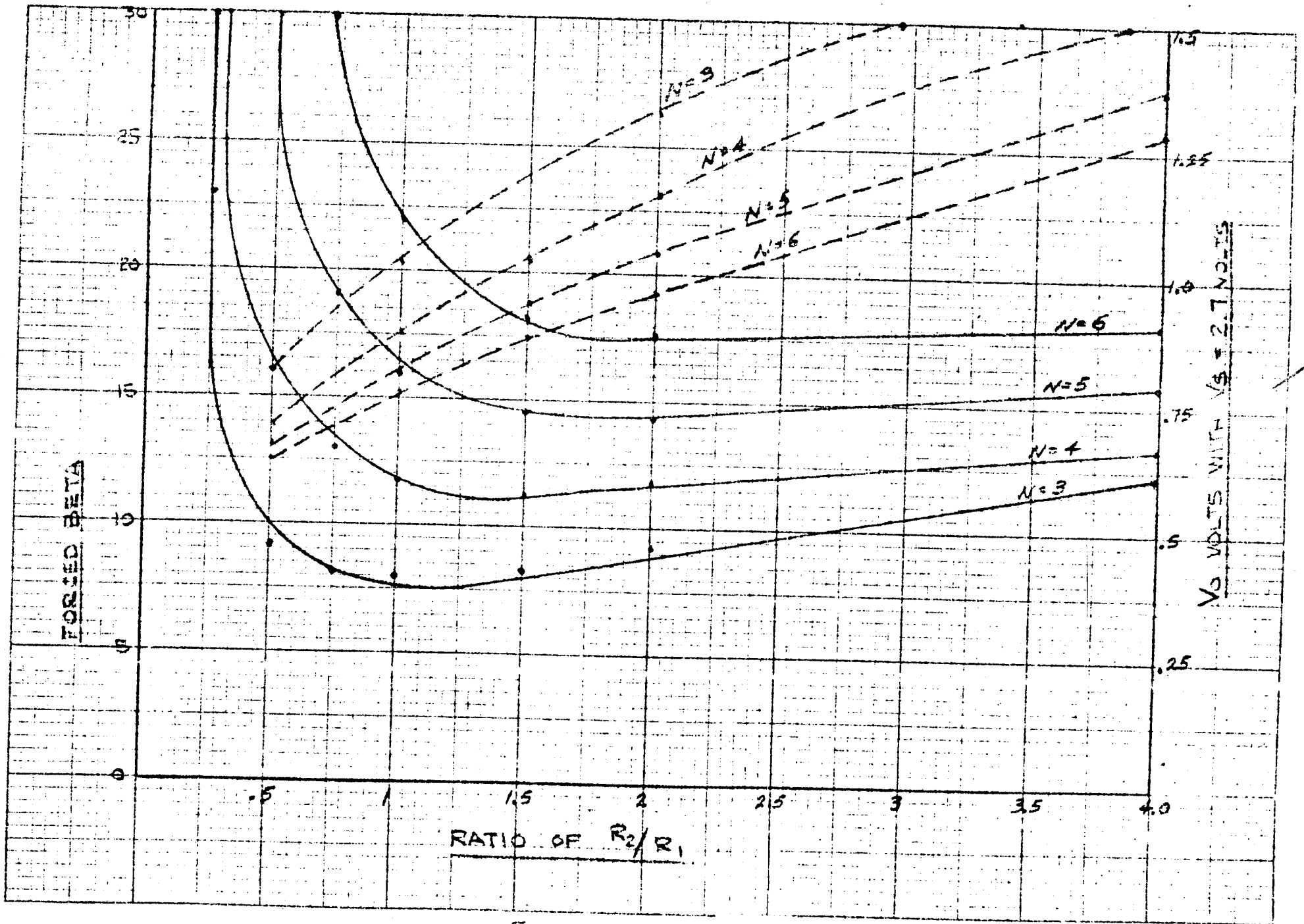

FORCED BETA
30
25
20
15
10
5
0
.5
1
1.5
2
2.5
3
3.5
4.0
RATIO OF R_2/R_1
V_0 VOLTS WITH V_S = 2.7 VOLTS
1.5
1.25
1.0
.75
.5
.25
N=9
N=4
N=5
N=6
N=6
N=5
N=4
N=3

FIGURE 5

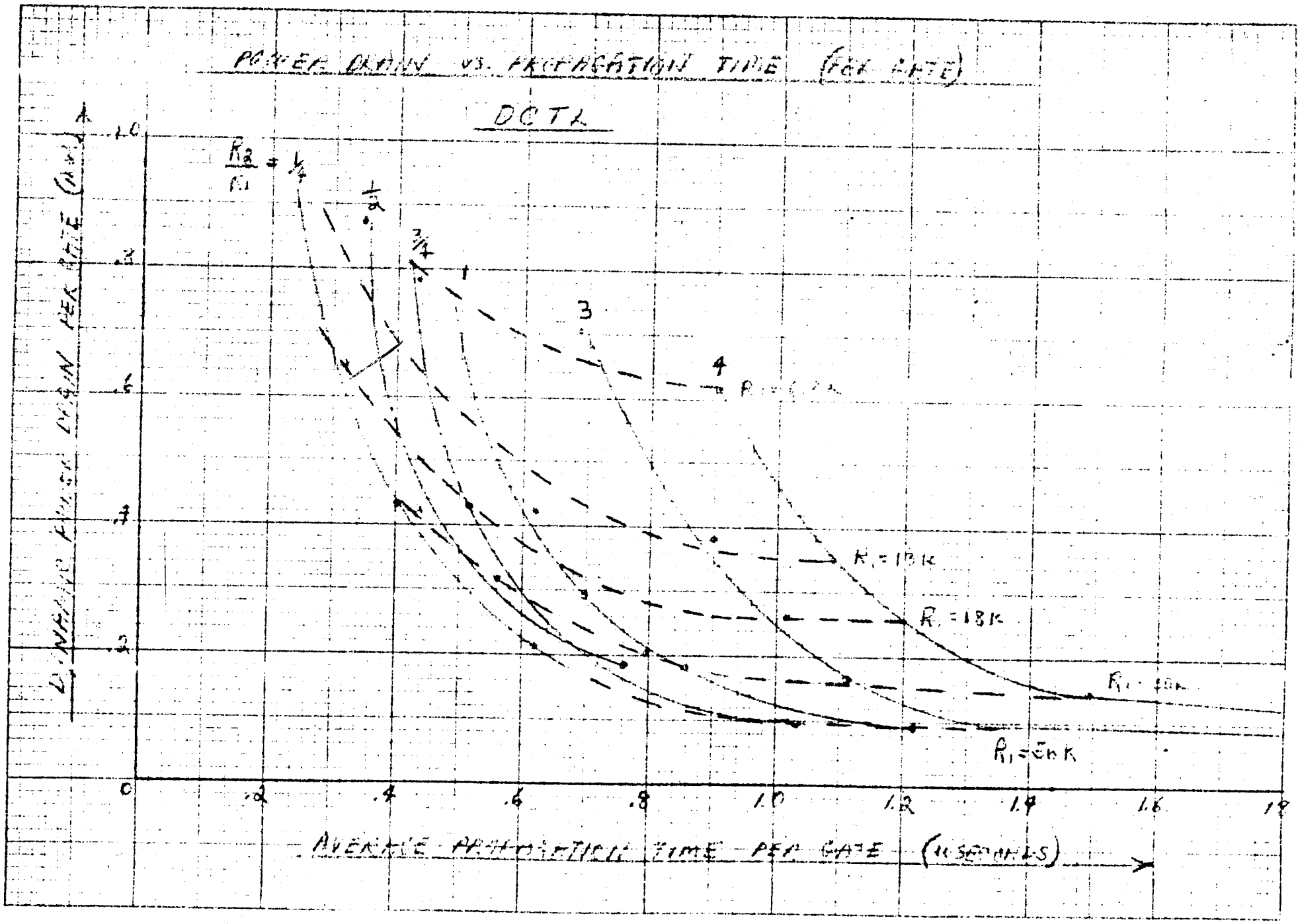

POWER DRAIN VS. PROPAGATION TIME (PER GATE)
DCTL
DYNAMIC POWER DRAIN PER GATE (mW)
AVERAGE PROPAGATION TIME PER GATE (μSECONDS)
R2/R1 = 1/4
1/2
3/4
1
3
4
R1 = 13K
R1 = 18K
R1 = 40K
R1 = 56K
0
.2
.4
.6
.8
1.0
1.2
1.4
1.6
1.8

FIGURE 16

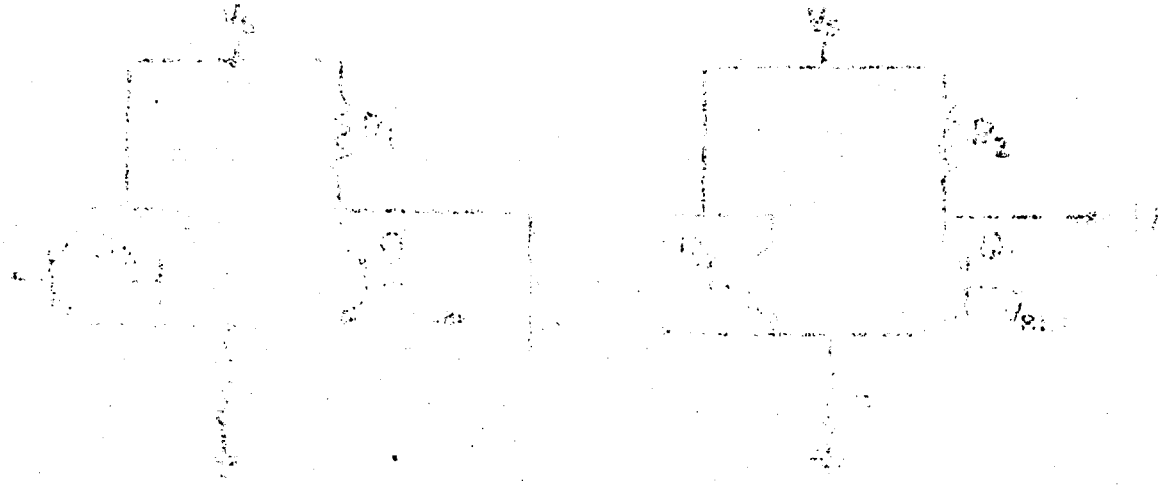
It should be noted that as R_1 becomes large with respect to R_1, the circuit more closely resembles a modified form of RTL than DCTL. Output voltage swings become large enough to be considered for AC coupled logic.

The speed versus power drain characteristics for both circuit extremes (DCTL and Modified RTL) do not offer any improvements over any of the circuits previously considered. The turn-off characteristics of DCTL are comparable with those of T^2L. Power drains are, however, much higher with DCTL than T^2L for constant speed requirements. Modified RTL exhibits much poorer performance than a number of other AC coupled circuits previously considered. Further investigations of the configurations outlined in this section will not be made.

[illegible]

[illegible] ECTL

are [illegible]



$$\frac{V_{ref} - V_{CE_{sat}}}{R_1} = \frac{V_{CE_{sat}}}{R_2} \qquad (1)$$

$$V_{CE_{sat}} = V_{CE_{sat}} - V_{CE_{sat}} + V_{CE_{sat}} \qquad (2)$$

$$\frac{V_{ref} - V_{CE_{sat}}}{R_1} = \frac{V_{CE_{sat}} - V_{CE_{sat}} + V_{CE_{sat}} - V_{CE_{sat}}}{R_2} + V_{ref} \qquad (3)$$

$$V_S - R_2 \frac{I_{C_{sat}}}{\beta} = V_{CE_{sat}} + I_{C_{sat}} R_1 \qquad (4)$$

$$\overline{I_{C_{Q_2}}} = \frac{V_{ref} - V_{BE_{Q_1}} - V_{CE_{Q_1}}}{R_1 \left(1 + \frac{1}{\beta}\right)} \tag{5}$$

$$\overline{I_{E_{Q_2}}} = \frac{V_{ref} - V_{BE_{Q_1}}}{R_1} = \overline{I_{C_{Q_2}}} + \overline{I_{B_{Q_2}}} \tag{6}$$

Emitter coupled logic can be utilized in either the saturated or nonsaturated mode of operation. In the illustrated saturated case the gate output is the collector of Q_1 and the inputs are the bases of the common collector group of transistors (Q_2). The output transistor is turned on only if all the inputs are at a low voltage, such as the saturated output of Q_1.

The design sequence used to optimize the design of the illustrated configuration is as follows:

a. Power supply levels, ha[illegible] reference voltage, and transistor base emitter and colle[illegible]-emitter saturation voltages are assumed.

b. Assume a value for V[illegible]$_2$ and solve for $V_{CE\ sat}$ in equation 2.

c. Assume a value for $\overline{I}$[illegible] and solve for R_1 in equation 5.

d. Solve for R_2 in equation [illegible].

e. Solve for I_{Vref} in equation 3.

f. Solve for I_C @ $\beta = 20$ in equation 5.

g. Solve for $\frac{\overline{I_C}}{\overline{N}}$ in equation 4.

The above equations were solved for various turn-off voltages (V_{off}) and current levels. The variation in performance characteristics as a function of turn-off voltage at a constant current level is outlined in Table 17.

$V_{ob} = V_{BI\,Sat} + V_{DEC}$	[illegible]	I_{Vref}	I_N	Prop. Time/gate
100	2.45 V	15.8	1.7	.56
300	2.25 V	15.4	2.9	.61
500	2.05 V	18.3	3.7	.69
700	1.85 V	19.6	5.9	.76

Table 17

The relationship between turn-off voltage and transistor beta requirements is of particular interest. Propagation time versus turn-off voltage extremes at various current levels were also investigated. The resultant power drain propagation time curves are shown in Figure 18.

The design evaluated above does not permit optimum performance of the emitter-coupled configuration since it is a single output, saturated design.

To permit non-saturated dual output circuit operation, the following configurations may be used:

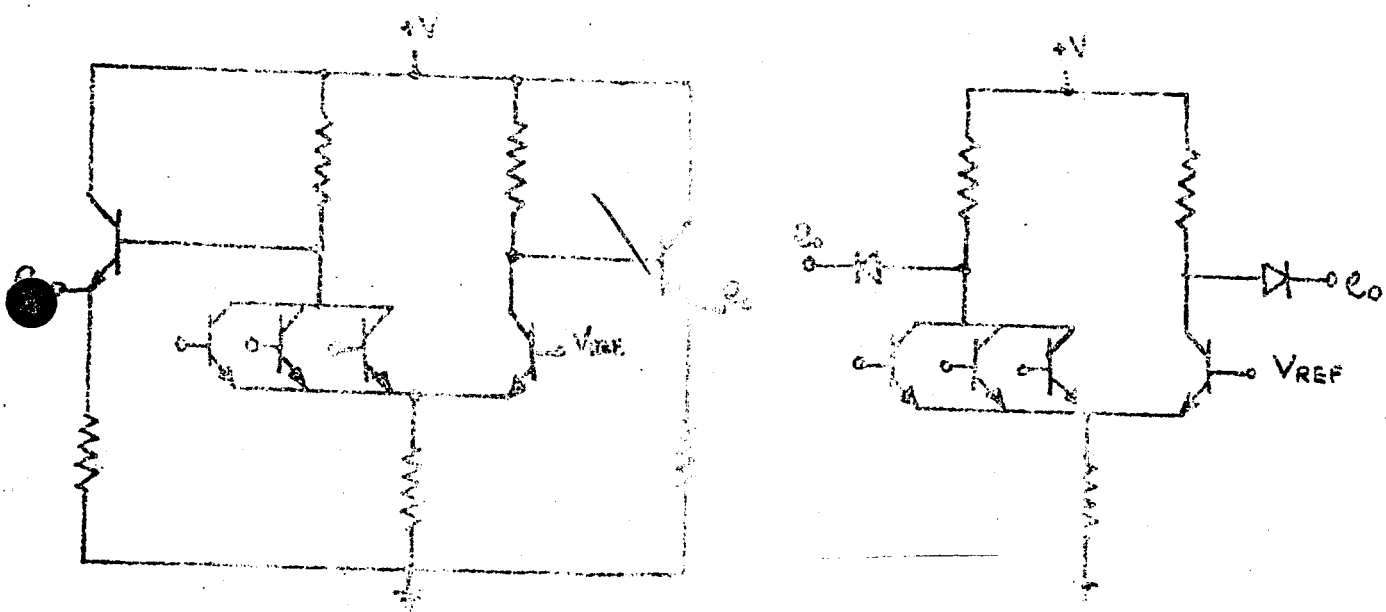
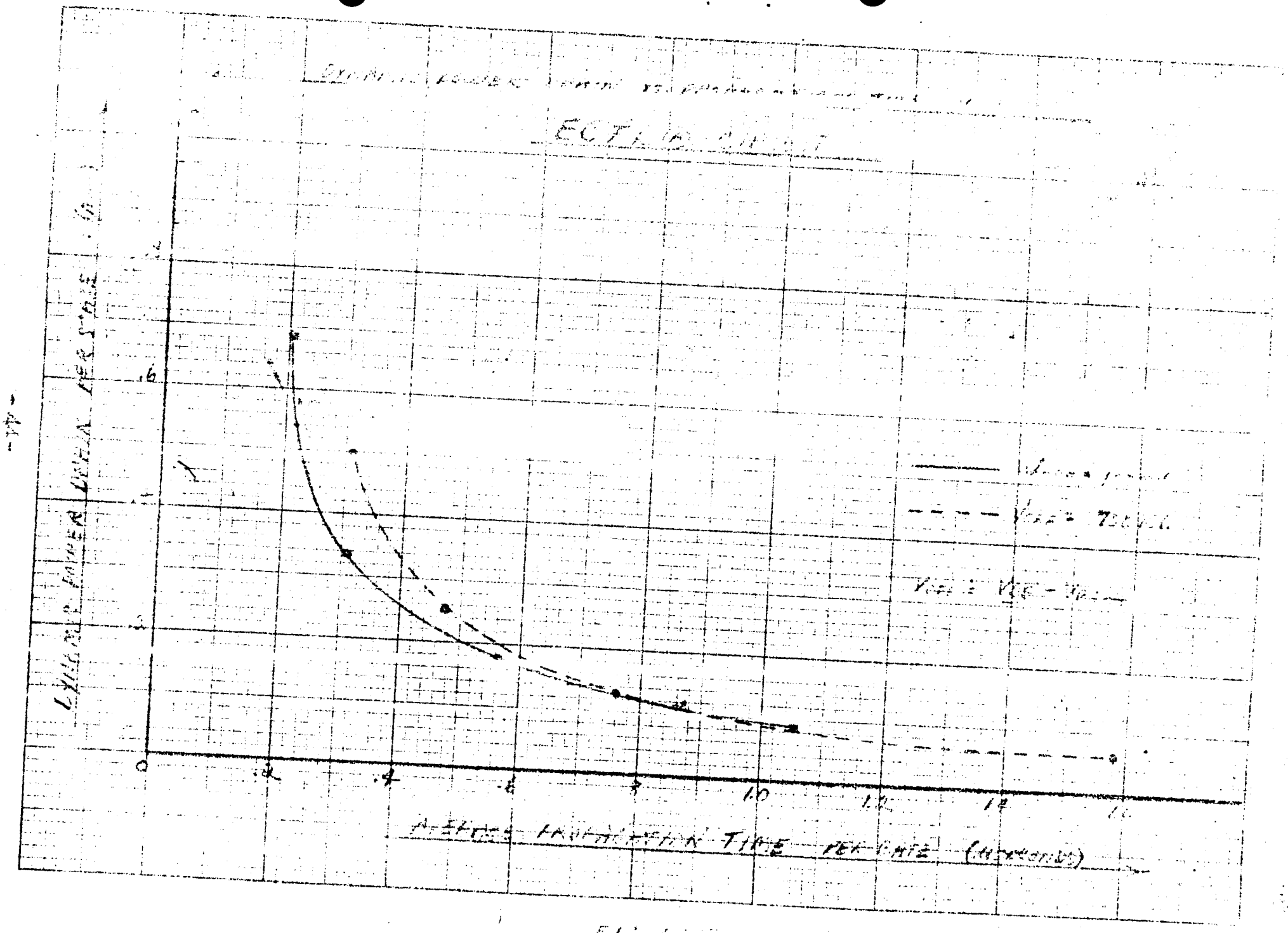


Figure 19



FIGURE

Worst case analysis of the above configurations becomes quite complex if non-saturated operation is required. The equations and methods of solution are not included in this report, since worst case operation with the above circuits could not be accomplished with reasonable resistor tolerances. To insure proper operation, it is necessary to add an additional voltage drop to the gate output voltage level to insure that the input voltage at the driven stages is sufficiently low to turn the input transistors off.

The non-saturated operation results in a rather wide range of output voltage levels for both the "1" and "0" case which adds additional complications to the turn-off problem. Voltage swings are also quite small and are dependent upon loading conditions.

These problems were not encountered in the saturated design discussed earlier by saturating the output transistor.

A nominally designed non-saturated ECTL circuit was breadboarded and evaluated to determine speed versus power drain relationships. Results (.5 usec tp @ 200 mW) indicated that the performance of non-saturated ECTL does not offer a significant performance advantage over saturated ECTL.

The general performance of ECTL presents no significant improvement over previously investigated circuits. The disadvantage of variable output voltage levels and the inability to obtain conservative non-saturated designs indicate that ECTL logic permits no significant advantage over other forms of direct coupled logic investigated.

2.8 SUMMARY

A summary of circuit performance at constant propagation time and constant minimum resistance is shown in Tables 20 and 21. It should be noted that beta requirements are indicated as forced beta per fan-out. Transistor beta should be larger than the required fan-out times this value. If low temperature operation is required the transistor beta degradation vs. temperature must also be considered.

The more promising circuits determined by the investigations outlined in this portion of the report appear to be DTL, complementary RDTL, and T^2L. Each of these configurations represent a general class of digital circuits.

T^2L - Direct Coupled Logic

DTL - Single Transistor A.C. Coupled Logic

Complementary RDTL - Complementary Logic

Each of the above configurations offer the optimum performance at low power drains within its own class. It is inherent to single transistor gates, such as DTL, to degrade in D.C. performance characteristics, as the voltage levels are lowered due to the dependance upon current sources to obtain turn-on and turn-off base current. The complementary circuit investigated, however, tends to improve in D.C. performance as voltage levels are lowered, and appears to be more compatible with low power requirements. A more detailed investigation of each of these configurations to determine which circuit offers the best performance in terms of the requirements previously outlined is made in Section 3 of this report.

TABLE 20

CIRCUIT	CIRCUIT TYPE	PROPAGATION TIME/STAGE	POWER DRAIN	MAX NOISE IMMUNITY	BETA/N	FAN-IN	FAN-OUT
T^4L	Direct Coupled	.5 μsec	110 μW	200 mv	3.5 @ N = 5	3	50%
DCTL		.5 μsec	320 μW	250 mv	5.5 @ N = 3	[illegible]	45%
		.5 μsec	360 μW	250 mv	6.5 @ N = 5	3	50%
ECTL		[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
		[illegible]	240 μW	700 mv	5.5 @ N = 3	3	[illegible]
[illegible]	Complementary	.5 μsec	260 μW	[illegible]	9.0	[illegible]	[illegible]
RDTL	Single Transistor Gate	.5 μsec	420 μW	500 mv	11.0	[illegible]	[illegible]
DTL		.5 μsec	105 μW	200 mv	4.0	3	[illegible]
		.5 μsec	310 μW	400 mv	6.0	3	[illegible]
		.5 μsec	190 μW	600 mv	5.0	3	100%

TABLE 21

CIRCUIT	CIRCUIT TYPE	PROPAGATION TIME / STAGE	POWER DRAIN	MAX NOISE IMMUNITY	FAN-IN	FAN-OUT	[illegible]
[illegible]	Direct Coupled	.5 μsec	110 μW	200 mv	3.5 @ N = 5	[illegible]	[illegible]
DCTL		.6 μsec	220 μW	250 mv	7.5 @ N = 3	[illegible]	[illegible]
		.88 μsec	216 μW	250 mv	6.5 @ N = 5	[illegible]	[illegible]
RCTL		.56 μsec	178 μW	100 mv	2.0 @ N = [illegible]	[illegible]	[illegible]
		.58 μsec	210 μW	300 mv	[illegible]	[illegible]	[illegible]
[illegible]		1.22 μsec	[illegible]	200 mv	[illegible]	[illegible]	[illegible]
CMOS	Complementary	.35 μsec	450 μW	[illegible]	[illegible]	[illegible]	[illegible]
		.25 μsec	250 μW	150 mv	12.0	[illegible]	[illegible]
RCTL	Single Transistor Gate	.17 μsec	1000 μW	500 mv	11.0	[illegible]	[illegible]
DTL		.18 μsec	385 μW	300 mv	4.0	[illegible]	[illegible]
		.4 μsec	405 μW	400 mv	6.0	[illegible]	[illegible]
		.3 μsec	395 μW	600 mv	5.0	[illegible]	[illegible]

3 [illegible]

3.1 Complementary RTL

The preliminary investigation of RTL gates used a design procedure that resulted in similar turn off voltages and dissimilar base current for the two gate transistors. To further investigate performance characteristics of the configuration the following design procedures were used:

A. Assume the maximum resistance value in the following group of designs [illegible] constant. For comperative purposes the maximum resistance value was assumed to be 50K Ω.

B. Various values of base currents were assumed for one of the gate transistors. One group of designs was completed with equal base turn-off voltages at various values of I_B as the design criteria. Resistor tolerances were assumed to [illegible] 10%. The results of these designs are given in Table [illegible].

I_{BO_1}	I_{BO_2}	$I_{C/N}$	R_1	R_2, R_4	[illegible]	V_{BEoff} Q_1, Q_2	$\beta_f Q_{1/N}$	$\beta_f Q_{2/N}$
5 μa	14.5 μa	131 μa	48K	24K	[illegible]	.14 V	2[illegible].2	9.0
7.5	16.2	139	45K	23K	[illegible]	.165 V	18.7	8.6
10	18.6	147	44K	22K	[illegible]	.18 V	14.7	7.9
15	23.4	161	40K	20K	[illegible]	.23 V	10.7	6.9
20	30.2	185	34K	18K	[illegible]	.25 V	9.3	6.1
30	45.7	240	25K	16K	50K	.30 V	8.0	5.3

Table 22

Although base turn-off voltages are equal, the magnitude of this parameter varies as the base current is varied.

The unequal [illegible] of base current also results in conflicting transistor beta requirements for the two gate transistors. The relationship between turn-off voltage and transistor beta requirements is obvious if the information shown in Table 22 is analyzed.

C. A second group of designs was completed using equal values of base current as the design criteria. Turn-off voltages for the two transistors in the gate were allowed to vary with respect to each other as the magnitude of base current was varied. The results of these designs are shown in Table 23.

$I_{B_{Q_1}}$ = $I_{B_{Q_2}}$	R_1	R_2, R_4	R_3, R_5	$V_{B\,Eff\,Q_1}$	$V_{B\,Eff\,Q_2}$	fQ_1Q_2/N
5 [illegible]	[illegible]K	24K	[illegible]	.29V	.14V	20.0
7.5 [illegible]	73K	23K	[illegible]	.30	.165V	14.3
10 [illegible]	67K	22K	[illegible]	.32	.18V	11.5
15 [illegible]	56K	20K	[illegible]	.35	.23V	8.7
20 [illegible]	52K	18K	[illegible]	.38	.25V	7.4

Table 23

There is again a trade-off between transistor beta requirements and transistor turn-off voltages as shown in Table 23.

The design information included above indicates that the design of a complementary gate with design criteria selected to provide equal base currents and turn-off voltages to obtain complementary performance characteristics is not feasible at the power supply levels available. The decision to attempt to design complementary gates is one of the many possible solutions but does present a logical choice of design criteria. It should be pointed out that a wide variety of gate performance characteristics

is possible within the areas as demonstrated in Tables 22 and 23.

If other non-complementary design criteria were desired the number of possible design approaches becomes astronomically large and will not be considered with the scope of this report.

To approach complementary performance, it is necessary to determine a compromise solution between the two design approaches ($I_{B\,Q1} = I_{B\,Q2}$ or $V_{BEO\,Q1} = V_{BEO\,Q2}$) outlined in Tables 22 and 23. Through inspection, it becomes apparent that a reasonable compromise may be obtained by varying the value of R_1 to reach a compromise between the conflicting transistor beta requirements and turn off voltages. The design values outlined in Table 24 were obtained in an arbitrary manner, but do indicate the relationships between the design approaches outlined in Tables 22 and 23.

R_1	$R_2 R_4$	$R_3 R_5$	Resistor Tol.	$I_{B\,Q1}$	$I_{C\,Q1}$	$V_{BEoff\,Q1}$	$V_{BEoff\,Q2}$	$\beta_{f\,Q1A}$	$\beta_{f\,Q2A}$	$I_{C\,N}$
45K	20K	50K	5%	21 μa	[illegible] μa	.19 V	185 V	6.7	5.3	142 μa
↓	↓	↓	7.5%	18.3 μa	[illegible] μa	.24 V	205 V	8.0	6.2	147 μa
			10%	15.7 μa	[illegible] μa	.29 V	234 V	9.6	7.2	151 μa

Table 24

Resistor tolerances were varied from 10% to ± 5% for this design to determine the effect of changing this design criterion on circuit performance.

A choice must now be made between investigation of a large number of designs to further clarify the power drain - propagation time relationship outlined in section II of this report or to fully investigate one or two designs for performance characteristics of the circuit with

respect to propagation time variations with loading (fan-in and fan-out) over the temperature range of interest. The latter approach offers the greater insight into any performance limitations that are not immediately apparent, and will be persued in the remainder of this report.

The circuit outlined in Table 24 was chosen as a typical design to be used for this evaluation. The power drain of this gate is approximately 500μ watts. Lower power drain gates can obviously be achieved if resistance values are increased. The subsequent decrease in switching speed characteristics would of course accompany such a change.

A group of limit sample transistors was selected to determine the effect of transistor storage time, frequency response and beta on circuit performance. The units selected consisted of four groups as outlined below:

1. $\underline{h_{FE}}$ $\underline{\tau_s}$
2. $\underline{h_{FE}}$ $\underline{t_s}$
3. $\overline{h_{FE}}$ $\overline{\tau_s}$
4. $\overline{h_{FE}}$ $\underline{t_s}$

The effect of loading on the gates was also investigated be varying input conditions up to fan-in of three and output conditions from fan-outs of up to four NAND and NOR gates simultaneously. Since complementary semiconductors and design techniques have been used throughout, the design procedures apply equally well to both NAND and

NOR gates shown in Figure 28.

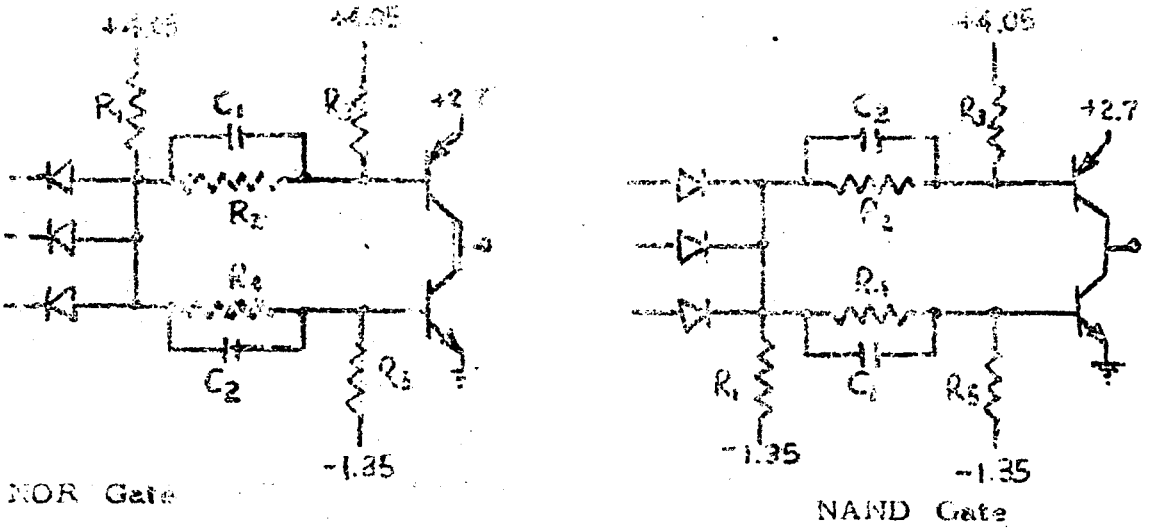


Fig. 28

DC performance characteristics outlined in Table 24 apply well to both configurations because of the symmetrical nature of the gate designs.

In determining the optimum values of speed-up capacitors to be used in the gates, it was found that optimum performance was obtained if the values of the speed-up capacitors were not identical as would be expected in a complementary circuit using complementary transistors. The advantage of unequal speed-up capacitors may be explained by considering the waveform at the gate node of the circuit. For one edge of the waveform the gate diodes are forward biased and reflect the input waveform at the gate node. As the gate diodes are reverse biased at the other edge of the input waveform, the gate node waveform is dependent upon the RC time constants inherent in the gate. The turn-off charge transferred to

the transistor around the speed-up capacitor ($\Omega = C\frac{dV}{dt}$) are, therefore, different for both edges of the waveform. Thus we necessitate to use unequal speed-up capacitors.

The large number of transistor parameters and loading variations inherent in the complementary circuit did not permit the determination of any specific values of capacity as the optimum values. Capacitor values of C_1=15pf and C_2=50pf offered the best circuit performance at 25°C with no loading variations. This circuit was evaluated for worst case propagation time over extremes of temperature.

The schematic diagram outlining the measurement techniques used to obtain two stage propagation time characteristics is shown in Figure 26.

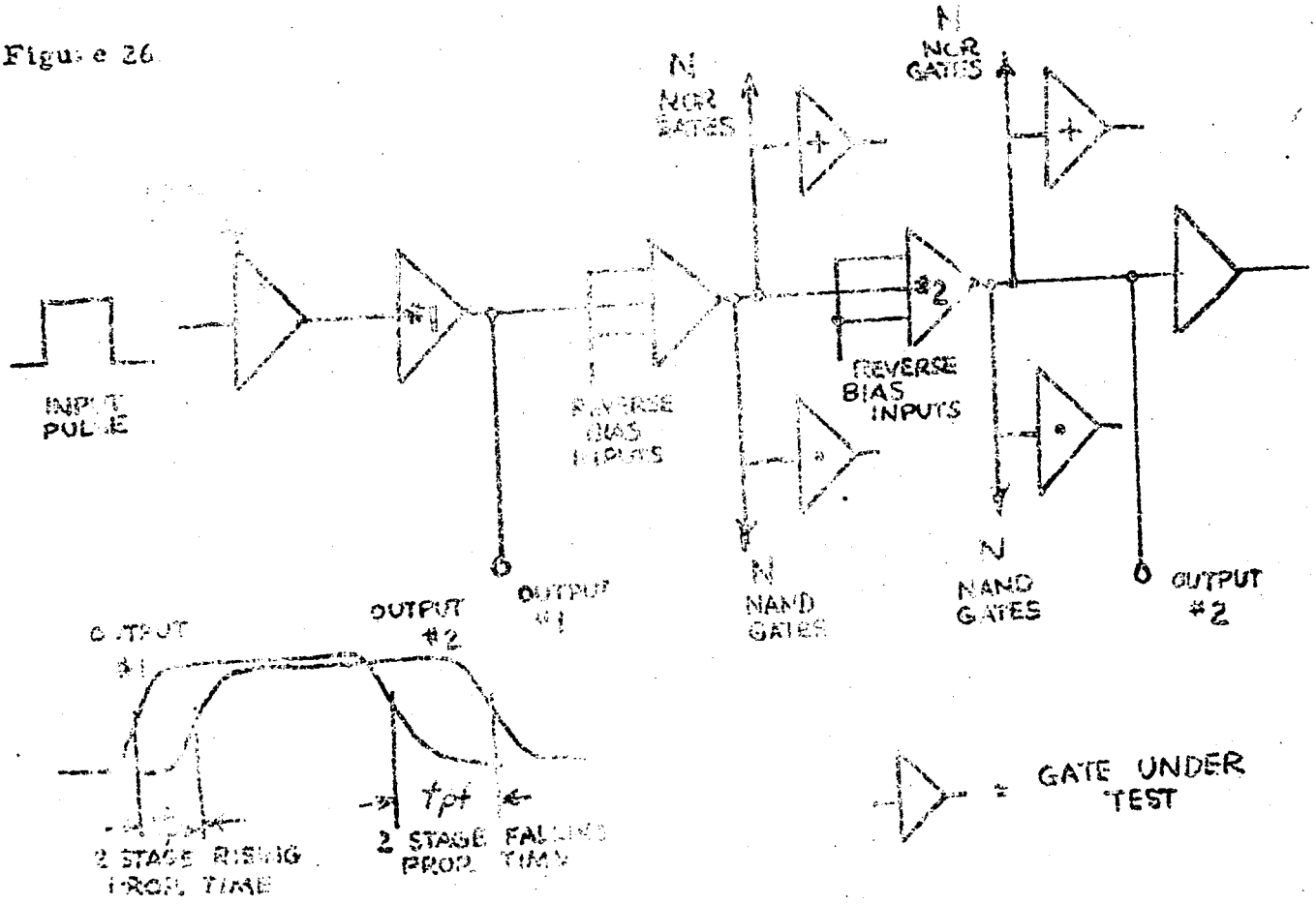


Fig. 26

Two stage propagation time was measured between the 50% points on the output waveforms of gates #1 and #2.

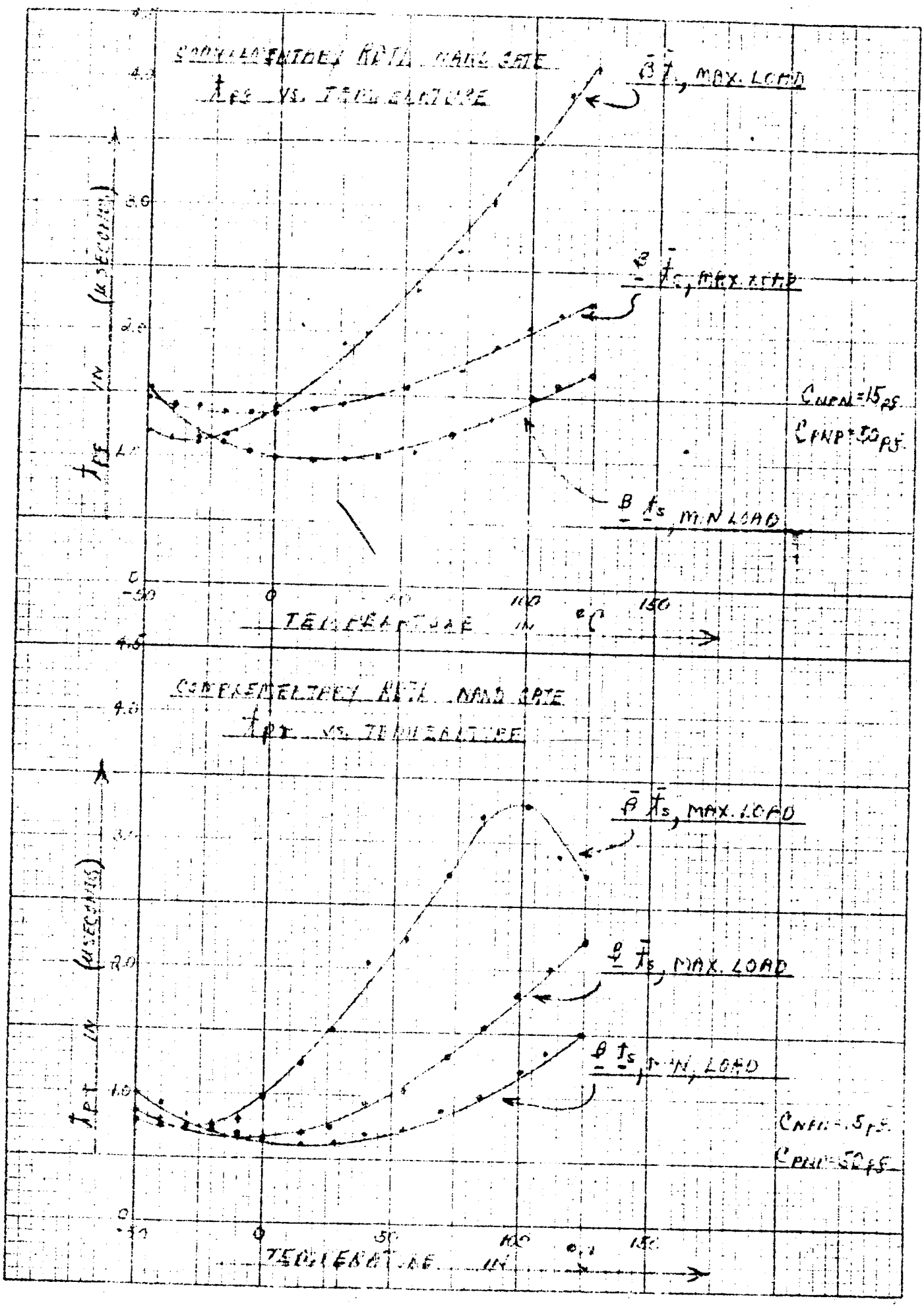
Typical performance characteristics as a function of transistor parameters with constant load, and performance characteristics as a function of loading effects with constant transistor parameters as a function of temperature was investigated. Maximum propagation time was obtained from conditions 1 and 2 outlined below and minimum propagation time was obtained from condition 3 outlined below.

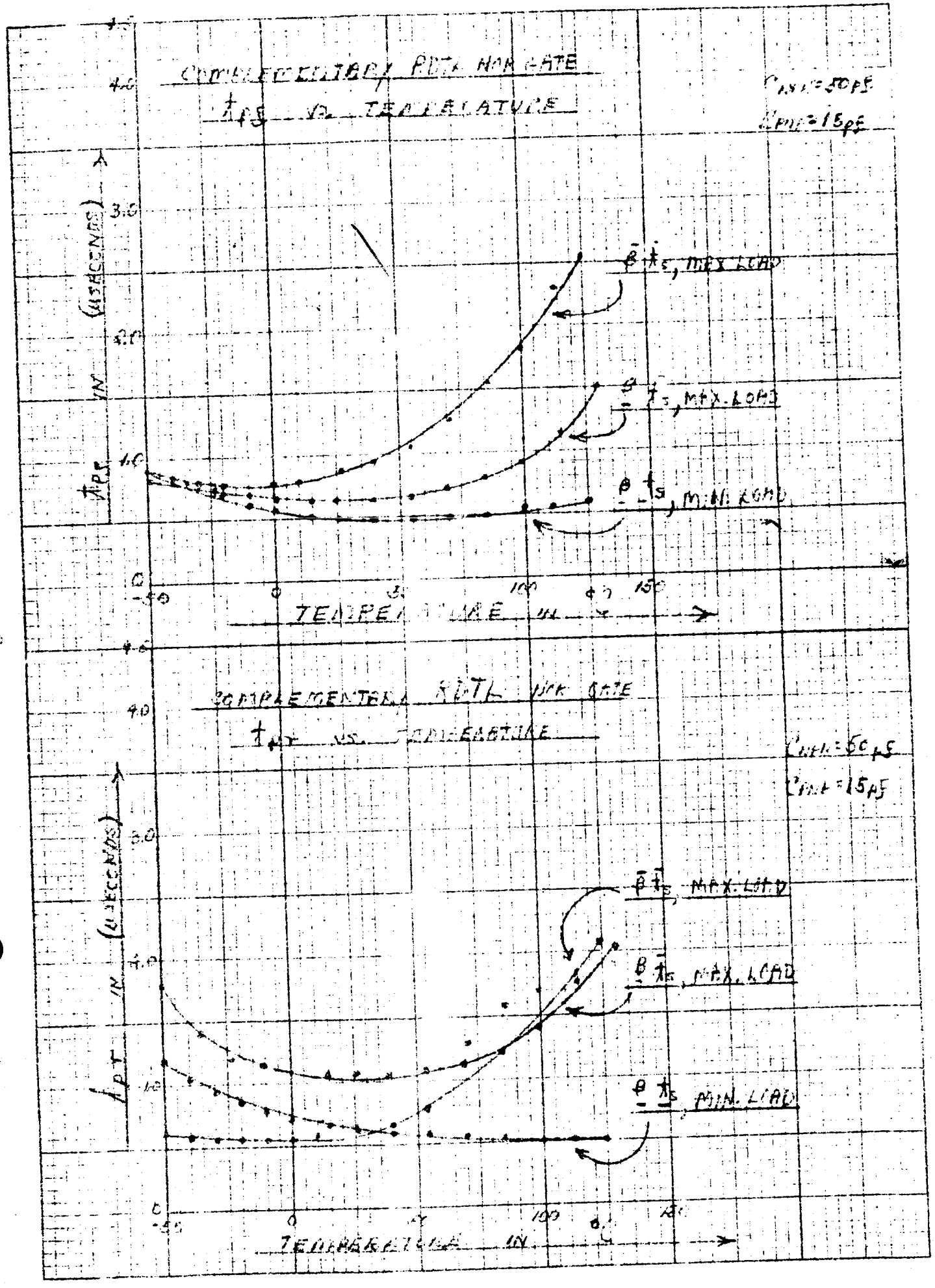
NAND and NOR Gates:

1. Minimum beta and maximum storage time transistors at maximum fan-in and fan-out conditions.
2. Maximum beta and maximum storage time transistors at maximum fan-in and fan-out conditions.
3. Minimum beta and minimum storage time transistors at minimum fan-in and fan out conditions.

The two stage propagation time of both gates for the above conditions is shown in Figure 27 and 28.

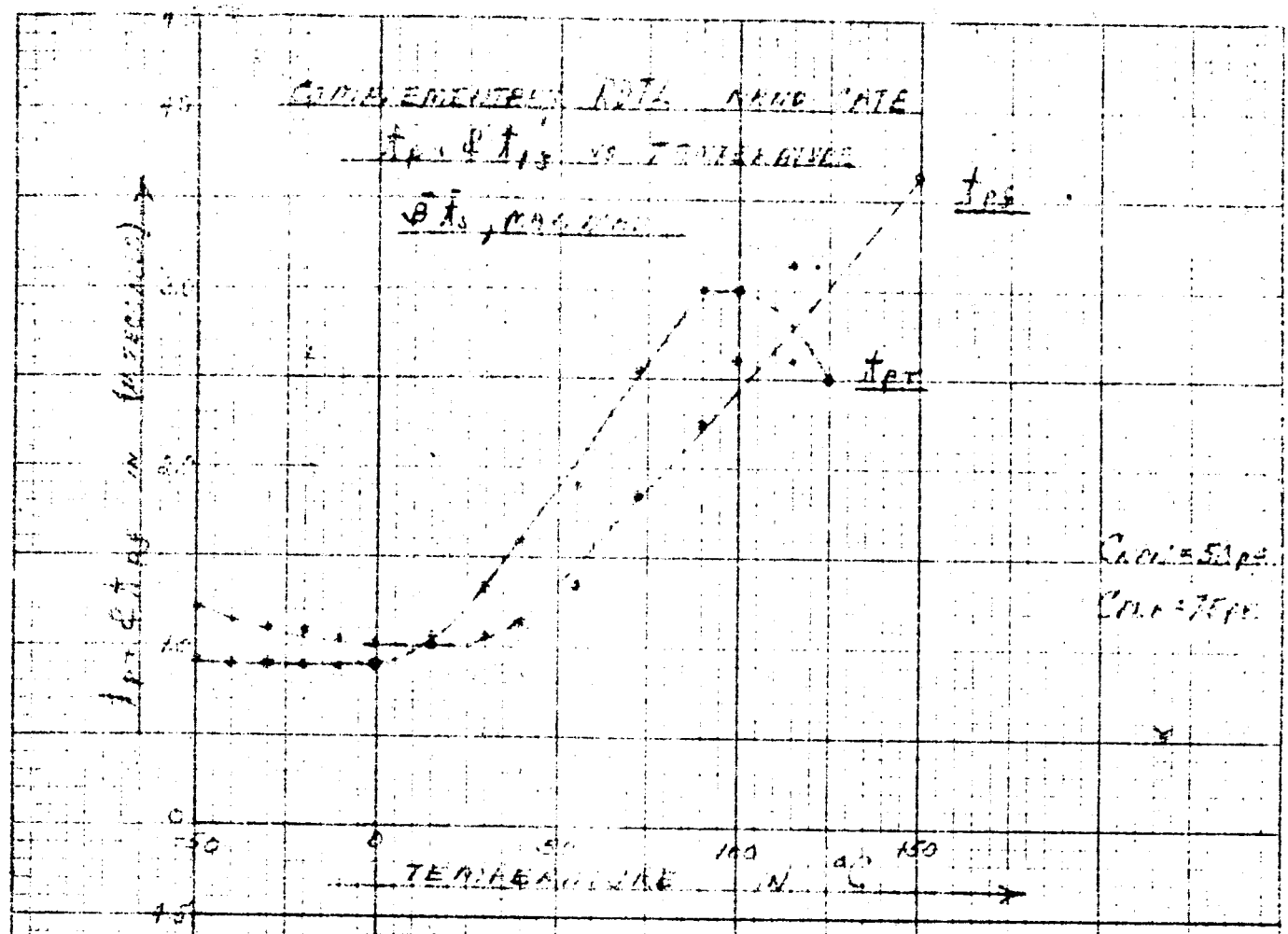
The speed-up capacitors were selected from 25 C performance characteristics and were not necessarily optimum over the entire temperature range. The relatively poor worst case performance of the gates at high temperatures tends to support this possibility. Larger values of capacity (C_1 = 50pf C_2 = 75pf) were used in the worst case propagation time conditions ($\overline{\beta}, \overline{t_s}$ transistors, max loading) to investigate this possibility.

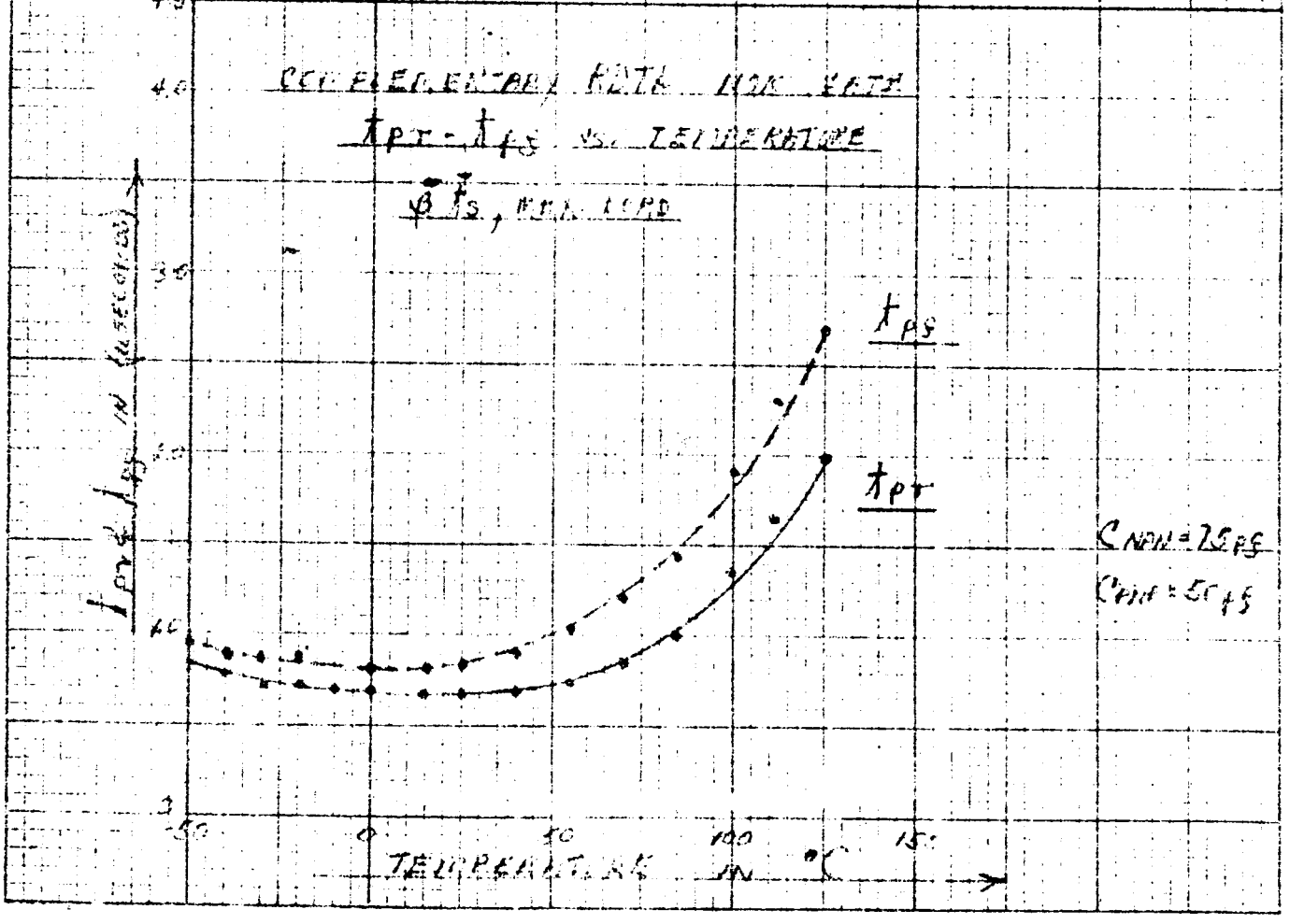

COMPLEMENTARY RDTL NAND GATE
t_{pf} VS. TEMPERATURE
$\bar{\beta}\,\bar{t}_s$, MAX. LOAD
$\underline{\beta}\,\bar{t}_s$, MAX. LOAD
$\underline{\beta}\,\underline{t}_s$, MIN LOAD
$C_{NPN}=15$ pf
$C_{PNP}=50$ pf
t_{pf} IN (μSECONDS)
TEMPERATURE IN °C
COMPLEMENTARY RDTL NAND GATE
t_{pr} VS. TEMPERATURE
$\bar{\beta}\,\bar{t}_s$, MAX. LOAD
$\underline{\beta}\,\bar{t}_s$, MAX. LOAD
$\underline{\beta}\,\underline{t}_s$, MIN. LOAD
$C_{NPN}=15$ pf
$C_{PNP}=50$ pf
t_{pr} IN (μSECONDS)
TEMPERATURE IN °C

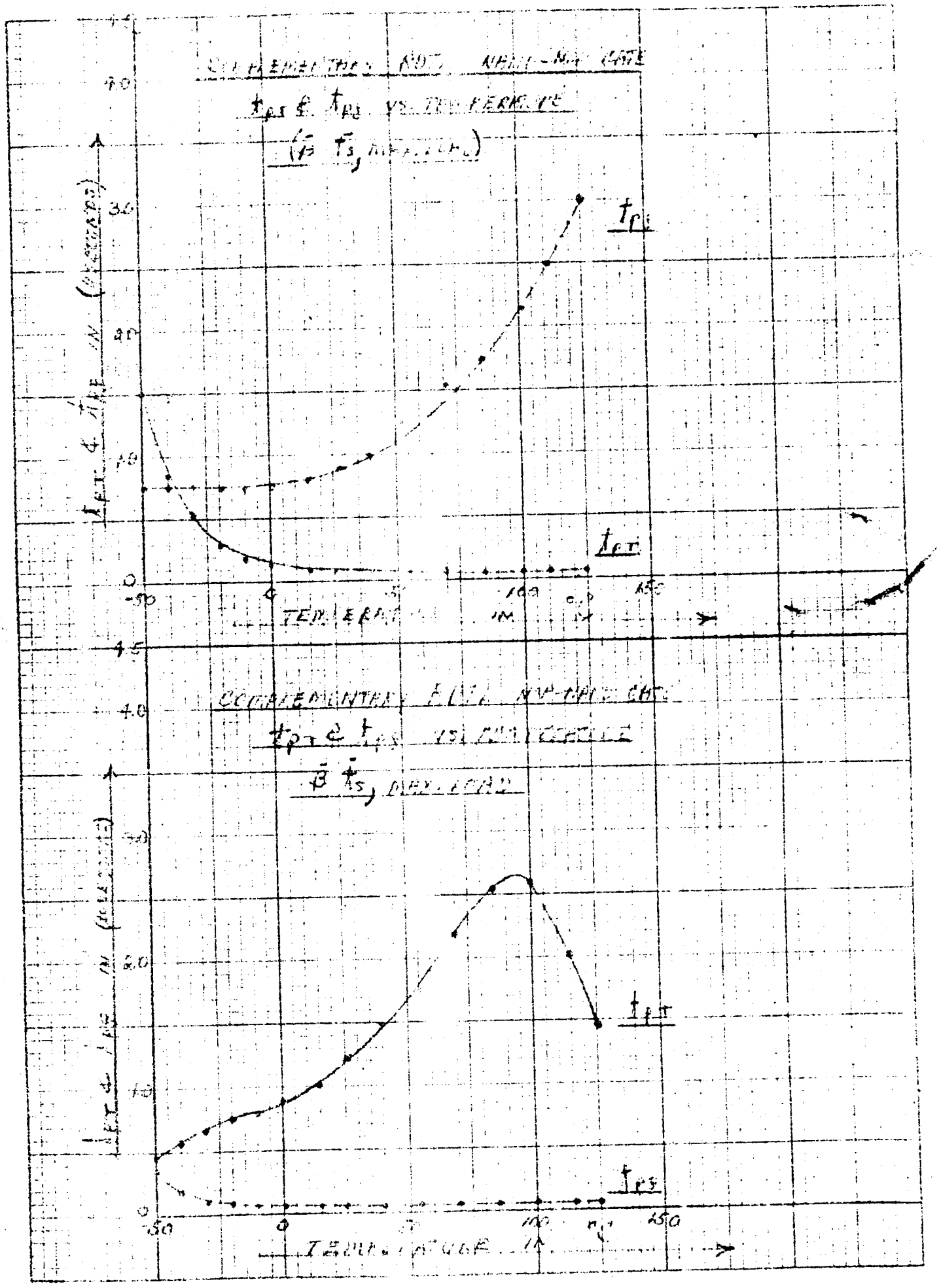

COMPLEMENTARY RDTL NOR GATE
t_{PS} vs. TEMPERATURE
C_{NPN} = 50 pF
C_{PNP} = 15 pF
t_{PS} IN (μSECONDS)
$\bar{\beta}\,\bar{t}_s$, MAX LOAD
$\underline{\beta}\,\bar{t}_s$, MAX. LOAD
$\underline{\beta}\,\underline{t}_s$, MIN. LOAD
TEMPERATURE IN °C
COMPLEMENTARY RDTL NOR GATE
t_{PT} vs. TEMPERATURE
C_{NPN} = 50 pF
C_{PNP} = 15 pF
t_{PT} IN (μSECONDS)
$\bar{\beta}\,\bar{t}_s$, MAX. LOAD
$\underline{\beta}\,\bar{t}_s$, MAX. LOAD
$\underline{\beta}\,\underline{t}_s$, MIN. LOAD
TEMPERATURE IN °C

The propagation time information obtained is shown in Figure 29. The improvement in performance characteristics indicate that these larger capacity values should be used to obtain performance improvements. These capacitor values were selected to be compatible with the flip flop requirements as outlined in the following section. The advantage of this compatibility will become obvious when final packaging of the circuit is considered.

The worst case propagation time performance characteristics of the gates in a NAND - NOR and NOR - NAND sequence was also investigated. The results are shown in Figure 30. The information outlined in Figure 29 and 30 are worst case circuit characteristics and should not be considered as typical performance.


COMPLEMENTARY RDTL NAND GATE
t_{pr} & t_{pf} vs TEMPERATURE
$\bar{\beta}\bar{t}_s$, MAXIMUM
t_{pf}
t_{pr}
t_{pr} & t_{pf} IN (μSECONDS)
TEMPERATURE IN °C
-50
0
50
100
150
0
1.0
2.0
3.0
4.0
4.5


COMPLEMENTARY RDTL NOR GATE
t_{pr} - t_{pf} vs. TEMPERATURE
$\bar{\beta}\bar{t}_s$, MAX. LOAD
t_{pf}
t_{pr}
t_{pr} & t_{pf} IN (μSECONDS)
TEMPERATURE IN °C
-50
0
50
100
150
0
1.0
2.0
3.0
4.0
4.5



t_{pT} & t_{pS} vs. TEMPERATURE
t_{pS}
t_{pT}
TEMPERATURE IN
t_{pT} & t_{pS} vs. TEMPERATURE
$\bar{\beta}\ \bar{t}_s$, MAX. LOAD
t_{pT}
t_{pS}
TEMPERATURE IN

30

[illegible]

[illegible] determine the optimum [illegible] the flip-flop [illegible] configurations shown in [illegible] were considered.

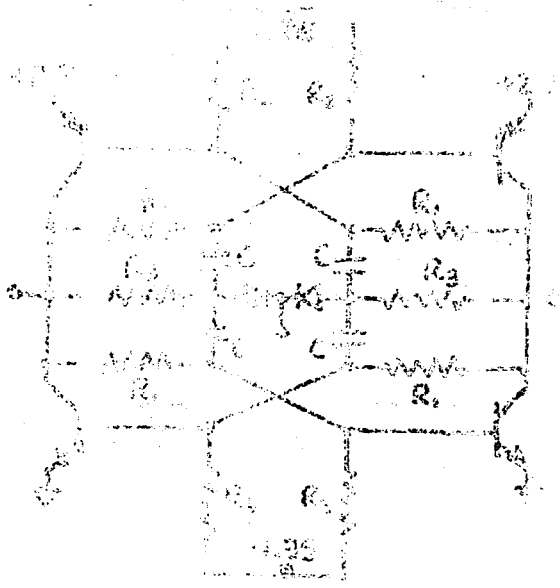


Fig. 31

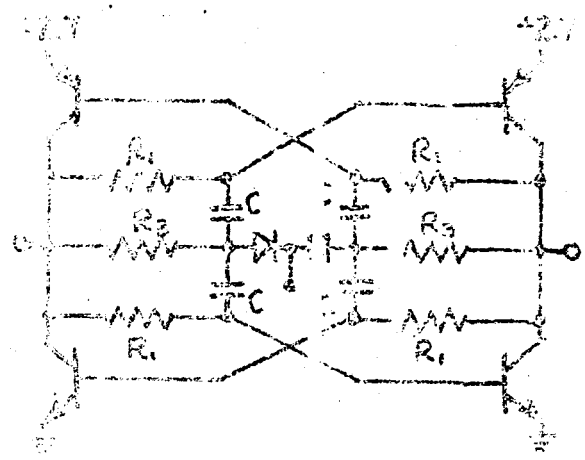


Fig. 32

When considering the flip-flop shown in Figure 31, a trade-off must [illegible] between flip-flop sensitivity, turn-off voltage, power drain, and to a resistance value. These considerations are conflicting if a constant base current is assumed. Low resistance value bias resistors will keep resistance values low but will result in higher transistor beta requirements and much lower triggering sensitivity. Power drain will also be high if [illegible] are made to minimize resistance values, particularly in vi[illegible] [illegible] for the bias resistors.

The possibility of [illegible]ying the triggering action of the flip-flop through combinations of steering and speed-up capacitors was investigated. It is desirable to limit the number of capacitors used in the flip-flop to facilitate integration of the circuit. Designs incorporating these various triggering techniques are shown in Figures 33 and 34.

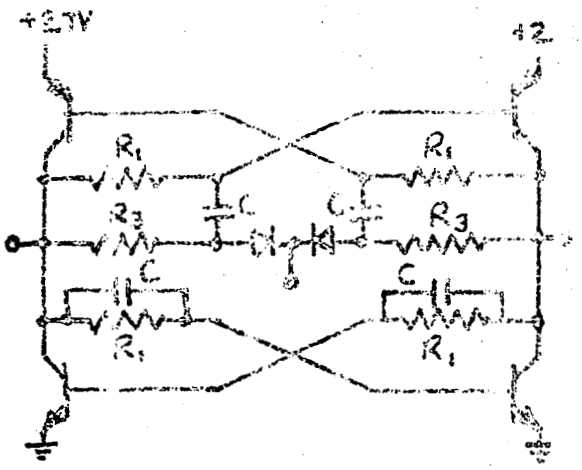


Fig. 33

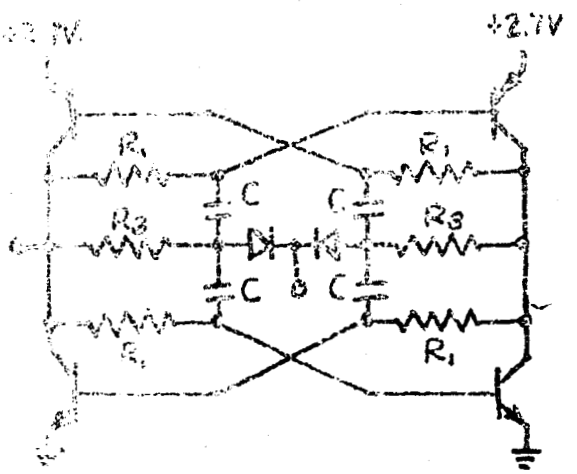


Fig. 34

The design shown in [illegible]ure 33 utilizes steering capacitors to trigger the FLIP's and speed-up [illegible]itors with the NPN transistors to speed up the regenerative action. [illegible] design shown in Figure 34 uses the more conventional steering techniques [illegible] obtain the complementing function.

The design using steering and speed-up techniques shows some performance advantage (triggering repetition rate) over the steered flip-flop at room temperature. When operation over a wide temperature range is considered, however, the steered version of the flip-flop exhibits

a much more uniform performance characteristic as shown in Figure 35.

Because of this performance advantage over a wide temperature range, the remainder of this report will consider only the flip-flop shown in Figure 34. Investigations of common cathode diode complementing inputs resulted in poorer performance than that exhibited by the configuration in Figure 34.

All flip-flop frequency response measurements were made with a gate described in the preceding portion of this report driving the flip-flop. The flip-flop driver was isolated from the pulse generator by inserting a series of gates between the pulse generator and the flip-flop.

As in the gate design, the greater emphasis will be placed upon a thorough evaluation of one design rather than a broad, less detailed evaluation of many designs.

It is desirable from a systems standpoint to have the flip-flop as compatible in performance and loading conditions (fan-in and fan-out) with the gates as possible.

The flip-flop configuration selected makes optimum use of base current because there is no bias resistor to bleed off potential base current. Preliminary investigations indicate that flip-flop base currents may be higher than gate base currents with somewhat lower DC input current requirements. The configuration shown in Figure 34 was evaluated with various combinations of R_1 and R_3, between 35KΩ and 75KΩ. The design that offered the best power drain, repetition rate and loading characteristics with the gates is shown in Figure 36.

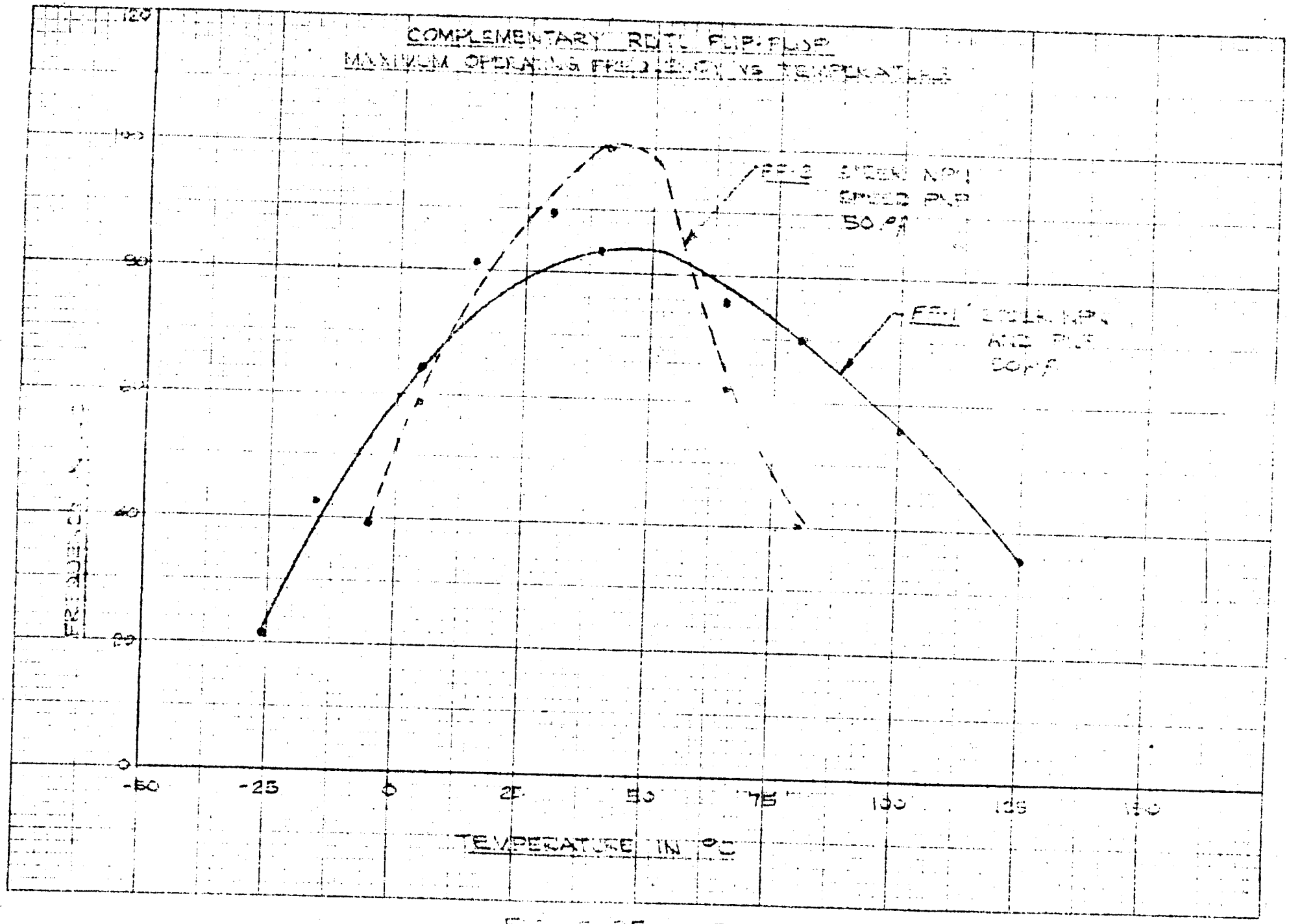

COMPLEMENTARY RDTL FLIP-FLOP
MAXIMUM OPERATING FREQUENCY VS TEMPERATURE
FREQUENCY
TEMPERATURE IN °C
-50
-25
0
25
50
75
100
125
150
0
20
40
60
80
100
120

FIGURE 35

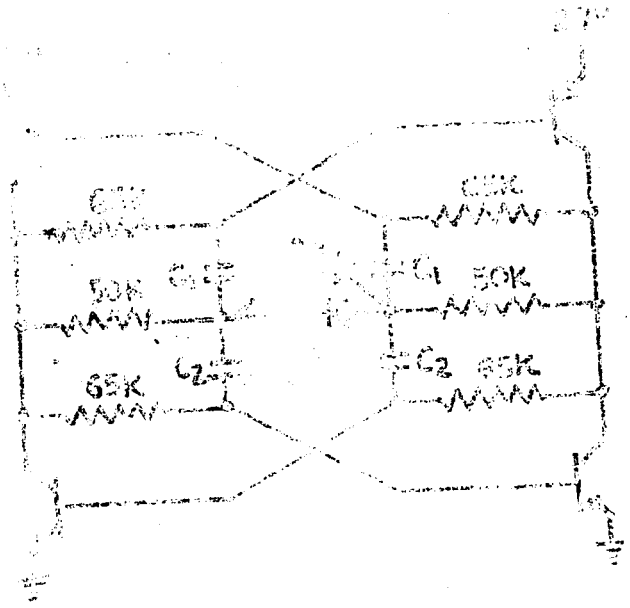


Fig. 36

The base current of the flip-flop shown above is approximately 1 1/3 times that of the gates and will result in slightly higher fan-out for the flip-flop. The input current required to trigger or set the flip-flop is lower than the equivalent input current of either gate, thus rating the flip-flop input characteristics conservatively as one equivalent load. Power drain is approximately 200 μ w.

The effect of capacitor values on frequency response was determined by varying both the magnitude and ratio of the PNP and NPN steering capacitors. The information obtained is plotted in Figure 37. Frequency response is normalized to the maximum frequency obtained over the temperature with $C_1 = C_2 = 50$ pf.

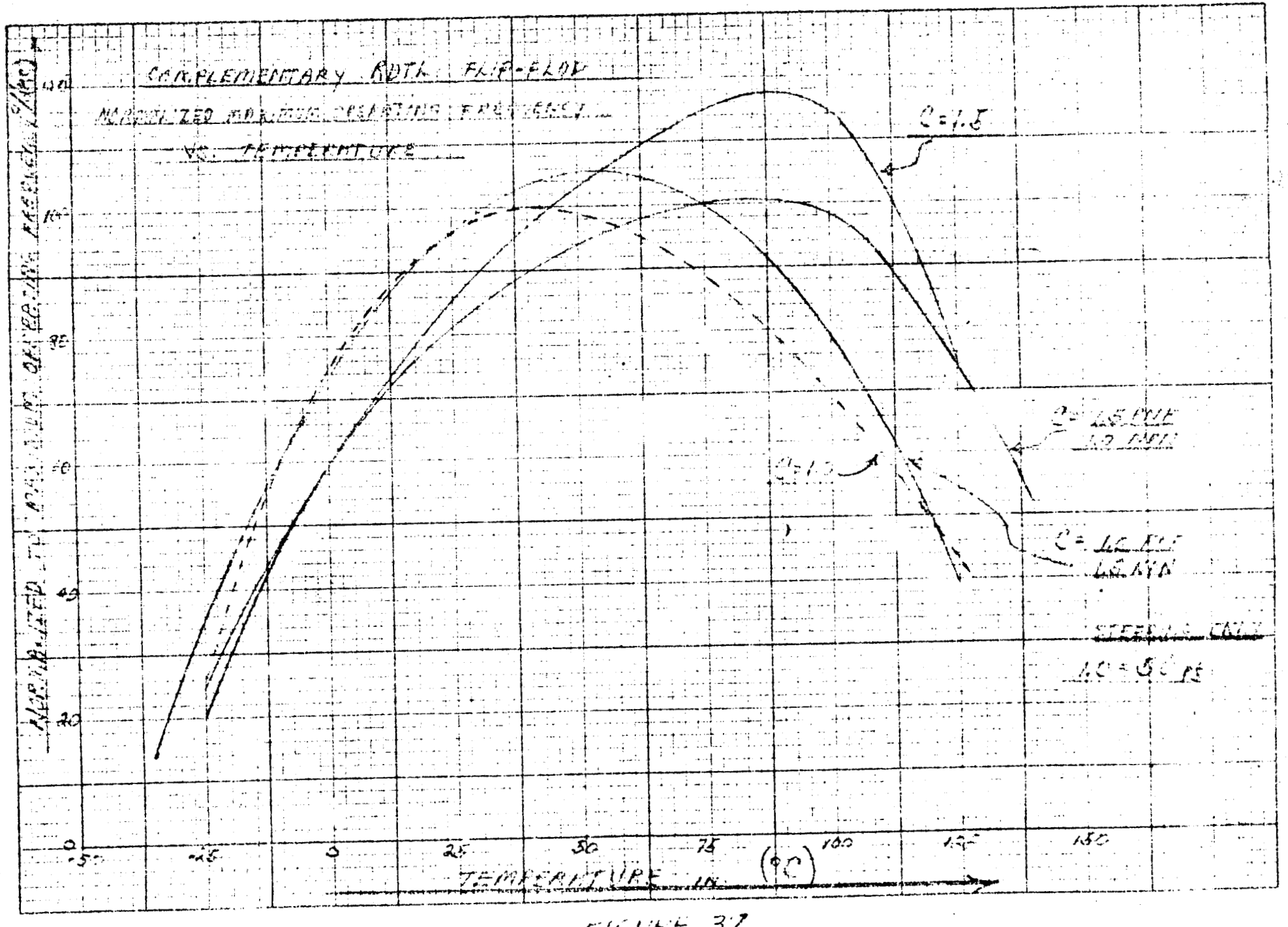
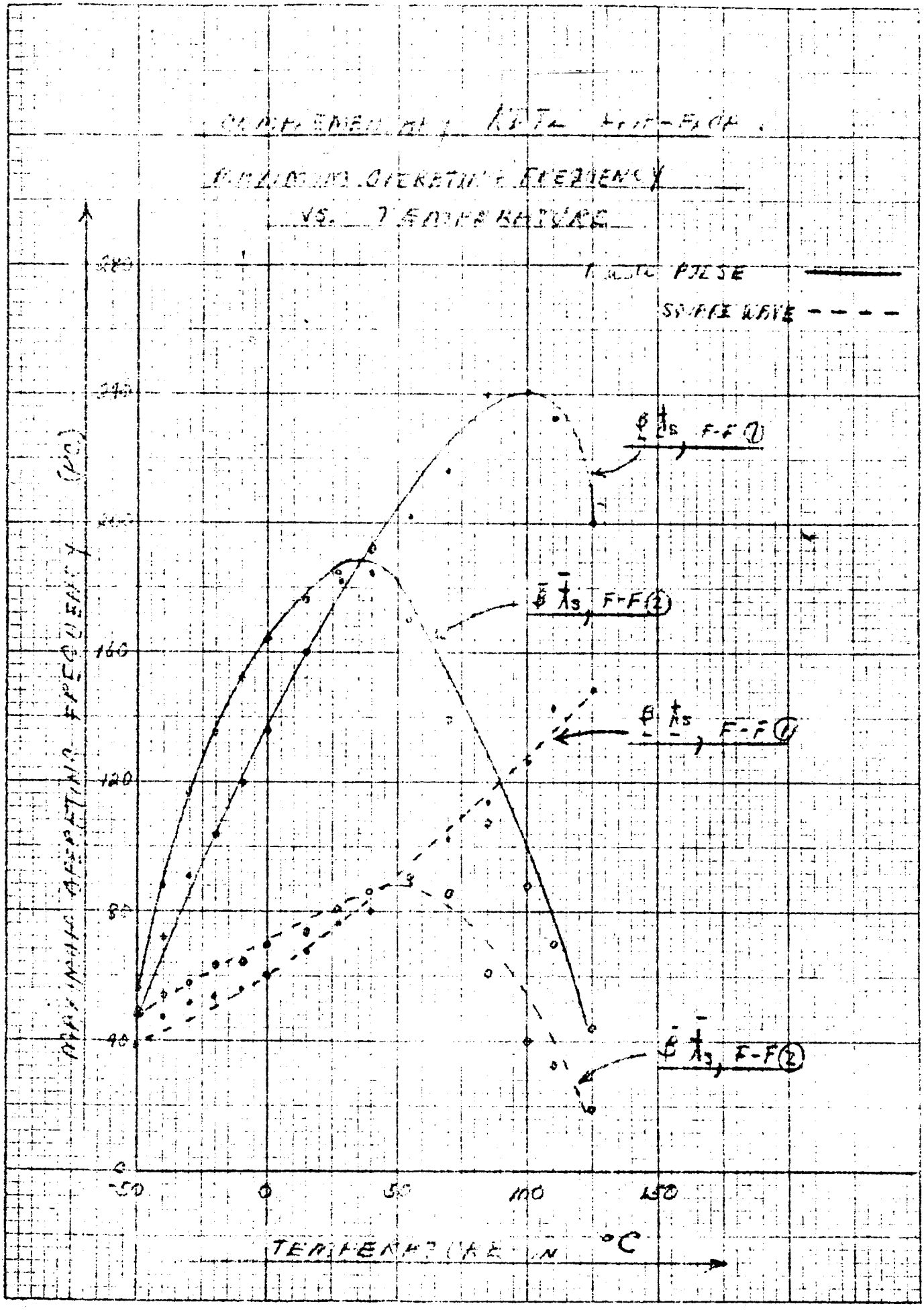

COMPLEMENTARY RDTL FLIP-FLOP
NORMALIZED MAXIMUM OPERATING FREQUENCY
VS. TEMPERATURE
C = 1.5
C = 1.0
C = 1.5 PNP / 1.0 NPN
C = 1.0 PNP / 1.5 NPN
STEERING ONLY
1.0 = 50 PS
NORMALIZED TO MAXIMUM OPERATING FREQUENCY (%)
TEMPERATURE IN (°C)
0
20
40
60
80
100
-50
-25
0
25
50
75
100
125
150

FIGURE 37

Optimum performance was obtained with the use of high speed diodes in the steering network.

The optimum performance in terms of the temperature ranges outlined in section I, was obtained with $C_1 = 50pf$ and $C_2 = 75pf$.

Flip flop performance variations with transistor characteristics were determined by evaluating performance using the same limit sample transistor used in the NAND and NOR gate evaluation. Performance characteristics were determined with both a square wave and 1μ sec pulse width input to the flip-flop. The resultant frequency response performance variations may be explained by considering the duty cycle of the input waveform and its effect on the recovery time required by the flip-flop after removal of the input pulse. The limit sample transistors also contribute to performance variations as shown in Figure 38.



VS. TEMPERATURE
PULSE
SQUARE WAVE
F-F ①
F-F ②
F-F ①
F-F ②
160
120
80
40
0
-50
0
50
100
150
°C

Power Driver

A power driver may be used to obtain fan-in or higher than those normally associated with complementary gates. This is usually accomplished by maintaining the same circuit configuration as the gates but changing the current levels. If lower resistor values are used the input current will be increased but larger values of base current will also be available. This will result in increased collector current capabilities with respect to the conventional gate, thus resulting in higher fan-outs for the power driver.

If the power driver is designed with the same criteria as the gates except at a higher current level, it is anticipated that performance characteristics will be quite similar to that of the gates. It is more probable from a logic design viewpoint that high fan-outs will be desired from either the NPN or PNP transistor but not both. This will result in non-complementary operation and complicates design and evaluation. As indicated earlier, non-complementary design will not be discussed in this report because of time limitations and the wide range of possible solutions.

3.2 DTL

The preliminary investigation of the DTL configuration indicated that the configuration that minimizes [illegible] profitable trade-offs between transistor base requirements, noise [illegible], propagation time and power drain is shown in Figure 39.

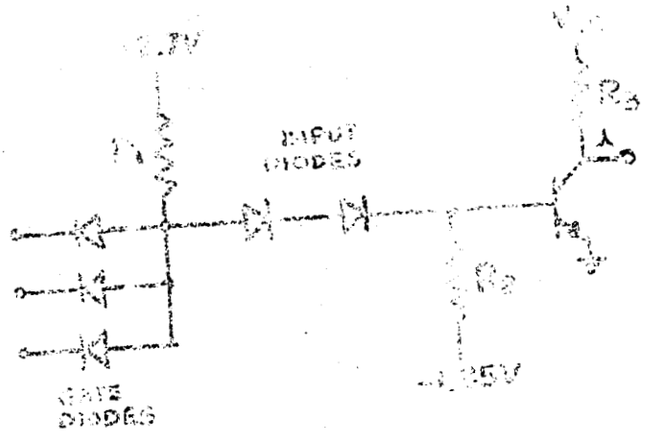


Figure 39

Investigations of the configuration in section 2 were made with collector supply voltages of 1.35 volts. Preliminary evaluation of DTL flip-flops indicated that a larger voltage swing is required at the trigger input of the flip-flop if operation with relatively small values of input capacitors is required.

It is, of course, desirable to use capacitors with low values in integrated circuits because capacity is directly proportional to substrate area. If low values of collector voltage are used, the gate diodes do not have

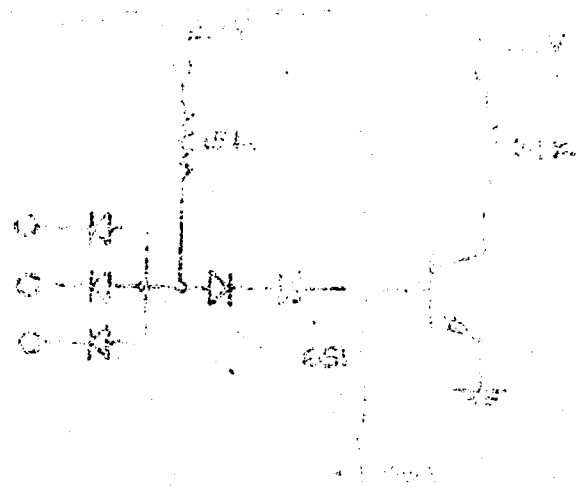
a large [illegible] and [illegible] to [illegible] noise spikes [illegible] ctor [illegible] increase gate power drain if [illegible] resistance is kept constant, and decrease switching speed if resistor current is kept constant. The limitation of 1.35 or 2.7 volt power supplies are such that a good compromise between these conditions becomes difficult, i.e. (1.35V too low and 2.7V is too high) particularly if the circuit shown in Figure 39 is used where [illegible] diodes and a transistor base-emitter voltage determine the gate node voltage when the gate transistor is conducting. Fan-outs of four and transistor forced betas of 25 were used with the 2.7 volt design. This requires the transistor beta to be higher than this value at the operating temperature in question.

The design results are shown in Table 40. Propagation times were determined in a 5 stage ring oscillator as described in section I.

V_{cc}	R_1	R_2		Avg. Power per gate	Avg. prop. time per gate
2.7V	24K	100K	[illegible]	335	.52
2.7V	18K	82K	[illegible]	384	.48
2.7V	15K	65K	[illegible]	520	.42
2.7V	12K	51K	[illegible]	608	.36
1.35V	24K	100K	[illegible]	234	.62
1.35V	18K	82K	[illegible]	300	.55
1.35V	15K	62K	2[illegible]	355	.50
1.35	12K	51K	22	405	.43

Table 40

As in Complementary RDTL, one of the above designs will be investigated in detail to determine extremes of performance variations. The circuit selected is shown in Figure [illegible].



Figure

Two stage propagation time variations were investigated as a function of fan-in and fan-out loading as shown in Figure 42.

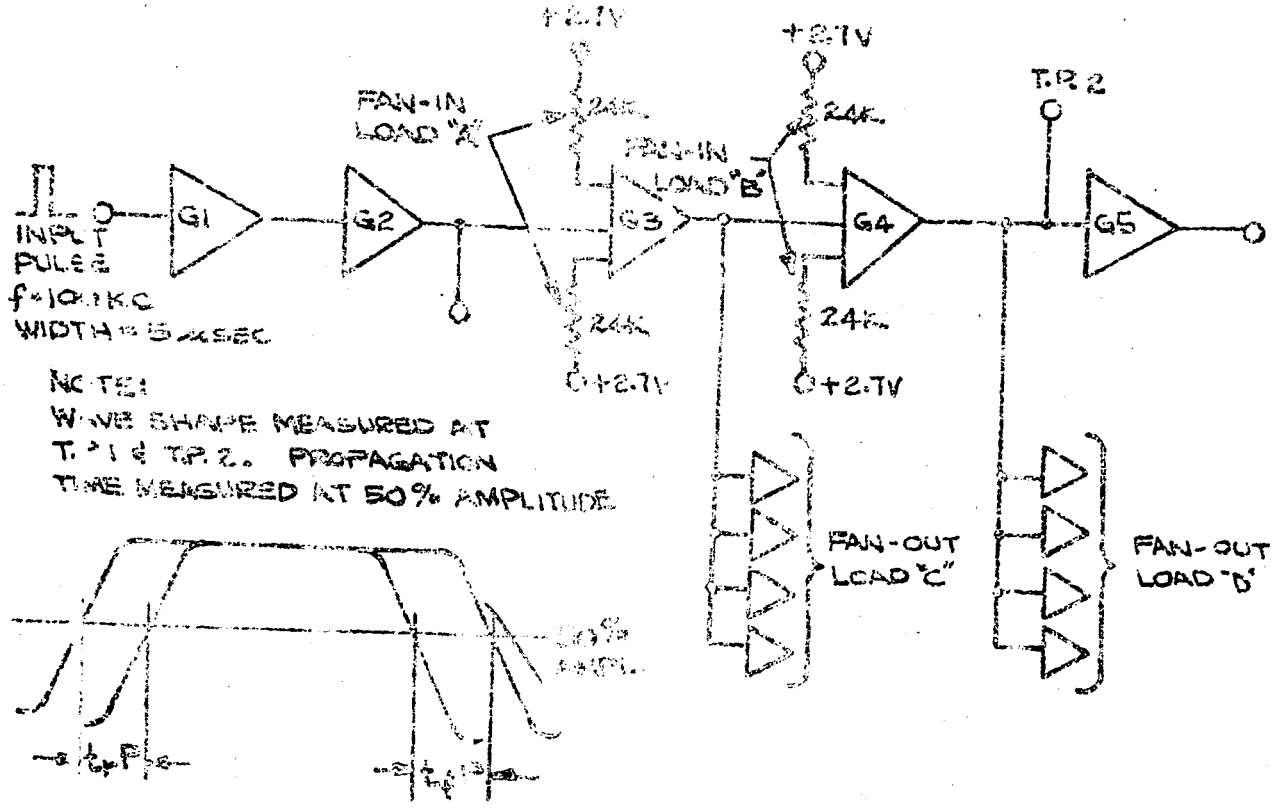


Figure 42

[illegible] to [illegible] of up to five equivalent loads were used. All possible combinations of fan-in and fan-out conditions for the two stages under investigation were evaluated. Propagation times were measured at the 50% amplitude pair [illegible] the input and output waveforms of the circuit pair. Worst case propagation times were determined by selecting limit sample transistors and evaluating performance characteristics for minimum and maximum loading conditions. The limit case transistors used were:

1. $\overline{\beta}$ $\overline{t_s}$
2. $\underline{\beta}$ $\overline{t_s}$
3. $\underline{\beta}$ $\overline{t_s}$
4. $\underline{\beta}$ $\underline{t_s}$

Collector supply voltages of 2.7 as required by flip-flop design consideration were used throughout the remainder of the gate and flip-flop performance investigation.

The effect of diode characteristics on gate performance has been briefly discussed in previous sections of the report. This characteristic was further evaluated by using a wide range of diodes in the worst case propagation time circuit pair outlined above.

A summary of diode characteristics and techniques used to measure reverse recovery characteristics is shown in Table 43.

Diode Type	Reverse Recovery to OV @ I_f=5ma	
H. S. Planar diode	.03 μ sec	I_R = .5ma
Planar Multi-diode	.06	
H. S. Alloy diode	.10	V_R = 2V
Planar Multi-diode	.30	
Planar Multi-diode	.70	

Table 43

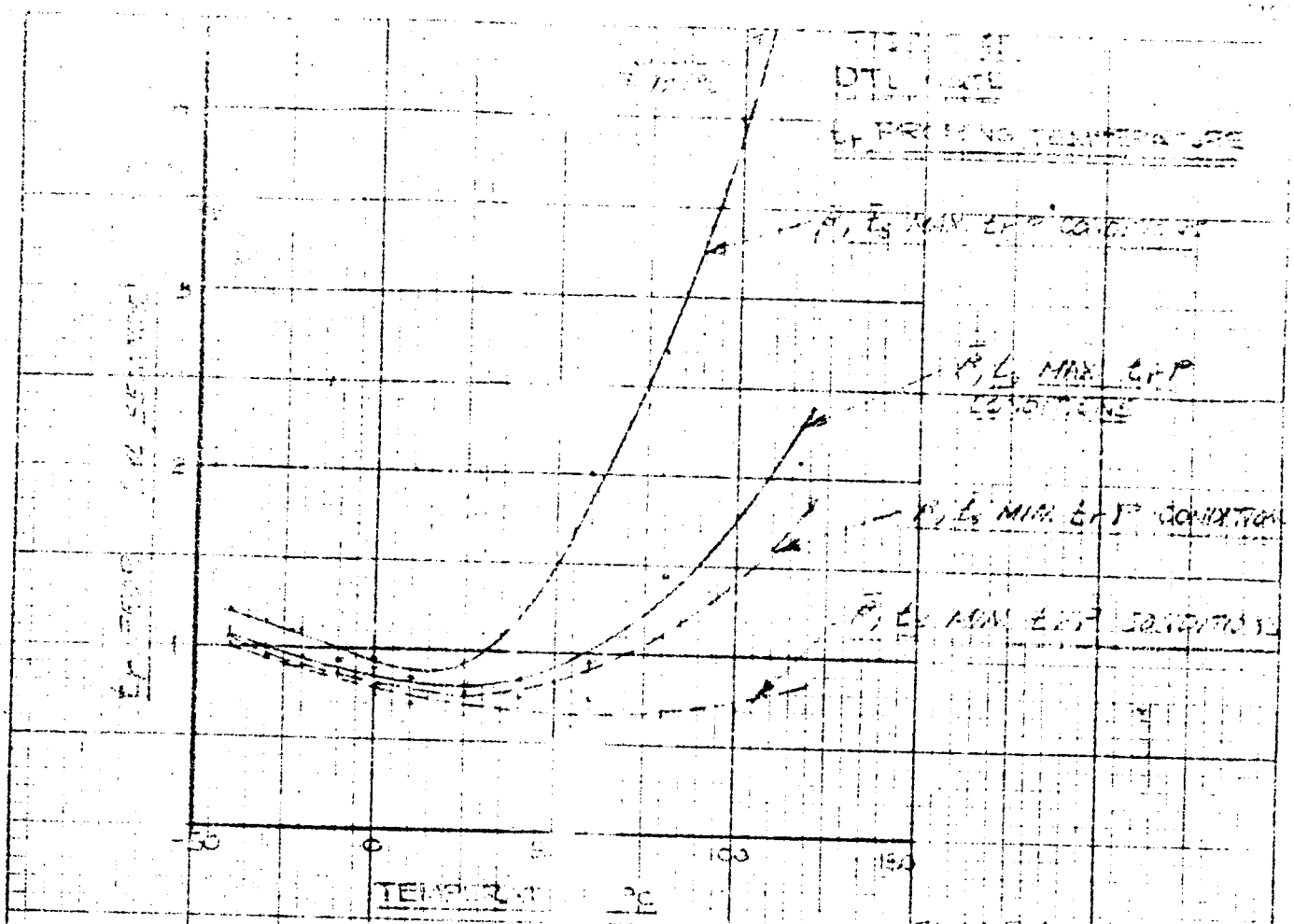
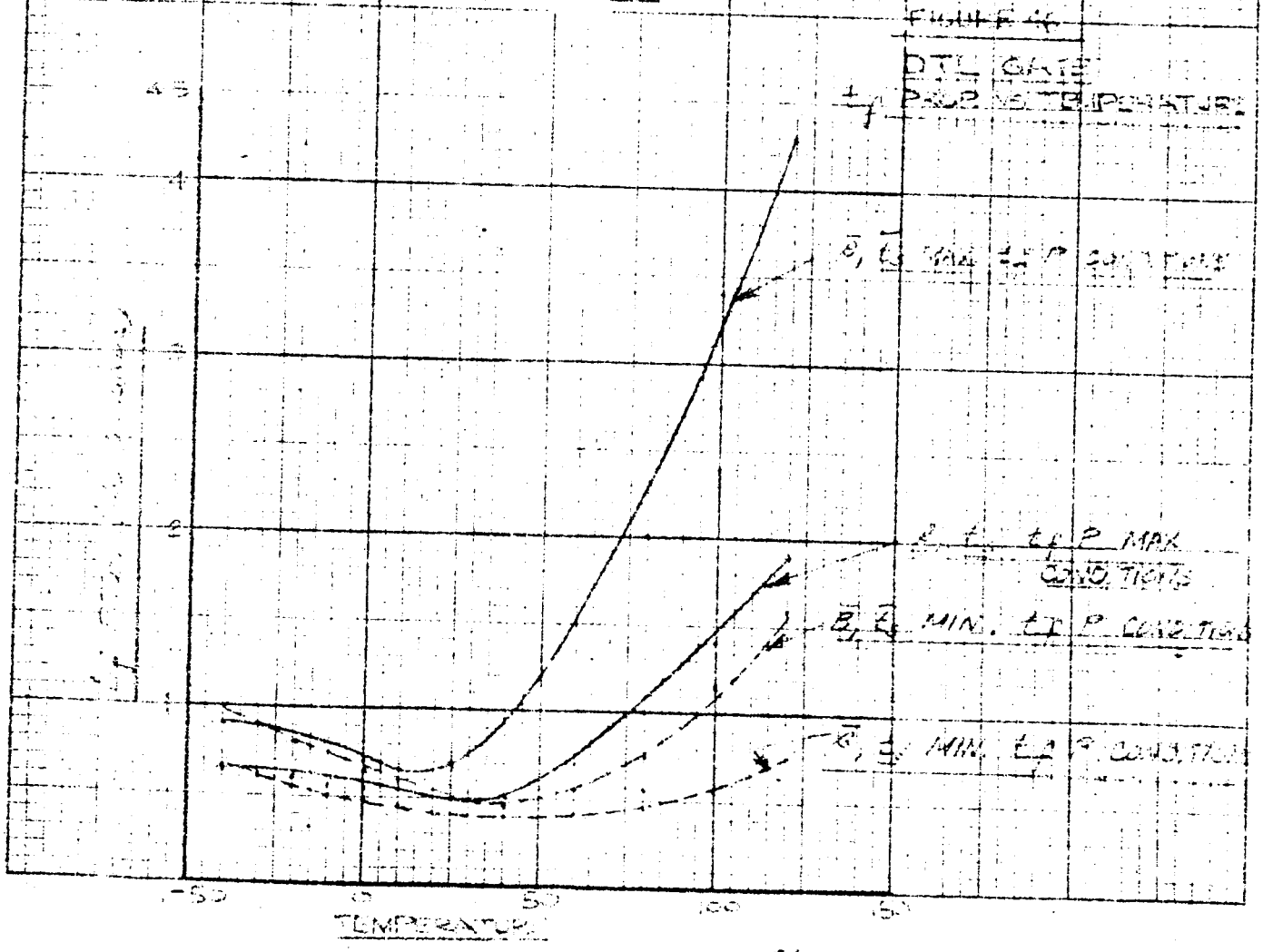

DTL GATE
t_r PROPING TEMPERATURE
$\bar{\beta}, \bar{t}_s$ MAX t_r P CONDITIONS
$\bar{\beta}, \bar{t}_s$ MAX t_r P CONDITIONS
$\bar{\beta}, \bar{t}_s$ MIN t_r P CONDITIONS
$\bar{\beta}, \bar{t}_s$ MIN t_r P CONDITIONS
-50
0
50
100
150
TEMPERATURE °C

FIGURE 46


DTL GATE
t_f PROP VS TEMPERATURE
$\bar{\beta}, \bar{t}_s$ MAX t_f P CONDITIONS
$\bar{\beta}, \bar{t}_s$ t_f P MAX CONDITIONS
$\bar{\beta}, \bar{t}_s$ MIN. t_f P CONDITIONS
$\bar{\beta}, \bar{t}_s$ MIN. t_f P CONDITIONS
4.5
4
3
2
1
-50
0
50
100
150
TEMPERATURE

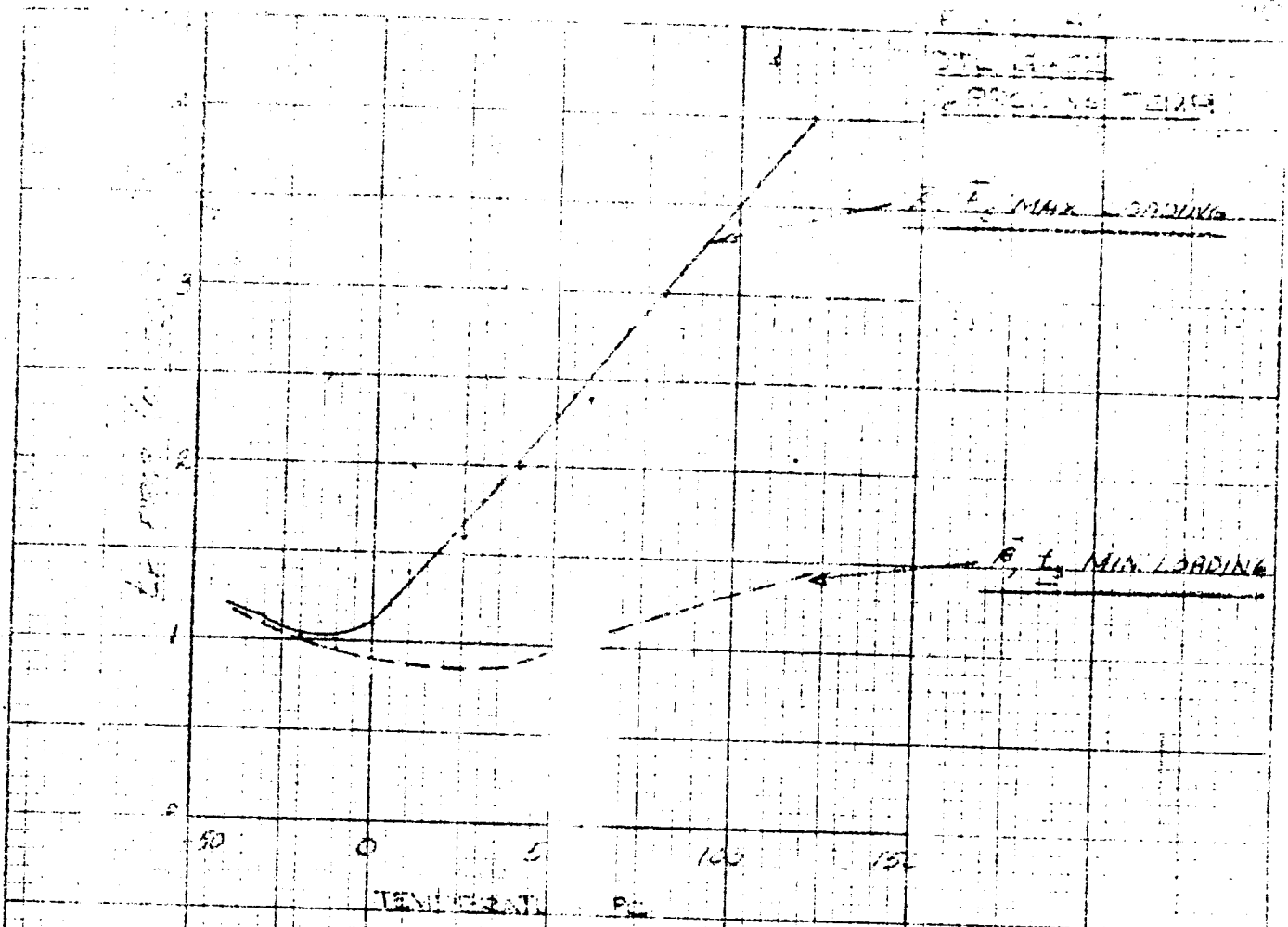
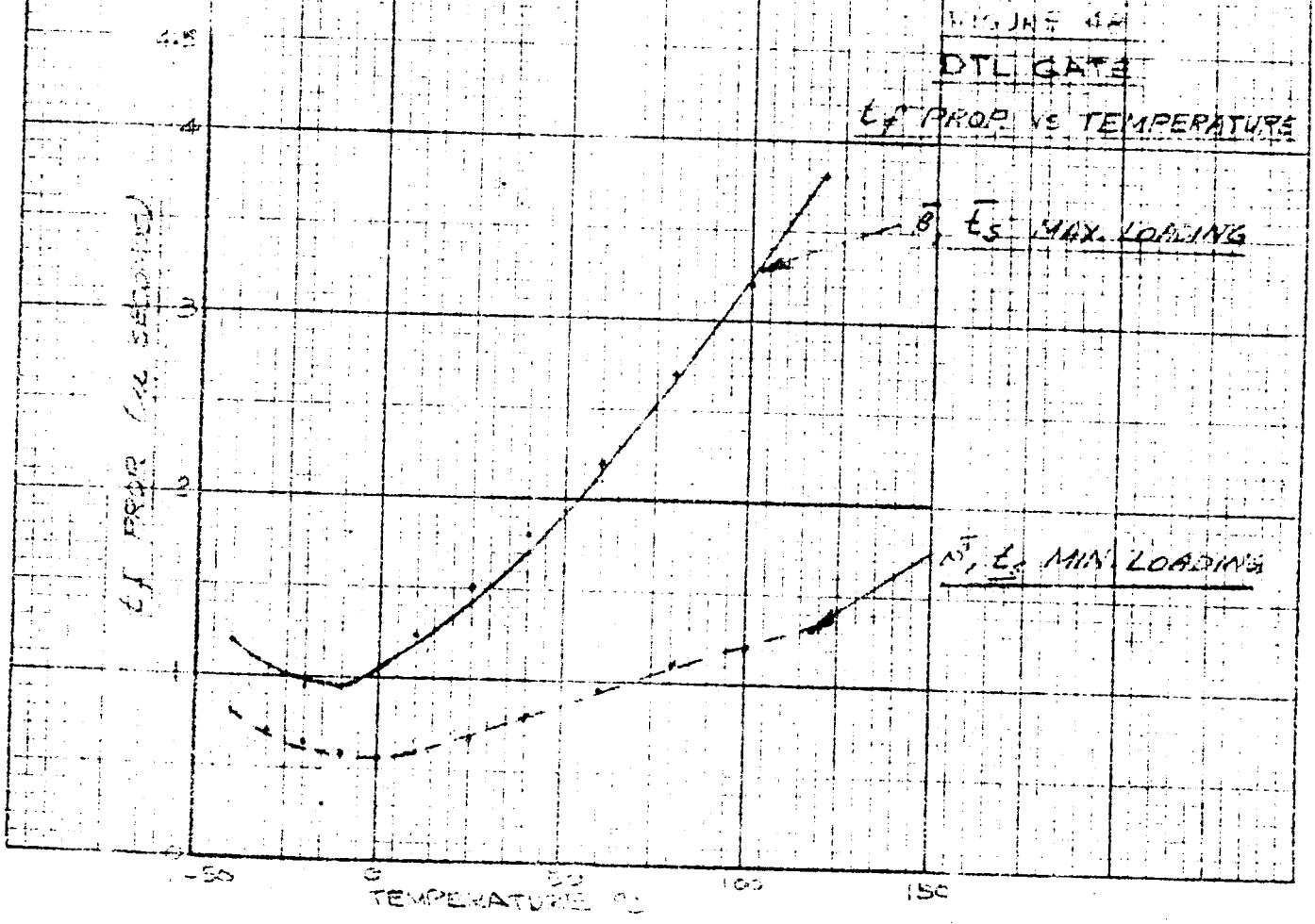


FIGURE 4A

DTL GATE

t_f PROP. VS TEMPERATURE



Collector Resistor (kΩ)	[illegible]	[illegible]	[illegible] — Max Load		[illegible] — Min Load	
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	.28
[illegible]	[illegible]	[illegible]	[illegible]	.53	[illegible]	.42
[illegible]	[illegible]	[illegible]	.88	.56	[illegible]	.48
[illegible]	[illegible]	[illegible]	[illegible]	.60	[illegible]	.52
[illegible]	[illegible]	[illegible]	[illegible]	.64	[illegible]	.56

Table 49

Minimum propagation time is a function of the value of the collector resistor, but the maximum propagation time is relatively independent of the collector resistance value because of the low effective collector resistance. Power drain, however, is directly proportional to collector resistance value and the supply voltage. The collector resistor will also have a direct relationship on flip-flop performance. When the relative independence of maximum gate propagation time, as indicated by the above data, is considered, it becomes obvious that the collector resistor value should be determined by the relationship of flip-flop repetition rate to gate power drain and beta requirements.

Flip Flop

As indicated in the evaluation of DTL gates various configurations may also be considered for use as a DTL flip-flop. Two configurations are shown in Figures 50 and 51. These flip-flops are essentially two cross coupled DTL gates with associated steering network.

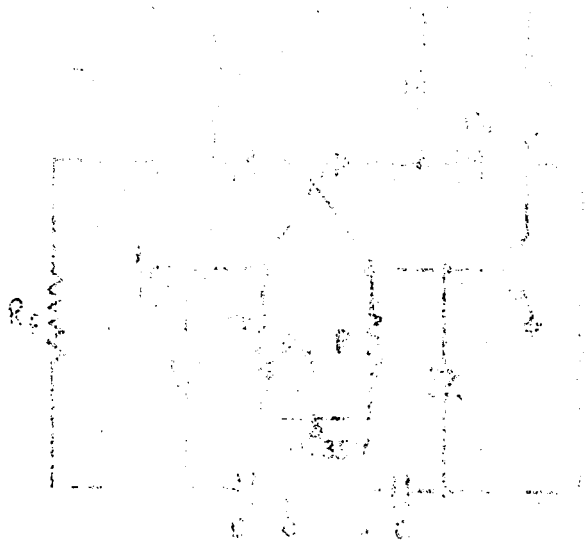


Figure 50

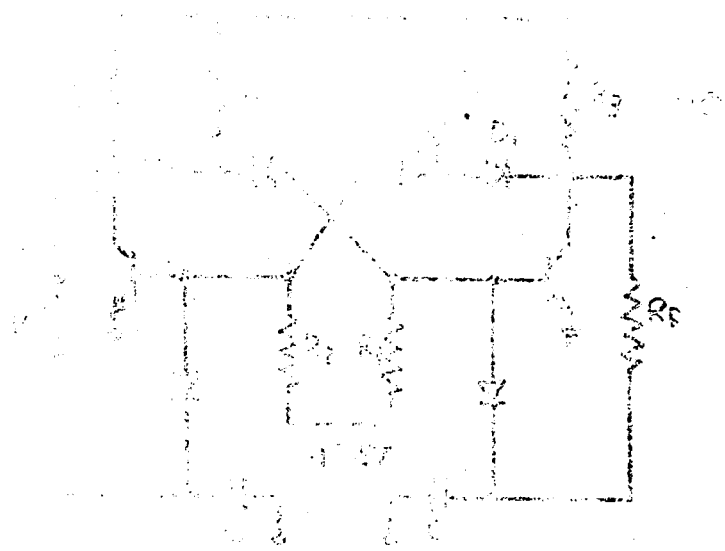


Figure 51

Simpler configurations [illegible] eliminating I_1 and I_1 were evaluated but [illegible] of the performance [illegible] shown by the illustrated configurations. The performance characteristics of both flip-flop types were investigated at various current levels. Collector supply voltage levels of [illegible] were used throughout the flip-flop evaluation to obtain the required frequency response characteristics over a wide temperature range. Frequency response characteristics were determined for the complementing function (input capacitors connected) with square wave input waveform. The input waveform was buffered from the flip-flop by inserting two DTL gates between the generator and the flip-flop.

The same limit sample transistors used in the gate investigation were used. Four designs of the flip-flop shown in Figure 50 compatible with the gate designs shown in Table 40 were evaluated. The results are given in Table [illegible].

[illegible]

[illegible] design shown in Table 52 was [illegible] the collector resistance of the driving [illegible] are shown in Tables [illegible] and [illegible]

[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	Max. Freq
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]KC
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	170
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	90

[illegible]

	R_1	R_2	R_3	C_c	Max. Freq
[illegible]	[illegible]K	6[illegible]	[illegible]K	[illegible]pf	115K
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	140
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	140
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

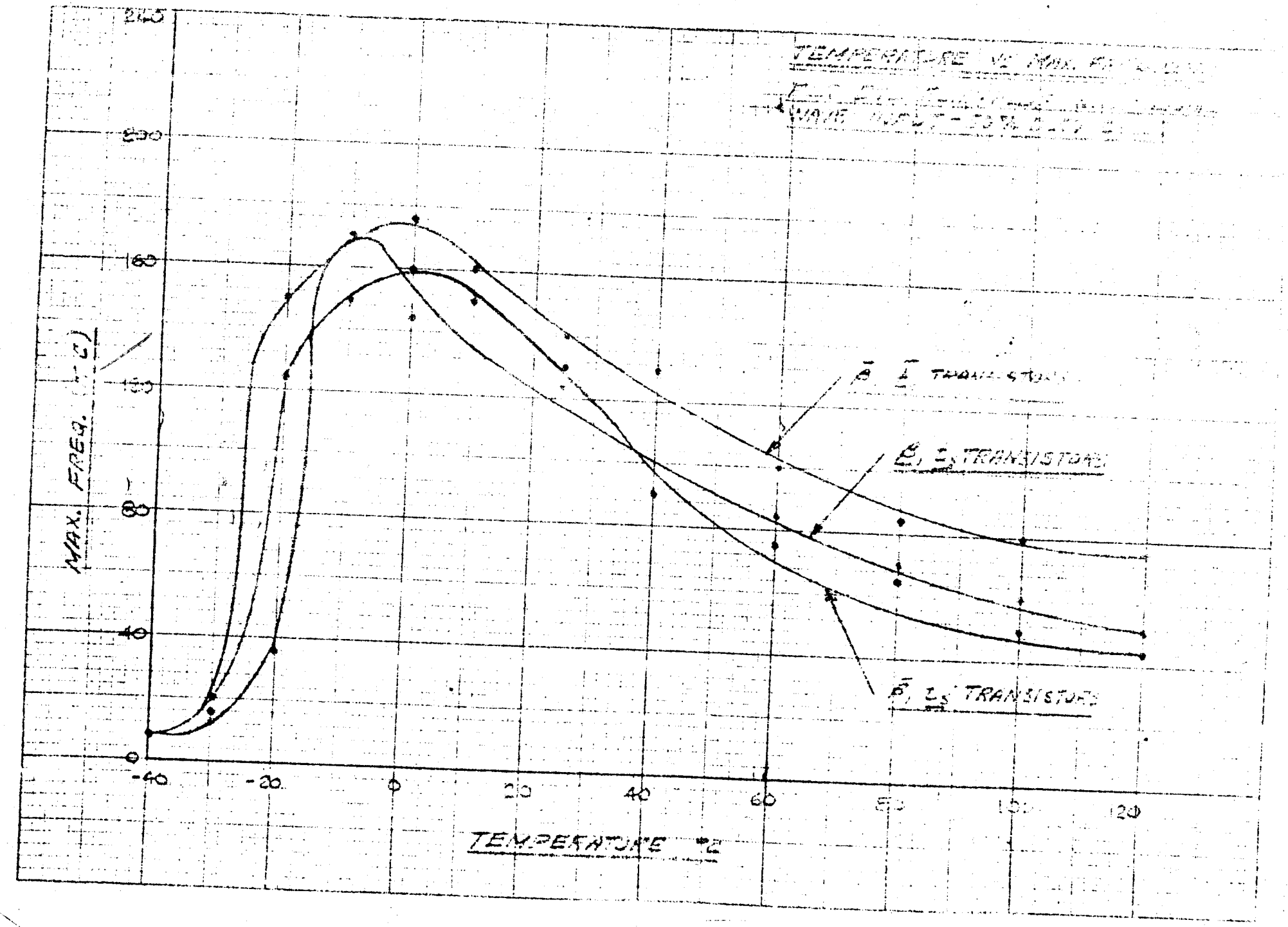
[illegible]

The [illegible] as a function of the steering resistor indicate that an optimum resistance value exist[illegible] improved performance was also obtained by using high speed planar [illegible] in the steering network and were used [illegible] the evaluation. Flip flop performance is also improved [illegible] the [illegible] of the gate collector resistance. The dependence [illegible] flip-flop characteristics on the RC time constants associated with the input waveform and the steering network is obvious. Increases in frequency response may be obtained by increases in circuit power drain through reduction of resistor values.

The designs outlined in Table 52 were not thoroughly optimized and thus show some minor variation from the expected power vs. frequency relationships. Performance of the flip-flop as a function of temperature and transistor variations is shown in Figure 55.

The steering network shown may be used to obtain the complementing function or as an A.C. set reset flip-flop by either connecting the input capacitors together or by using each capacitor as an A.C. input.

The flip-flop shown in Figure 51 was also evaluated and resulted in consistantly higher operating frequencies. The noise margin inherent to this configuration as discussed in previous sections tends to prohibit further consideration [illegible] less operating frequence is of paramount importance. [illegible] in operating frequency may be explained by considering the much lower turn-off voltage inherent to the single input diode configuration.



TEMPERATURE VS MAX. FREQ.
MAX. FREQ. (°C)
TEMPERATURE °C
240
200
160
120
80
40
0
-40
-20
0
20
40
60
80
100
120
β, I TRANSISTORS
β, I TRANSISTORS
β, I TRANSISTORS

FIGURE 55

[illegible] power driver to supplement the standard gate [illegible] by [illegible] the gate shown in Figure 41. The turn-on bar [illegible] doubled by [illegible] the gate resistor from 15KΩ to 10KΩ. The resultant [illegible] capabilities of this "power driver" thus doubled if the load [illegible] considered to be conventional gates. Performance characteristics were evaluated by inserting the driver into the worst case two stage propagation time test circuit with a fan-out of 10 and evaluating minimum and maximum performance. The resultant rising and falling propagation time measurements shown in Figures 56 and 57 may be compared with gate performance characteristic shown in Figures 45 and 46.

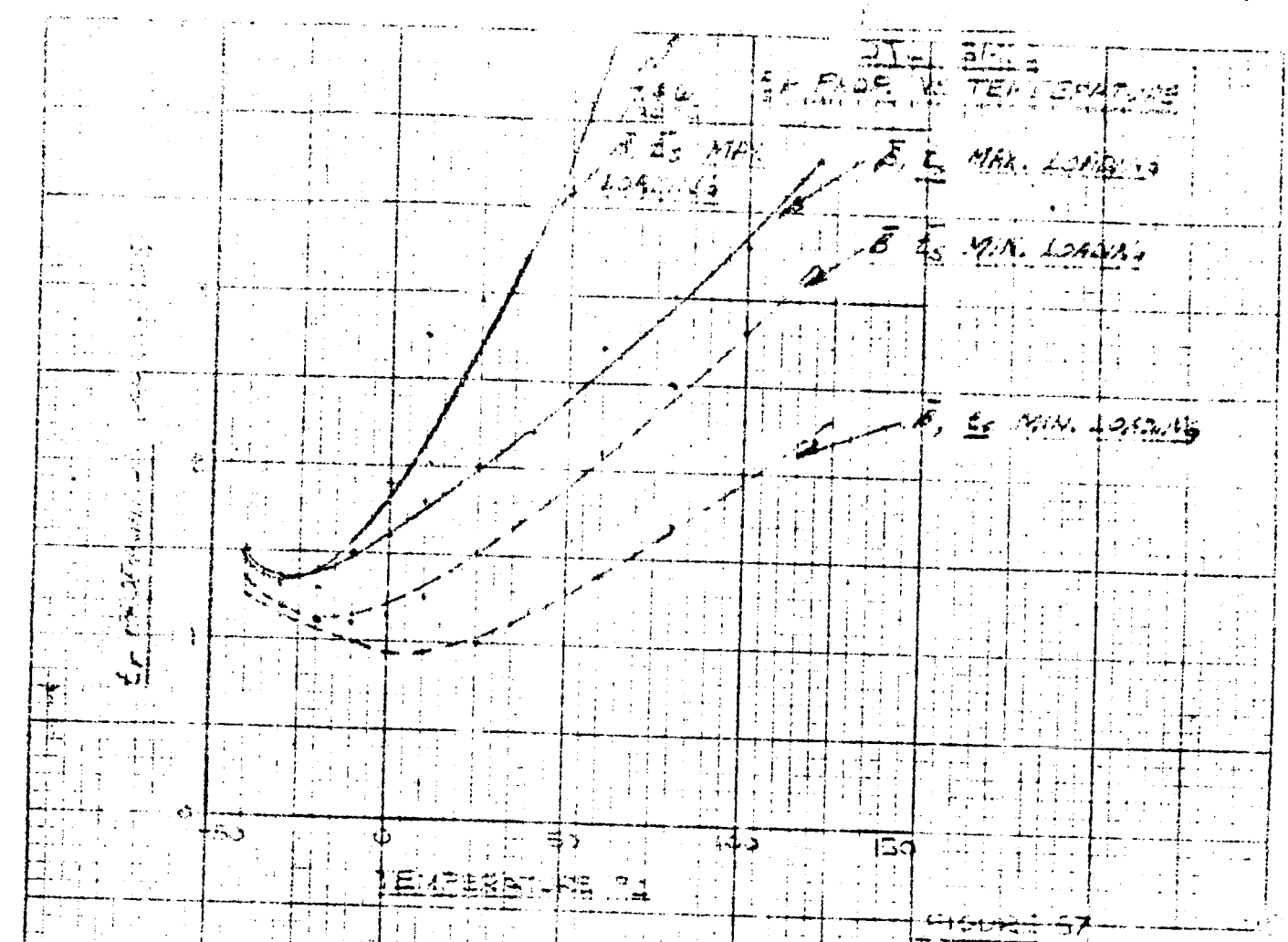
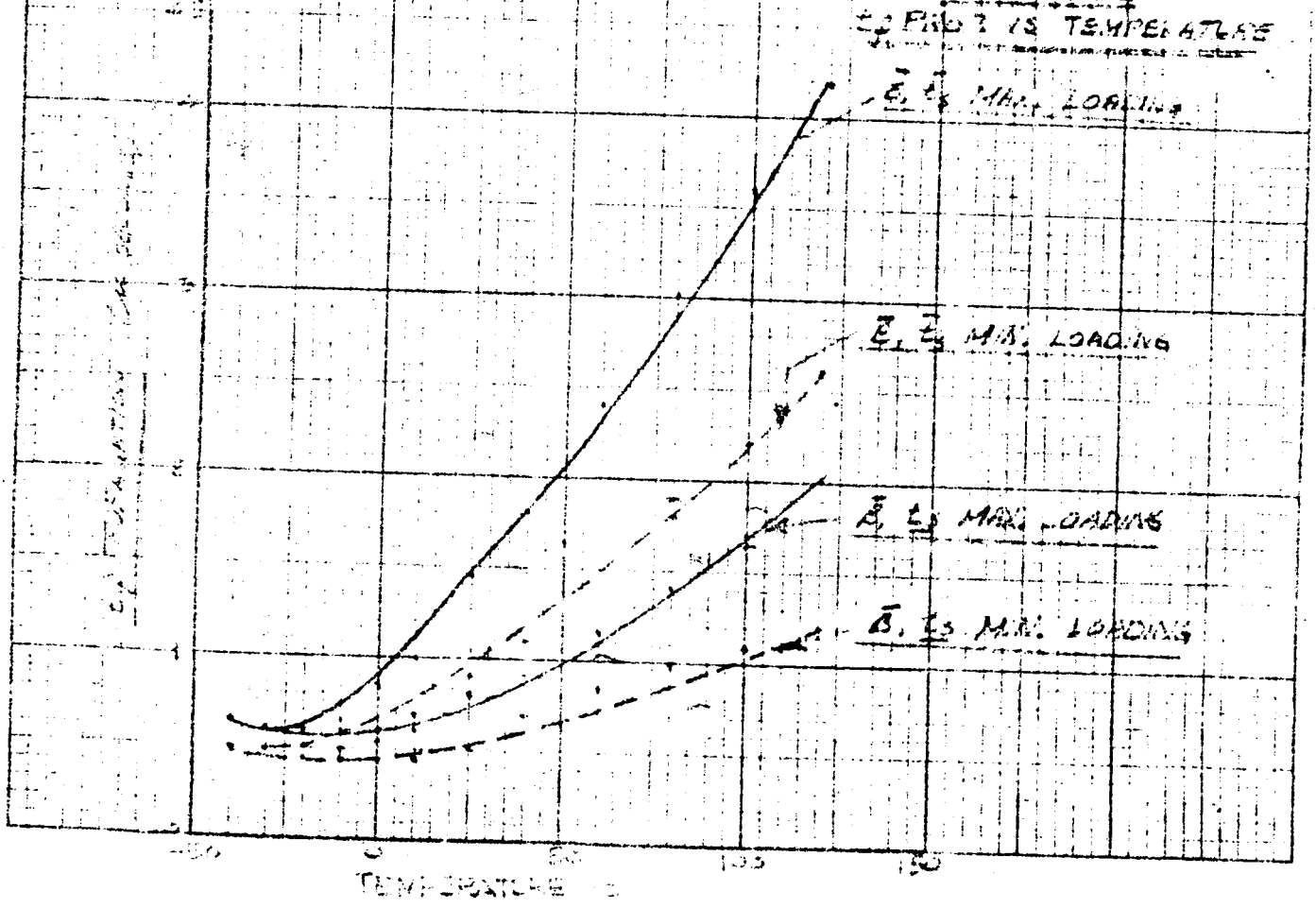

DTL GATE
t_f PROP. VS TEMPERATURE
$\bar{\beta}$, $\bar{t}_s$ MAX. LOADING
$\bar{\beta}$, $\bar{t}_s$ MIN. LOADING
$\bar{\beta}$, t_s MIN. LOADING
t_f PROPAGATION
TEMPERATURE °C
-50
0
50
100
150

FIGURE 57


DTL GATE
t_f PROP. VS TEMPERATURE
$\bar{\beta}$, $\bar{t}_s$ MAX. LOADING
$\bar{\beta}$, $\bar{t}_s$ MIN. LOADING
$\bar{\beta}$, t_s MAX. LOADING
$\bar{\beta}$, t_s MIN. LOADING
t_f PROPAGATION
TEMPERATURE °C
-50
0
50
100
150

[illegible]

The [illegible] propagation time performance [illegible] of the T[illegible] [illegible] in section II of this report. [illegible] figurations, [illegible] will be further evaluated by [illegible] investigation of [illegible] gate configuration shown in Figure 58.

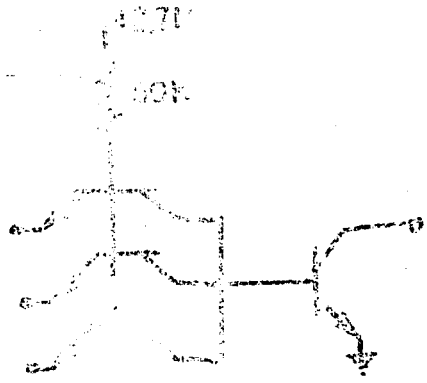


Figure 58

Turn-off voltage and base bleed-off current of the gate are both dependent upon the DC characteristics of the transistors used. Turn-off voltage is determined by the collector emitter saturation voltage of the output transistor and the offset voltage of the gate transistor. Base bleed-off current is determined by the inverse beta of the gate transistor. Both of these conditions were described in section II of this report.

Three groups of gate transistors were selected with the following ranges of inverse beta.

	β_I	β_f
high β_I	.5 - .7	75 - 100
med β_I	.2 - .3	20 - 40
low β_I	.1 - .15	10 - 20

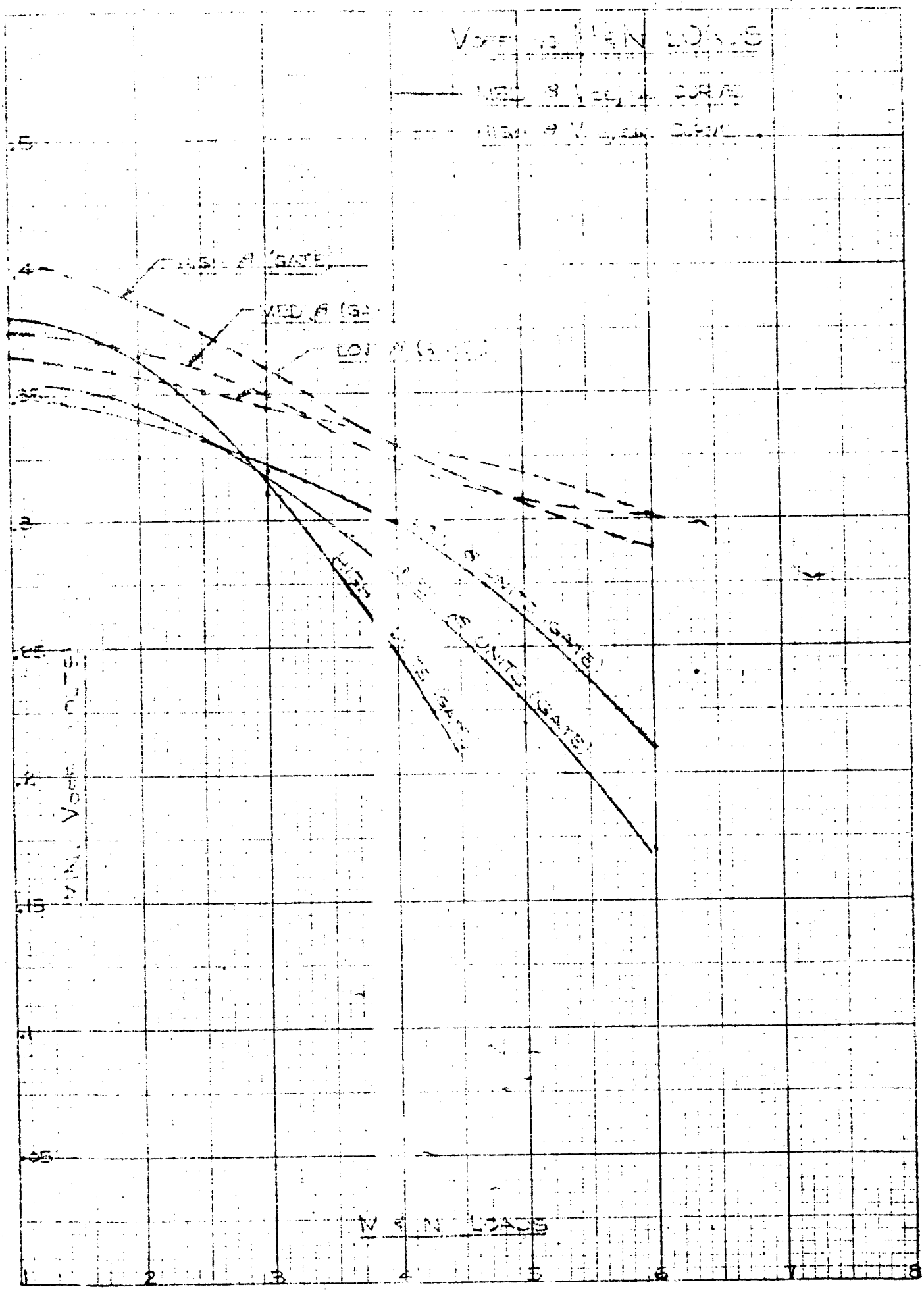
The results obtained are shown in Figure 59. Gate turn-off conditions were determined as a function of loading and component variations utilizing the gate transistors described above and limit samples of two beta ranges of output transistors. The output transistors selected were medium (30-75) and high (75-150) beta units with maximum values of forward offset voltage and saturation resistance for each of the beta ranges.

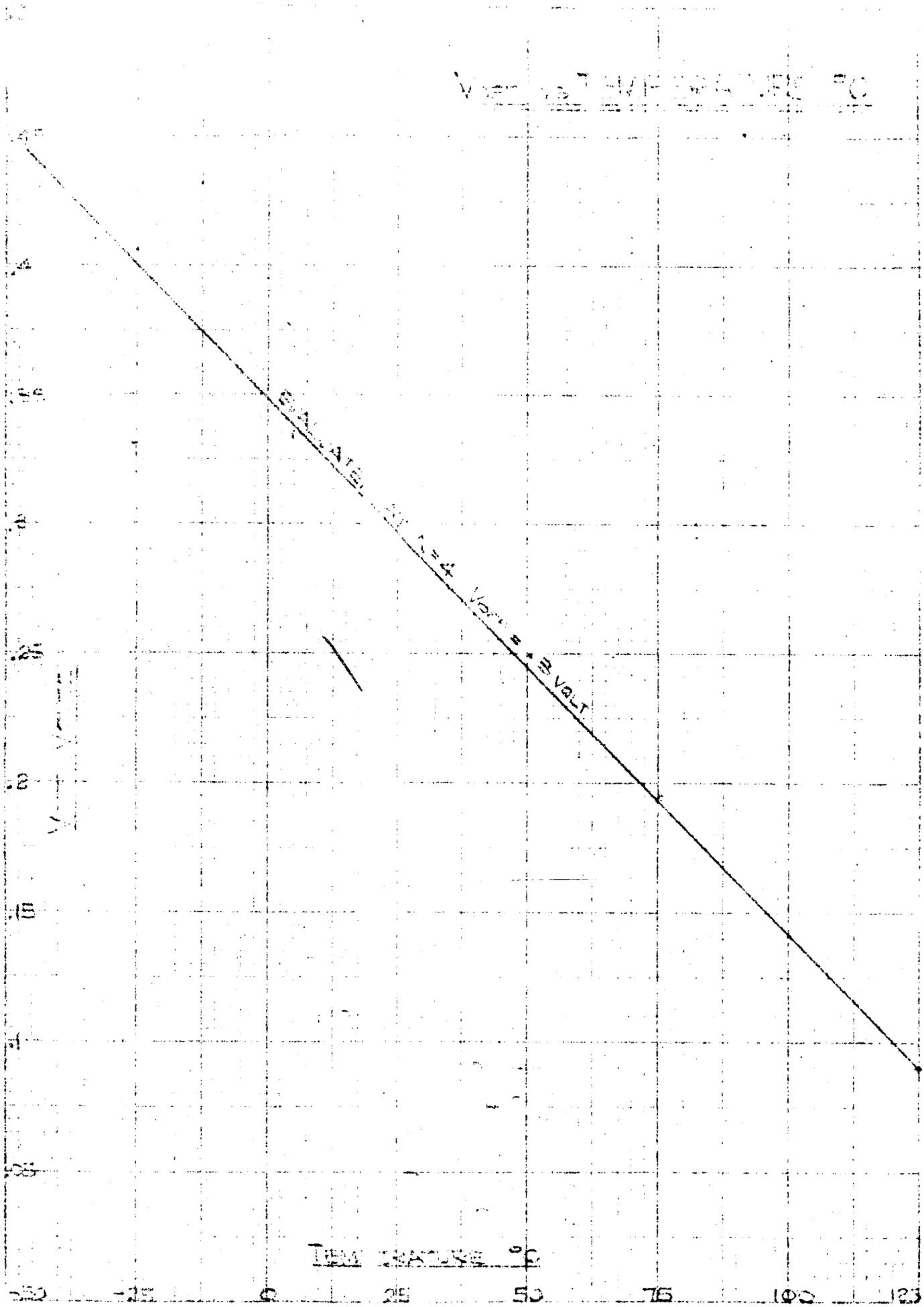
A typical variation of turn-off voltage with temperature is shown in Figure 60.

The reduction in base current through the current bleed-off effect described in section II was evaluated by breadboard techniques. Limit samples were selected for all output transistor base-emitter voltages. The three groups of gate transistors previously described were also used. Actual base current to the gate under investigation was measured as a function of loading conditions to determine the magnitude of current diverted to gate transistors in parallel with the gate under test. The diagram of the test set used is shown in Figure 61.

The results obtained are shown in Figures 62, 63, and 64. Each of these figures indicates base current variations as a function of gate fan-in and fan-out loading for each of inverse beta ranges investigated. The data is normalized to percent of maximum base current to permit a more universal application of the curves.

This information was used to determine output transistor beta requirements for each of the ranges of gate transistor inverse beta investigated.


.5
.4
.3
.2
.1
1
2
3
4
5
6
7
8



TEMPERATURE °C
-50
-25
0
25
50
75
100
125
.25
.2
.15
.1
.05

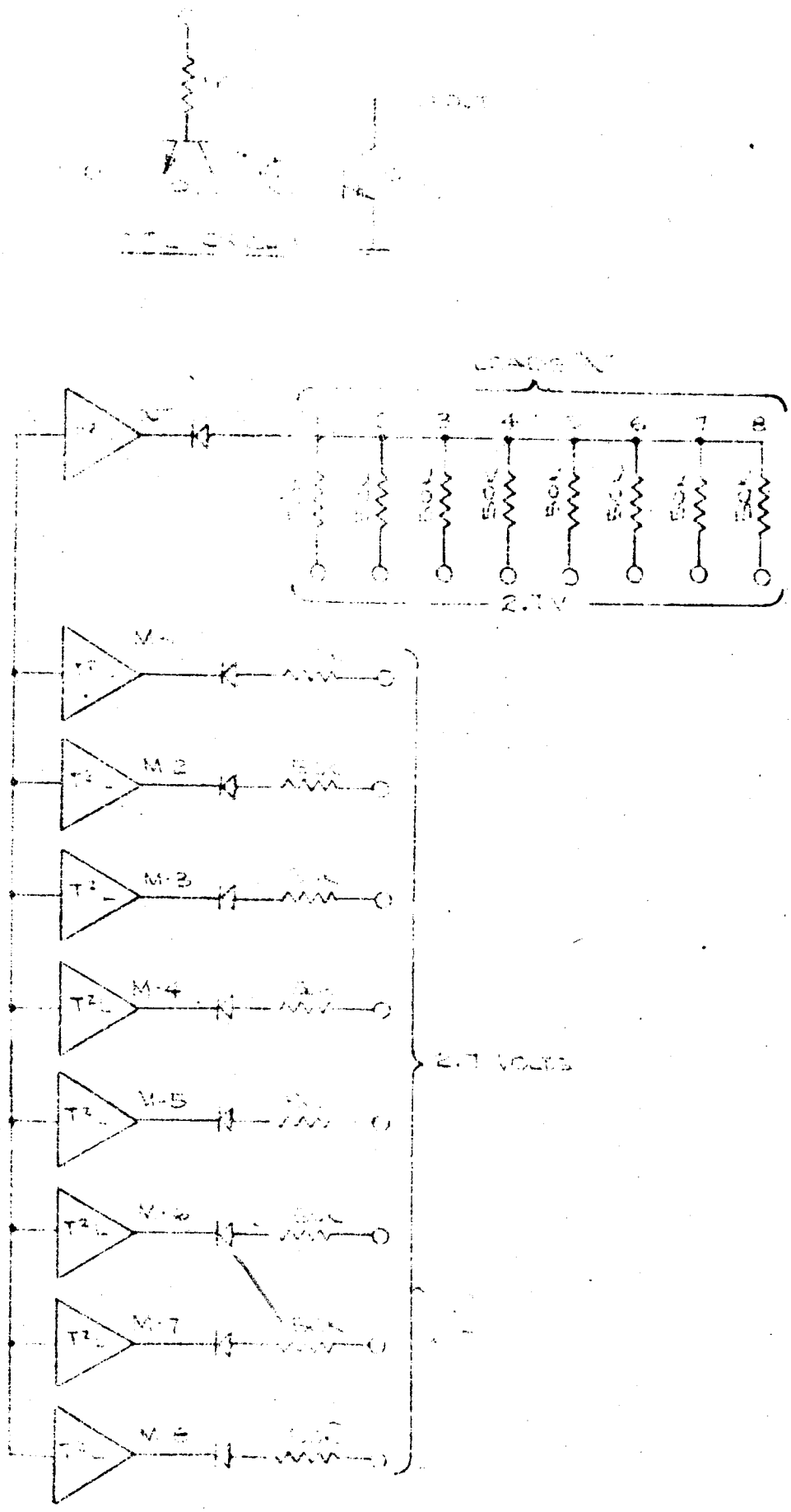
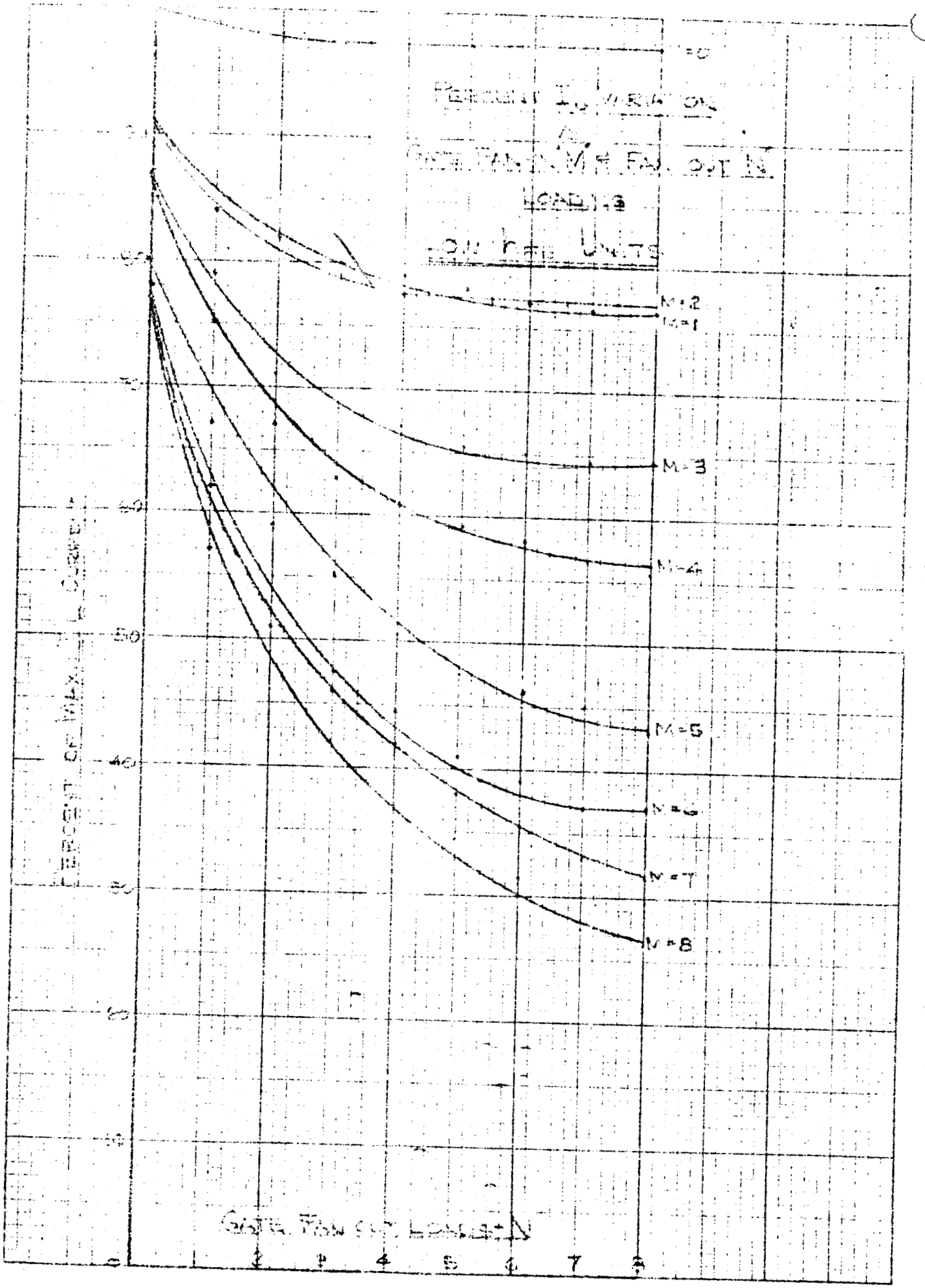
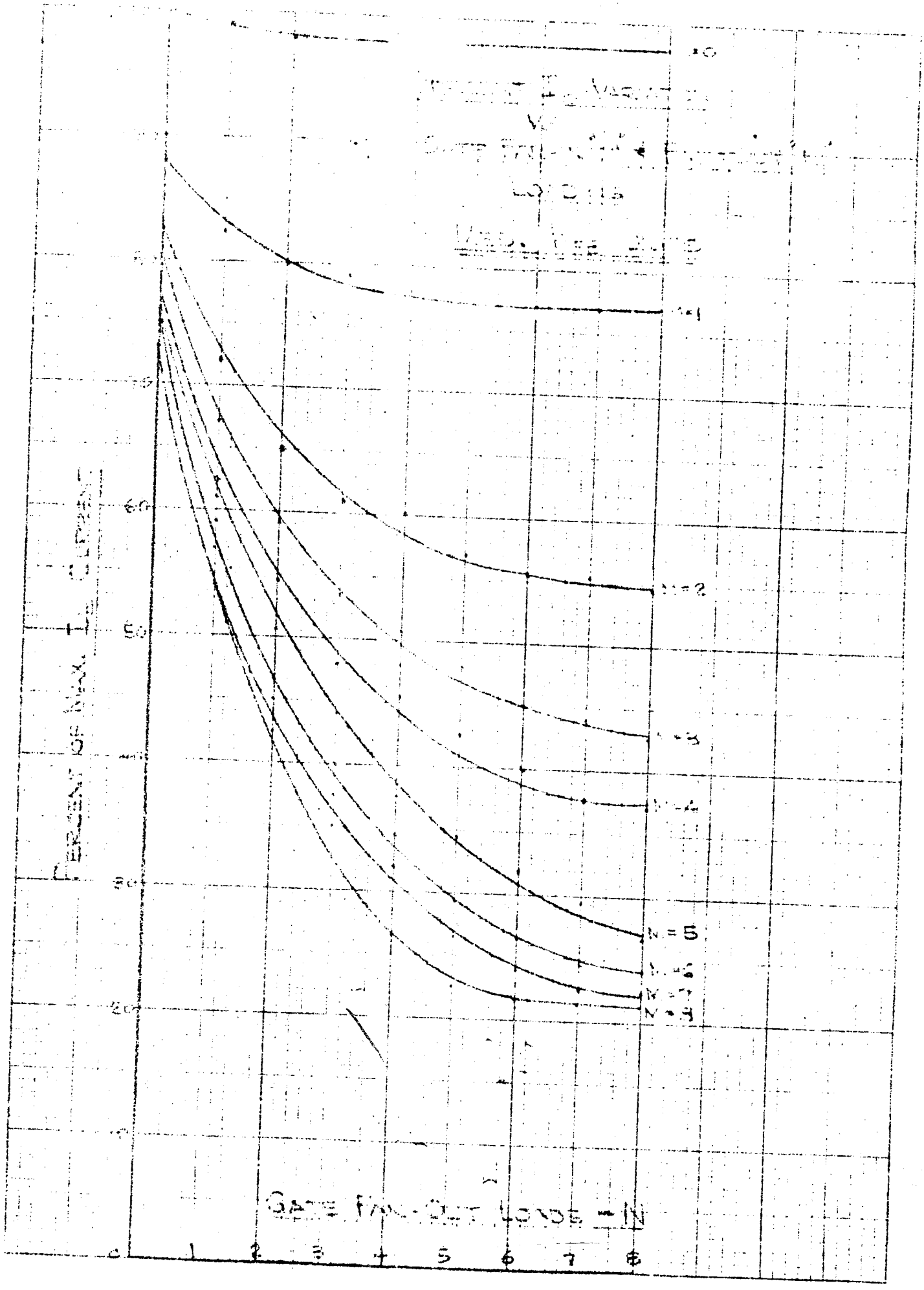


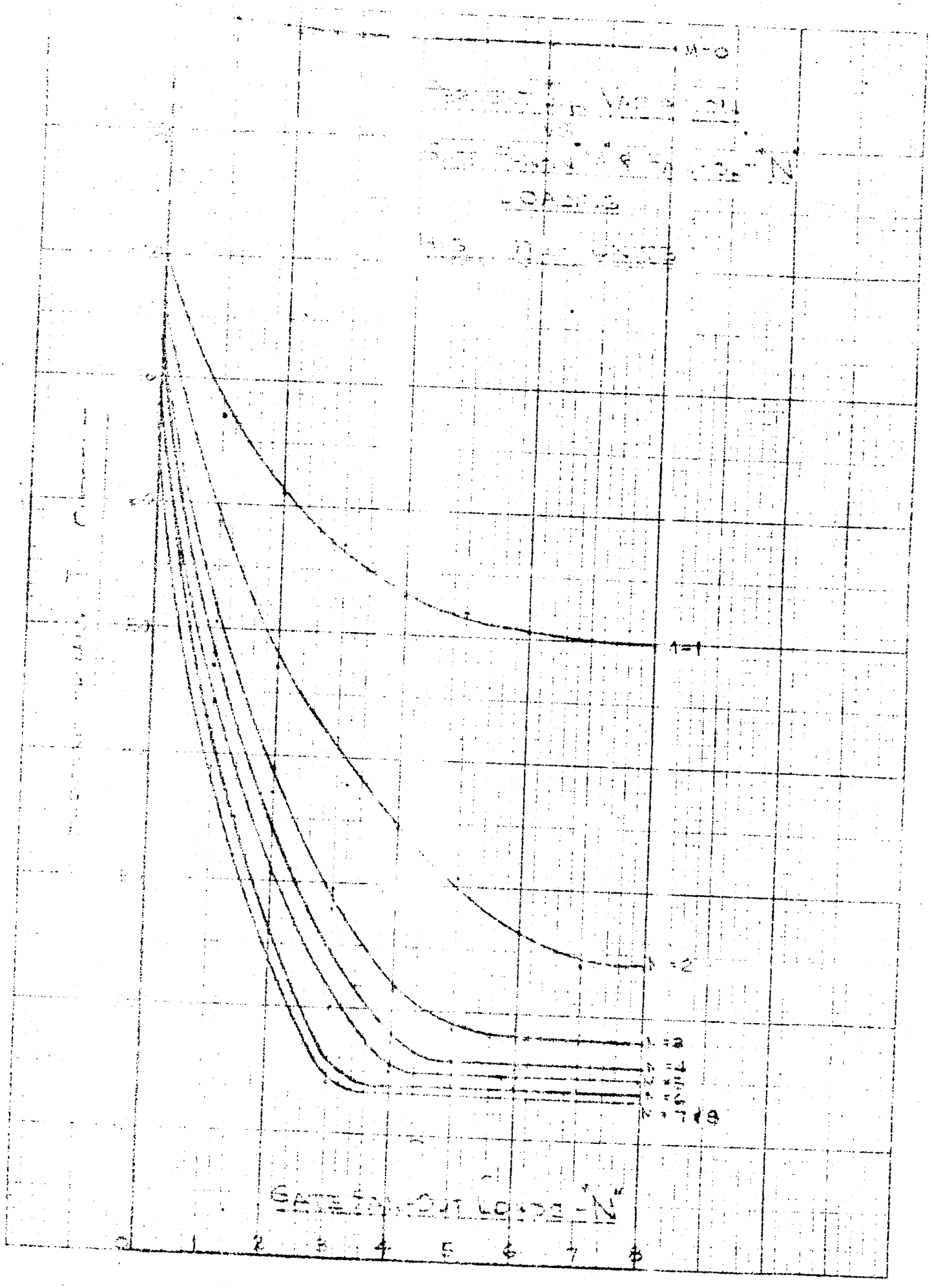
FIGURE 61



PERCENT I_L VARIATION
GATE FAN-IN M & FAN-OUT N
LOADING
LOW h_{FE} UNITS
M=2
M=1
M=3
M=4
M=5
M=6
M=7
M=8
PERCENT OF MAX. I_L CURRENT
GATE FAN OUT LOADING N
0
1
2
3
4
5
6
7
8



PERCENT OF MAX. I_D CURRENT
GATE FAN-OUT LOADS - N
0
1
2
3
4
5
6
7
8
20
30
50
60
N=2
N=5

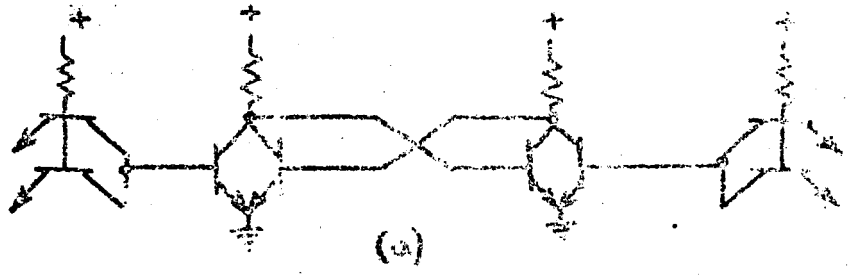

M=0
N=1
N=2
N=3
N=4
N=5
N=6
N=7,8
0
1
2
3
4
5
6
7
8

The results are shown in Figure 65.

Transient performance of the T^2L configuration was determined by evaluating worst case two stage propagation time as a function of loading conditions and transistor variations. The transistors used were the same units used in the evaluation of propagation time variations in the DTL configuration. The schematic diagram outlining the measurement techniques used to obtain two stage propagation time characteristics is shown in Figure 66.

Performance variations versus temperature of worst case rising and falling propagation time as a function of transistor and loading variations are shown in Figures 67 and 68.

Since T^2L is a direct coupled circuit, the output voltage swing of the gate is quite small and prohibits the use of an AC coupled flip-flop. Direct coupled complementing flip-flops may be obtained by using either of the configurations shown in Figure 69. Two of the circuits shown below are required to obtain the complementing function.



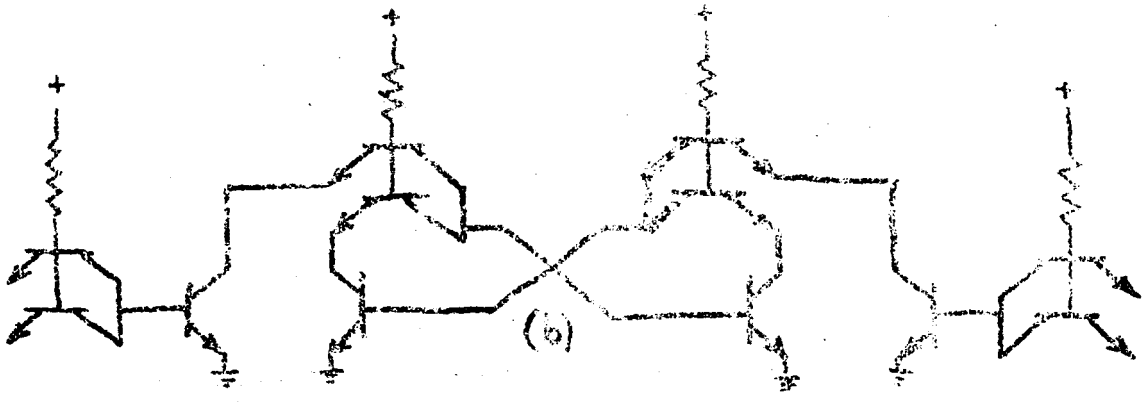
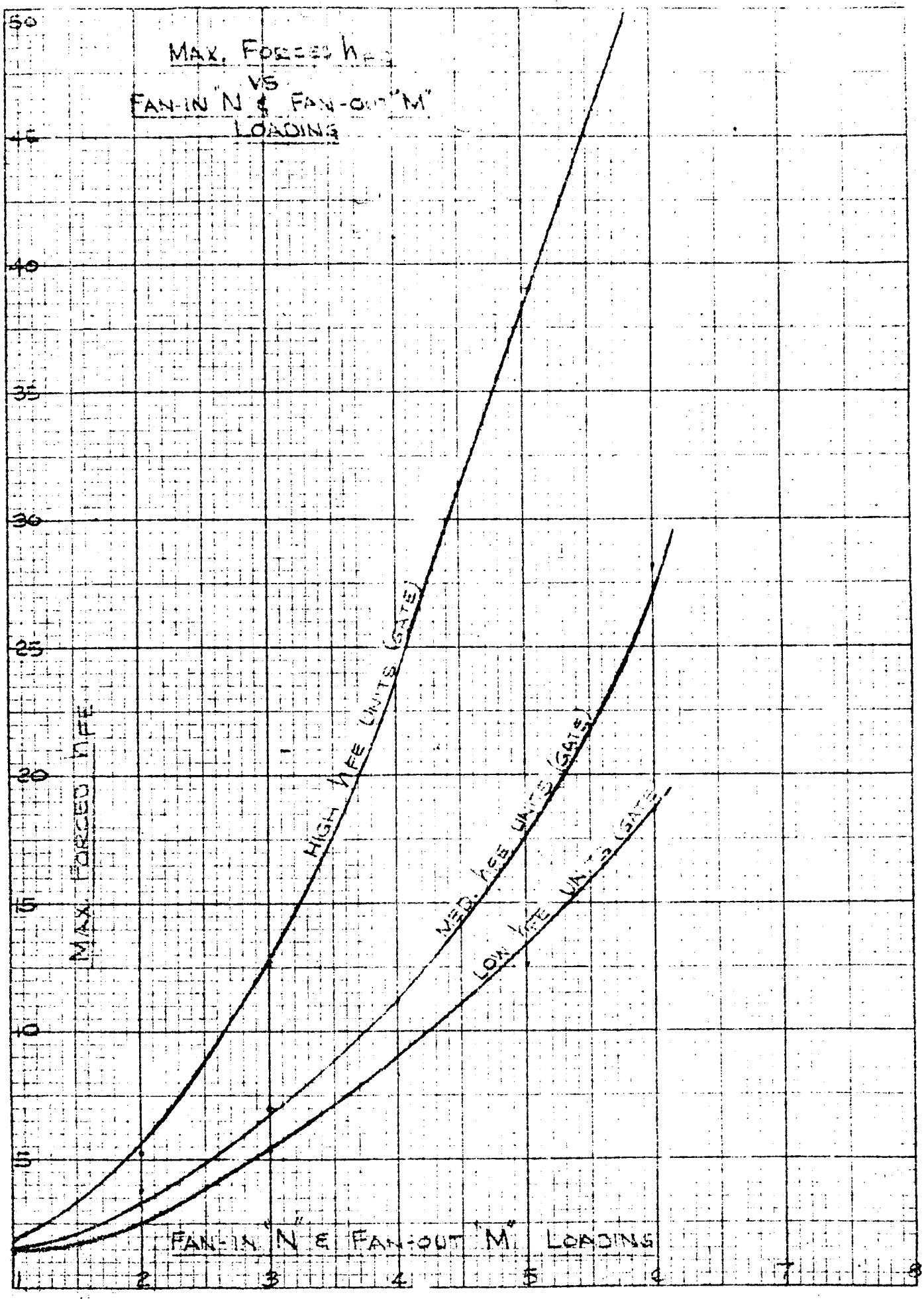
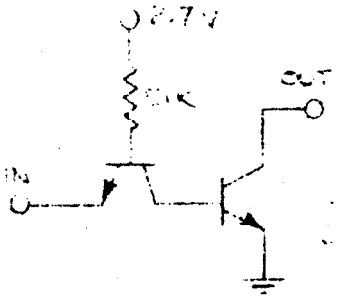


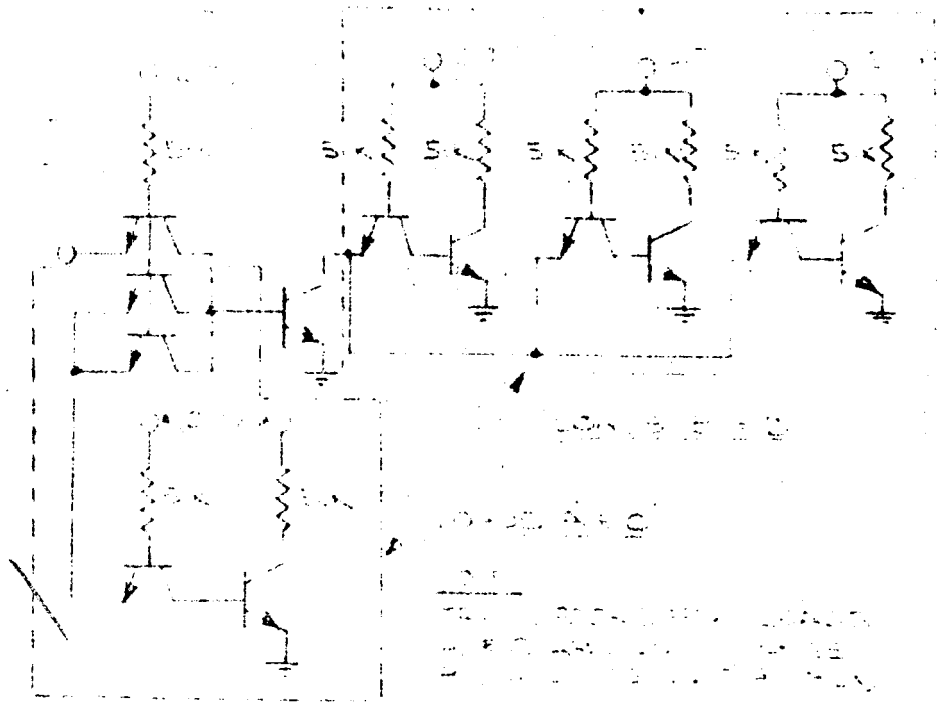
Figure 6

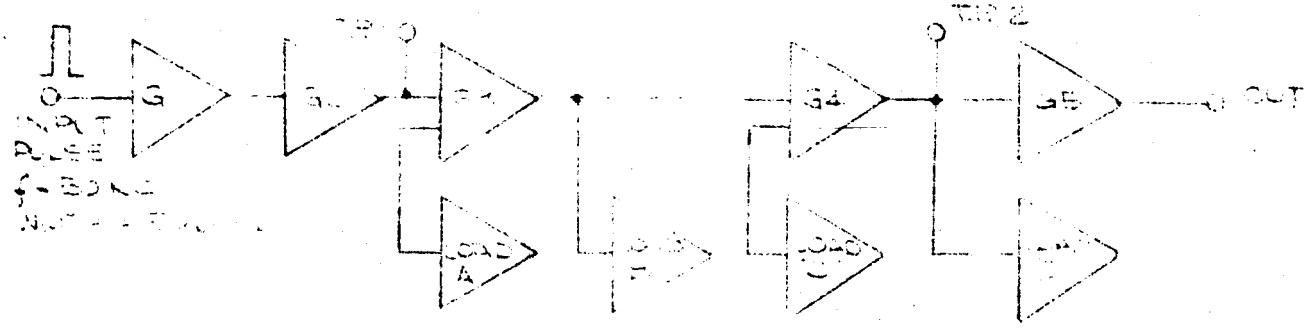


K&E 10 X 10 TO THE INCH 359-5DG
KEUFFEL & ESSER CO. MADE IN U.S.A.

TTL GATE

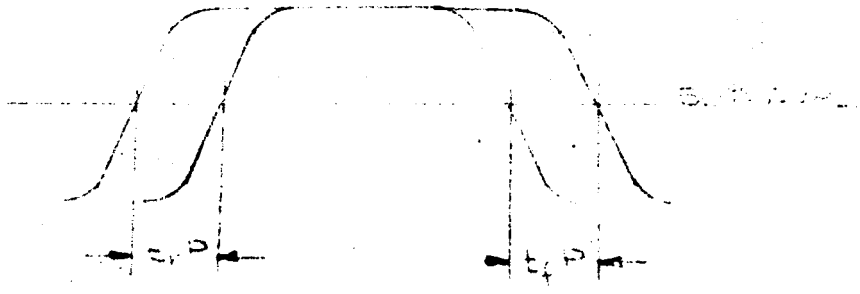


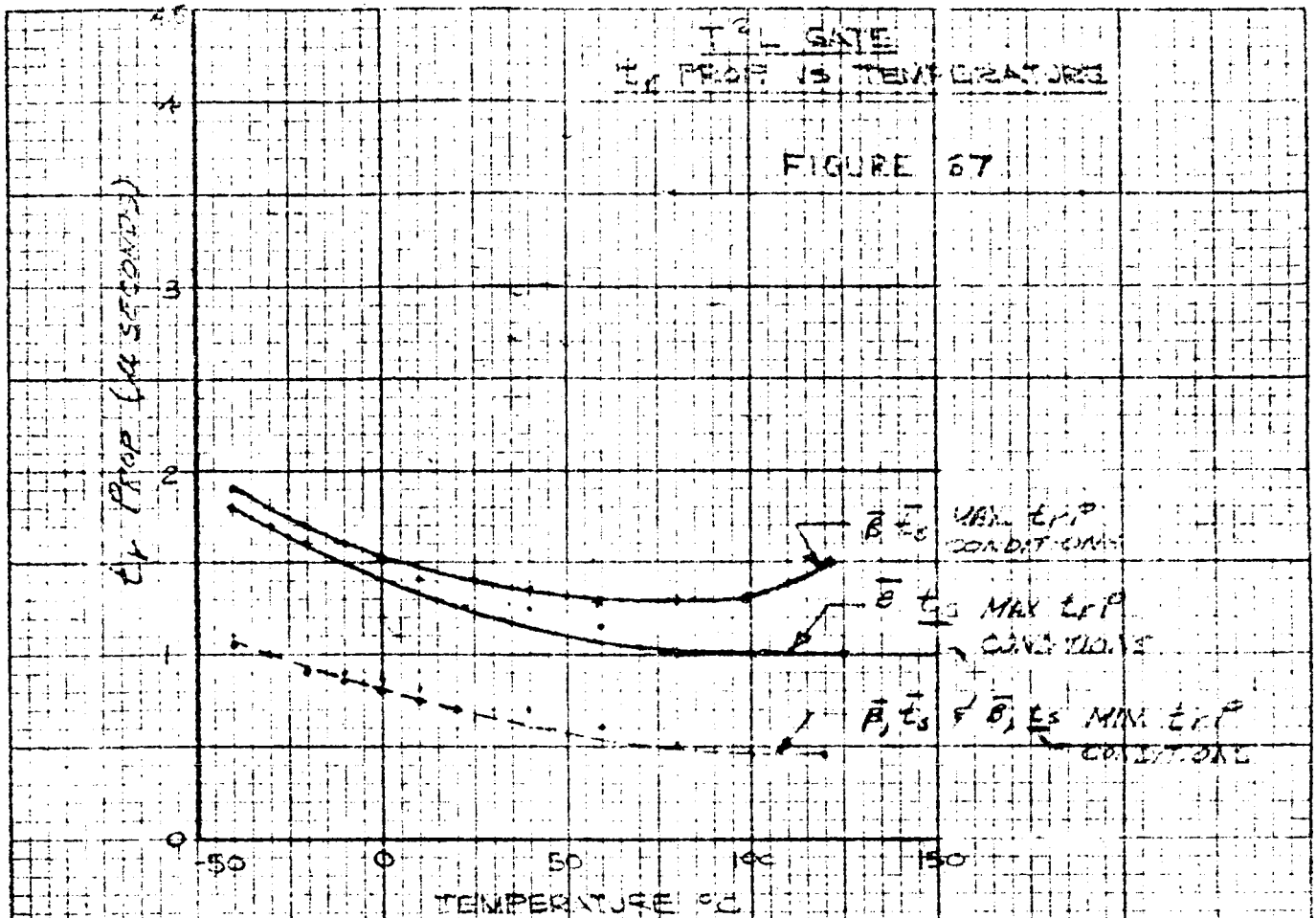


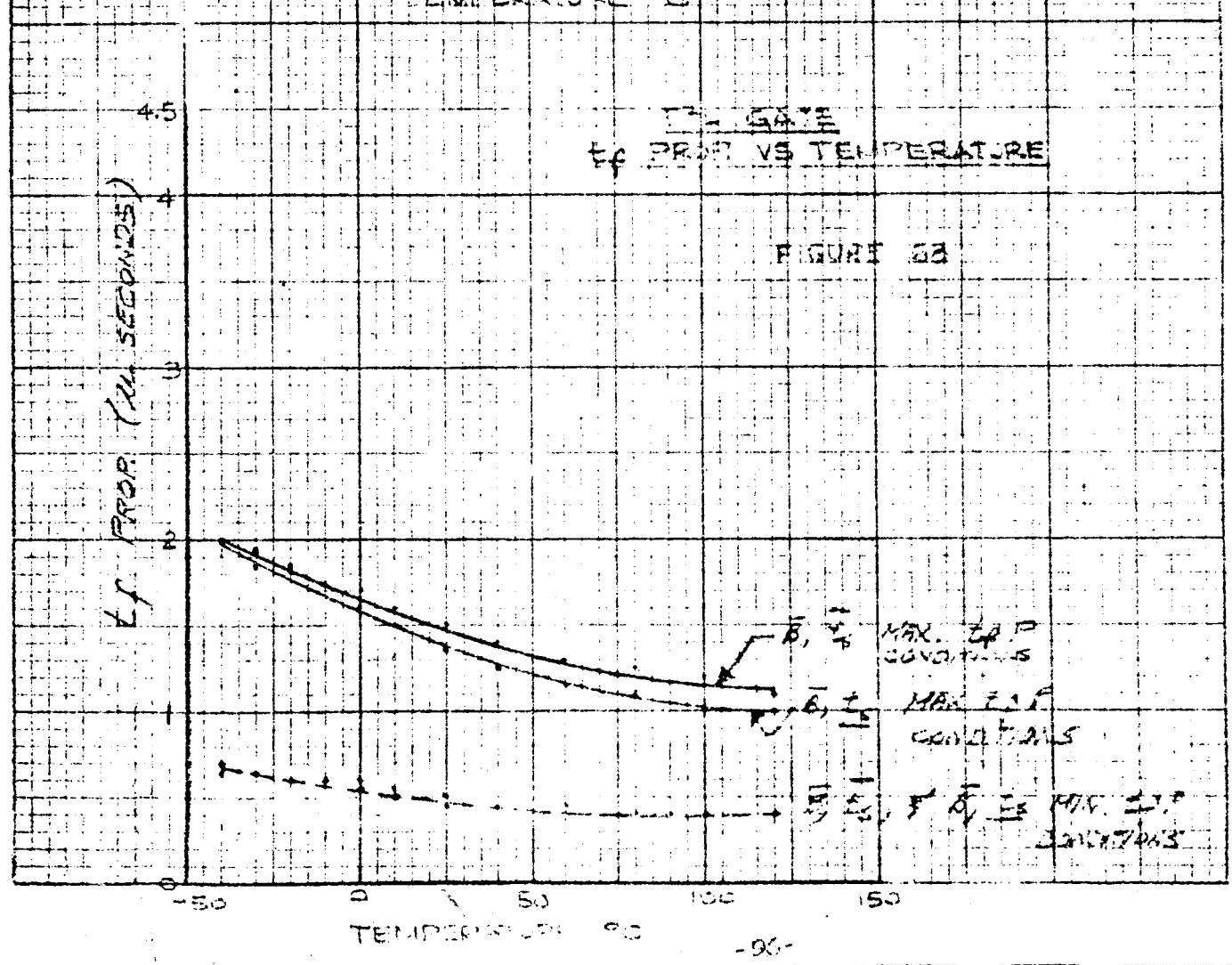


NOTE

WAVE SHAPE MEASURED AT
T.P. 1 & TP 2.
PROPAGATION TIME MEASURED
AT 50% OF AMPLITUDE AS
SHOWN BELOW.




T² - GATE
t_r PROP VS TEMPERATURE
FIGURE 67
t_r PROP (μ SECONDS)
4
3
2
1
0
-50
0
50
100
150
TEMPERATURE °C
$\bar{B}$, $\bar{t}_s$ MAX. t_r P CONDITIONS
$\bar{B}$ t_s MAX t_r P CONDITIONS
$\bar{B}$, $\bar{t}_s$ & $\bar{B}$, t_s MIN t_r P CONDITIONS


T² - GATE
t_f PROP VS TEMPERATURE
FIGURE 68
t_f PROP. (μ SECONDS)
4.5
4
3
2
1
0
-50
0
50
100
150
TEMPERATURE °C
$\bar{B}$, $\bar{t}_s$ MAX. t_f P CONDITIONS
$\bar{B}$, t_s MAX t_f P CONDITIONS
$\bar{B}$, $\bar{t}_s$ & $\bar{B}$, t_s MIN. t_f P CONDITIONS

The required [illegible] of [illegible]

Figure 70.

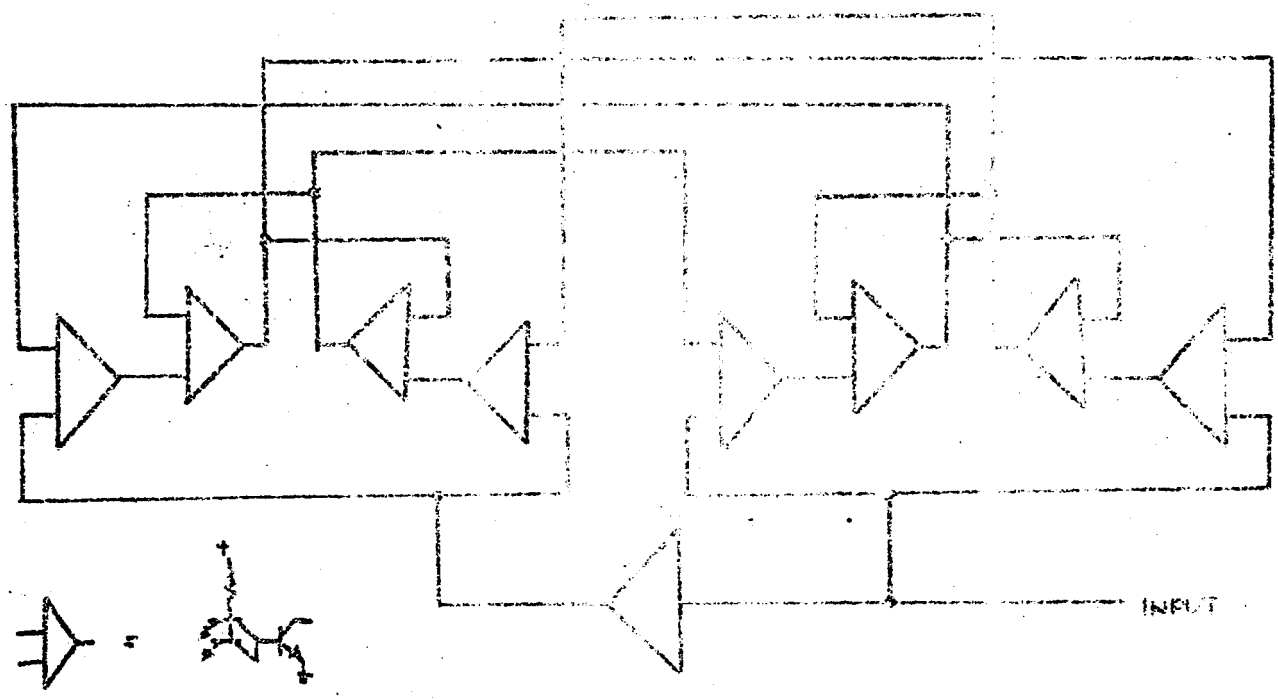


Figure 70

The flip-flops may be analyzed by utilizing the information determined for the T^2L gates since they are direct coupled. Both configurations were breadboarded and exhibited complementing frequencies of greater than 100KC.

The flip-flop shown in Figure 69 (a) is the least desirable since the base emitter voltage problem (current hogging) inherent to DCTL must also be considered in this case. For this reason the flip-flop shown in Figure 69 (b) will be considered throughout the remainder of this report.

Performance characteristics [illegible] to be compatible with gate performance [illegible] investigations of the flip-flop were [illegible] since analysis of the gate propagation time characteristics may be used to determine flip-flop performance characteristics.

Power Driver

The possibility of using a high fan-out (N = 10) gate to supplement the standard gate was investigated by using a gate with a lower resistance value of 25 KΩ. This "power driver" is equivalent to two loads, but will have fan-out capabilities of more than twice that of the normal gate. Performance characteristics were evaluated by substituting this gate into the worst case two stage propagation time test circuit with an allowable maximum fan-out of ten loads. The rising and falling propagation time measurements shown in Figures 70 and 71 indicate that the performance characteristics of the power driver are compatible with the standard gate performance characteristics shown in Figures 67 and 68.

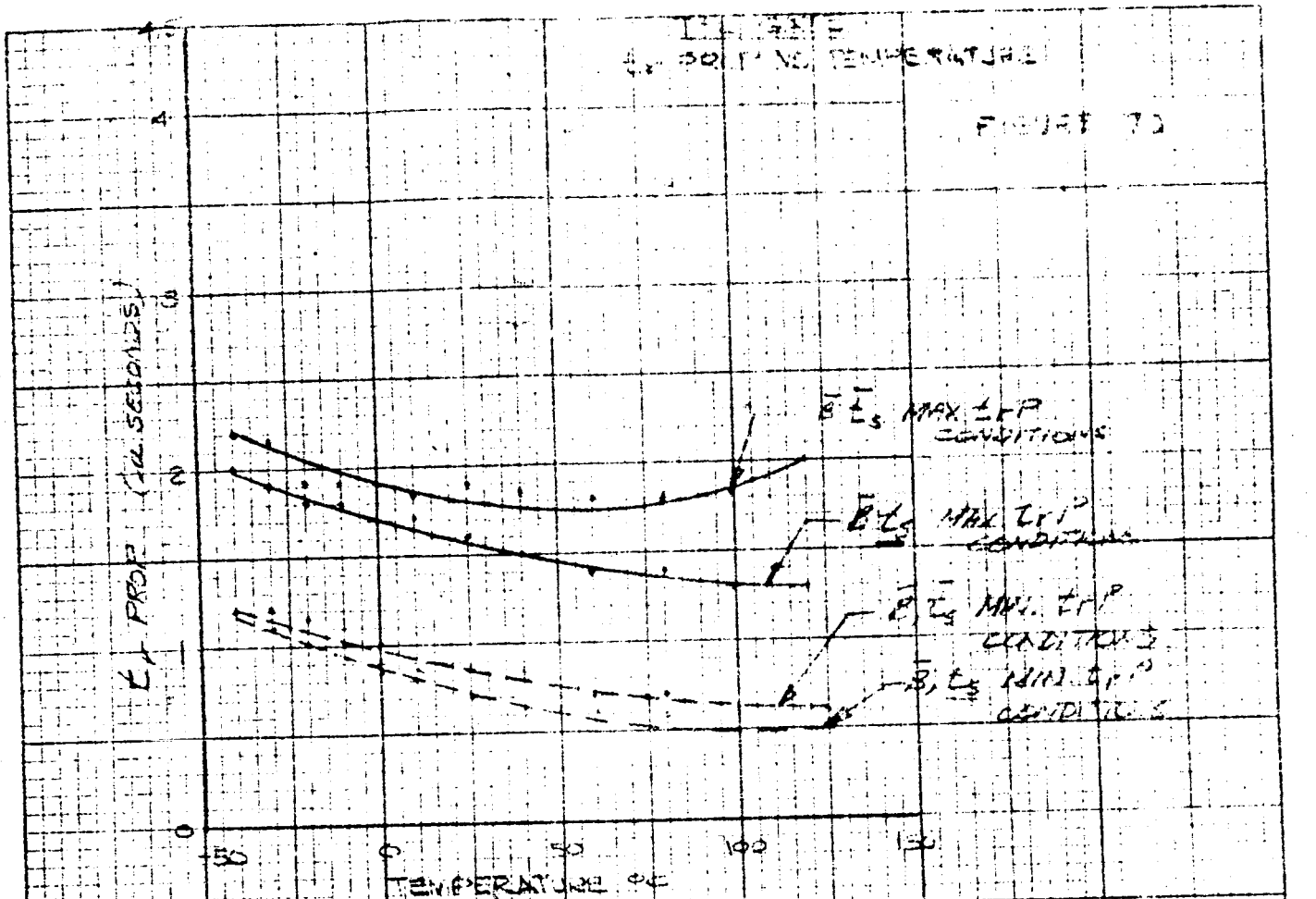


FIGURE 70
t_r PROP (μ SECONDS)
4
3
2
1
0
-50
0
50
100
150
TEMPERATURE °C
$\bar{B}\,\bar{t}_s$ MAX t_r P CONDITIONS
$\bar{B}\,t_s$ MAX t_r P CONDITIONS
$\bar{B}\,\bar{t}_s$ MIN. t_r P CONDITIONS
$\bar{B}\,t_s$ MIN. t_r P CONDITIONS

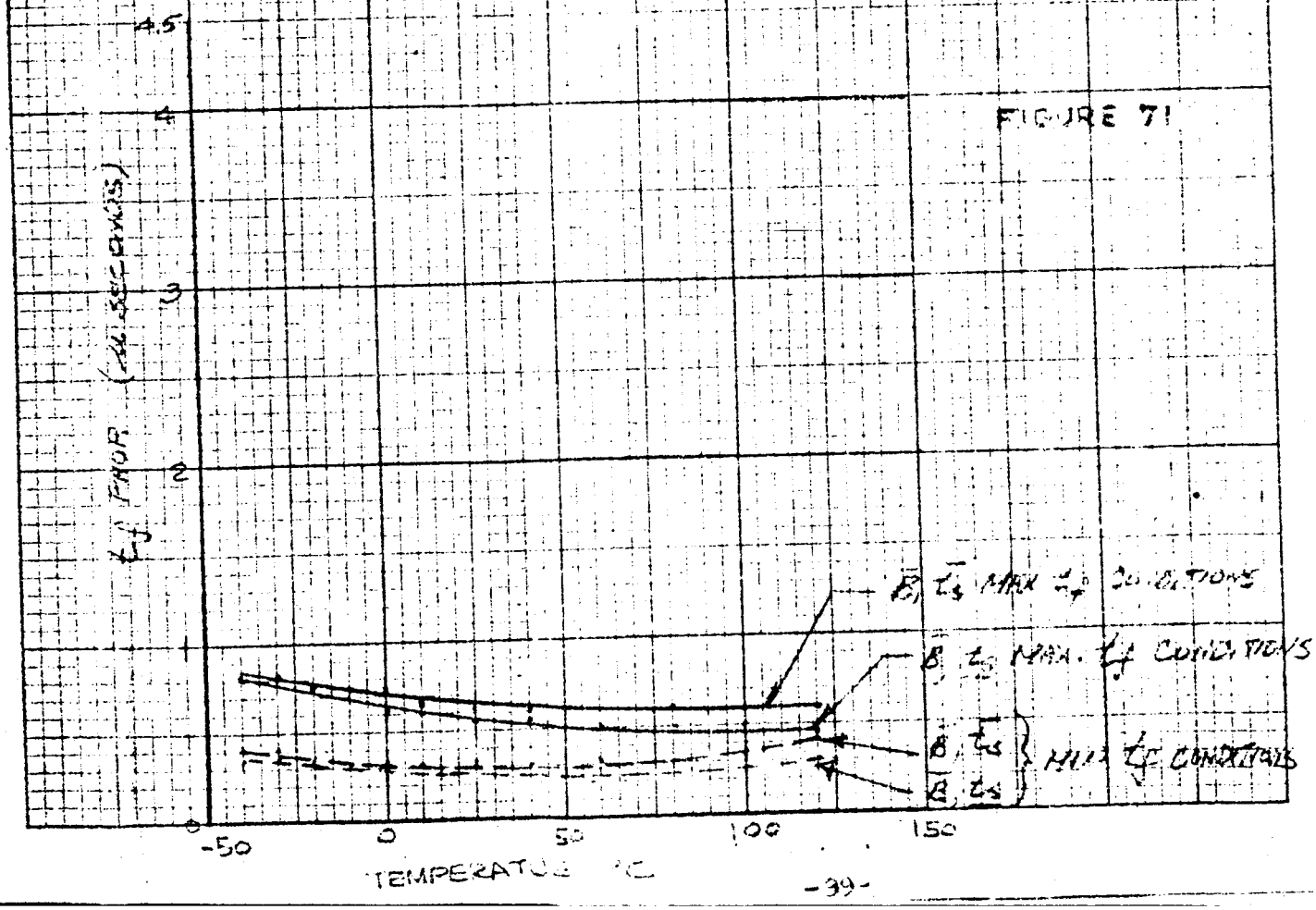


FIGURE 71
t_f PROP (μ SECONDS)
4.5
4
3
2
1
0
-50
0
50
100
150
TEMPERATURE °C
$\bar{B}\,\bar{t}_s$ MAX t_f CONDITIONS
$\bar{B}\,t_s$ MAX. t_f CONDITIONS
$\bar{B}\,\bar{t}_s$
$\bar{B}\,t_s$
MIN t_f CONDITIONS

3.4 SUMMARY

The circuits investigated in Section III are not necessarily the design that is recommended for final fabrication. The intention of the circuit evaluation portion of this report is to investigate two phases of circuit performance:

A) Performance variations as a function of variable power drain, as outlined in Section II.

B) Performance variations as a function of component variations and loading characteristics at constant power drain, as outlined in Section III.

Interpretation of Sections II and III should permit the reader to determine circuit performance characteristics over a wide range of operating conditions.

When each of the circuits investigated are considered, the operation of the circuits in a system as well as the individual performance characteristics must be evaluated. Although direct coupled circuits (I^2L) permit the lowest power drain and exhibit the most consistent performance characteristics over a wide temperature range, they have more drawbacks than are readily apparent.

The complementing flip-flop is quite complex in that it requires the equivalent of eight gates. Power drain for a complementing flip-flop is subsequently quite high. This requirement is necessary since the output voltage swing of the gate is quite small and prohibits the use of AC

steering networks. T^2L is also more susceptible than other configurations because of the small turn-off voltage at the transistor base. The active gating elements also tend to increase noise susceptibility because of the lack of a current limiting resistance element. The turn-off voltage is also temperature dependent and decreases with increasing temperature. There is a conflicting requirement on the gate transistor because low offset voltages are required to minimize the turn-off voltage problem and low inverse beta is required to prevent significant reductions in base current through base bleed-off current. It is usually quite difficult to obtain these characteristics in the same device. It is felt that these drawbacks more than out-weigh the low power drain characteristic of this gate.

The remaining configurations (DTL and complementary RDTL) both permit AC coupled flip-flops because of the larger output voltage swings. The original attempt to use very low collector supply voltages in the DTL configuration resulted in poor flip-flop performance over wide temperature range and a very small reverse bias on the gate diodes.

The larger collector supply voltage (2.7 volts) improved both situations but resulted in larger power drains. The DTL gate performance is highly dependent upon the switching characteristics of the input diodes. Worst case gate performance at high temperatures resulted in consistantly poor performance characteristics independent of diodes used. The gate switching characteristics and flip-flop frequency response are also dependent upon capacitance at the output node of the gate. If large values of collector

resistances are used, the fall time of the gate becomes quite large. The basic configuration also prohibits the use of separate NAND and NOR gates. An AND-OR logic sequence must be obtained through logic inversion at alternate gates. The flip-flop is less complex than a direct coupled type since it consists of two cross-coupled gates with an associated steering network. The steering network inputs may be connected and used as a complementing input or used separately as an AND set and reset as would be required in a shift register.

The complementary RDTL configuration has the advantage of permitting both NAND and NOR gates to be easily fabricated with similar design and performance characteristics. The ability of either type of gate to drive both NAND and NOR gates simultaneously is also a considerable advantage. The logical designer is permitted much greater flexibility since the AND-OR logic sequence may now be supplimented by AND-AND and OR-OR gate combinations without logical inversion. The complementary output transistor pair also permits the presence of a transistor rise time at both the rising and falling edge of the waveform, thus enhancing the switching speed of the circuit through the elimination of RC time-constant fall times. Worst case propagation time also degrades at high temperatures but not as appreciably as the DTL gate. Turn off voltage is about half way between the values exhibited by DTL and T^2L. Beta requirements are slightly higher but are not prohibitive.

The flip-flop configuration is less complex than two gates and has considerably lower power drain that other flip-flops considered. The

regenerative action of the flip-flop [illegible] excellent [illegible] and fast time. The configuration shown in Section V is basic and permits a reasonable degree of flexibility. Further logic advantages may be obtained by utilizing input capacitors in the complementing, set and reset modes.

Considering circuit performance and system's requirements as outlined in Section I, the complementary RDTL logic appears to offer the best performance characteristics. The problems involved in integrating the circuits must also be considered before a final selection can be made. A discussion of integration considerations characteristics is outlined in Section IV of this report.

4. CHARACTERIZATION

4.1 Component Characteristics

A. Semiconductors

The transistors and diodes used in the circuit evaluation (Sections 2 and 3) were devices obtained from Spectry Semiconductors standard production line. They are planar devices and are directly applicable to multiple chip fabrication techniques.

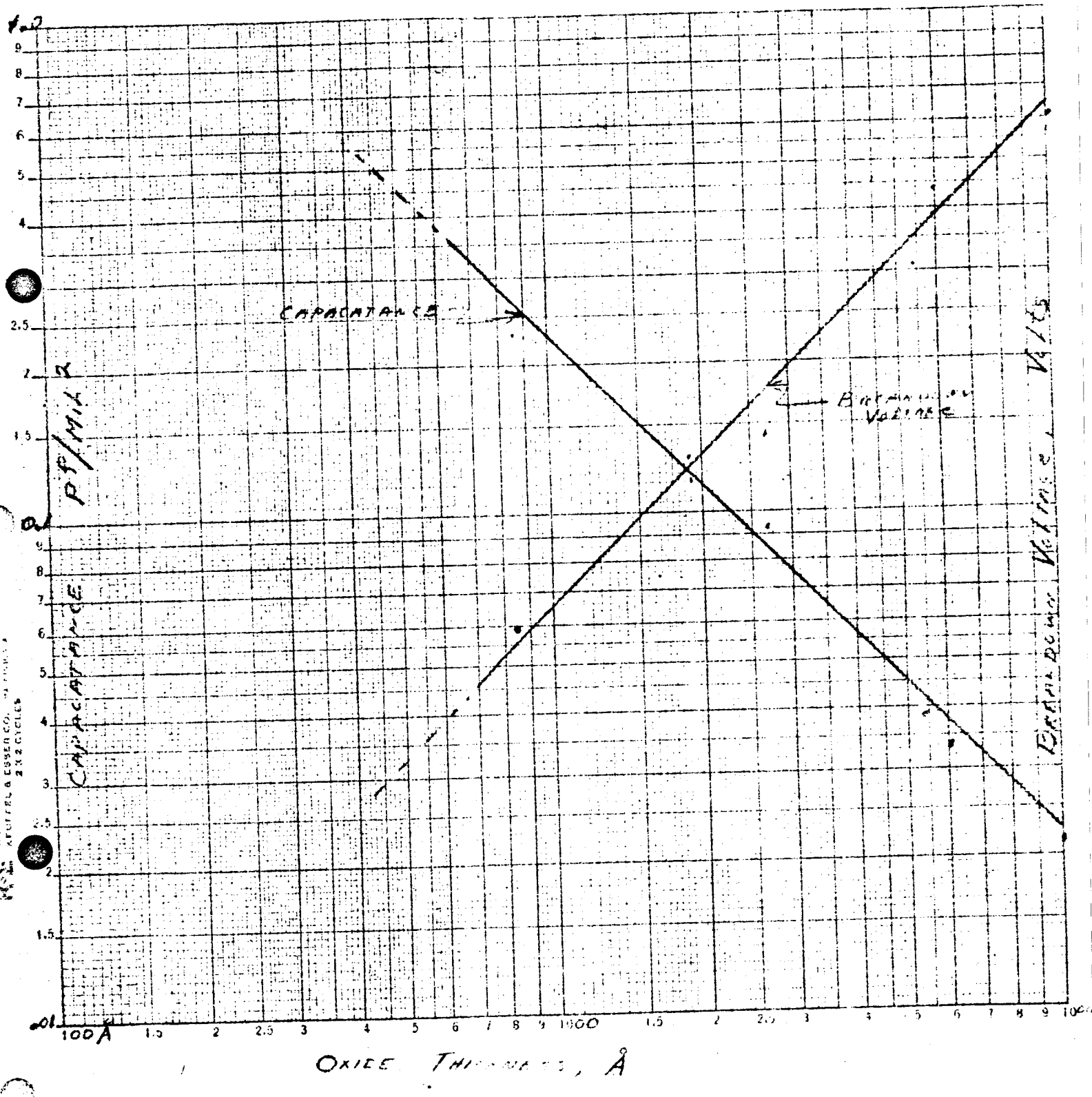
As previously mentioned, small signal transistors were used to obtain the high beta and low leakage required for circuit operation at low current levels. Transistor beta requirements vary from circuit to circuit and can be determined from information contained in Sections 2 and 3.

B. Capacitors

Capacitors will be fabricated with Si-SiO_2-Al structures. This method makes use of the high dielectric strength of thermally grown silicon oxide. The oxide is grown by a process similar to that employed to grow oxide layers on planar transistor surfaces. This allows precise control of oxide thickness and physical properties.

The maximum capacitance obtainable is limited by the area available. A graph of capacitance/mil^2 and breakdown voltage vs. oxide thickness is shown in Fig. 72.

Typically, a 60 pf ± 10% capacitance with a breakdown voltage of 100V may be fabricated in a 20 x 20 mil area. Temperature


CAPACITANCE
BREAKDOWN VOLTAGE
CAPACITANCE PF/MIL²
BREAKDOWN VOLTAGE VOLTS
OXIDE THICKNESS, Å
100 Å
1000
LOGARITHMIC
KEUFFEL & ESSER CO.
2 X 2 CYCLES

coefficient of capacitance is negligible and DC leakage current is $\sim 10^{-10}$ amps at 70% of breakdown voltage.

Capacitors may be formed integrally with other circuit elements. As shown in the proposed circuit structure, Fig. [illegible], the capacitors are formed on the same silicon block as the diode groups. The silicon forming one side of the diode also serves as one capacitor electrode. Oxide thickness can be controlled to give required capacitance independent of diode characteristics.

C. Resistors:

Resistors may be of two types: layers, or T. thin films. In each case, the actual resistance element will be a long thin strip, 1 to 4 mils wide and up to several hundred mils long.

The diffused resistors consist of a p-type diffused strip in an n-type silicon block with an oxide passivated surface. Resistors from 10 to 50,000 Ω may be fabricated on a 35 x 35 mil silicon chip. Tolerances on individual elements are ± 5%, temperature coefficients are +.1%/°C above room temperature, -.05%/°C below room temperature.

Because of the p-n junction isolating the resistor strip, there is a distributed capacitance along the resistor whose effect on circuit performance must be considered. In many cases it will be negligible.

The total distributed capacitance associated with a 50,000 Ω resistor is typically 15 pf. Several lumped parameter approximations to

the distributed have been developed [illegible] approximation valid for resistors [illegible] shown below in Fig. 73.

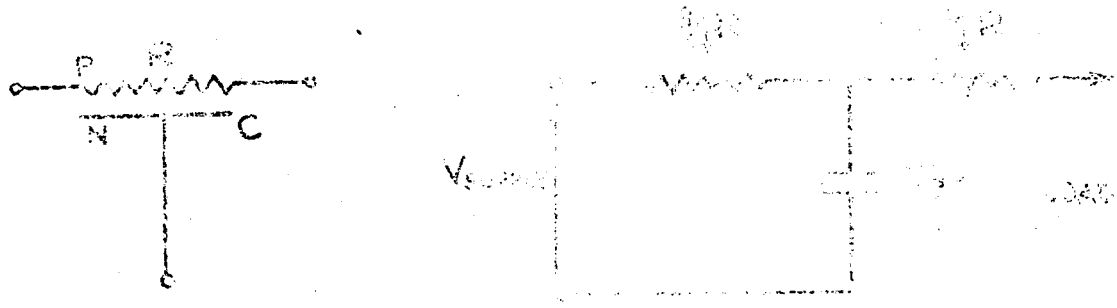


Fig. 73

The required reverse bias on the distributed diode along the resistor can be insured by tieing the n-type resistor block to the most positive supply voltage. This also minimizes the distributed capacitance.

Thin film resistors are formed by sputtering Ta on oxidized Si wafers. Photoresist techniques, similar to those used for planar transistors, are employed to delineate the pattern. Sheet resistivities from 100 to 500 $\Omega/\square$ can be obtained using pure Ta. Higher values can be obtained from Tantalum oxide films formed by sputtering Ta with a small, controlled partial pressure of O_2.

Temperature coefficients of thin film resistors are considerably less than diffused resistors and distributed capacitance values are typically 1/2 to 1/4 of those found in diffused resistors.

4.2 Circuit Performance vs. Integration Techniques

When investigating the possible integration of the circuits outlined in Section 3, the use of I.S.C. substrates, separate chips or combinations of these techniques must be considered. It is well known that the use of I.S.C. techniques result in rather severe parasytic effects, particularly at the low current levels being considered in this report. These parasytics consist primarily of distributed capacitance and leakage current associated with each diode isolated component block in the substrate and resistive paths shorting components to each other. Reductions in these parasytic effects have been achieved through triple diffusion and/or epitaxial techniques rather than the more conventional isolation diffusion techniques. The high transistor beta at low current levels and low isolation leakage requirement, however, are consistently obtainable through the use of isolation diffusion techniques. The parasytics associated with these techniques are quite high. Isolation diode capacitance associated with an integrated transistor meeting the performance characteristics previously outlined is 25 pf. When compared with the Cob of 4-5 pf of a conventional transistor the effects of complete circuit integration on performance can be evaluated semi-quantitatively. Distributed capacitance associated with other components are comparable with values determined for the transistor.

*I.S.C. - Integrated Semiconductor Circuits

Configurations such as RTL and T^2L are particularly susceptible to performance degredation from these parasytics since switching characteristics are dependent upon the RC time constants at the gate output. The problem associated with T^2L is even greater since the large Cob of the gate transistors appears across the output transistors base-emitter junction. The capacitance of the input diodes in DTL will act in the same fashion if low power high speed operation is needed. These parasytics will tend to prohibit this requirement. It is for this reason that integrated circuits normally require at least twice the power drain to obtain performance compatible with separate component circuits.

The complementary circuits offer a solution to the parasytic problem since the output waveform is not dependent upon RC time constants. When the fabrication of both PNP and NPN transistors on a single substrate is considered, other difficulties are encountered. The problem is discussed in detail below.

The problem of producing NPN and PNP transistors in the same silicon substrate is very difficult at best. In this situation, the difficulty is compounded because of the requirement for complementary operation at extremely low current levels. No devices of this type have been developed to date for operation at low current levels. For this reason, it is not considered practical to include both NPN and PNP low level transistors in the design of an I. S. C. circuit at this time.

Several NPN-PNP devices have been reported on at technical meetings. Those devices utilized the base diffusion for one transistor as

the collector for the other. [illegible] quired than for single transistors, but the collector, base and emitter doping levels for the NPN differed by an order of magnitude or more from the PNP. For complementary operation at low levels, our experience indicates nearly equivalent doping levels are desirable. A possible NPN-PNP structure suitable for inclusion in an I. C. microcircuit is shown below in Fig. 74.

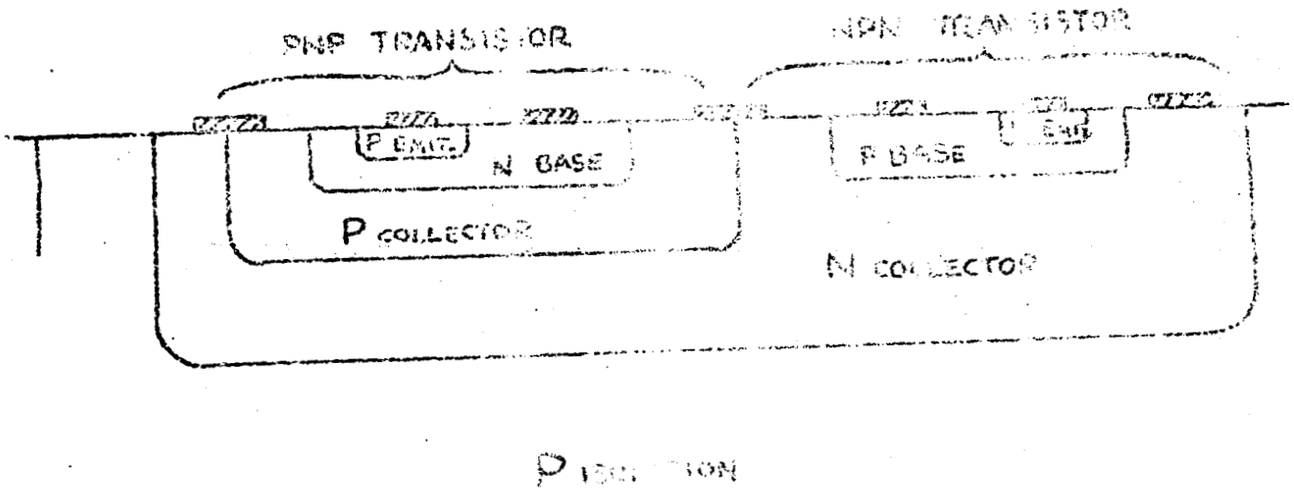


Fig. 74

Fabrication of this type device would pose a number of formidable problems which would require considerable development time. Several of these are listed below.

1. The fabrication of the two collector regions would require either epitaxial growth with masking of selected areas -- i.e., grow an n-layer with holes, then fill the holes with p-type material for the PNP collectors) or an extremely light doping diffusion process would have to be

developed to form the collector regions. Both procedures require considerable development work to be practical.

2. Once the collector regions are formed, 50 to 60% additional major processing steps would be required over the number needed to make transistors or microcircuits with only NPN transistors. The additional steps would reduce the yield considerably.

3. In fabricating planar transistors, the beta is controlled to the desired level by adjusting the emitter diffusion time to compensate for small variations in other previous diffusion steps. In an integrated NPN-PNP device, the two units cannot, of course, be independently controlled, hence extremely tight limitations would be placed on all diffusion processes. The requirement for high betas and low current operation increase the degree of control required. The higher the beta, the more sensitive a transistor is to small variations in diffusion processes. It is doubtful if presently employed diffusion processes provide sufficient control to insure a reasonable yield of adequately matched complementary devices.

4. Optimum surface treatments are different for NPN and PNP devices. These surface treatments involve cleansing procedures prior to processing, oxidation atmospheres, etc., and are critical to insuring low leakage currents and good low level operation.

5. Isolation diode capacitance for the NPN-PNP device would be about twice that of a single transistor.

Solutions to the above problems are not obvious at the present time, hence, an I. S. C. type circuit requiring both NPN and PNP transistors with characteristics similar to Sperry low level complementary units will not be feasible for the immediate future.

An alternate solution that does not limit performance characteristics as stringently as an I. S. C. substrate is the use of a multiple chip circuit. In this approach, separate diffused or thin film components are substituted on a one to one basis for the conventionally constructed circuit. The performance characteristics of this type of circuit closely approach that of the conventionally constructed circuit. The components can also be individually selected to provide consistent performance characteristics. The basic limitation of this approach is the large number of required interconnections between the separate components.

It is possible to minimize interconnections and maintain the good circuit performance characteristics of multiple chip circuits. This may be accomplished by minimizing the number of chips by combining components and interconnections into a smaller number of component chips. This approach is the best compromise between the low power circuit performance requirements and fabrication techniques. The application of this fabrication approach to the recommended family of circuits is discussed in Section 5.

5. CIRCUIT RECOMMENDATIONS

5.1 In view of the previously discussed circuit performance and integrated component characteristics, it is recommended that complementary RDTL logic be considered as the optimum circuit configurations for low power applications. It should be recognized that any digital design is the result of a number of design assumptions and performance trade-offs that does not result in completely optimized performance for any configuration. Complementary logic is recommended because it consistently approaches the requirements outlined in Section 1 of this report.

Considerable logic flexibility is available and performance characteristics afford a better compromise between noise margins, switching speed, power drain and component requirements than other circuits investigated.

The final design of a family of complementary circuits is contingent upon NASA's final performance requirements which may be determined from the preliminary information included in this report. Final design may be determined by mutual consent between NASA and Sperry Semiconductor during the early portion of phase II of contract NAS1-2619.

A brief discussion of proposed circuit fabrication techniques and an example of their application to the family of complementary circuits is given in the following sections.

bonding of gold wire between the various contact points. Interconnecting in this manner is kept to a minimum by using evaporated connections in such things as resistor networks or wherever possible. The device is now tested for some circuit performance functions and after having satisfactorily demonstrated this it is ready for final encapsulation. This is accomplished using the proven semiconductor device procedures of deionized wafer washing, vacuum baking and top shield welding. Following encapsulation is a schedule of final electrical testing with a sample of the circuits produced being turned over to a quality control group for reliability testing that will determine the mean time between failure and environmental capabilities.

5.3 Final Circuit Packaging

The application of separate chip fabrication techniques to the packaging of CRDTL circuits can best be illustrated with the gate and flip-flop configurations. These packages serve as typical examples of the single and stacked ceramic substrate designs that can be fabricated on multipin TO-5 type headers.

The CRDTL NOR gate is assembled on a single metalized ceramic wafer. As illustrated in Fig 75, the three metalized areas serve as isolating islands for the five semiconductor chips that comprise the circuit. Diode and capacitors are diffused on a single chip and the resistors have been produced in a series network with bonding taps appropriately located for interconnections. When all elements have been

5.2 Circuit Fabrication

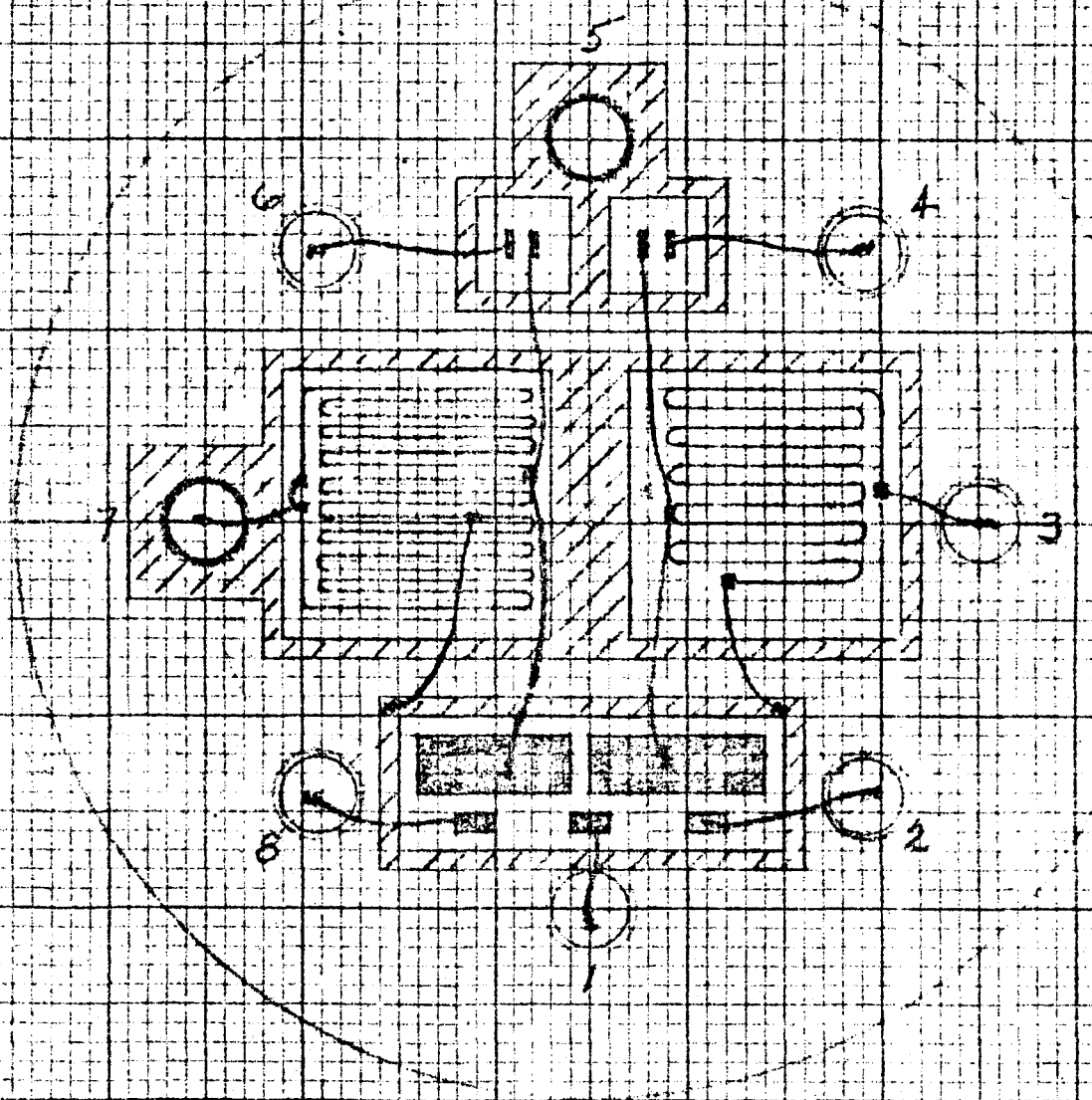
A review of the fabrication techniques that are applicable to the packaging of semiconductor integrated circuits can involve a discussion of a number of different processes and a variety of equipment depending upon the degree of sophistication intended. When it becomes desireable to optimize circuit performance by using selected active components, the separate chip assembly techniques can be used for this purpose.

For separate chip assemblies the multipin TO 5 type headers are usually used. Isolation of the circuit elements is provided by the use of one or more ceramic wafers with appropriately metalized areas. Gold plating over the metalizing provides a surface on which silicon chips can be alloyed with the silicon eutectic preforms. Using conventional resistance heating equipment the various circuit elements in chip form are bonded to the ceramic substrate. At this point, electrical probing on the wafer is done to check device parameters and insure that sound contacts have been made. Circuit candidates in wafer form are now ready for header mounting. The wafers are oriented in such a way that the metalized areas correspond with appropriate pins on the header. Metalizing has been produced around pin holes where electrical contacts are to be brought out of the package, and brazing rings of a lower alloying temperature than Au-Si are used to produce these electrical connections and also provide mechanical rigidity between the substrate and header. The remaining circuit interconnections are now made by the thermo compression

FIG 75

CRDTL NOR GATE

COMPONENT - WIRE LAYOUT



alloyed in place, the wafer is brazed to the header at pins 3 and 5, see Fig. 76, using Au-Ge brazing rings. Thermocompression bonding of the interconnection wire completes the assembly and the device is ready for final encapsulation and testing.

In the case of the GRDTC flip-flop, the assembly is more difficult due to the fact that interconnection will have to be made between two substrates. This is accomplished as illustrated in Fig. 77 and Fig. 78 by producing metalized areas around the interconnecting pins 3 and 5. Wafer No. 2, see Fig. 79 is assembled first and brazed to the header at pin 5. After the wire bonding at this level is completed the second assembled wafer is placed on the header. Some slight spacing between them is required to prevent damage to the wiring and this is accomplished by having the underside of wafer No. 2 ridged. The second wafer is now brazed to the header at pins 3, 5 and 6 and the wire bonded in the conventional manner completing the assembly.

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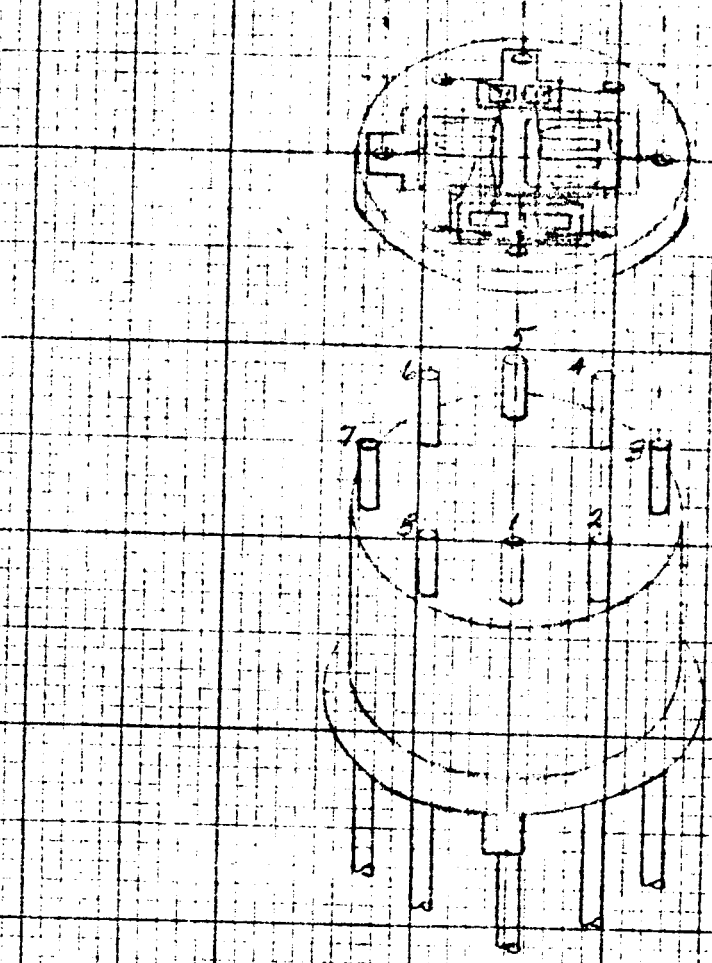
FIG 7b
CIRCUIT [illegible]
FINAL [illegible]



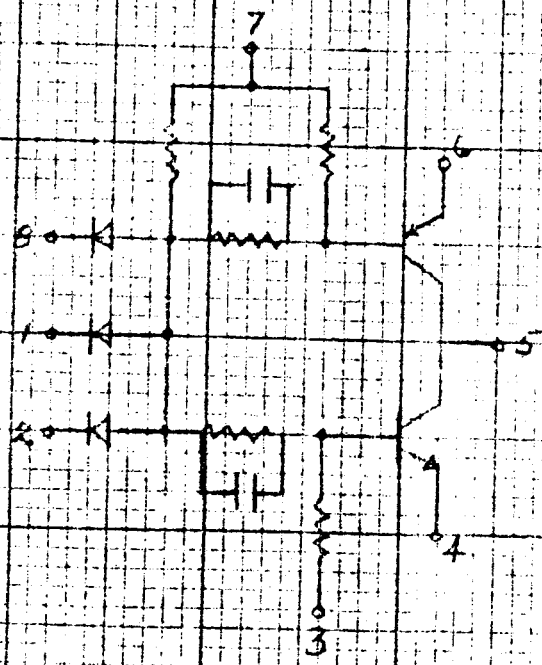


FIG 17
CRDTL FLIP-FLOP
COMPONENT WAFER LAYOUT #1

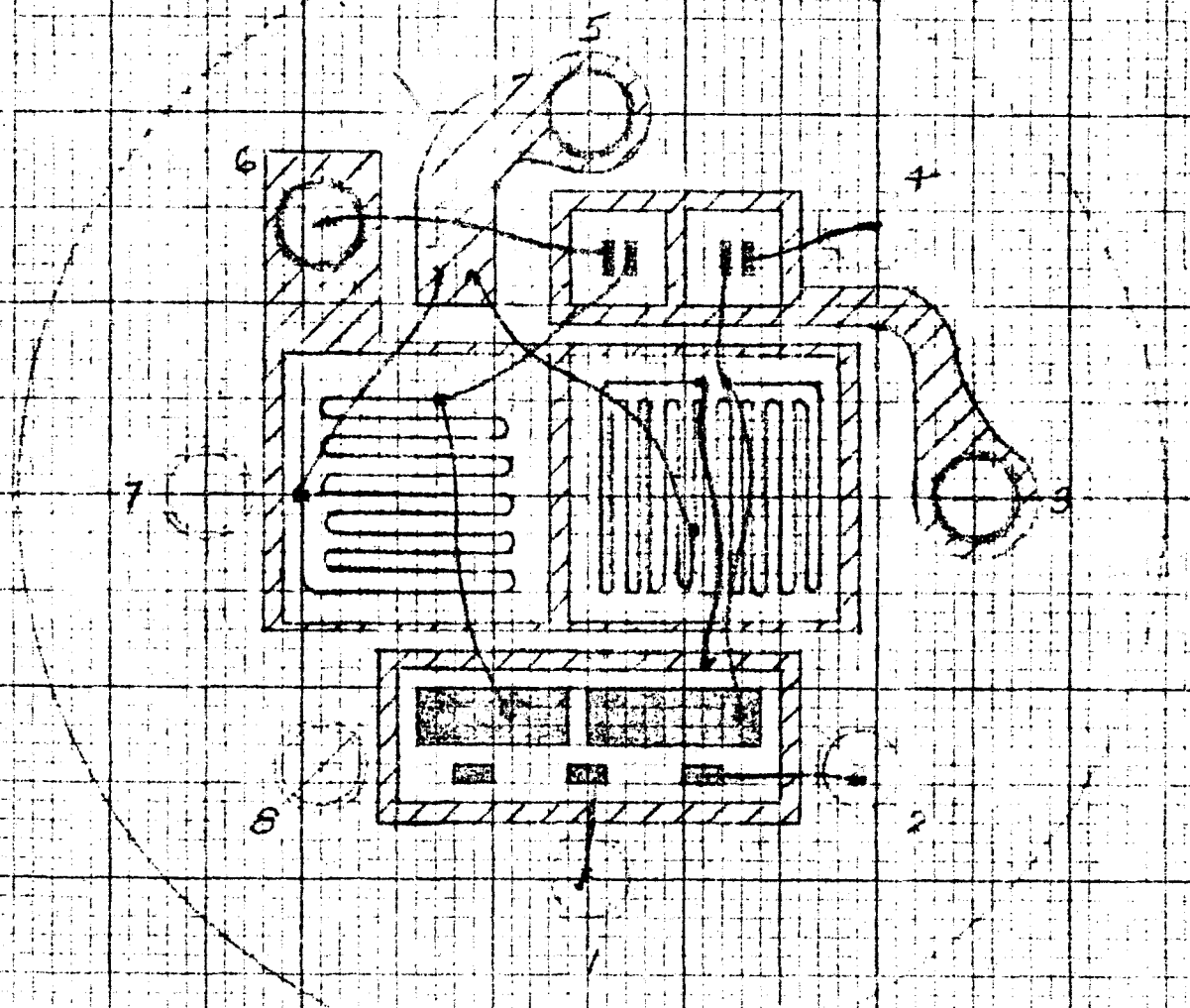


FIG. 75
CRDTL FLIP FLOP
COMPONENT WAFER LAYOUT #2

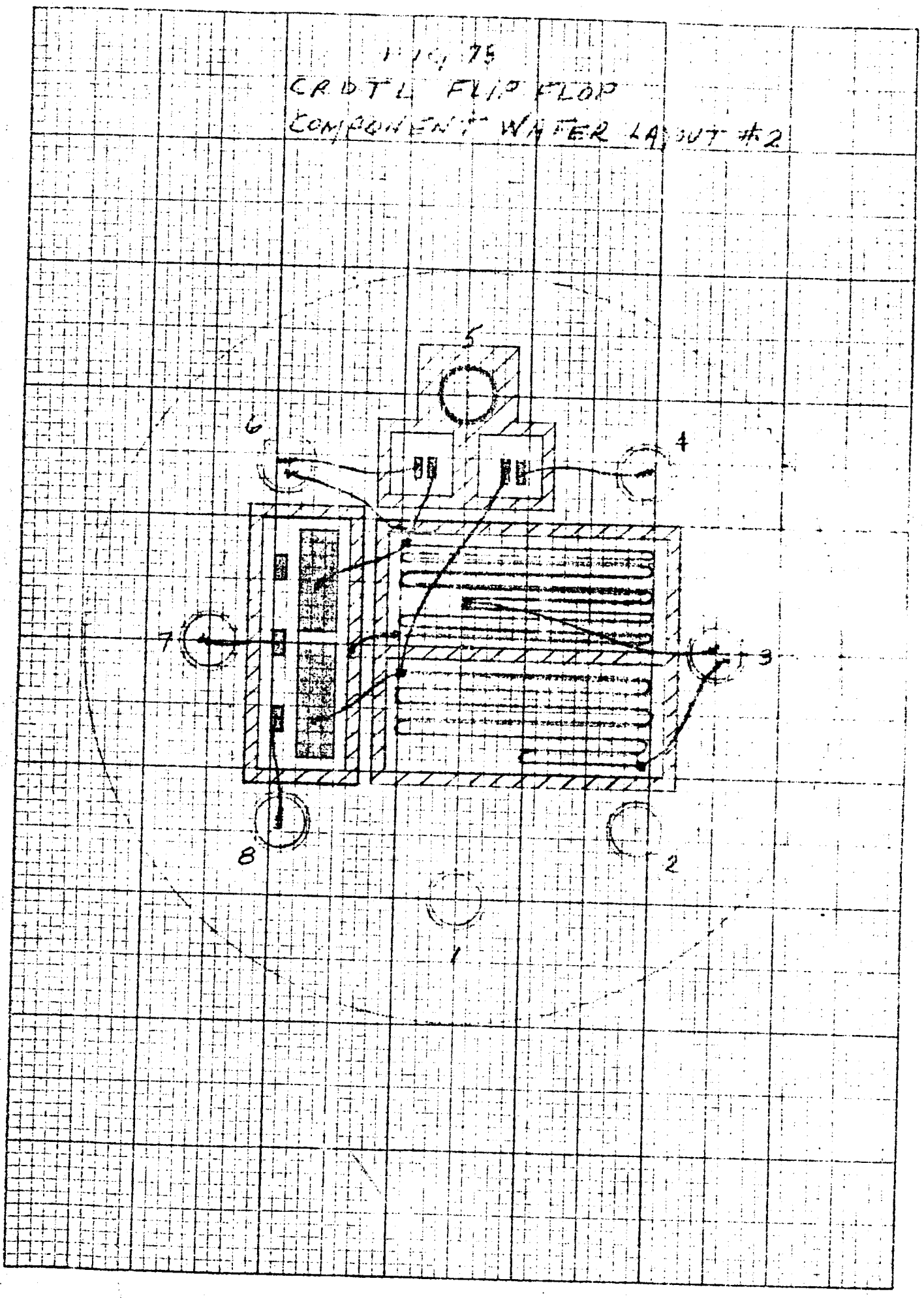
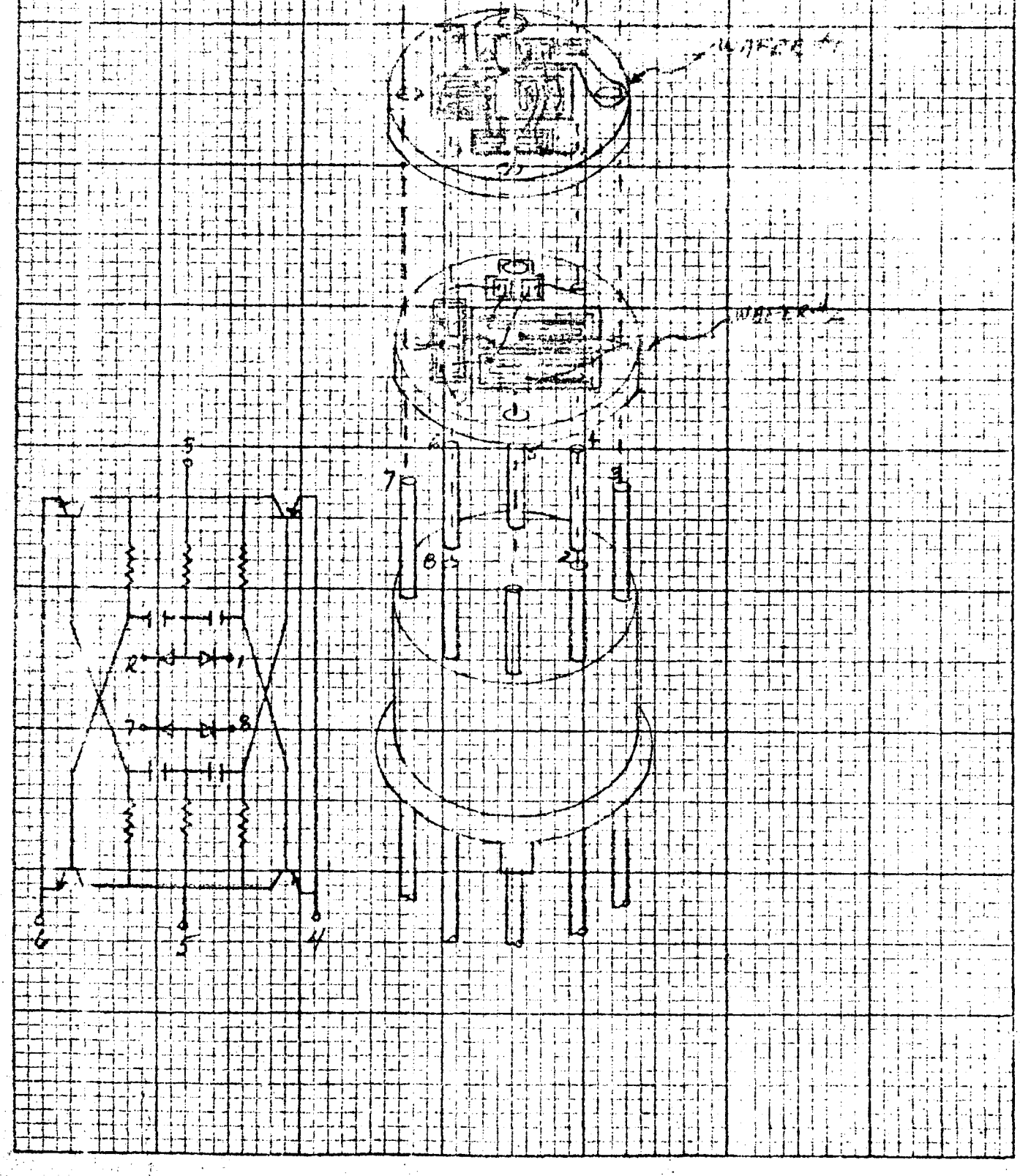



FIG 79
CADMIUM FLIP FLOP
FINAL ASSEMBLY