NASA TECHNICAL NOTE

NASA TN D-2311

c.1
LOAN COPY: R... TO
AFWL (W
KIRTLAND AF
TECH LIBRARY KAFB, NM
0154920

NASA TN D-2311

THE MRIR-PCM TELEMETRY SYSTEM — A PRACTICAL EXAMPLE OF MICROELECTRONIC LOGIC DESIGN

by Paul M. Feinberg

Goddard Space Flight Center
Greenbelt, Md.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • JULY 1964

TECH LIBRARY KAFB, NM

0154920

THE MRIR-PCM TELEMETRY SYSTEM — A PRACTICAL EXAMPLE OF MICROELECTRONIC LOGIC DESIGN

By Paul M. Feinberg

Goddard Space Flight Center
Greenbelt, Md.

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

For sale by the Office of Technical Services, Department of Commerce,
Washington, D.C. 20230 -- Price $0.75

THE MRIR-PCM TELEMETRY SYSTEM— A PRACTICAL EXAMPLE OF MICROELECTRONIC LOGIC DESIGN

by
Paul M. Feinberg
Goddard Space Flight Center

SUMMARY

Digital satellite systems containing microelectronic circuitry require the use of unique design techniques. This report describes the logic design for one such unit, the medium resolution infrared – pulse code modulation (MRIR-PCM) telemetry system. In addition, basic microelectronic design techniques are given.

CONTENTS

Summary i

INTRODUCTION 1

NIMBUS AND TIROS MRIR-PCM SYSTEMS 1

MICROELECTRONIC DESIGN 4

MRIR-PCM LOGIC CIRCUITRY 11

General 11

Nimbus Record Logic 12

Tiros Record Logic 14

Nimbus and Tiros Playback Logic 15

CONCLUDING REMARKS 17

ACKNOWLEDGMENTS 18

THE MRIR-PCM TELEMETRY SYSTEM— A PRACTICAL EXAMPLE OF MICROELECTRONIC LOGIC DESIGN

by
Paul M. Feinberg
Goddard Space Flight Center

INTRODUCTION

The medium resolution infrared—pulse code modulation (MRIR-PCM) logic system is a versatile telemetry unit originally intended as a subsystem in only the Nimbus satellite but later modified for use in the Tiros satellite as well. In the MRIR system, voltages representing meteorological and experimental data are sampled in a format sequence, converted to digital form, stored on a digital tape recorder, and, upon interrogation, transmitted at a constant bit rate to a readout station on the ground.

Among the unique features in the logic system is circuitry which permits transmission of binary words of variable length – the word length being dependent on the amount of wow and flutter of the digital tape recorder. Because the effects of tape recorder wow and flutter are compensated for by variable word lengths, transmission errors introduced from tape recorder speed variation are eliminated.

To minimize system weight, size, and power dissipation, microelectronic circuitry has been used extensively in the implementation of the logic design. All microelectronics used in the MRIR system were produced under precise quality control programs to give improved reliability at the circuit level that could be translated directly into improved system performance and reliability.

NIMBUS AND TIROS MRIR-PCM SYSTEMS

In most respects the logic designs for the Nimbus and Tiros MRIR-PCM systems are identical; block-diagrams are shown in Figures 1 and 2. Inputs from a 100 cps two phase clock and from a 200 kc clock are shaped to provide all the timing pulses required to operate either MRIR system. In the Nimbus as well as the Tiros system, analog meteorological data from 5 radiometer sensors is sequentially passed through analog gates to an analog-to-digital converter. Digitization of the analog data, whose range varies between 0 and -6.4 volts, is accomplished with a conversion accuracy of 1 part in 128. The total converter uncertainty over the operating

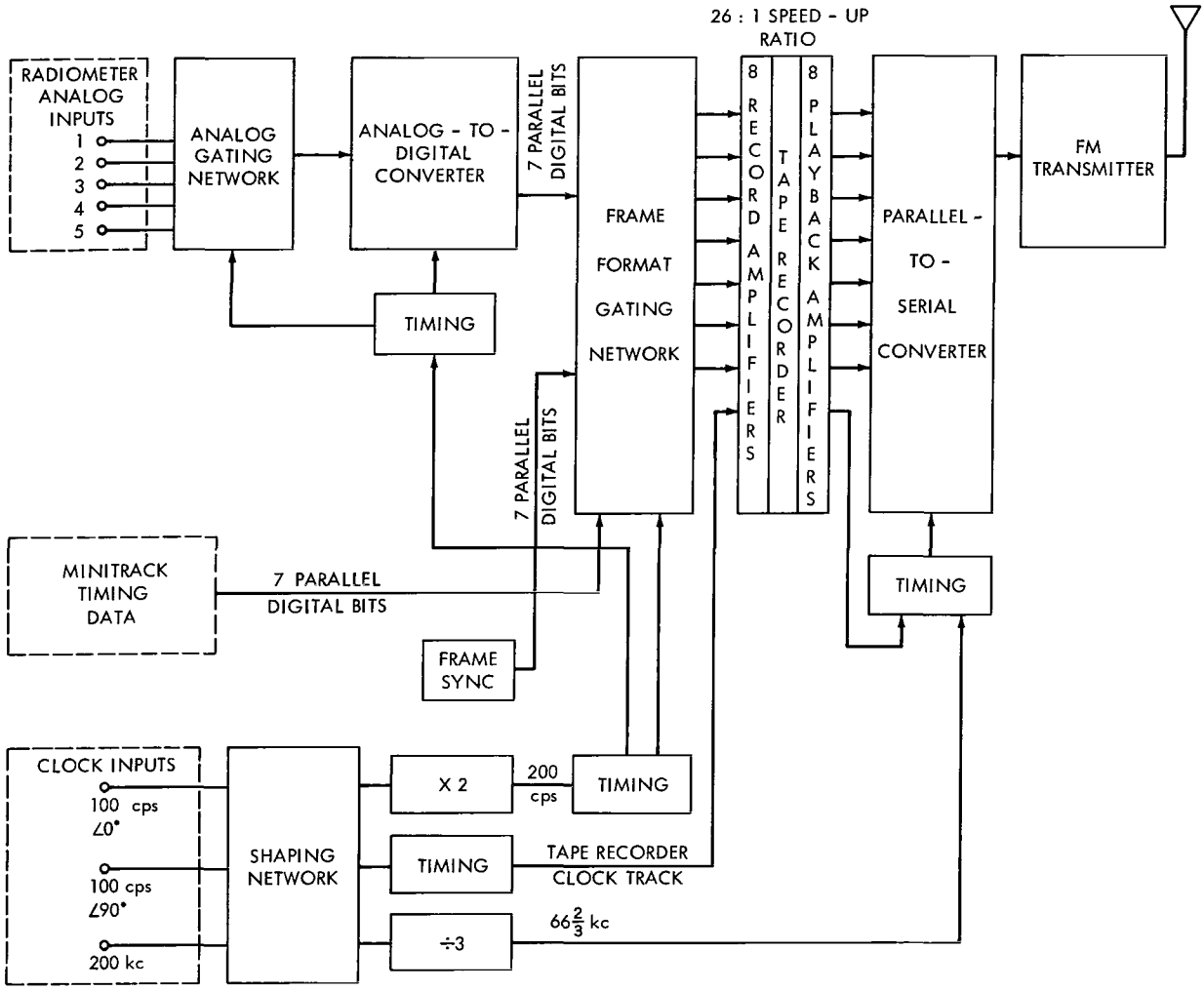


Figure 1—Nimbus MRIR-PCM system block diagram.

temperature range is ±25 mv (1/2 the least significant bit) plus ±15 mv (inaccuracy due to coder threshold variations). The output of the analog-to-digital converter consists of 7 bit parallel binary words, 0000000* representing the first level (0 volts) and 1111111* representing the 128th level (-6.4 volts).

In Nimbus the 7 bit parallel radiometer data is formatted with a 7 bit Minitrack timing data word and a 7 bit frame synchronization word to produce a 60 msec Nimbus main frame (Figure 3). Each 7 bit word is stored in parallel on 7 tracks of an 8 track tape recorder; on the 8th track of the tape, a square wave "clock" is recorded, out-of-phase with the data bits recorded on the 7 other tracks.

*In the Nimbus and Tiros MRIR system (except where indicated), "1" = ∇, true, or zero volts; "0" = +, false, or +3 volts.

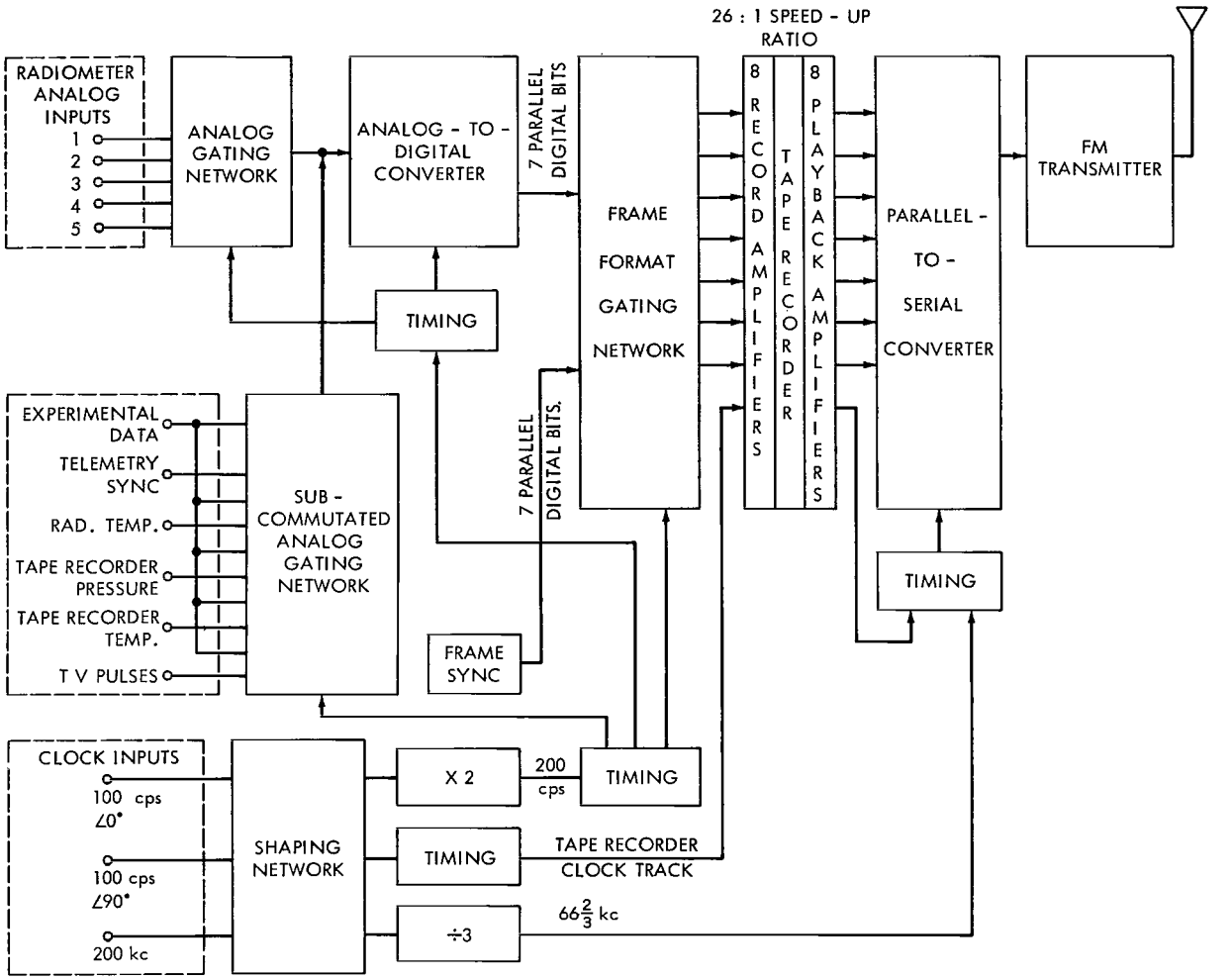


Figure 2—Tiros MRIR-PCM system block diagram.

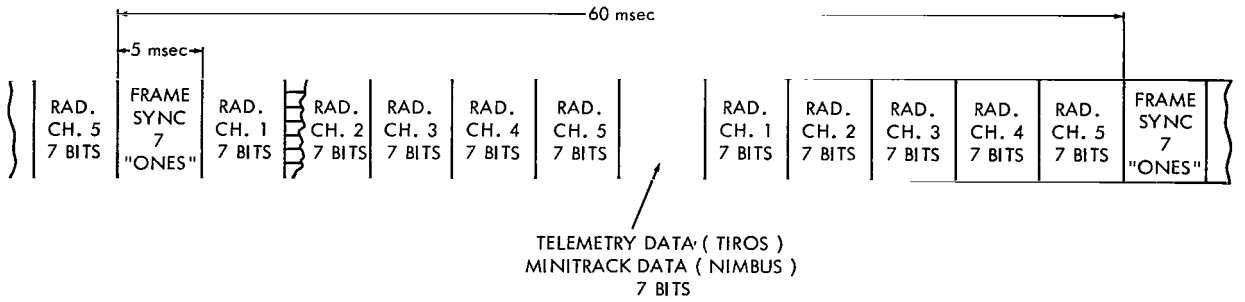


Figure 3—Nimbus and Tiros digital main frame format.

In Tiros, because of different satellite requirements, the subcommutated telemetry network replaces the Nimbus Minitrack circuitry. TV picture pulses, radiometer temperature, tape recorder pressure, tape recorder temperature, and subcommutated frame synchronization are sampled on this subcommutated channel. A super-subcommutated experiment which alternates with the above telemetry data is also available in this frame position.

The Tiros subcommutated data are sequentially passed to the analog-to-digital converter and coded, exactly as if they were radiometer data, to a 7 bit parallel binary equivalent. Sampling of the Tiros subcommutated data channel occurs in the same time position as the sampling of the Minitrack data occurs for Nimbus (Figure 3), and, as in Nimbus, the Tiros main frame length is 60 msec. The Tiros subcommutated frame length is 600 msec.

The digital data stored on the tape are played back into identical Numbus and Tiros logic systems at a 26:1 speed-up ratio. The recorded out-of-phase clock track is used to develop a pulse to "load" the other 7 parallel bit tracks into a shift-register parallel-to-serial converter. This register takes the 7 bit parallel word, adds a word synchronization bit, and serially shifts the data word into the modulation input of an FM transmitter. After a data word is shifted out of the parallel-to-serial converter, "1's" are transmitted until another load pulse presents the next 7 bit parallel data word to the converter. The injected "1's" compensate for, and are therefore independent of, tape recorder wow and flutter; thus, errors introduced by tape recorder speed variation are eliminated.

MICROELECTRONIC DESIGN

All microelectronic networks in the MRIR-PCM system, excluding the analog-to-digital converter and record and playback amplifiers, are Texas Instruments Series 51 Solid Circuits. This series of networks uses the RCTL (Resistor-Capacitor-Transistor-Logic) NOR/NAND configuration. RCTL logic is relatively insensitive to input noise and supply voltage variation. Although use is limited to relatively slow speeds (about 500 kc maximum), the RCTL Series 51 networks are well suited to the maximum MRIR clock rate of 200 kc. Module reliability was a prime factor in selecting networks; low network power drain and flat packaging, affording optimum heat disipation and packing density, were other important considerations. Schematic diagrams for each Series 51 solid circuit network are shown in Figure 4.

All gate inputs, and the reset, set, and preset inputs of the flip-flops are considered dc loads; the dc fan-out of each network – the number of parallel loads that can be driven from one series 51 output node – is shown in Figure 4. The ac loading occurs when any network drives the clock input of a flip-flop. An added input capacitance of 100 pf per clock pulse limits ac fan-out to 5.

Fan-in, the number of inputs that can be connected to a network gate, can be increased by connecting the output nodes of two gates while not connecting the supply voltage (V_{cc}) of one of the two gates.

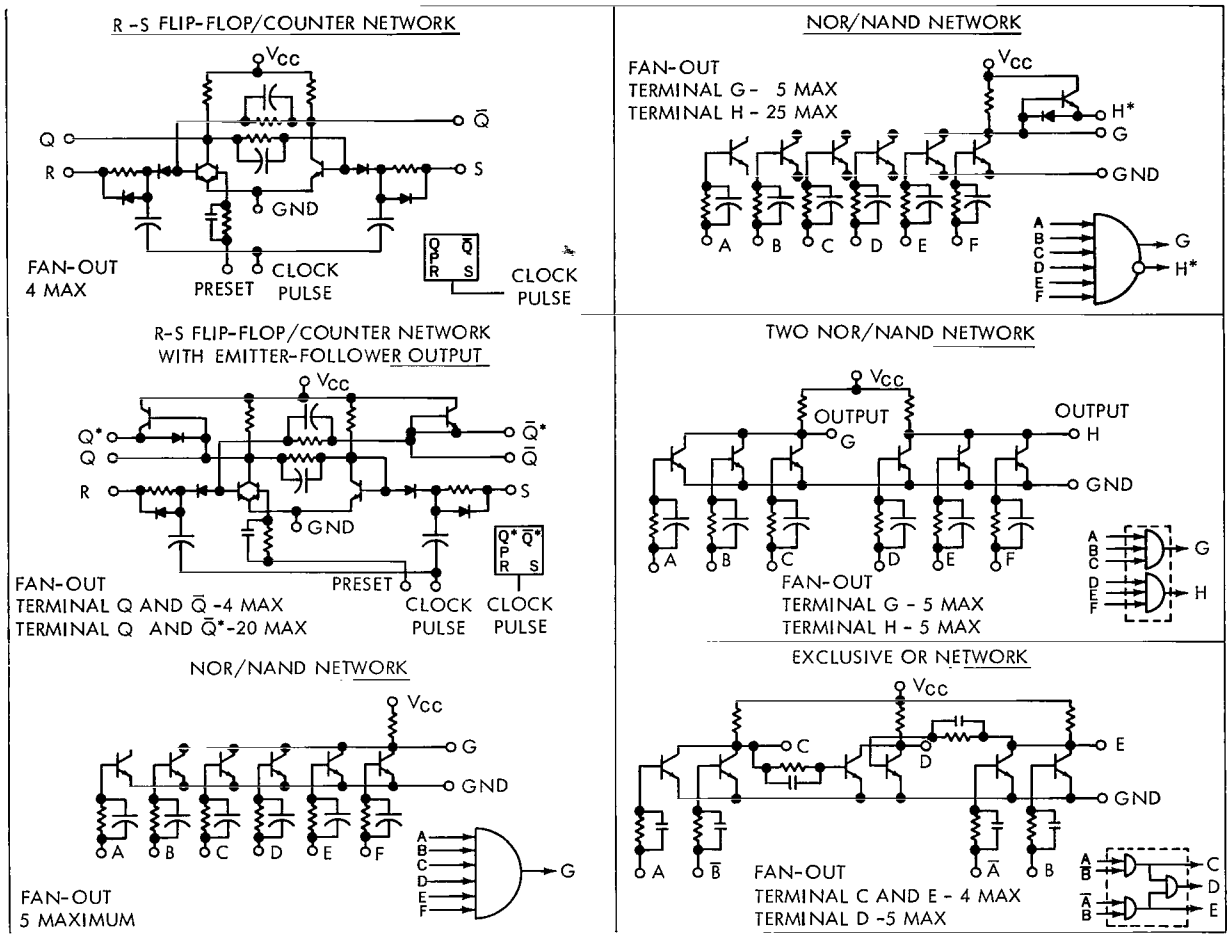
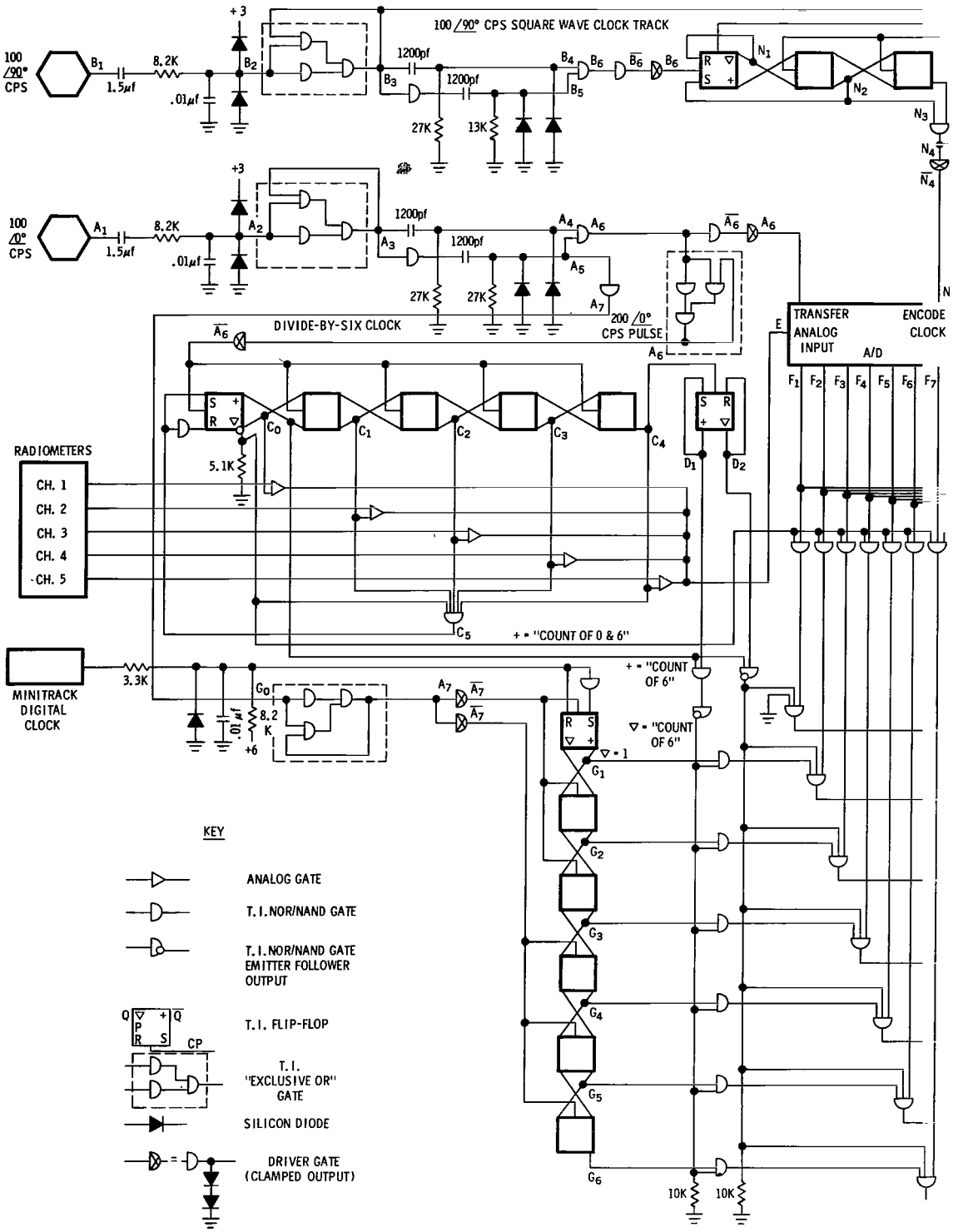


Figure 4—Series 51 solid circuit networks.

The flip-flop specifications call for a clock pulse not to exceed the steered input voltage. If this is not followed, the excess charge on the clock-input capacitor can cause false clocking. Since in asynchronous systems any gate may have to be used as a clock-pulse source, the logic design must insure that each clock pulse does not exceed the steered input voltage. In the MRIR system the clock-pulse voltages are kept lower than the steered input voltages by the clamping of the clock-pulse gate output with 2 silicon diodes. These diodes are clamped in the forward direction to approximately 1.2 volts.

A clock-pulse negative-going edge (fall time) of 200 to 500 nsec allows the greatest range of clock-pulse voltage with no effect on the shift register operation. A fast clock negative-going edge can be developed by connecting the "exclusive or" gate as a Schmitt trigger; "exclusive or" gates are used solely for this purpose in the MRIR system (Figures 5 and 6).

If emitter-follower outputs of the flip-flop networks are used, the emitter-follower output must be sufficiently loaded to fully turn on the gate. If a gate is not fully turned on, a threshold


100 /90° CPS SQUARE WAVE CLOCK TRACK
100 /90° CPS
100 /0° CPS
+3
1.5μf
8.2K
.01μf
1200pf
27K
13K
DIVIDE-BY-SIX CLOCK
200 /0° CPS PULSE
TRANSFER ANALOG INPUT
ENCODE CLOCK
A/D
RADIOMETERS
CH. 1
CH. 2
CH. 3
CH. 4
CH. 5
5.1K
+ = "COUNT OF 0 & 6"
+ = "COUNT OF 6"
▽ = "COUNT OF 6"
MINITRACK DIGITAL CLOCK
3.3K
8.2 K
+6
10K
KEY
ANALOG GATE
T.I. NOR/NAND GATE
T.I. NOR/NAND GATE EMITTER FOLLOWER OUTPUT
T.I. FLIP-FLOP
T.I. "EXCLUSIVE OR" GATE
SILICON DIODE
DRIVER GATE (CLAMPED OUTPUT)

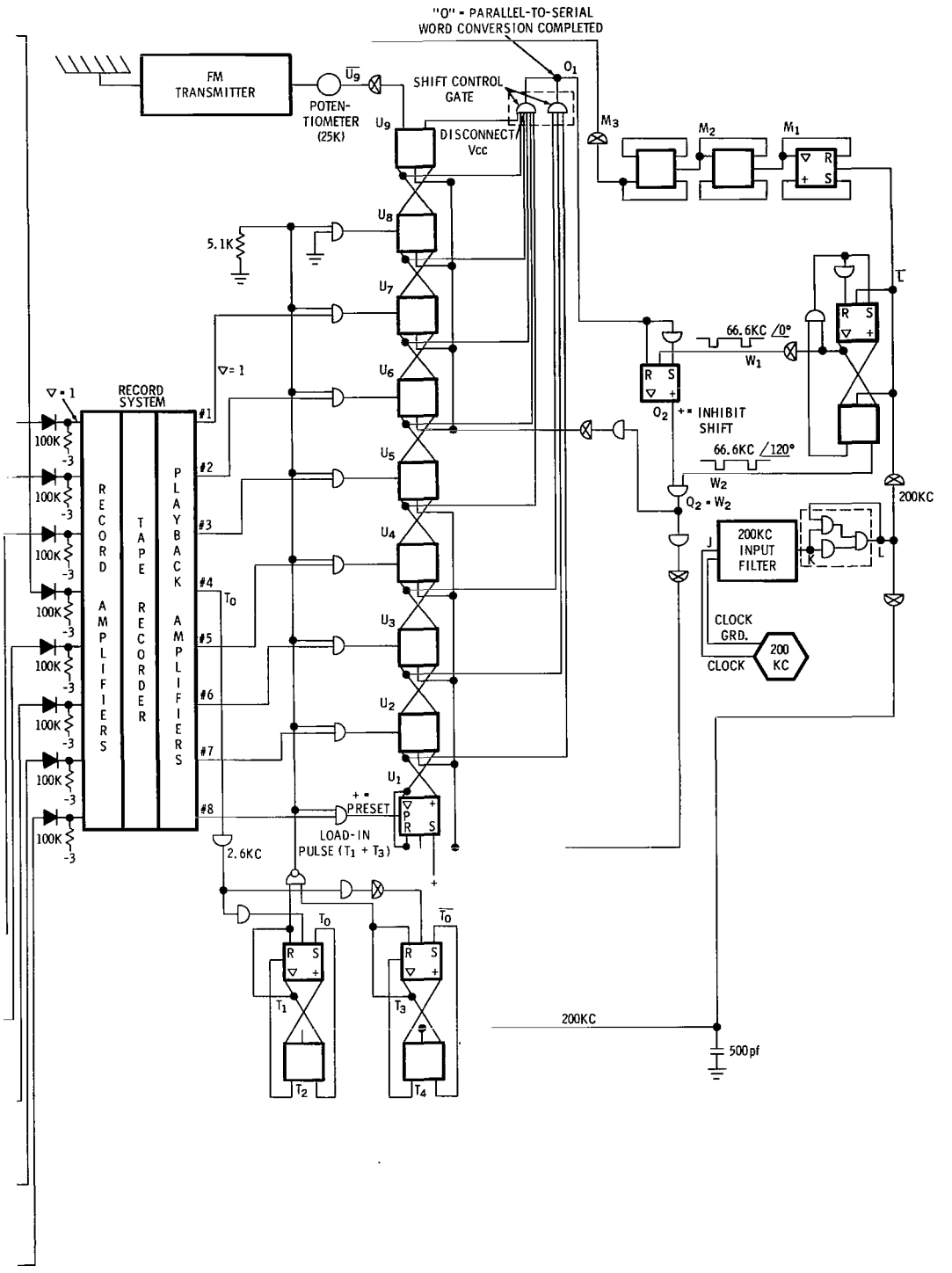
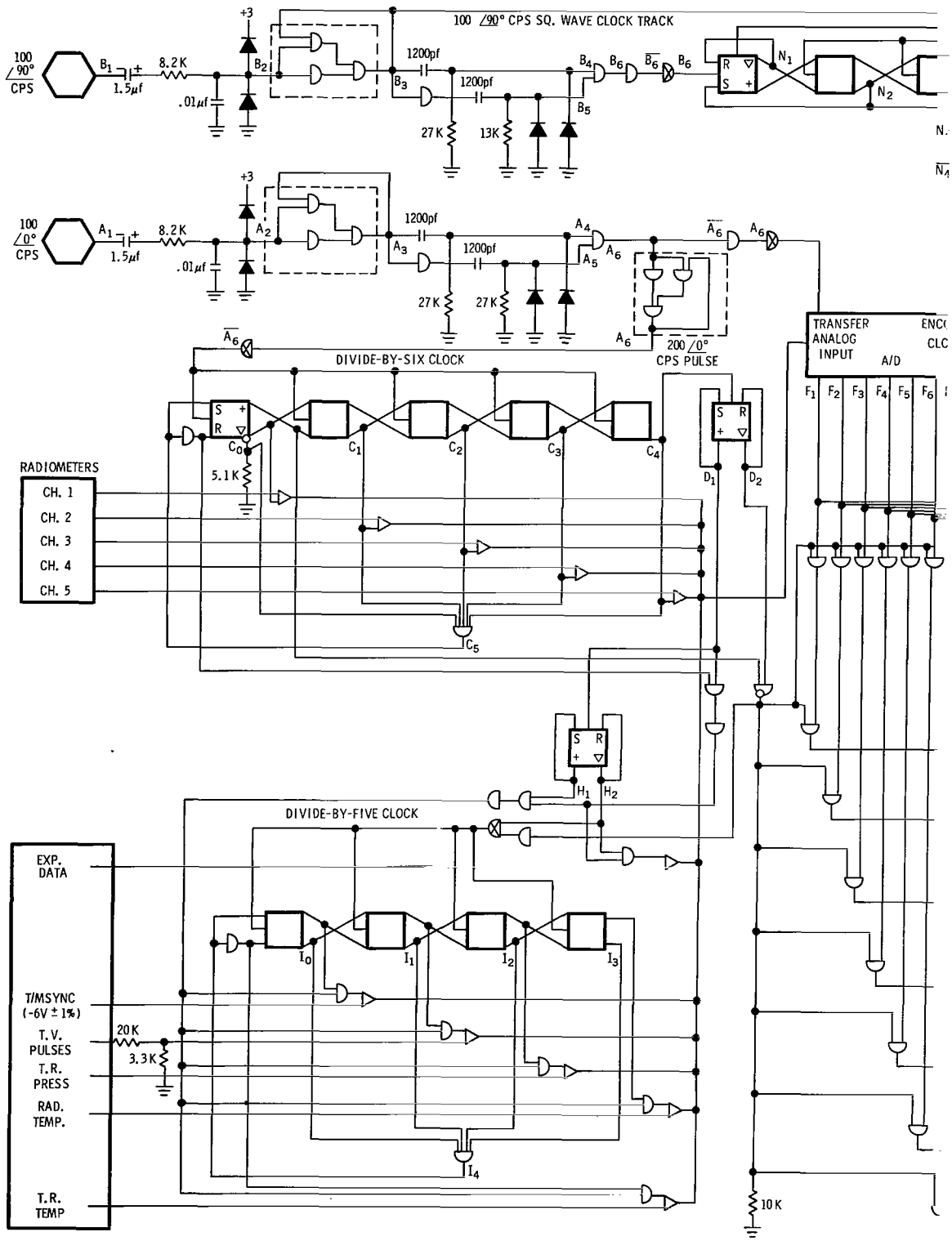


Figure 5—Nimbus MRIR logic circuitry.


100 ∠90° CPS SQ. WAVE CLOCK TRACK
100 ∠90° CPS
100 ∠0° CPS
+3
8.2K
1.5μf
.01μf
1200pf
27K
13K
200 ∠0° CPS PULSE
DIVIDE-BY-SIX CLOCK
DIVIDE-BY-FIVE CLOCK
RADIOMETERS
CH. 1
CH. 2
CH. 3
CH. 4
CH. 5
5.1K
TRANSFER ANALOG INPUT
A/D
EXP. DATA
T/MSYNC (-6V ± 1%)
T.V. PULSES
T.R. PRESS
RAD. TEMP.
T.R. TEMP
20K
3.3K
10K

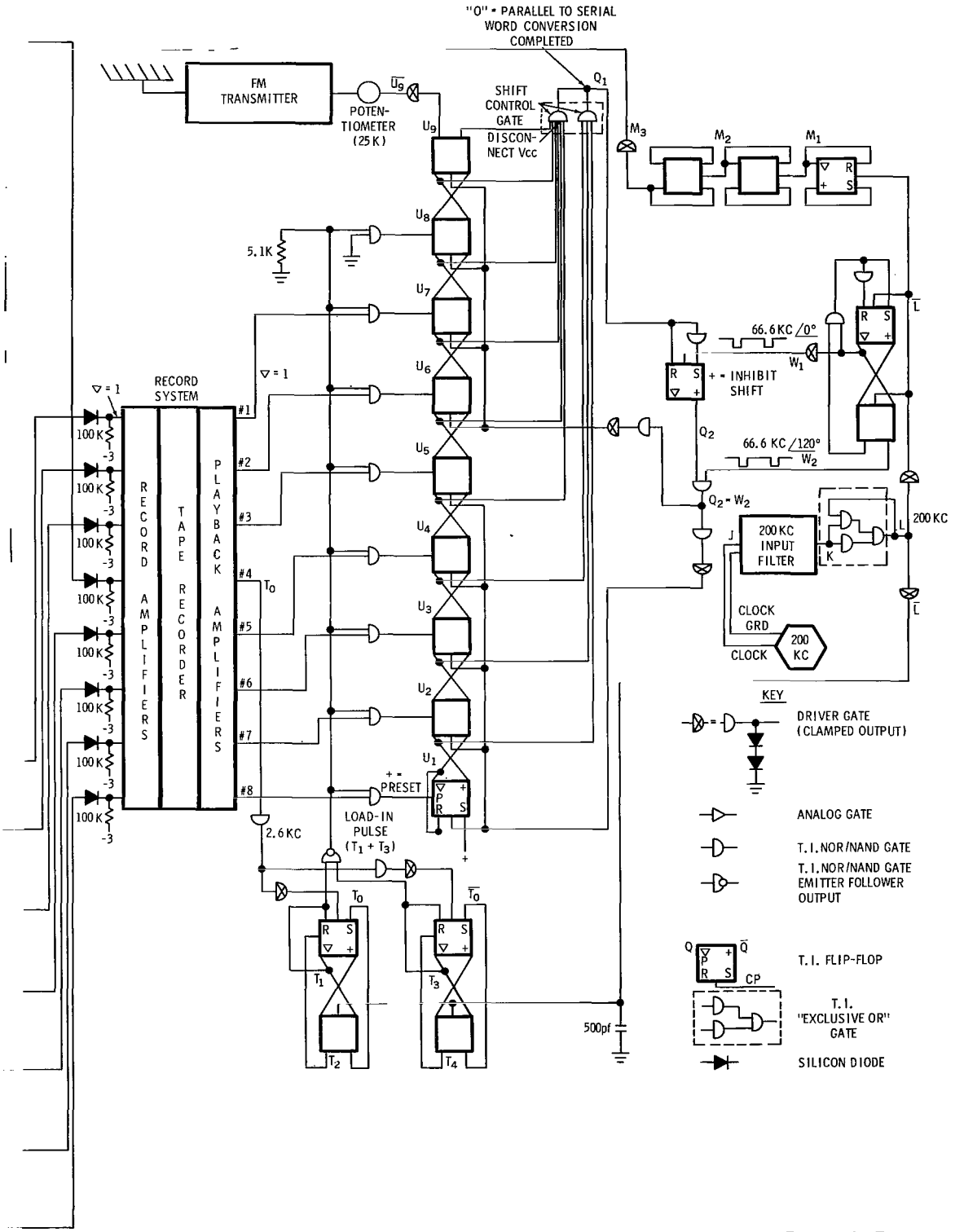


Figure 6—Tiros MRIR logic circuitry.

condition can develop in which a network cannot correctly distinguish between a "0" and a "1". To insure turn-on of lightly loaded emitter-follower outputs, an external resistor of 5K ohms or more, depending on the load, should be attached from the emitter-follower output to zero volts.

To minimize Series 51 susceptibility to noise, gate inputs and flip-flop presets which are not used should be grounded. Also, if possible, each clock-pulse shiftline should be designed to remain at a "false" level (+ volts) only at the shift time and to remain at "true" level (zero volts) at all other times.

MRIR-PCM LOGIC CIRCUITRY

General

Complete circuit diagrams of the Nimbus and Tiros MRIR-PCM logic systems are shown in Figures 5 and 6 respectively; timing charts correlated to circuit points of Figures 5 and 6 are included as separate diagrams. The numerous system clock-pulses generated from the 100 $\angle 0°$ cps and 100 $\angle 90°$ cps external sources are shown in Figure 7. The developed 200 $\angle 0°$ cps pulses ($\bar{A}_6$) are used to clock the main commutated divide-by-six ring-counter. Pulses from this counter are used to sequentially pass the analog meteorological data from each radiometer channel and to generate required frame format pulses. Each radiometer channel is sampled 33 times per second.

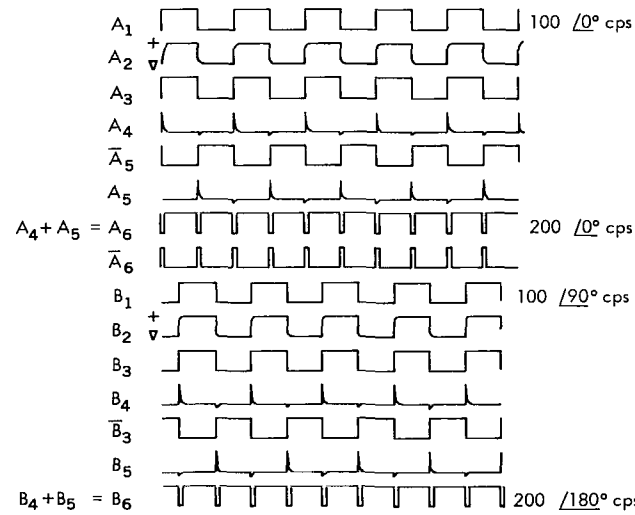


Figure 7—Timing chart for MRIR system clocks. (All timing pulses refer to points on Figures 5 and 6).

The passed analog radiometer data are sent to the system analog-to-digital converter, a low-power microelectronic unit engineered by CBS Laboratories. This converter encodes using the "successive approximation" or "bit-at-a-time" technique. Complete encoding occurs in 8 clock pulses or 320 μ sec. The developed system clock pulses necessary to operate the analog-to-digital converter are shown in Figure 8. The converter encode pulse ($\bar{N}_4$) has been developed so that each pulse negative-going edge (fall time) is synchronous with a 25 kc converter clock negative-going edge; encoding is initiated at this synchronous edge time, occuring approximately at the center of each analog sample. After complete encoding, the 7 bit parallel binary data is held until a transfer pulse is received at the analog-to-digital converter. This transfer pulse allows readout for 5 msec.

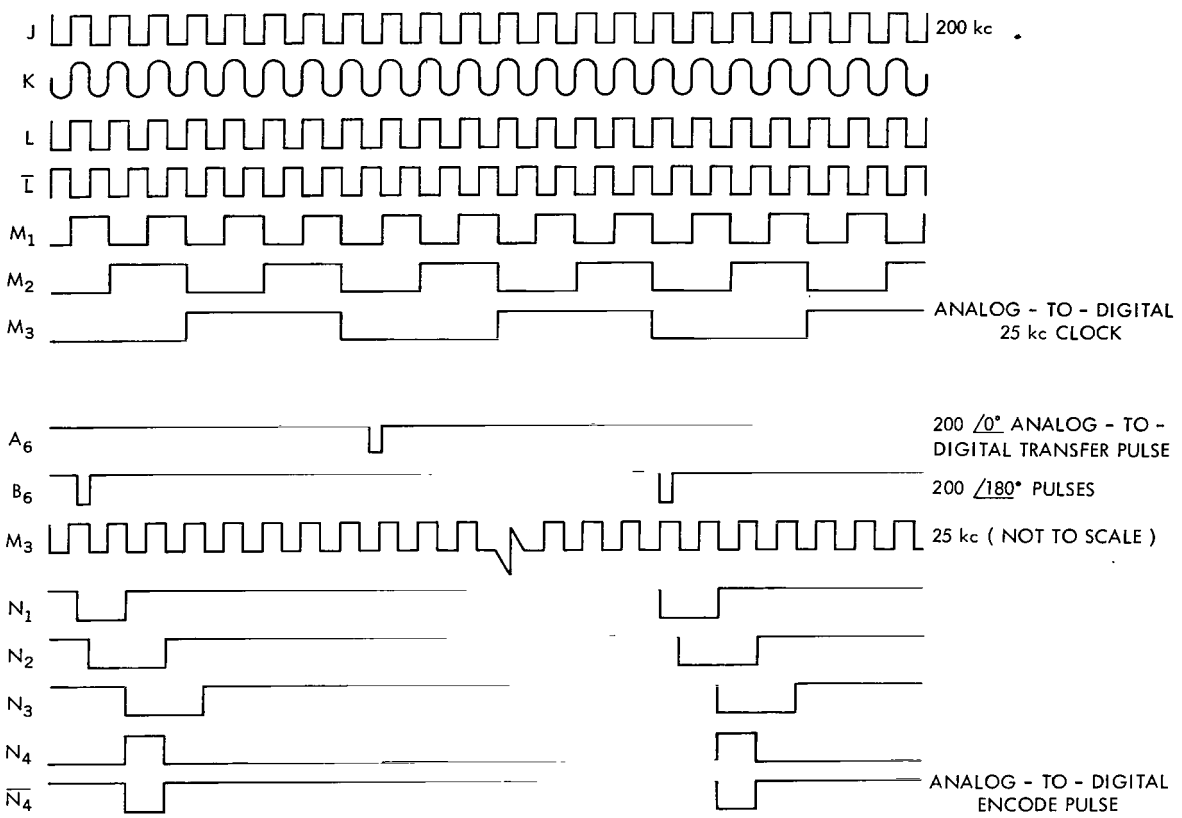


Figure 8—Developed MRIR analog-to-digital converter clocks. (All timing pulses refer to points on Figures 5 and 6; they vary between + and ∇ volts.)

Nimbus Record Logic

The complete timing chart for the record portion of the Nimbus logic system is shown in Figure 9. During each Nimbus 60 msec frame, two samples of each radiometer channel are digitized and sent to the record amplifiers to be recorded on tape. Each of the 7 parallel bit outputs of the analog-to-digital converter is sent through two control gates which function as inverters when the bits are passed. The control gates pass the converter data throughout all frame "counts" (relative frame time positions) except the counts of 0 and 6; at the counts of 0 and 6 the control gates inhibit the reading of the converter output and pass to the record amplifiers either frame synchronization (at the count of 0) or Minitrack data (at the count of 6). Thus, at a given count, control gates pass the converter data, the frame synchronization data, or the Minitrack data, inhibiting the other two from being read into the tape recorder system (Figure 9).

The Nimbus Minitrack clock generates real time in the form of an NRZ time code. The MRIR minitrack circuitry shapes the 100 msec-per-bit serial time-code, which is coherent with the 100 /90° cps external clock, and transfers the bits down a 6 bit shift register. During each frame count of 6, parallel read-in of the Minitrack shift-register takes place.

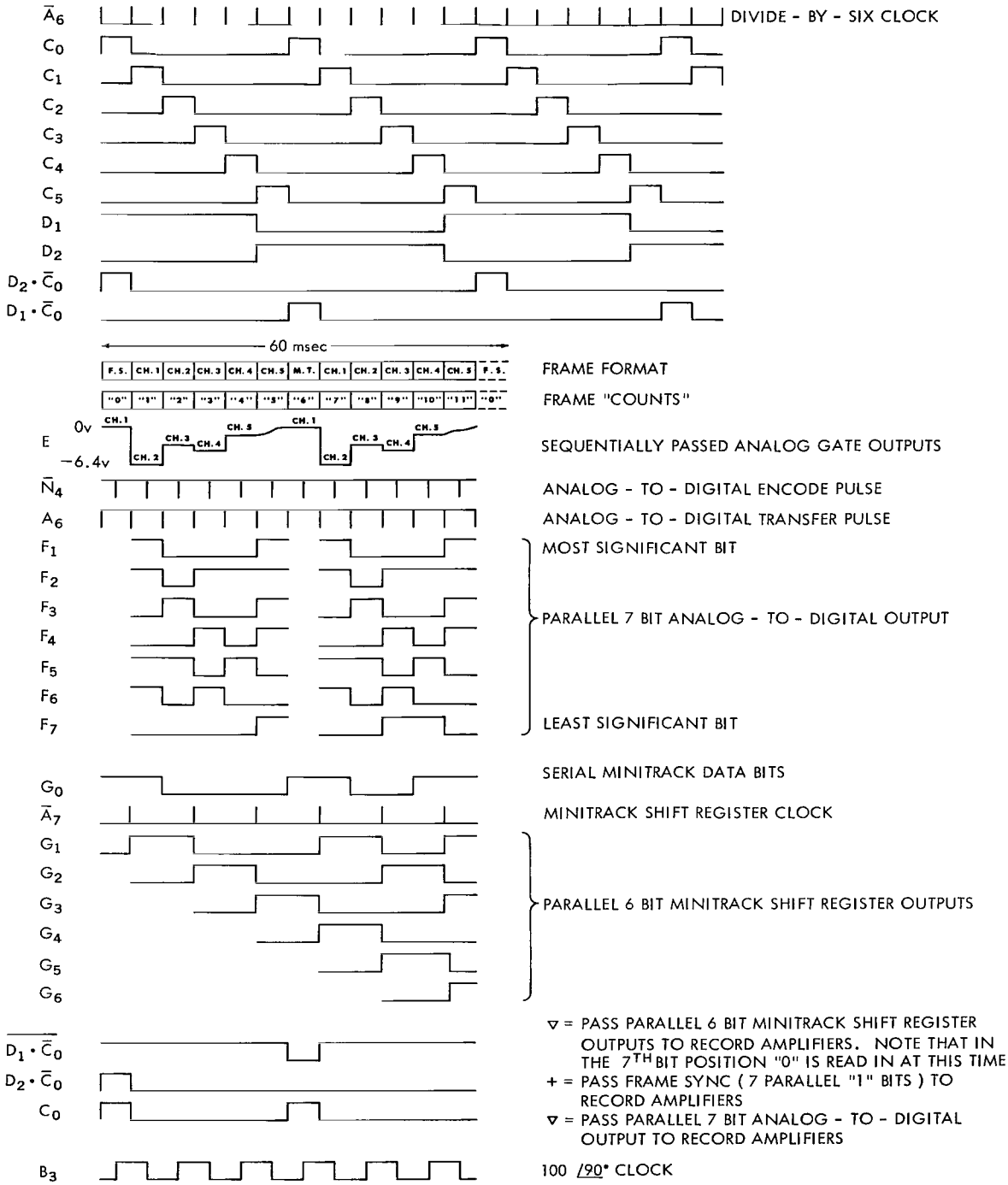


Figure 9—Timing chart for Nimbus record logic. (Unless otherwise specified all timing pulses vary between ▽ and + volts.)

The count of 0 pulse, which is sent to control gates and passed to the record system, generates the unique system code word 1111111; this word is used for frame synchronization. When the code of 1111111 appears at the parallel output of the analog-to-digital converter, the 6-input gate with inputs from each of the 6 most significant converter bit outputs, inverts the converter least significant bit to prevent a 1111111 code from being passed during converter read-in. To prevent the frame synchronization code from appearing during the 6 bit Minitrack read-in, an additional 7th bit position is continuously read in as a "0".

It should be noted that all data is "inverted" just before transmission; therefore, the frame synchronization word is actually transmitted as 0000000.

The diode-resistor network in front of each of the record amplifiers is used to transform the gate outputs to appropriate levels for the CBS microelectronic record amplifiers.

Tiros Record Logic

In the Tiros record logic system, the Nimbus Minitrack circuitry is replaced by a subcommutated telemetry network; complete timing for the Tiros record logic is shown in Figure 10. In the subcommutated network the TV picture pulse, radiometer temperature, tape recorder pressure, tape recorder temperature, and subcommutated frame synchronization, all in analog form, are each sampled once every 600 msec and passed to the analog-to-digital converter. Experimental data are alternated with each of the aforementioned datum and sampled once every 120 msec.

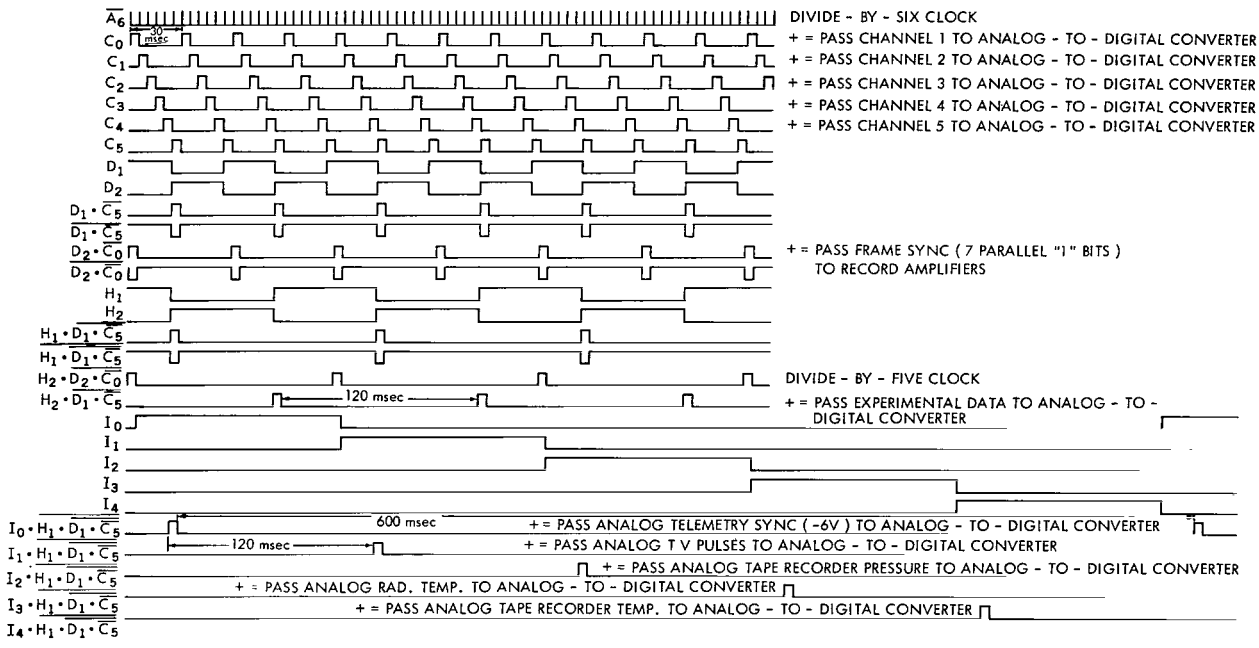


Figure 10—Timing chart for Tiros record logic. (All timing pulses refer to points on Figures 5 and 6; they vary between + and ▽ volts.)

When the Tiros frame data is decoded at the MRIR ground station, the subcommutated digital data is separated from the radiometer data, converted back to analog levels, and then channeled to a visual readout unit.

Nimbus and Tiros Playback Logic

Timing charts for the identical Nimbus and Tiros playback logic are shown in Figures 11 and 12. During playback the 7 bit parallel data words are stored or loaded into the parallel-to-serial converter by a pulse developed from each edge of the out-of-phase square wave clock track. Timing considerations, which will be subsequently discussed, make it necessary to load into the converter with a short duration pulse. A unique synchronizer frequency doubler was therefore designed to develop the load pulses (Figure 11). Depending on the noncoherency of the 3 kc and 200 kc clocks of this circuit, the load pulses vary from approximately 0.5 to 6 μsec in width: a resistor-capacitor frequency doubling network maintaining the same short pulse widths over temperature was found to be physically impractical to implement.

The load pulse is used not only to store the parallel bits (one data word) of playback data in the parallel-to-serial converter but also to logically force flip-flop output U_8 to the "0" state. This "0" is the system word synchronization bit used for ground station decommutation purposes.

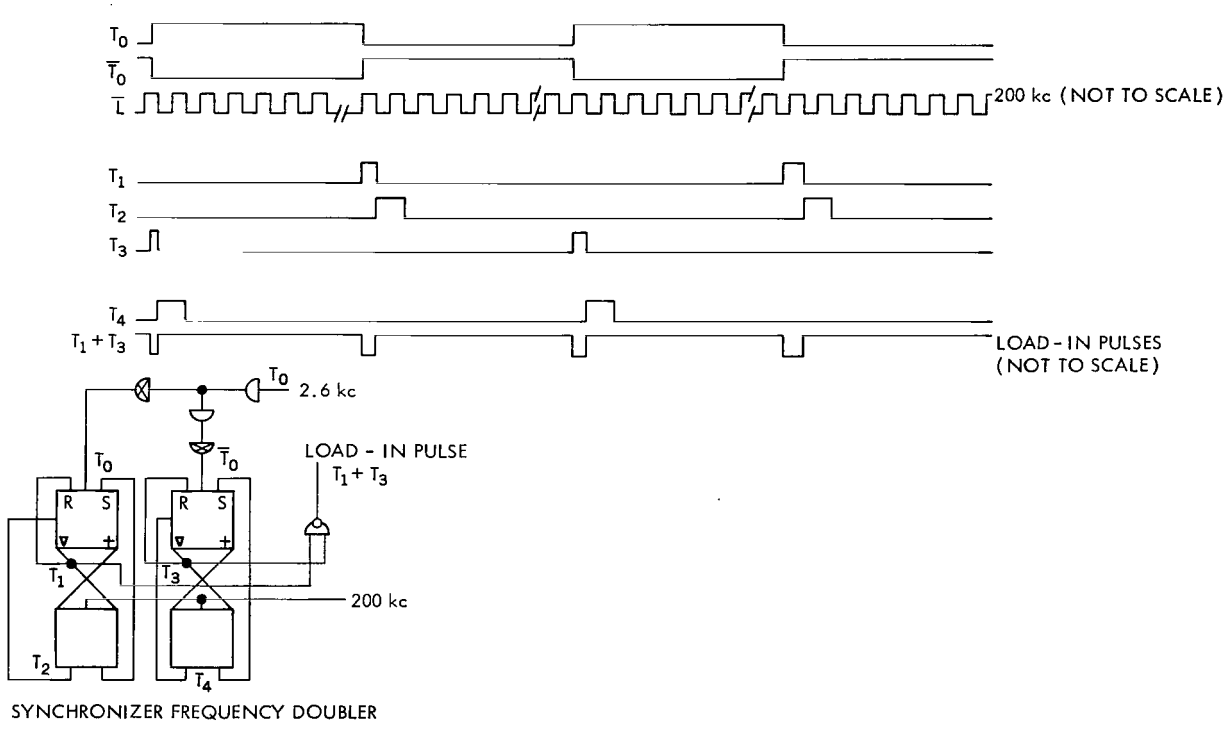


Figure 11—Timing chart for synchronizer-frequency doubler pulses. (All timing pulses refer to points on Figures 5 and 6; they vary between + and ∇ volts.)

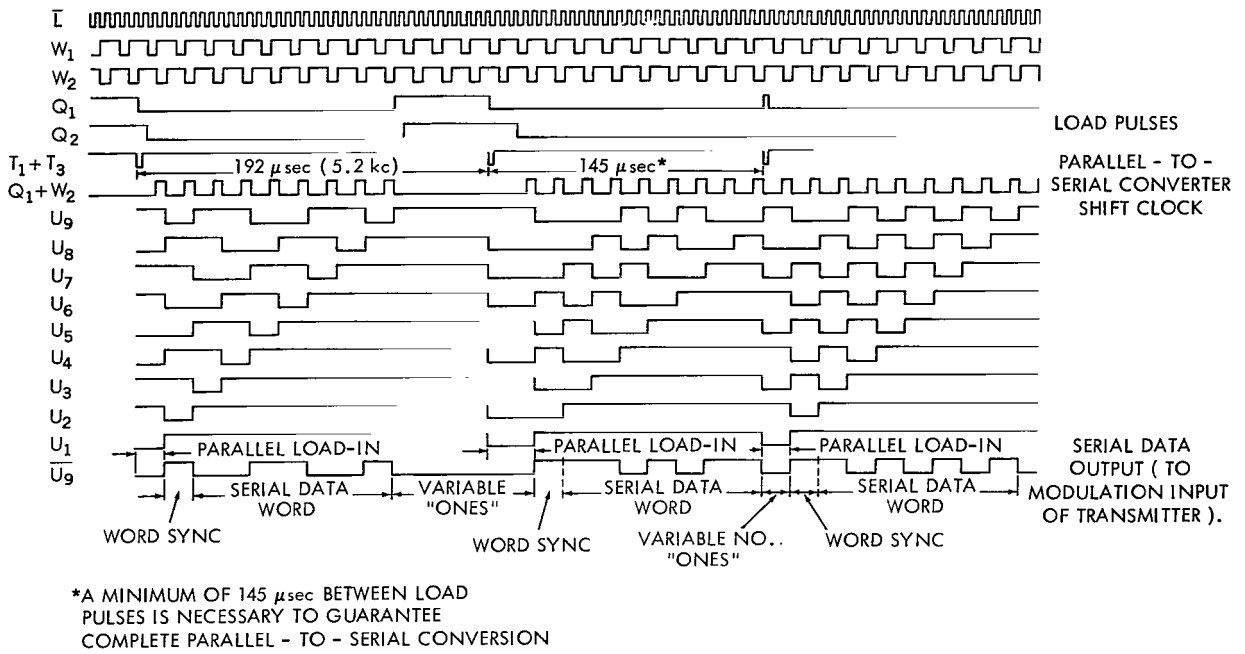


Figure 12—Timing chart for Nimbus and Tiros MRIR playback logic. (All timing pulses refer to points on Figures 5 and 6; they vary between + and ∇ volts.)

The word synchronization bit is also used to logically indicate that a parallel data word has been stored in the converter and is ready to be serially transmitted. The stored data bits are then shifted out of the parallel-to-serial converter. To prevent concurrent converter load-in and shifting, a 10 to 25 μsec delay is generated between load-in and the start of shifting. Shifting of the data bits continues until all "0's" remain at the "shift control gate" inputs. At this time the converter control circuitry inhibits further shifting, and shifting will not resume until another load pulse stores the next parallel data word. The load pulses would occur approximately 192 μsec apart if wow and flutter were not present in the tape recorder and if a perfect square wave clock were recorded. Tape recorder speed variations cause load pulses to be 192 $\pm$ 5 μsec apart. An additional 10 μsec variation between load pulses has been estimated to be due to the recorded square wave nonsymmetry. Since a maximum time of 145 μsec, representing 9 shift pulses plus control delay time is necessary to completely shift out any data word, at least 32 μsec remain after a data word is shifted out until the next data word is stored in the converter. In the time interval between serial data words, the converter output $\bar{U}_9$, which goes to the transmitter to be deviated $\pm$20 kc, is at the "1" state.

The parallel-to-serial converter load pulses are not coherent with the converter shift clock; therefore, if the last converter flip-flop with output U_9 were not provided, word sync "0" bits narrower than the bit rate could be initially transmitted after each load-in. This converter output flip-flop, which provides the transmitted bit rate, is independent of the load-in pulses and thus provides an unvarying transmission bit rate.

In the ground station, after frame sync is established, "1's" will be sensed until a word sync "0" bit occurs. After word sync is sensed, a counter channels the next 7 data bits, and "1's"

appear until the next word sync "0" bit. This cycle is continuously repeated throughout decommutation.

CONCLUDING REMARKS

The Nimbus and Tiros MRIR-PCM preprototype systems have been fabricated and tested (Figures 13, 14, and 15); prototype and flight model production has begun. The microelectronic circuitry employed in the MRIR-PCM systems has proven to be readily adaptable and ideally suited to present and future aerospace requirements.

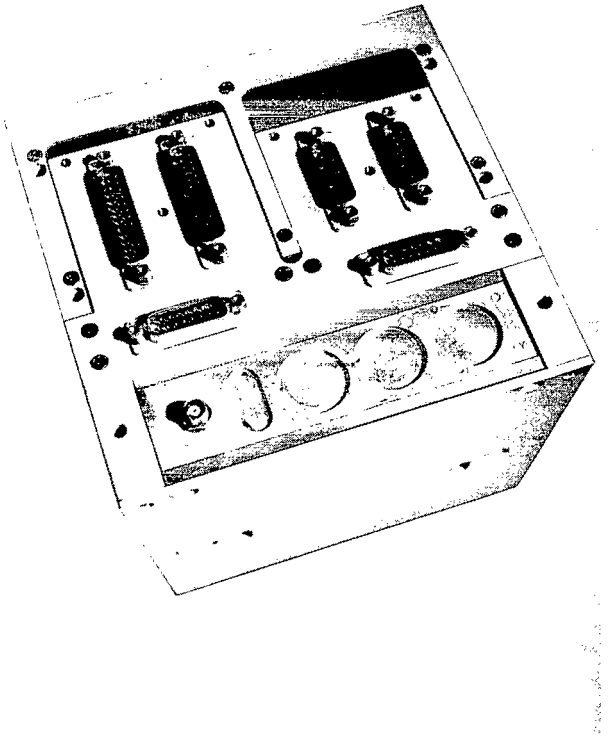


Figure 13—MRIR preprototype.

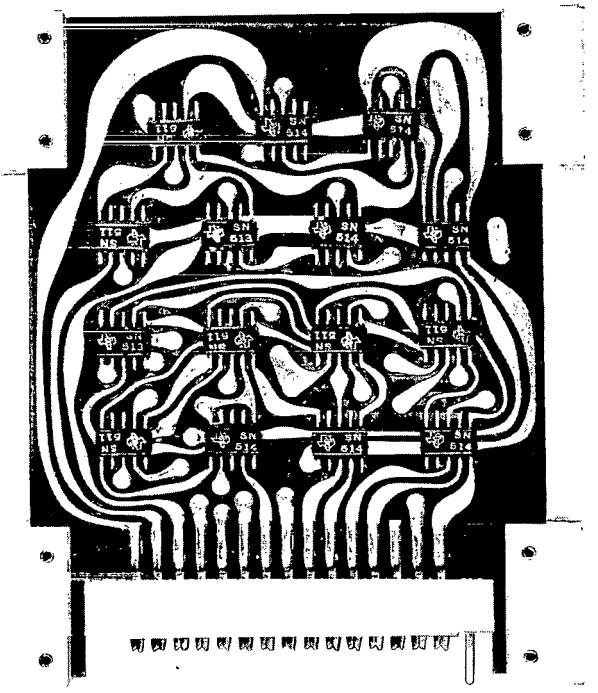


Figure 14—MRIR preprototype logic module.

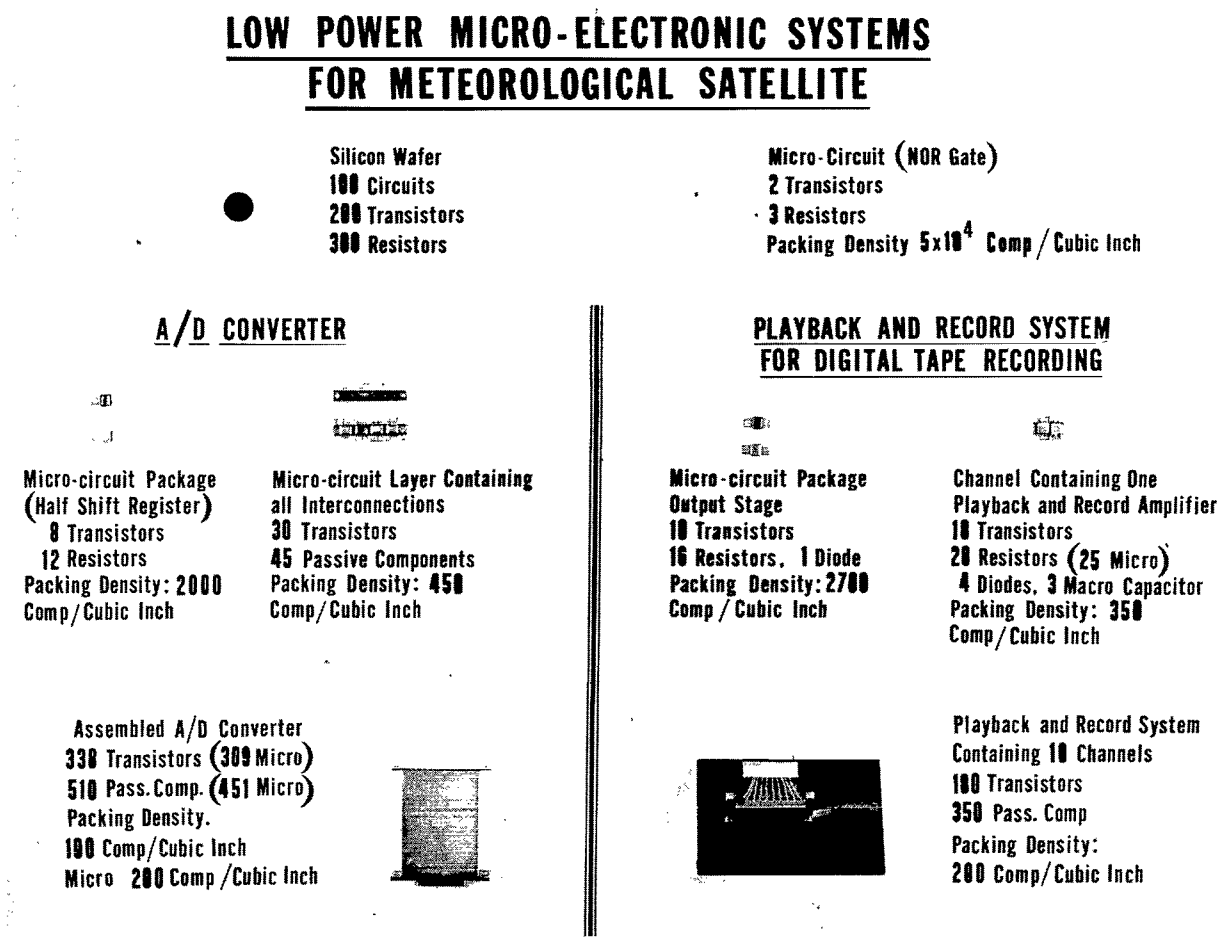


Figure 15—MRIR analog-to-digital converter and record system microelectronics.

ACKNOWLEDGMENTS

The author would like to express his appreciation to Mrs. Marjorie Townsend, Mr. John Lesko, and Mr. Marvin Maxwell for their assistance in the preparation of the MRIR logic design.

(Manuscript received September 3, 1963)

NASA-Langley, 1964 G-504

2/7/85

"The aeronautical and space activities of the United States shall be conducted so as to contribute . . . to the expansion of human knowledge of phenomena in the atmosphere and space. The Administration shall provide for the widest practicable and appropriate dissemination of information concerning its activities and the results thereof."

—NATIONAL AERONAUTICS AND SPACE ACT OF 1958

NASA SCIENTIFIC AND TECHNICAL PUBLICATIONS

TECHNICAL REPORTS: Scientific and technical information considered important, complete, and a lasting contribution to existing knowledge.

TECHNICAL NOTES: Information less broad in scope but nevertheless of importance as a contribution to existing knowledge.

TECHNICAL MEMORANDUMS: Information receiving limited distribution because of preliminary data, security classification, or other reasons.

CONTRACTOR REPORTS: Technical information generated in connection with a NASA contract or grant and released under NASA auspices.

TECHNICAL TRANSLATIONS: Information published in a foreign language considered to merit NASA distribution in English.

TECHNICAL REPRINTS: Information derived from NASA activities and initially published in the form of journal articles.

SPECIAL PUBLICATIONS: Information derived from or of value to NASA activities but not necessarily reporting the results of individual NASA-programmed scientific efforts. Publications include conference proceedings, monographs, data compilations, handbooks, sourcebooks, and special bibliographies.

Details on the availability of these publications may be obtained from:

SCIENTIFIC AND TECHNICAL INFORMATION DIVISION

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Washington, D.C. 20546