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FOR
RESEARCH AND DEVELOPMENT STUDY
ON
DC TO DC CONVERTER
ENGINEERED MAGNETICS MODEL EMCR131
CONTRACT NO. NAS5-3470
REPORT NO. 1419

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SUMMARY AND CONCLUSIONS

This report covers the third phase of design of a highly efficient DC-DC converter consisting of four regulated, isolated, and short circuit protected outputs. The second quarterly report discussed the problems that were encountered in connection with the regulating loop that provides coarse voltage regulation to the output series regulators. In particular, loop stability and ripple problems were discussed.

This third period of study was expended to optimize the design of the regulation control loop and series regulator circuits. To accomplish this, it was found necessary to compromise and obtain less than the desired efficiency due to the deviation of the regulating loop from its theoretical performance. In analyzing this problem, an alternate approach (described later in the report) was designed offering promise to meet the primary program goals. Initial tests show achievement of these goals with the possible exception of output ripple. To reduce the output ripple, further study must include output filter designs that would not adversely affect static or dynamic load regulation.

It is felt that, with sufficient time to study these problems, the alternate approach can be developed to meet all required program goals.

I. INTRODUCTION

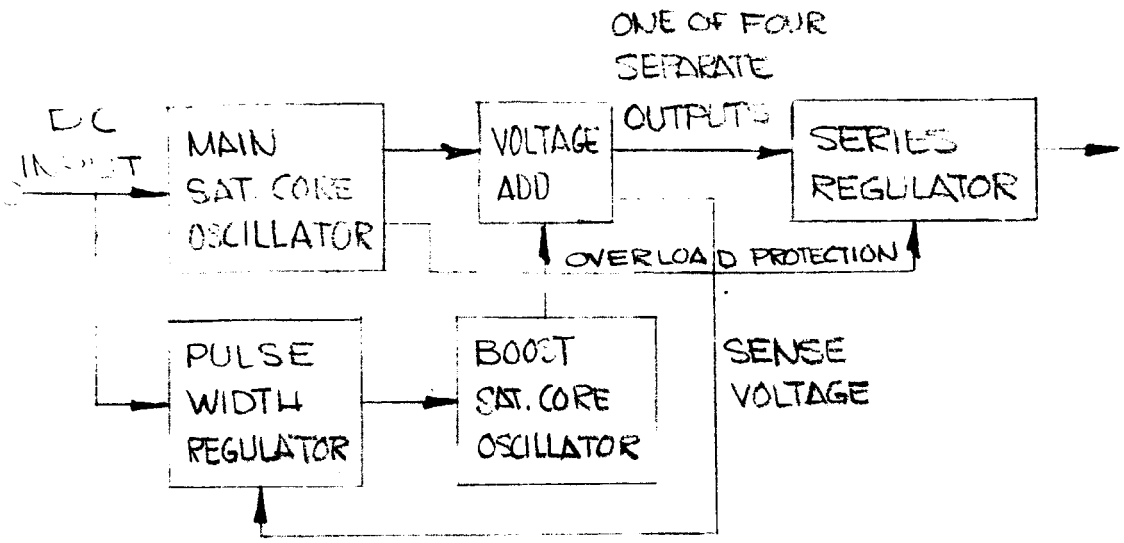
This report describes the third quarterly period of effort to develop a DC to DC converter of very high efficiency.

During this third phase of work, considerable effort was expended on optimization of the regulation control loop and series regulator circuits. In the course of optimizing these circuits, it was necessary to design a new approach to increase the efficiency. An approach was developed to circumvent the use of four series regulators, and is described in Section II of this report. The new approach is to include four pulse width regulators one for each output, and to preclude the use of four series regulators. Section II describes in detail the problems effecting the new approach.

Those areas which will deviate from the design specification by using the four pulse width regulators innovation are those which usually require series regulators; specifically load transient response, output spikes, and output impedance. Output voltage transient due to load changes will probably be about ±1% as opposed to the design goal of ±1/2%. The transient recovery time of 10 MS, however, can be met without series regulators. Output spikes may be on the order of 60 MV p-p instead of the desired 10 MV p-p. Output impedance will not suffer appreciably. More capacitance will be needed on the output. This is due to the fact that the pulse width regulator has a lower frequency cutoff point than a series regulator. Consequently, the output capacitor will have to provide a low impedance down to a lower frequency than it would have to do in a series regulator.

II. DISCUSSION

A. The basic "block diagram" approach that was studied up to this time was the following.



As the input voltage changes, the output of the pulse width regulator changes in the opposite direction so as to maintain the sum of the output of the two saturable core oscillators at approximately a constant level. As the input voltage approaches its maximum value of 20 VDC, the output of the pulse width regulator approaches zero. In the beginning phases of work on this circuit it was anticipated that the pulse width regulator could be made to operate satisfactorily down to zero output voltage. At maximum input voltage, the pulse width regulator and boost oscillator would be completely off resulting in the desired maximum efficiency at maximum input voltage.

There are two main problems associated with this approach. One is control loop stability and the other is ripple.

The problem of loop stability resulting from control loop conflicting requirements, proved to be much more complex than at first anticipated. For adequate dynamic load response, the frequency response of the control loop must be fast and, at the same time, proper circuit operation must avoid false triggering

problems. The sense point (a full wave rectified square wave derived from additive windings on each of the two oscillator transformers) contains the negative transients that are common to all rectified, non-filtered outputs of saturable core oscillators. These negative transients are about four volts in magnitude at the 12 volts sense point. A negative transient of only 100 MV will trigger the detection-to-pulse circuit* in the pulse width regulator. Thus the sense point must be filtered to prevent the pulse width regulator switching circuitry from locking into the oscillator frequency. Since the detection-to-pulse circuit has a high impedance input, the filtering at this point must be quite substantial. The difficulty that was encountered in attempting to solve this problem was that the amount of filtering that was needed to prevent false triggering lowered the frequency response of the control loop to the point that the output ripple of the pulse width regulator rose to intolerable levels. The problem was further complicated by the non-magnetic requirement of the circuitry. False triggering of the pulse width regulator was caused by electromagnetic interference radiation as well as conducted noise on the sense leads. This type of false triggering was appreciably reduced by enclosing the low level circuitry with mu-metal. However, magnetic shielding is not acceptable due to the non-magnetic requirement of the circuit.

* See previous quarterly report for discussion of this circuit.

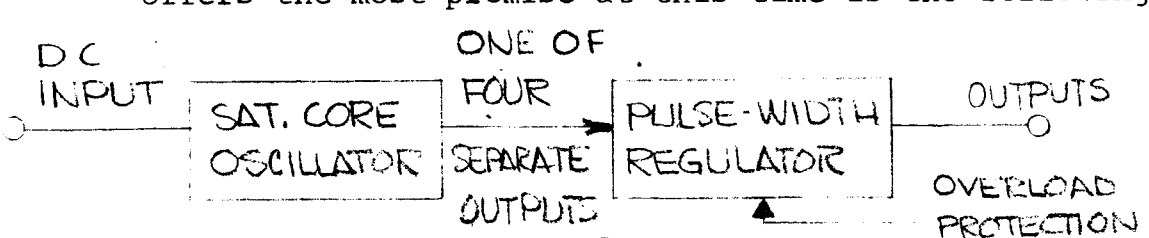
The current driven boost oscillator was operated satisfactorily down to zero volts input from a separate dc voltage supply during the previous quarter before being integrated into the entire system. The problem with ripple arises from the fact that the sense voltage remains at 12 volts while the output voltage from the pulse width regulator changes from 11.5 volts to zero volts with changes in input voltage. The peak-to-peak value of the ripple at the output remains constant. Thus as the output from the pulse width regulator decreases, the percentage ripple from the pulse width regulator increases.

The unsatisfactory ripple performance was considerably aggravated by the control loop stability problem such that the system ripple could not be reduced to a tolerable level. When the dc input voltage to the boost oscillator is about one volt, and this voltage contains 50 percent ripple, then the output ripple from the two oscillators on the 12 volt outputs is between 0.7 and 1.0 volt p-p. This is a prohibitive amount of ripple and drops the efficiency to about 80%, an unacceptably low value. Study of the detail loop requirements indicates that the transformer coupling necessary for isolation introduces intolerable high frequency phase shifts.

B. When it became apparent that the efficiency goal would not be met with the approach described in paragraph A, appraisal was made of the complete circuit. Certain aspects of the above approach are compatable with the efficiency requirement and should be retained. Specifically, the desirable aspects of the circuit are the current-driven oscillators and the pulse width regulator circuit. The current-driven oscillators are the most efficient type of saturable core oscillators. They also generate much smaller current spikes on the input which reduces any R.F.I. problem. The pulse width regulator, by itself, is the most efficient method of voltage regulation. Losses in the pulse width regulator are almost neglibible except for the unavoidable losses in the commutating diode. There are two undesirable aspects of the circuit which do not appear to be compatable with the efficiency requirement. These are the complexity and instability of the input voltage regulation control loop and the use of series regulators on the output. The instability of the control loop results in an unacceptable level of

ripple ahead of the series regulators. The Honeywell transistors that were going to be used for the series regulators can operate effectively with only 0.3 volts across them for one amp load currents. The satisfactory operation of the overall circuit was dependent on maintaining the voltage regulation ahead of the series regulators to about a two percent total deviation from nominal so that the low operating voltage of these transistors could be used to advantage. The dc regulation at these points was regulated to this accuracy. However, the ripple was of such a magnitude and frequency that it could not be filtered out by a reasonable amount of capacitance. Therefore the ripple had to be removed by the series regulators. This necessitated about 1.3 volts across the series regulators on the 12 volt outputs and a corresponding percentage drop across the series regulators in the 20 and 50 volt outputs. The series regulators have the added disadvantage of needing a separate bias supply for the series transistor to operate them efficiently. If this bias supply is not used, the base current for the series transistor must be supplied across the entire input voltage to the series regulator. Assuming for one amp load that 40 MA of base drive is needed, then the loss on one 12 volt output due to base drive would be approximately (12)(.04) = .48 watts or 4%.

C. On reappraising the circuit, a slightly different approach appears more desirable. This alternate approach became attractive when the pulse width regulator was improved as a result of detailed studies of the loop stability problem. The approach that offers the most promise at this time is the following.



This approach completely eliminates one series link of voltage regulation using a pulse width regulator on each of the four outputs for both input voltage and load regulation. The stability of the switching circuit of the pulse width regulator is very good since the voltage sense point is the output and this point is highly filtered and not susceptible to electromagnetic interference. This is due to the fact that the voltage sense point is of a low impedance. The primary switching action of the pulse width regulator is also operating under much better circumstances in this circuit. For example, on the 12 volt line, assuming for the moment there is no drop across the switching transistors, the voltage input to the pulse width regulator varies from 12 to 20 volts as the input voltage varies from 12 to 20 volts while the output voltage remains at 12 volts. The ratio of output to input voltage thus varies only from one to 0.6. In the original circuit this ratio varied from one to zero. Since the percentage of time that the series switch is closed equals $\frac{E_{out}}{E_{in}}$, the "on time" of the switch theoretically had to go to zero. Since no turn off circuit could be used, as described in the last report, the storage time limited the minimum time that the switch could be "on" once it was turned "on." This, plus the response time of the control, limited the minimum "on time" to at least 3μsec. This problem was the main reason the pulse width regulator would not work down to zero output voltage. In the alternate approach, which now appears to be most desirable, the output voltage is constant. This allows for a simple and efficient turnoff circuit to be used for the switching transistor as explained in the second quarterly report.

D. A slight modification will have to be made to the saturable core oscillator if the approach described

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D. A slight modification will have to be made to the saturable core oscillator if the approach described

in paragraph C is to be used. A current driven oscillator needs to be continuously loaded to function properly. The pulse width regulator does not present a constant load to the oscillator as the series switch is alternately opening and closing. To keep the oscillator functioning properly when the switch is open, a small amount of conventional type voltage feedback must be added to the base drive circuit. This drive power need only be sufficient to drive the switching transistors to the point of handling the no-load current drain. This no-load loss is already negligible so that the added power consumed in this additional drive power will not affect the efficiency. The fact that the load current in each of the four secondary windings on the oscillator transformer is a pulse, rather than a continuous current, will necessitate a new type of current sensing. The average current in the secondary windings is not equal to the load current. It is a function of both input voltage and load current. A unique type of current limiting circuit will have to be developed for this type of circuit to preserve the potential high efficiency.

III. PROPOSED PROGRAM FOR NEXT REPORTING PERIOD

The new pulse width regulator circuit will be optimized for efficiency, voltage regulation, and minimum ripple. A new circuit will be made to provide short circuit protection. The saturable core oscillator will be modified so as to operate under no-load conditions.