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APPLICATION OF INTEGRATED CIRCUITS TO TELEMETRY SYSTEMS

by J. Michael Balderston

Goddard Space Flight Center
Greenbelt, Md.

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SUMMARY

In June 1962, a continuing study of integrated circuits as applied to scientific satellite telemetry systems was initiated at Goddard Space Flight Center. This paper describes some results of investigations of standard commercially available Texas Instruments Series 51 Solid Circuits. The possibility of altering circuit functions by the addition of external components was verified. Three telemetry encoder subsystems were designed using the solid circuits. Conclusions and recommendations for future studies are presented.

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APPLICATION OF INTEGRATED CIRCUITS TO TELEMETRY SYSTEMS*

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INTRODUCTION

In recent years the continuing search for electronic circuitry of smaller size and increased reliability has brought about the field known as molecular electronics, or integrated circuitry. In one phase of this field, individual components are replaced by areas within a solid state material; these areas are generally produced by means of a planar diffusion technique that is a recent refinement of transistor technology. Interconnections are made by means of deposited leads. Thus, a single block of semiconductor material may replace a complete circuit such as a flip-flop, an IF stage, or an amplifier. Because of tolerance problems and various other difficulties, most commercially available integrated circuits have been digital (flip-flops, gates, inverters, etc.); however, several companies are investigating audio and RF circuit applications.

The particular integrated circuits used in the evaluation discussed here were the Texas Instruments (TI), Inc., "Solid Circuits." When the investigations were started (June 1962), the only circuits available in quantity were these and the Fairchild semiconductor "Micrologic" circuits; the TI circuits were chosen on the basis of power dissipation (2 mw versus 15 mw per circuit) and package configuration (the TI package lends itself more easily to welded, cordwood construction).

The circuits investigated were: a flip-flop (Type 510 or 511) which, by different external connections, could be used as a counter-divider, a shift register, or a set-reset stage; a six-input NOR gate (Type 512 or 513); a circuit containing two three-input NOR gates (Type 514); and an Exclusive-Or circuit (Type 515).

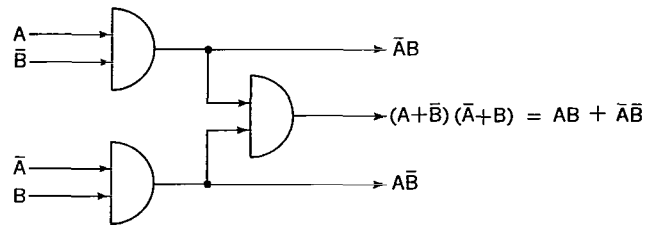
TIMING CIRCUITS

Astable Multivibrator

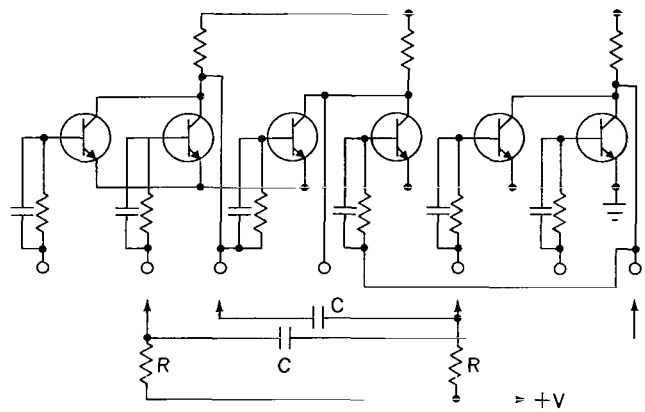
In any telemetry system involving time-division multiplexing, a timing source is required. For purposes of miniaturization and for compatibility with other parts of a telemetry system realized with integrated circuits, the astable multivibrator shown in Figure 1 was built. It employs one Type 515 Solid Circuit, two capacitors (C), and two resistors (R). Note that by providing the appropriate signals to the unused gate inputs, the astable multivibrator could be synchronized by an external reference, or gated to run or stop. Selection of R and C gives different values of frequency. It was

*This work has also been reported at the NASA Microelectronics Symposium, Langley Research Center, July 17, 1963.

found that C had to be greater than 0.002μf for proper operation; R could be varied from 5 K to open. For R = 120 K and C = 0.01 μf, the output frequency was approximately 800 cps at room temperature and with a 3 volt supply. The temperature stability was poor, about 0.1 percent per °C; this was attributed to the fact that the internal base resistors were of semiconductor material.



Logic diagram of Type 515 Exclusive-Or circuit.



Circuit diagram of an Exclusive-Or circuit and additional components.

Figure 1—Astable multivibrator.

Monostable Multivibrator

In any logic system, it occasionally becomes necessary to generate a fixed delay period. This is sometimes done by gating of the system clock; however, it is often simpler to use a monostable multivibrator, which generates a fixed duration pulse each time it is triggered. The monostable multivibrator of Figure 2 was built with one Type 510 Solid Circuit, two resistors, two capacitors, and one diode. At room temperature, and with a 3 volt supply, the following values of output pulse duration resulted from varying C_T:

t = 40 μsec.	C_T = 0.01 μf
310 μsec.	0.1 μf
3.0 msec.	1.0 μf

The trigger sensitivity was 2 volts.

Elimination of External Components

In order to make production economically feasible TI, Fairchild, and now others have concentrated on a standard line of "building blocks." At the other extreme, Motorola is concentrating on custom circuits. A happy medium, now being introduced by TI and General Electric, is a standard substrate used as a "parts bin," which allows a variety of circuit configurations merely by the changing of internal and external interconnections. The astable and monostable circuits discussed above, for instance, could be reduced to the point where the only external elements required would be the timing capacitors. A Schmitt Trigger circuit, the construction of which was unsuccessfully attempted with the standard Solid Circuits, could also be realized.

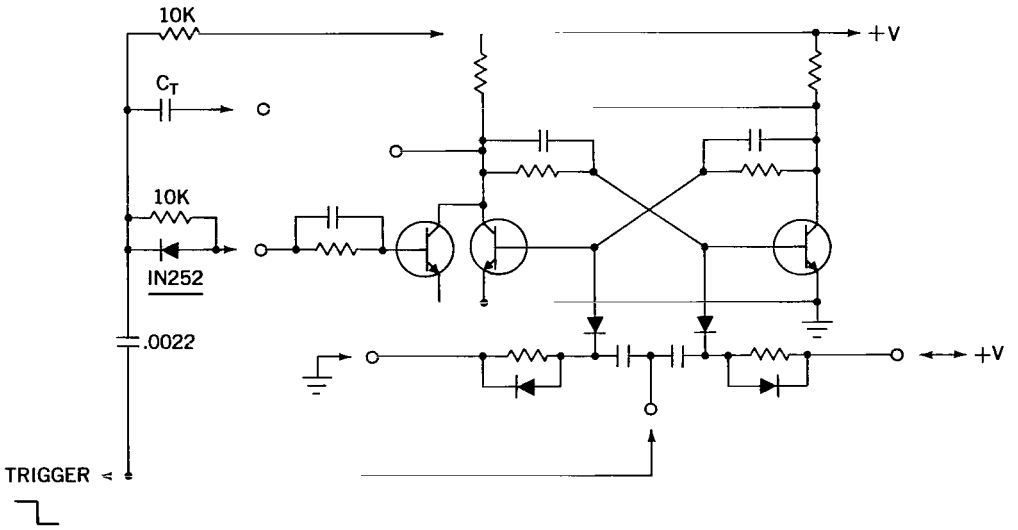


Figure 2—Monostable multivibrator built with one Type 510 Solid Circuit, two resistors, two capacitors, and one diode.

CLOCK READOUT

In past satellites that used the PFM (Pulse Frequency Modulation) encoding process there was no provision for an on-board clock readout. Such a readout would be useful in reducing data from certain experiments, such as those in which the time of an event is of interest and in which satellite time rather than ground station time is of prime importance. For one application, it was desired to provide a 22-bit sequence counter and readout for use with an Explorer XII—type Telemetry Encoder. The resulting design was never breadboarded because the project for which the application arose was later shelved; however, the block diagram of the proposed counter is included here (Figure 3) to demonstrate the scale of subsystems which may readily be implemented using the Solid Circuits.

PFM CLOCK AND MATRIX

The clock and matrix for the Explorer XII series PFM encoders supplies timing signals to the rest of the telemetry and to the experiments. It consists merely of a frequency source, a countdown chain, and a number of gate circuits. A block diagram of such a system is shown as Figure 4. The output functions shown are the particular ones used in Explorer XIV, and obviously could be changed by a different gating arrangement. The only unusual feature is the function of gates 3A, 3B, 4A, 4B, and 9. The explanation for their presence is as follows.

In the PFM scheme currently in widespread use, frame synchronization is aided by width modulation of the first channel frequency burst. In particular, the first burst is 15 msec in duration, the first blank is 5 msec, and all other blanks and bursts are 10 msec. Existing encoders provide a signal to accomplish this width modulation by changing the bias on a magnetic core oscillator for one channel period. On the other hand, the Solid Circuit encoder accomplishes the width modulation by

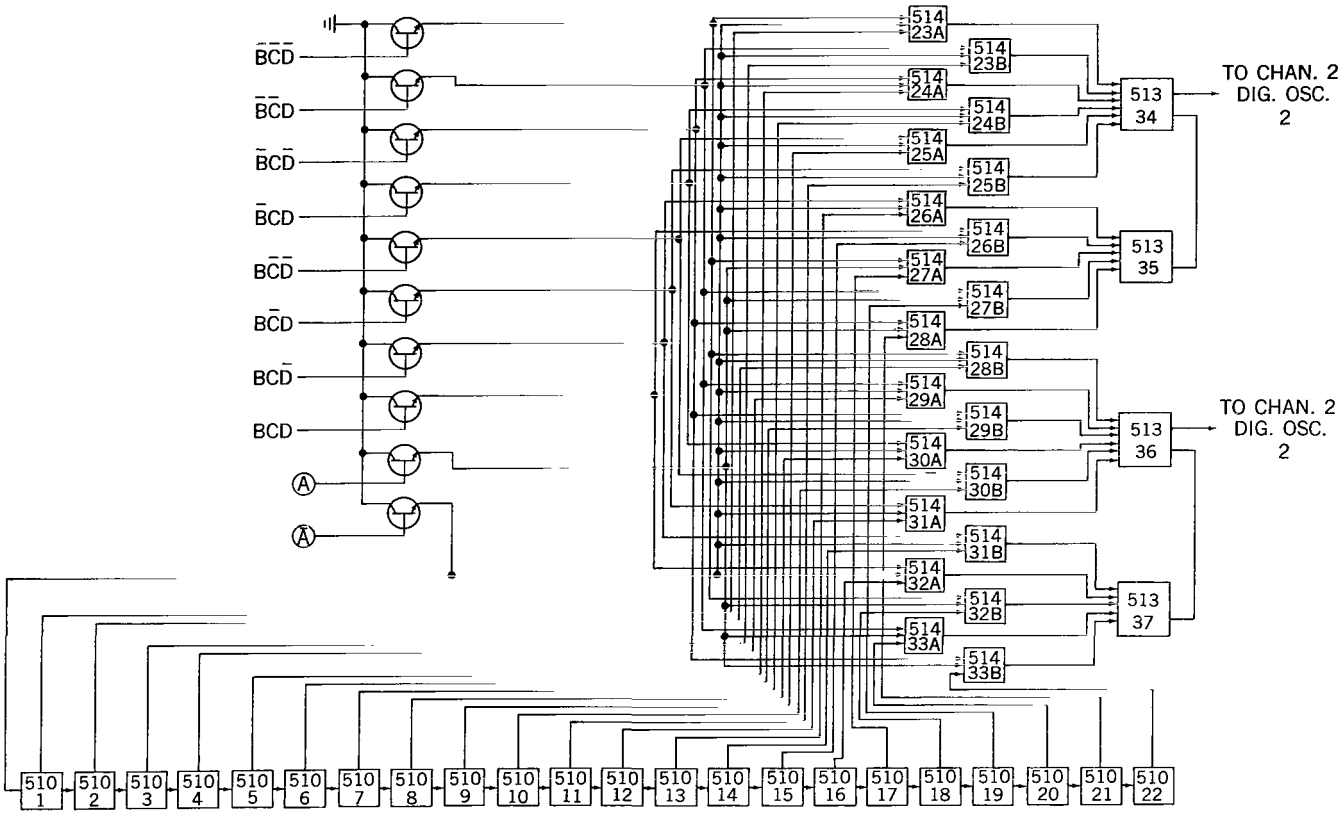


Figure 3—Block diagram of a clock accumulator and matrix designed with TI Solid Circuits.

means of the aforementioned gates and an extra countdown stage. The output of the additional countdown stage thus has a 10 msec period. The gates add one half cycle (5 msec) from this stage to the output of the next stage once each frame to provide the desired output (S).

This system was breadboarded and, with a 20 K resistor added between the gate 4B output and the binary 5 input, functioned properly with a 3 volt supply from -10°C to +60°C. Over this temperature range, the supply voltage could be varied from 2.5 volts to 3.5 volts without affecting operation other than to change the clock period. The addition of an external resistor was made necessary by troubles with the input circuit of the Type 511 Solid Circuit. These troubles were a result of too great a trigger sensitivity, and showed up as false triggering of the flip-flop. The manufacturer claims to have corrected this problem in later lots; for the units used, however, the resistor was necessary to attenuate the binary input signal.

PCM TELEMETRY ENCODER

Since the Solid Circuits are digital, they must be used in an all-digital system for their benefits to be fully realized. Thus, they would be of more use in a Pulse-Code Modulation (PCM) system than in the PFM systems presently in use; and the PCM encoder of Figure 5 was built with that in

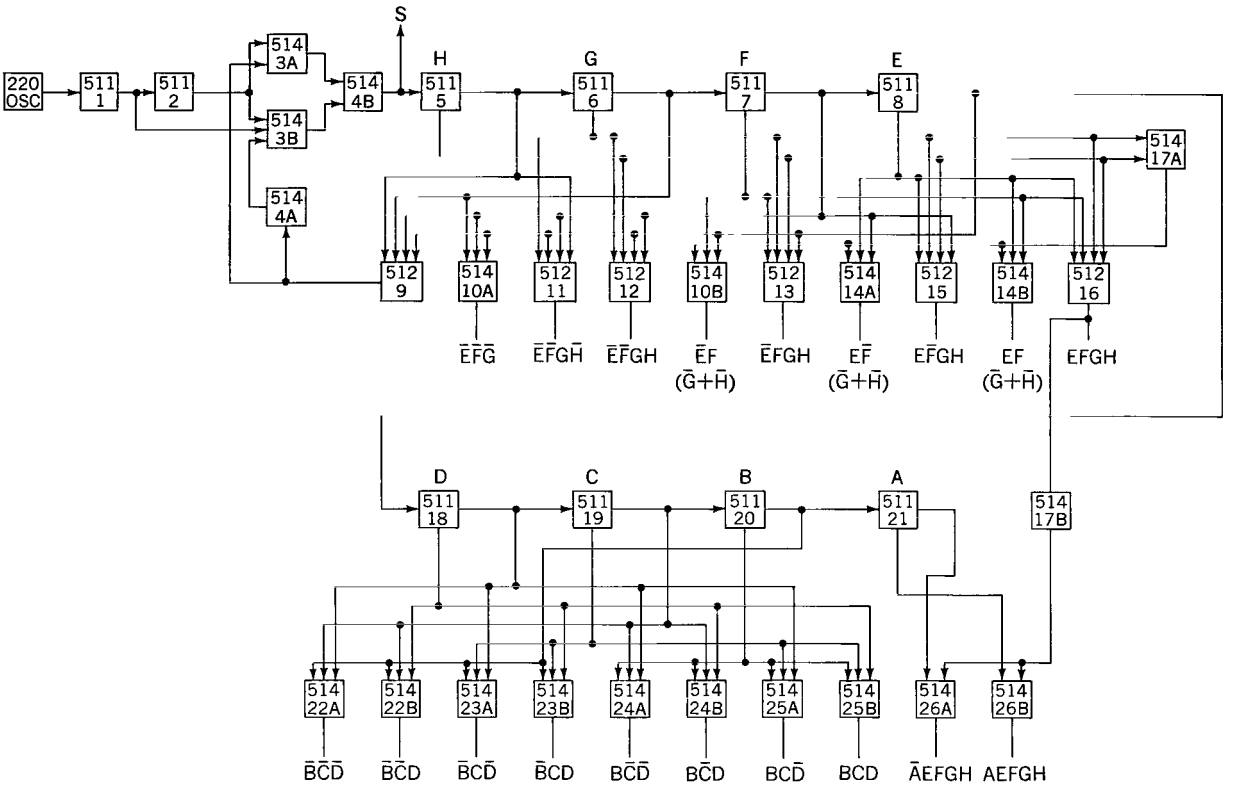
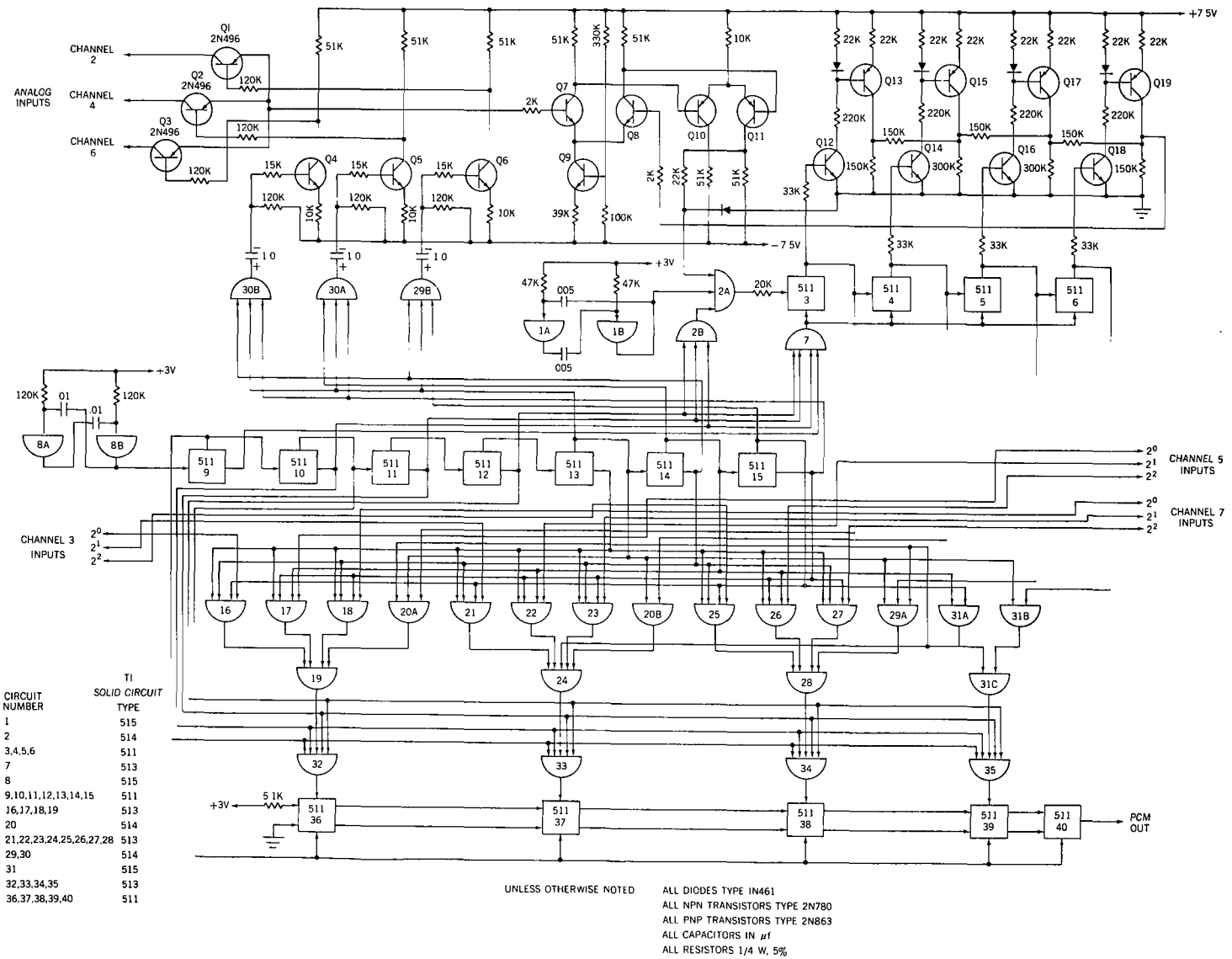


Figure 4—Block diagram of a clock and matrix designed with TI Solid Circuits.

mind. This is an eight-channel, 4 bits/channel system with an output rate of 200 bits/sec. The first two channels (0 and 1) are used to transmit a sync pattern of alternating zeroes and ones. This particular pattern was chosen only for ease of implementation and is definitely not desirable for use in any flight model. Channels 2, 4, and 6 are read from an analog-to-digital converter (transistors Q7 through Q19) whose input is switched between three analog inputs by transistors Q1 through Q6. Channels 3, 5, and 7 are read directly from 3-bit digital inputs, with the first bit of these channels always one.

No attempt was made to optimize the analog-to-digital converter; in fact, 5 percent resistors were used although the precision of four bits is ±3 percent. The converter was checked for stability (as opposed to absolute accuracy) over a temperature range from -10°C to +60°C and was found to vary less than ±2 percent even with the crude compensation used (diodes in the base circuits of Q13, Q15, Q17, and Q 19 to compensate for V_{BE} changes). Also, the analog switching circuits (Q1 through Q6) were not optimized, and thus the converter output was one count high because of the V_{CE} of the switching transistors. The nominal analog input of the range is 0 to +5 volts; the digital inputs are 0 volts for logic zero and +3 volts for logic one.



CIRCUIT NUMBER	TI SOLID CIRCUIT TYPE
1	515
2	514
3,4,5,6	511
7	513
8	515
9,10,11,12,13,14,15	511
16,17,18,19	513
20	514
21,22,23,24,25,26,27,28	513
29,30	514
31	515
32,33,34,35	513
36,37,38,39,40	511

UNLESS OTHERWISE NOTED
ALL DIODES TYPE IN461
ALL NPN TRANSISTORS TYPE 2N780
ALL PNP TRANSISTORS TYPE 2N863
ALL CAPACITORS IN μf
ALL RESISTORS 1/4 W, 5%

Figure 5—Demonstration model of a PCM telemetry encoder designed with TI Solid Circuits.

CONCLUSIONS

The immediate advantages of using presently available Solid Circuits in these applications are decreased size, weight, and cost. Because of the smaller number of interconnections, there is also the potential advantage of increased reliability, although this has not yet been proved. One disadvantage is the increased power required (Appendix A). For example, the eight-channel, 4 bit/channel PCM encoder discussed above requires about 110 mw of power, as compared with approximately 90 mw for the 272-channel, 7 bit/channel UK-2 PFM encoder which uses conventional components in low-dissipation circuits. All of these remarks apply also, of course, to other types and of integrated circuits, such as the Fairchild Micrologic, Sperry Semi-Nets, Signetic Integrated Circuits, etc. In fairness it should be mentioned that the increased power requirements would be partially offset by increased converter efficiency. This would follow from the higher power itself and also from the relaxed voltage regulation requirements (typically, ±10 percent for the supply to the Solid Circuits in the digital portion of the system).

There are two basic reasons for the relatively high power requirements of all these circuits. First, present techniques limit the available resistance range of diffused resistors to less than 50 K, and even this limit is reached only at considerable expense to the consumer. Second, because the whole circuit is on a single semiconductor substrate, it is difficult to provide NPN and PNP transistors (which would permit construction of complementary flip-flops). Several stopgap solutions (two packages, two chips in a single package) have been proposed for the second problem to avoid the more difficult techniques required to diffuse both type (PNP and NPN) transistors.

Future investigations should be directed first to reducing the power requirements for typical applications such as the ones shown here. This should be both from a device standpoint (e.g., higher resistance values) and from a configuration standpoint (e.g., series gate circuits instead of parallel gates).

Appendix A

Power Distributions

The power requirements given below are average, based on a 3 volt supply and a 2 milliwatt typical dissipation per collector node. All figures have been rounded to the nearest milliwatt.

Table A1

Power Requirements for the Clock Accumulator and Matrix Shown in Figure 3.

Circuit (see Figure 3)	Number of Solid Circuits @ 2 mw	Duty Cycle	Power Dissipation (mw)
Circuits 1 through 22	22	100%	44
Circuits 23 through 33	22	255/256	44
Circuits 34 through 37*	2	50% (avg)	2
Total for Solid Circuits			90
Input Transistors	10	7/8	18
Total power dissipation			108

*While there are four circuits, there are only two collector nodes.

Table A2

Power Requirements for the Clock and Matrix Shown in Figure 4.

Circuit (see Figure 4)	Number of Solid Circuits @ 2 mw	Duty Cycle	Power Dissipation (mw)
Circuits 1, 2, 5 through 8, and 18 through 21	10	100%	20
220-cps Oscillator	1	100%	2
Circuits 3A and 4B	2	50% (avg)	2
Circuits 3B and 4A	2	100%	4
Circuit 9	1	100%	2
Circuits 10A through 17A	10	15/16 (avg)	19
Circuit 17B	1	1/16	0
Circuits 22A through 25B	8	7/8	14
Circuits 26A and 26B	2	127/128	4
Total power dissipation			67

Table A3

Power Requirements for the PCM Encoder Shown in Figure 5.

Circuit (see Figure 5)	Number of Solid Circuits @ 2 mw	Duty Cycle	Power Dissipation (mw)
Circuits 1A, 1B, 8A, and 8B	4	100%	8
Circuits 2A and 2B	2	100% (max)	4
Circuits 3 through 6	4	100%	8
Circuit 7	1	15/16	2
Circuits 9 through 15	7	100%	14
Circuits 16 through 31B (less 19, 24, and 28)	14	15/16 (avg)	26
Circuits 19, 24, 28, and 31C	4	1/16 (avg)	1
Circuits 32 through 35	4	100% (avg)	8
Circuits 36 through 40	5	100%	10
Total for Solid Circuits			81
Transistors Q1 through Q19 and associated resistors			29
Total power dissipation			110

NASA-Langley, 1964 G-424

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