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THE DIGITAL TAPE RECORDER ANALYZER

by Joseph A. Sciulli

Goddard Space Flight Center
Greenbelt, Md.

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Goddard Space Flight Center

SUMMARY

The test instrument described herein was designed for the purpose of performing error analyses on spaceborne digital tape recorders. In addition to its two basic functions of detecting errors in a clock track recorded on tape and performing a parity check, under various test conditions, the analyzer's design flexibility will enable simple modification of future models for increased capability. This report describes the theory of operation of the present model and provides operating instructions, together with complete drawings and component listings.

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THE DIGITAL TAPE RECORDER ANALYZER

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INTRODUCTION

The requirement to test spaceborne digital tape recorders during qualification tests and system integration has generated the need for a test instrument capable of making significant analyses. The instrument described herein has two basic capabilities:

1. Detecting errors in a clock track recorded on a tape
2. Performing a parity check

Although the instrument has only two basic functions, it can be set up to make tests under various conditions. In addition, flexibility has been incorporated into the design so that future models of the analyzer may be easily modified for increased capability. The purpose of this report is to describe the theory of operation and to provide operating instructions for the tape recorder analyzer.

THEORY OF OPERATION

Background

The tape recorder analyzer is a test instrument designed to perform error analyses on spaceborne digital tape recorders. The analyzer was designed specifically to test a 200-foot endless loop, 8-channel digital tape recorder for both Tiros and Nimbus spacecrafts. The tape recorder has a record speed of about 0.4 inch/second and a playback speed of about 10.4 inch/second, giving a playback speedup ratio of 26:1. If the tape is assumed to be perfect, the main sources of error in the recorder can be attributed to such things as tape dropout, tape flutter, and tape skew. The specification for the tape recorder subsystem states that the analyzer will be used to record signals on one complete tape. For acceptance of the recorder, there shall be less than 24 total errors (clock and/or data errors) on the tape, not including errors at the splice.

The accuracies of both the clock channel and the data channels can be checked with this analyzer. Approximately 75 percent of the instrument consists of micrologic modules, with the remaining 25 percent consisting of conventional solid-state circuitry. Micrologic modules were

chosen for the major portion of the design because of their proven reliability for both spacecraft and ground equipment.

The tape recorder analyzer closely simulates the conditions to which the recorder would be subjected during flight operations. The instrument can be set up for a number of different test situations.

The accuracy of the data channels is determined by continuously forcing one data channel to be in a certain state with respect to the other six data channels during record time. This channel is called the "parity channel" and, during playback, a continuous examination is made to insure that this preselected state is maintained. The accuracy of the clock is determined by generating test signals which permit the continuous examination of the clock signal to insure that it falls within the allowed tolerance.

The following pages give a more detailed and comprehensive explanation of the operation of the tape recorder analyzer.

General Description

Figure 1 shows the main parts of the system with single-line interconnections. The data input to the tape recorder can be selected at two different points:

1. At the input to the 6-bit shift register
2. At the input to the 6-bit storage register

At the input to the 6-bit shift register, either an external known data pattern, an internal generation of pseudo-random data patterns, or the random code generator can be selected. The 6-bit shift register converts the incoming test data from serial to parallel form. The six output wires of the shift register are fed to a bank of six 3-position switches, where either a known data pattern, a scaler connection of each bit of the 6-bit storage register, or the six output wires from the 6-bit shift register can be selected.

Odd parity is continuously generated during record time by controlling a parity bit with the initial parity checking circuitry and recording the parity bit on the 7th data channel. Odd parity is defined as an odd number of logical 1's contained in N data bits. In the case of 6 bits, odd parity would be indicated if there were one, three, or five 1's in the 6 bits. For example, if A, C, and E in Figure 2 are 1's, odd parity would be indicated. If, however, only A and C are 1's, even parity would be indicated. If *even* parity exists at the recorder inputs, the parity checking circuitry forces the parity to be odd by making the parity bit a 1 (an example is shown in Figure 3). The eight record amplifiers are therefore driven by six data channels, one parity channel, and a 100-cps clock channel which is 90 degrees out of phase with the data so that the data may be strobed at the center of each bit.

During tests the playback outputs of the recorder consist of six data channels, one parity channel, and a 2.6-kc clock channel. The six data channels and the one parity channel are fed in

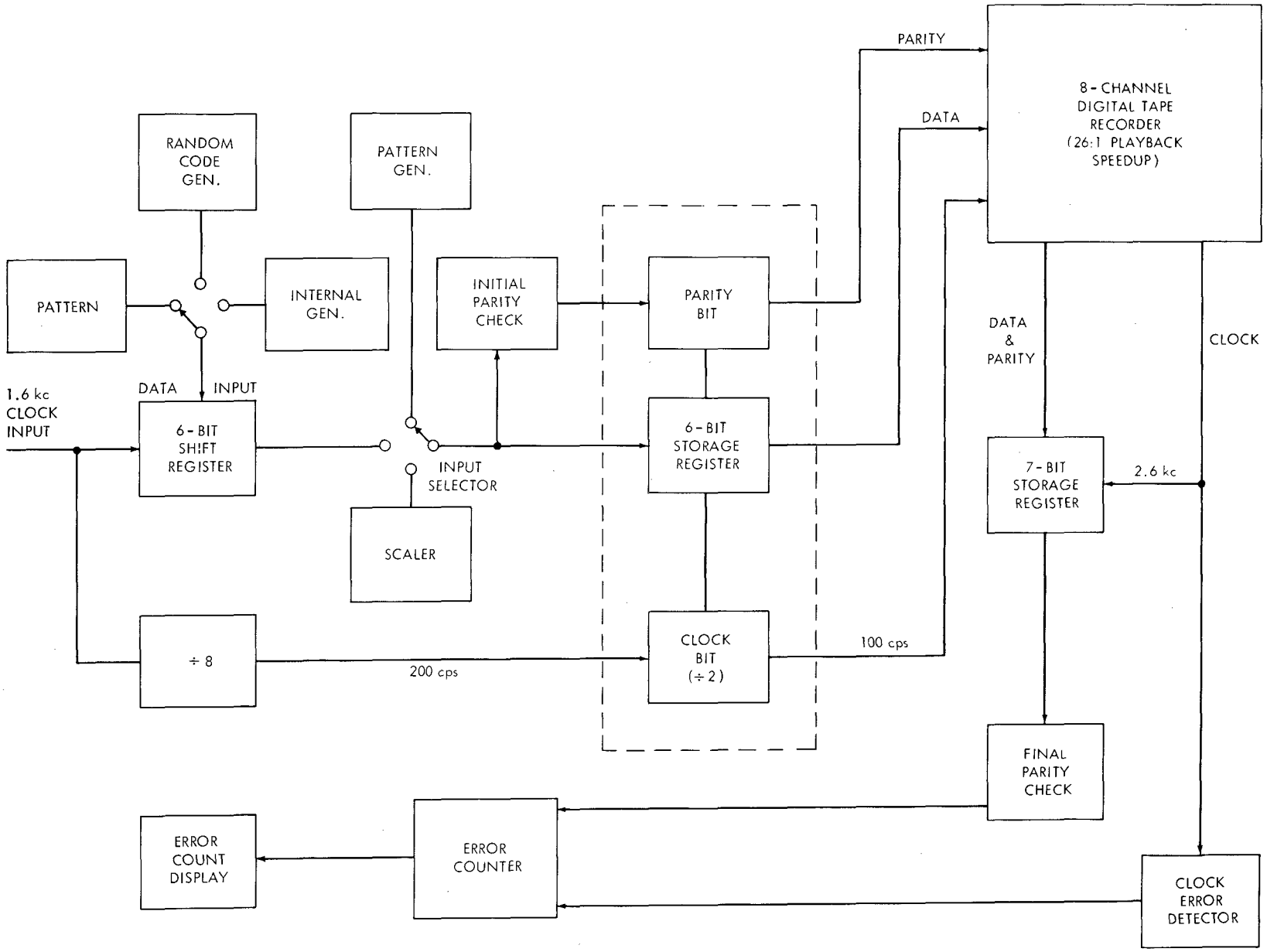


Figure 1—The tape recorder analyzer.

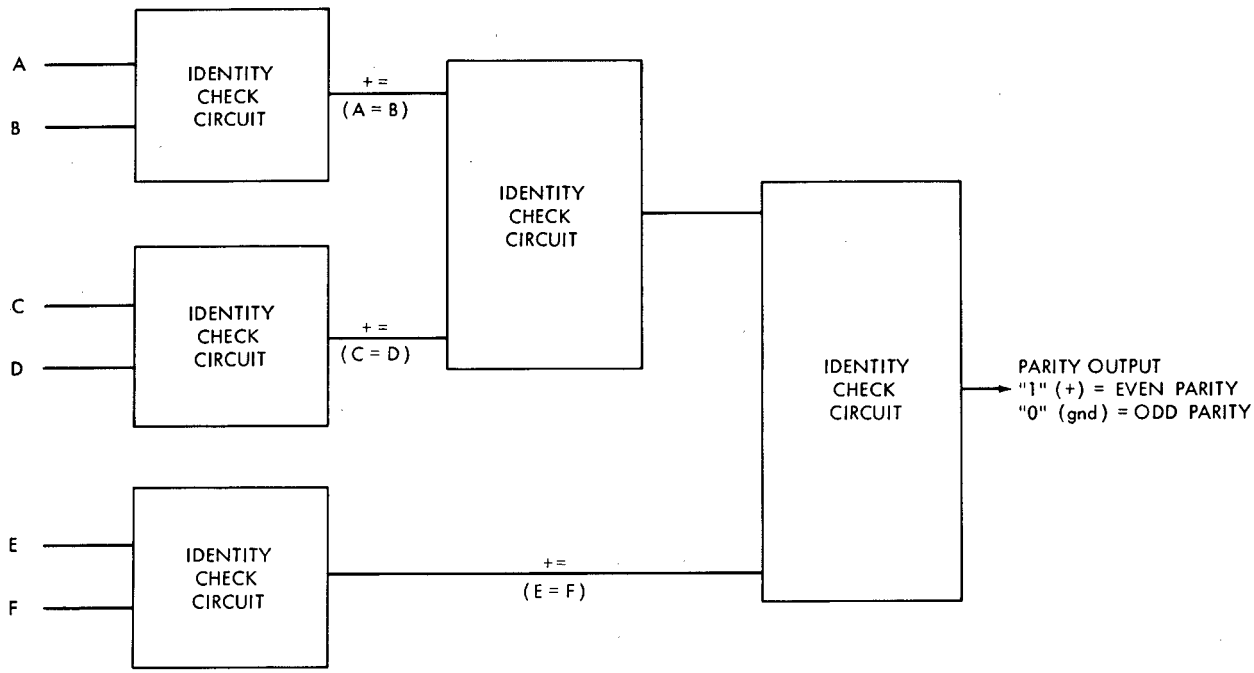


Figure 2—Parity checking network.

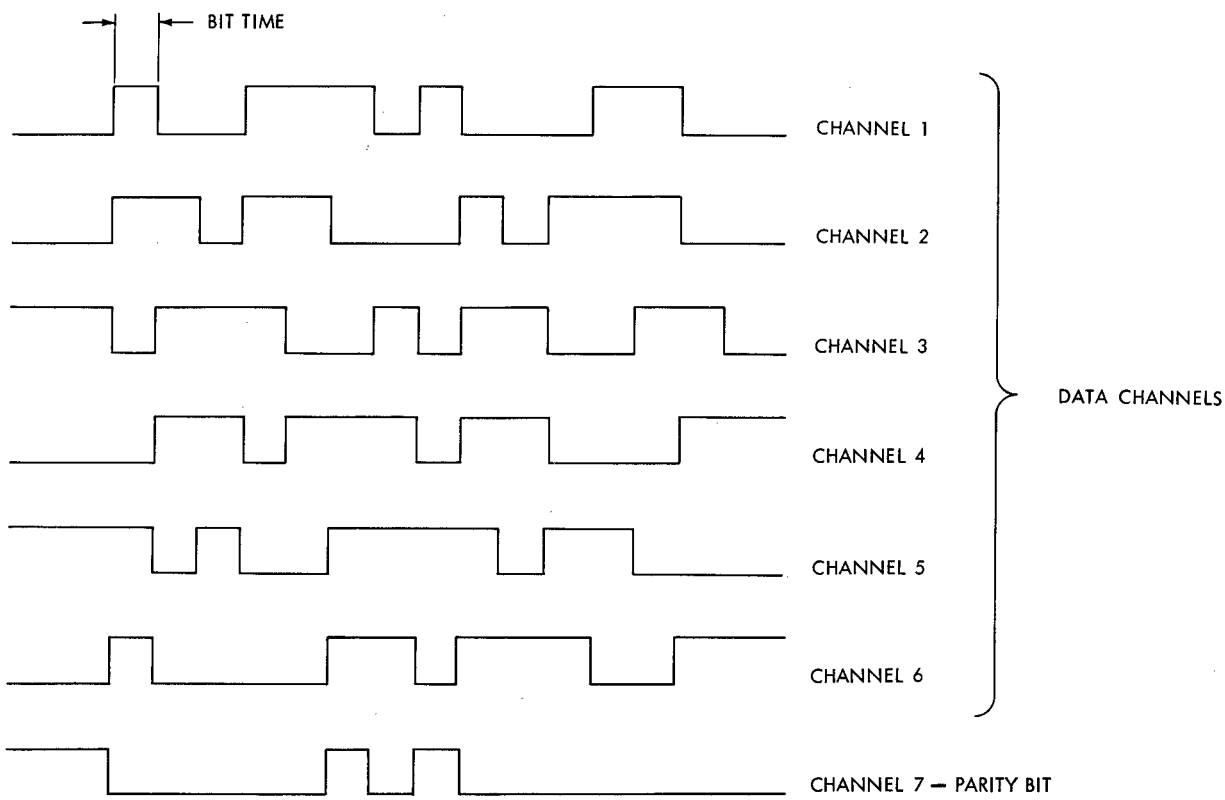


Figure 3—Example: making parity odd.

parallel to a 7-bit storage register which is driven by the 2.6-kc clock signal. At the output of the 7-bit storage register the data are checked to insure that odd parity has been maintained. Parity checks are made by a network of identity checking circuits, as shown in Figure 2. The function of the parity checking network is to compare the six inputs and produce an output which indicates that either odd parity or even parity exists. Since the recorder inputs always see an odd number of 1's in the seven data channels, the parity at the outputs also should be odd as long as no error has occurred. If the check made at the output of the recorder indicates *odd* parity, it is assumed that no error has occurred. If *even* parity is indicated at the output, an error is detected and counted. Under this assumption, it is possible occasionally to count or not count a parity error (data error) falsely; that is, it is possible for a data error to occur without changing parity. This case would occur if, during a certain bit time, one channel changed from 1 to 0 and another channel changed from 0 to 1. However, it has been determined that this event will only occur approximately 0.025 times as often as an error caused by only one channel changing state. It is therefore reasonable to say that the case of the cancelling double error is very remote with respect to the more practical case of a single error. In addition, the tests to be made do not require completely accurate error counts to obtain significant results.

The accuracy of the clock is examined to insure that it falls within the specified tolerance. The data error detector and the clock error detector are both designed so that their outputs provide a pulse each time an error occurs. The outputs of both detectors are then fed to the error counting and error display circuitry.

Clock Errors

Both clock phase errors and missing clock pulses are considered clock errors. The design objective is to develop a countable pulse each time either type of error is detected.

Phase Errors

To develop a phase error detector, each stage of the clock signal must be continuously checked for its accuracy in period within maximum and minimum tolerances. The following discussion refers to the timing diagram of Figure 4. So that both edges of the clock may be tested, a pulse $\overline{\mathbf{T}}$ of approximately 10 μsec in width is generated by each edge of the 2.6-kc clock. Thus, there should be 192.5 μsec between each developed pulse; a tolerance of 192.5 ± 30 μsec has been established. The pulse train $\overline{\mathbf{T}}$ is used to trigger one-shot multivibrator **A** which is cascaded with one-shots **B**, **C**, and **D**. Pulses **A** and **B** are each 81 μsec in width. **A** and **B** are gated together to develop a 162-μsec signal which is used to check the short end (162.5 μsec) of the tolerance. The pulse train $\overline{\mathbf{T}}$ is gated with this 162-μsec signal to generate $\overline{(\overline{\mathbf{A}} + \overline{\mathbf{B}} + \overline{\mathbf{T}})}$. An error pulse is developed if the clock signal falls below the 162.5-μsec lower tolerance limit.

Missing Clock Pulses

To check the long end of the period tolerance, one-shot **C** is set at 60 μsec, giving a tolerance coverage—along with **A** and **B**—of 222.5 μsec. As shown in the timing diagram, the falling edge of

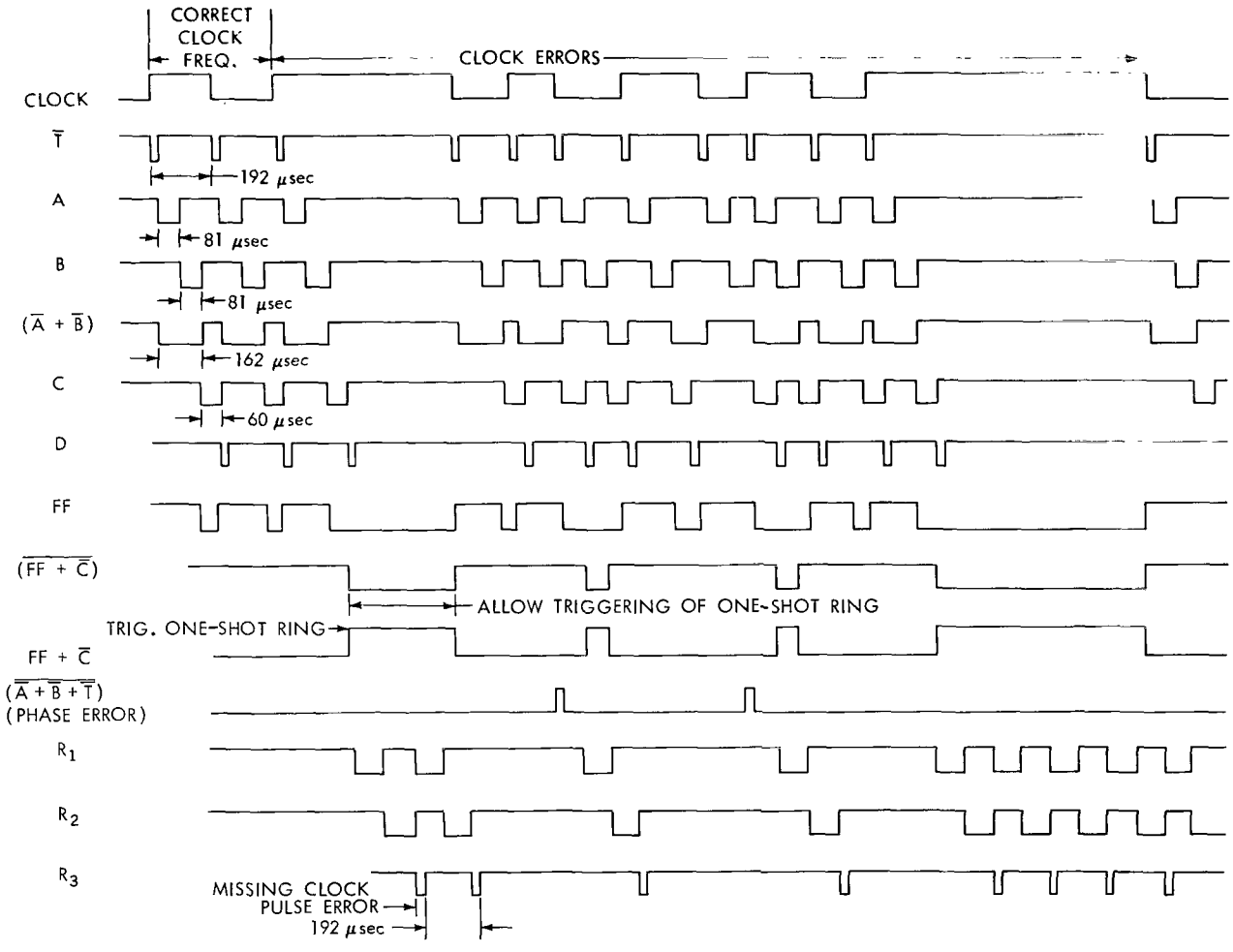


Figure 4—Timing diagram.

one-shot C is used to trigger a flip-flop which is reset (through the preset input) as soon as the next clock pulse occurs. The output of this flip-flop is in its "1" state (positive voltage) as long as the clock pulses occur within tolerance. If, however, the clock pulses begin to occur out of tolerance, the flip-flop output stays in its "0" state (ground). This allows the triggering of a one-shot ring (3 one-shots cascaded and closed on itself) shown in Figure 5 (also note timing diagram). The purpose of the one-shot ring is to generate a signal which is identical to the expected clock pulse signal $\overline{T}$. The one-shot ring is turned on just as the first clock pulse is missed. The pulses generated by the one-shot ring are then counted as errors until the clock is corrected and the one-shot ring is shut off.

Special Circuits

A number of circuits which are utilized in the tape recorder analyzer system require some explanation for a more complete understanding of the entire system.

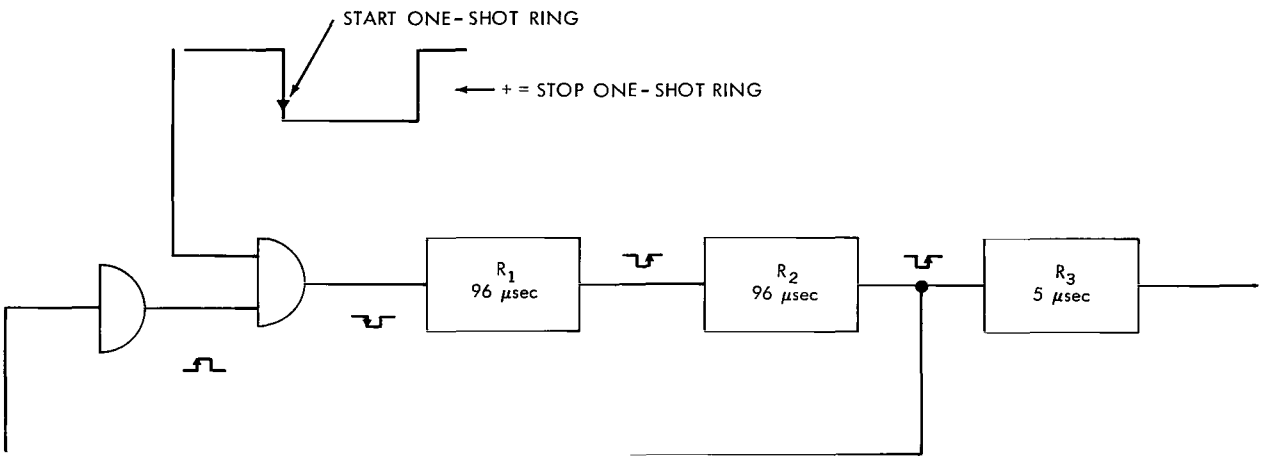


Figure 5—One-shot ring.

Random Code Generator

The purpose of the random code generator, shown in Figure 6, is to develop random sets of data in order to test the tape recorder under realistic conditions. A frequency-modulated 200-kc signal is developed by a noisy multivibrator and is fed to a binary scaler whose output is fed to a single-shift register bit, which is strobed by the 1.6-kc clock signal. The noisy multivibrator is simply a standard free-running multivibrator into which 60-cycle noise has been inserted by means of a filament transformer whose secondary is in series with the base-biasing resistor. The output of the multivibrator (Figure 7), a 200-kc frequency-modulated square wave, is then fed to the trigger input of the binary-scaler bit which gives the signal symmetry. Since the triggering (falling) edge of the FM signal is varying in phase and the shift register bit is strobed at a very

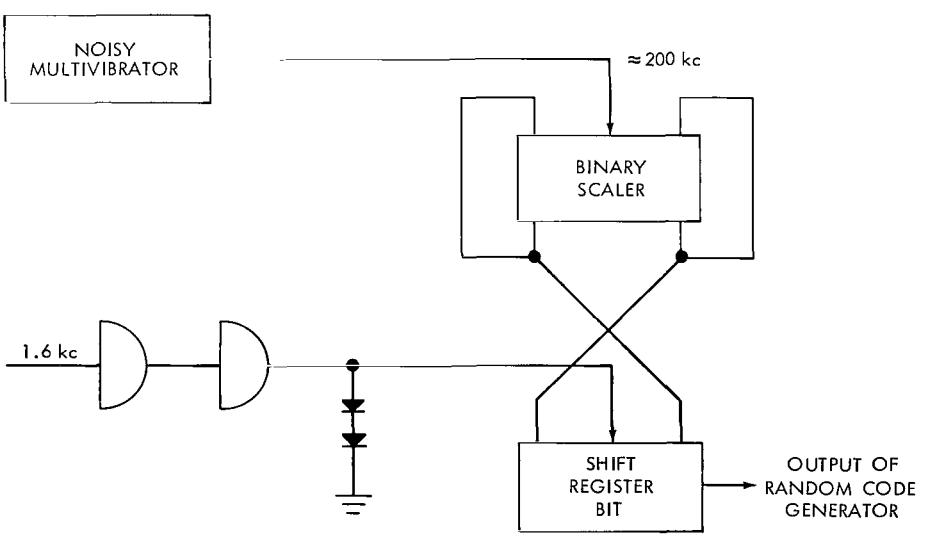


Figure 6—Random code generator.

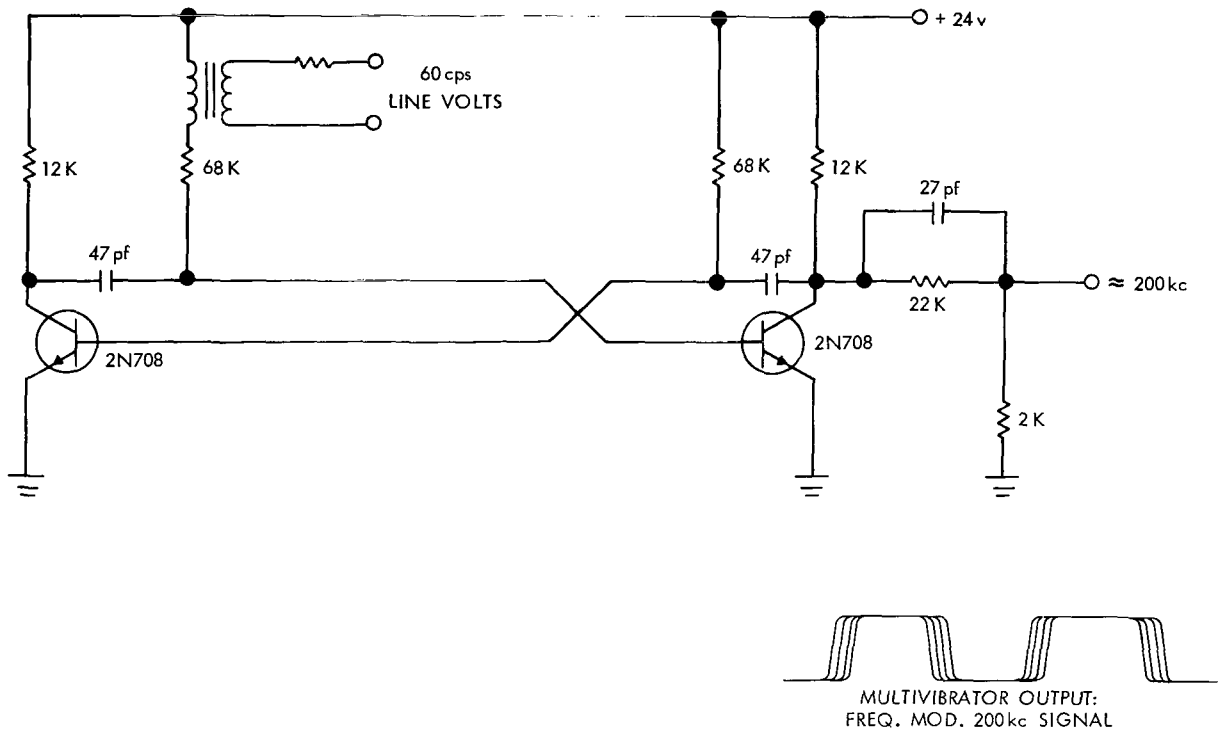


Figure 7—Frequency-modulated multivibrator.

low frequency compared with the multivibrator frequency, the output of the shift register bit is consequently a random generation of test data bits.

One-Shot Multivibrator

A number of references have been made herein to one-shot multivibrators. All the one-shots mentioned are essentially the circuit shown in Figure 8 with various values of capacitance resulting in various pulse widths.

Pulse Generator—Frequency Doubler

In the discussion of the clock error detector it was mentioned that, to check both edges of the clock, a 10-μ sec pulse is generated at each edge. The circuit which performs this function is shown in Figure 9. The timing diagram shown in Figure 9 essentially explains the function of the circuit. The falling edge of the 3-kc clock signal triggers flip-flop A, which sets up the proper condition at the R and S inputs of flip-flop B, which is triggered at the much faster 200-kc rate. As soon as flip-flop B switches, its output is fed back to the preset of flip-flop A and resets it, thus resulting in a pulse output at each falling edge. The 200-kc signal need not be phase-coherent with the 3-kc clock signal. Performing an identical process on the opposite phase of the clock and combining the two pulse outputs results in a frequency doubling.

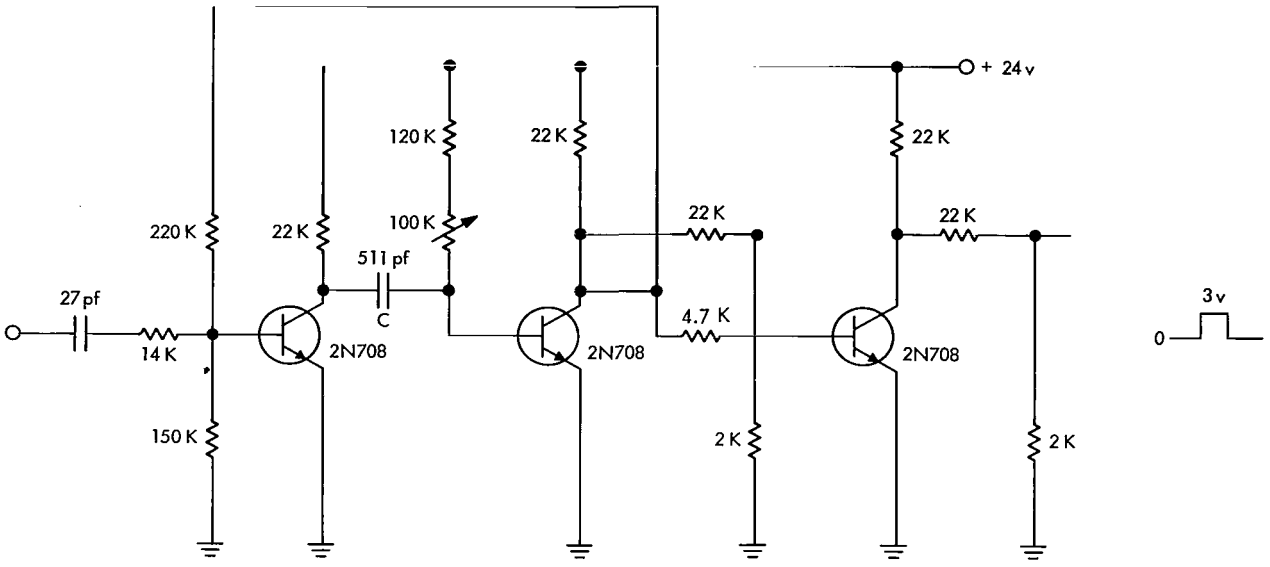


Figure 8—One-shot multivibrator.

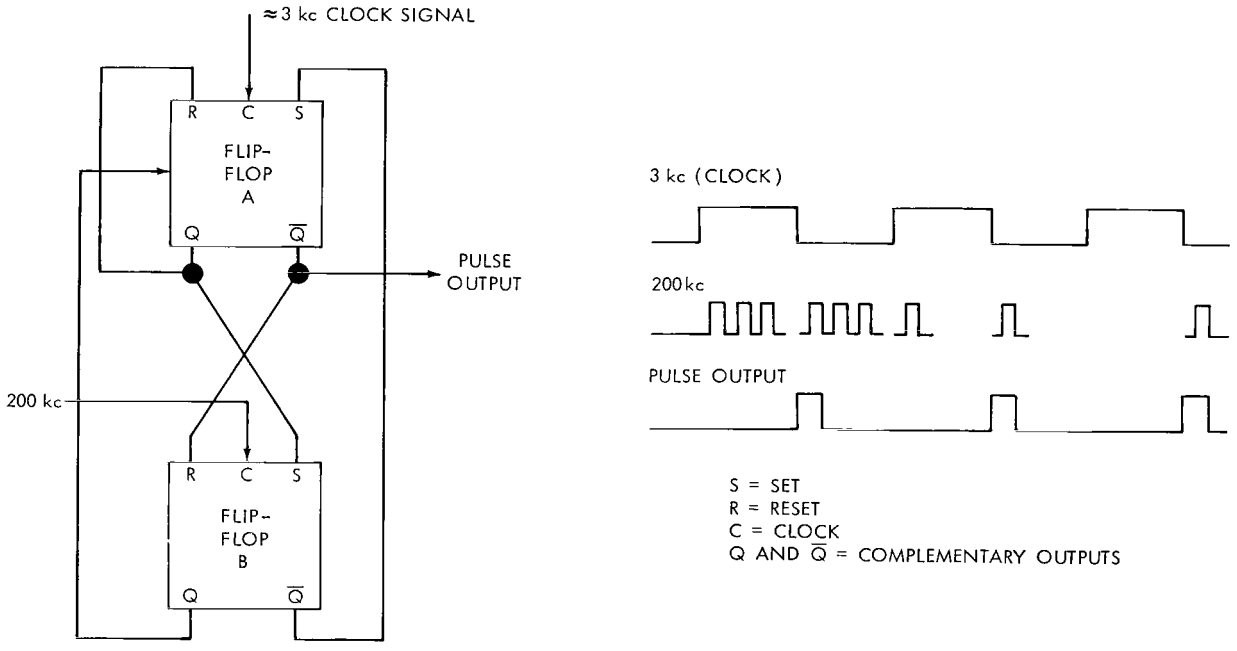


Figure 9—Pulse generator — frequency doubler.

Additional Design Considerations

General

Since the analyzer will be used by a number of individuals under various conditions, substantial mechanical and electronic protection was incorporated into the instrument. At the same time, the analyzer was designed for ease of operation and maintenance.

Mechanical and Electronic Protection

Occasionally, a power supply or signal generator is inadvertently applied to a piece of equipment in a manner that could seriously and permanently damage the equipment. For this reason, every power supply and signal generator input to the analyzer has been provided with special protection circuits which insure that dangerously high signals are not applied directly to the delicate micrologic modules and conventional solid-state circuitry.

The mechanical frame of the analyzer makes it adaptable for either enclosure or rack mounting, in addition to providing protection for the components. Thus the analyzer is a single self-contained unit, except for power supply and signal generators.

All input jacks which take a standard G-R connector have been spaced such that the connection can be made in only one way and thus eliminate the possibility of dangerous shorting of independent signals.

Operation and Maintenance

For ease of operation the analyzer has been designed so that it can be activated regardless of any switch setting. However, to use the instrument properly, the operator should have a thorough knowledge of the proper switch settings and procedure. Since all the main controls and monitoring points are located on the front panel with appropriate identifications, the operation of the analyzer during tests is very simple.

Maintenance also is easy to perform, since every printed circuit card and every solder joint can be reached without turning a screw.

Flexibility

As previously mentioned, the analyzer was designed to test the 200-foot endless loop, 8-channel digital recorder. Because of the flexibility incorporated into the design, it would be easy to modify the analyzer to test other digital recorders as well. If the specifications for qualification should change at any time, it is a simple matter to recalibrate a number of one-shots so that the analyzer may be utilized.

Another important consideration is the ability of this instrument to analyze prerecorded tapes which have been recorded with either even or odd parity. This capability means that it is possible to analyze tapes during flight operations. The analyzer therefore could be included as part of the ground station and could be used to determine the accuracy of the recorder and the tape at any time and to determine the reliability and accuracy of the recorder by making life tests during flight operations. It also is possible to locate defective spots on the tape to some degree. Utilizing these capabilities, the analyzer could conceivably aid in making more significant data analyses.

OPERATING INSTRUCTIONS

General

To utilize the tape recorder analyzer to maximum advantage, one should become as familiar as possible with the mechanics of operating the instrument. During the following discussion, refer to Figure 10 to become familiar with the controls and procedure.

Initial Procedure

Equipment

In addition to the analyzer itself, a few additional pieces of equipment are necessary to perform tests on the 8-channel recorder:

3 Power Supplies: +3 v at 75 ma, -3 v at 10 ma, and +24 v at 110 ma

1 Frederick Pulse Pattern Generator, Model 201 (or equivalent): capable of 35 bits

2 Square-Wave Generators, HP Model 211A (or equivalent)

1 Strip Chart Recorder

1 Dual-Trace Oscilloscope, Tektronix Type 533A (or equivalent)

Front Panel — Description

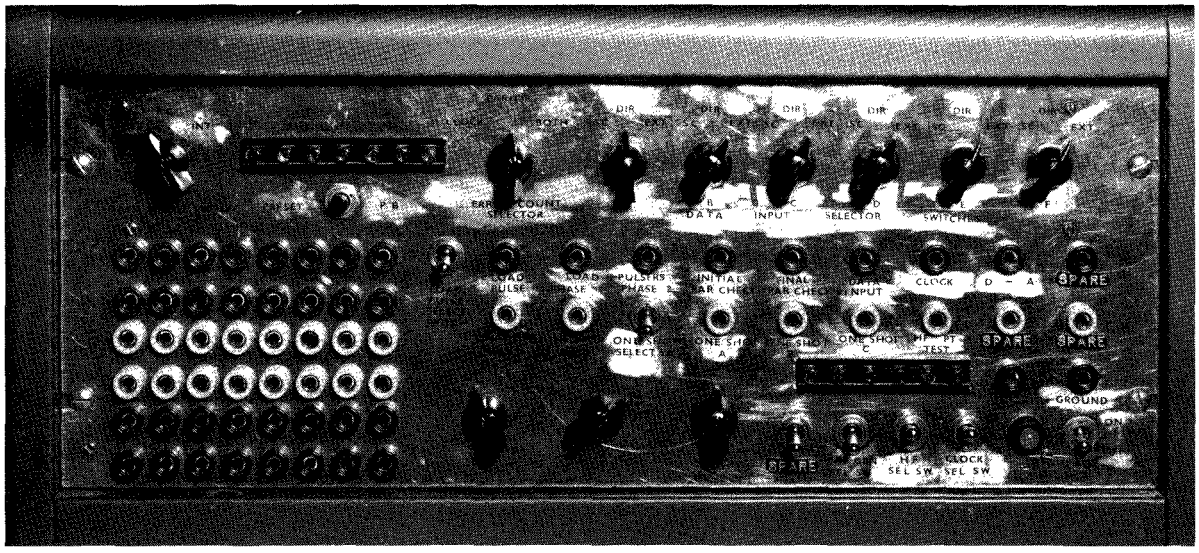
On the front panel [Figure 10(a)] are located all the switches and test points necessary for normal operation of the analyzer during tests. The DATA SELECT SWITCH chooses the type of test data pattern to be used. The ERROR COUNT SELECTOR switch chooses the error count to be displayed. The DATA INPUT SELECTOR SWITCHES choose the connection of the data storage register according to the test being made. The PRESET PB (pushbutton) resets the error count display to zero. The patch panel (6 x 8 array of jacks) is used to cross-patch the record and playback channels. The various test points and toggle switches are all utilized during normal tests.

Back Panel — Description

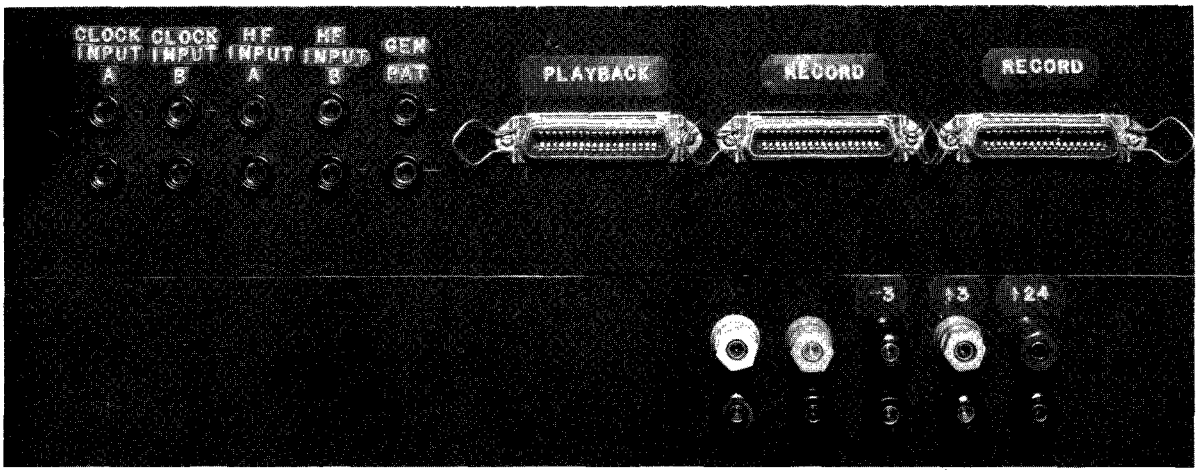
On the back panel [Figure 10(b)] of the analyzer are located all power supply and signal generator inputs used during normal testing. Also on the back panel are located three 36-pin connectors which are used to connect the record and playback channels of the recorder to the analyzer. The two connectors marked RECORD are logically identical. This means that two recorders could be recorded simultaneously. However, only one recorder can play back at a time.

Patch Panel

At the lower left of the front panel a 6 x 8 array of jacks makes up a patch panel on which any of the eight record channels of the analyzer may be directed to any of the record amplifiers of the



(a) Front panel



(b) Back panel

Figure 10—The tape recorder analyzer control panels.

recorder. Each pair of vertically opposite, identically colored jacks is a jumper pair in series with one of the record or playback channels. The red set of jacks (upper two rows) is in series with record output connector 1, the yellow set (middle two rows) is in series with record output connector 2, and the green set (lower two rows) is in series with the playback input connector. On normal testing of one recorder, each red pair and each green pair is shorted, with the yellow set of jacks open. To record on two tapes simultaneously, the yellow pairs of jacks also must be shorted. Each pair of jacks has been positioned so that it can be shorted with a standard G-R connector. For any other patching arrangement use the patching leads provided.

Power Supply and Signal Generator Connectors

Make the scope trigger and scope ground connections on the front panel. On the back panel, connect *but do not turn on* +3v, -3v, and +24v power supply voltages, CLOCK INPUT HF input (100-kc), and GEN PAT (pattern generator). On the front panel choose proper position for the clock select switch (CLOCK SEL SW), high-frequency select switch (HF SEL SW), and pattern-generator select switch (PAT GEN SEL SW) according to the connections made.

Switches and Controls

On the front panel insure that LOAD PULSE SELECT SWITCH and ONE SHOT SELECT SW are both in the "normal" positions. Choose PAT (pattern generator), RC (random code generator), or INT (internal generator) at DATA SELECT SWITCH. At the bank of six DATA INPUT SELECTOR SWITCHES, choose SC (scaler), DIR (direct) or EXT (external) inputs.

Power ON

Turn on +3v, -3v, +24v, CLOCK INPUT, HF INPUT (100-kc), and GEN PAT on the back panel. Utilizing the monitoring tests points on both the front and back panels, check power supplies and signal generators for their accuracy. Depress PRESET PB (front panel) to reset the error counting mechanism.

Test Procedure

General

The specification and statement of work for the 8-channel digital tape recorder subsystem specifies that the tape recorder analyzer is to be utilized in tests before vacuum thermal. The specification states that the analyzer will be used to record a complete tape. There shall be less than 24 total errors (either clock or data errors) not including errors at the splice. To perform this test properly, the following procedure should be used.

Test Setup

The initial test procedure described in the section "Initial Procedure" should be performed before beginning tests on the recorder. The operator should be satisfied that the analyzer is

performing satisfactorily in the RECORD mode. He should insure that all record channels of the analyzer are providing appropriate test data according to the data input selected. Every record channel of the analyzer also should be checked to insure that the amplitude of a logical 0 is approximately -0.1 volt in amplitude. The record amplifiers are so sensitive that a logical 0 of a few tenths of a volt of positive amplitude could be interpreted as a logical 1. The level of the logical 0's can be adjusted by controlling the -3 volt power supply. The 1.6-kc clock signal and the 100-kc high-frequency signal must be square waves with amplitudes of approximately 3 volts above ground. The external oscillator input of the pattern generator must be driven by the 1.6-kc clock signal, and the NRZ output of the pattern generator should be applied to the pattern generator input of the analyzer. The amplitude of the pattern generator also should be approximately +3 volts above ground.

When satisfactory operation of the analyzer is achieved, the record channels of the analyzer should be connected to the inputs of the record amplifiers using the harness provided. During recording there should be no connection between the playback channels of the analyzer and the playback amplifiers. A full recording requires approximately 100 minutes. This time can vary somewhat, and therefore at least 110 minutes should be allowed for a full recording.

After a full tape has been recorded, the record connections should be removed and the playback connection made. The D-A converter output on the front panel should be connected to one channel of the strip chart recorder. The purpose of the D-A converter and the strip chart recorder is to give an indication of the location of the splice and also the number of errors which are encountered at the splice. The indicator lights on the front panel give a digital readout of the number of errors counted. At the end of the playback cycle the number of errors at the splice is subtracted from the error count indicated by the lights. Note that it is possible to count parity errors only, clock errors only, or both simultaneously. The preset pushbutton is used whenever the error count is to be reset to zero.

CONCLUDING REMARKS

The tape recorder analyzer is a test instrument which was specifically designed to aid both NASA and contractor personnel in testing and qualifying the 8-channel digital recorder. The instrument has been electronically and mechanically designed to be simple to operate and maintain, and as foolproof as possible. In addition to performing the primary function of making error analyses on the 8-channel digital recorder, it is believed that with careful operation the analyzer can be conveniently utilized to troubleshoot and locate sources of error in the recorder at the same time. This instrument can be easily modified to test future digital tape recorders and can be used to analyze prerecorded tapes.

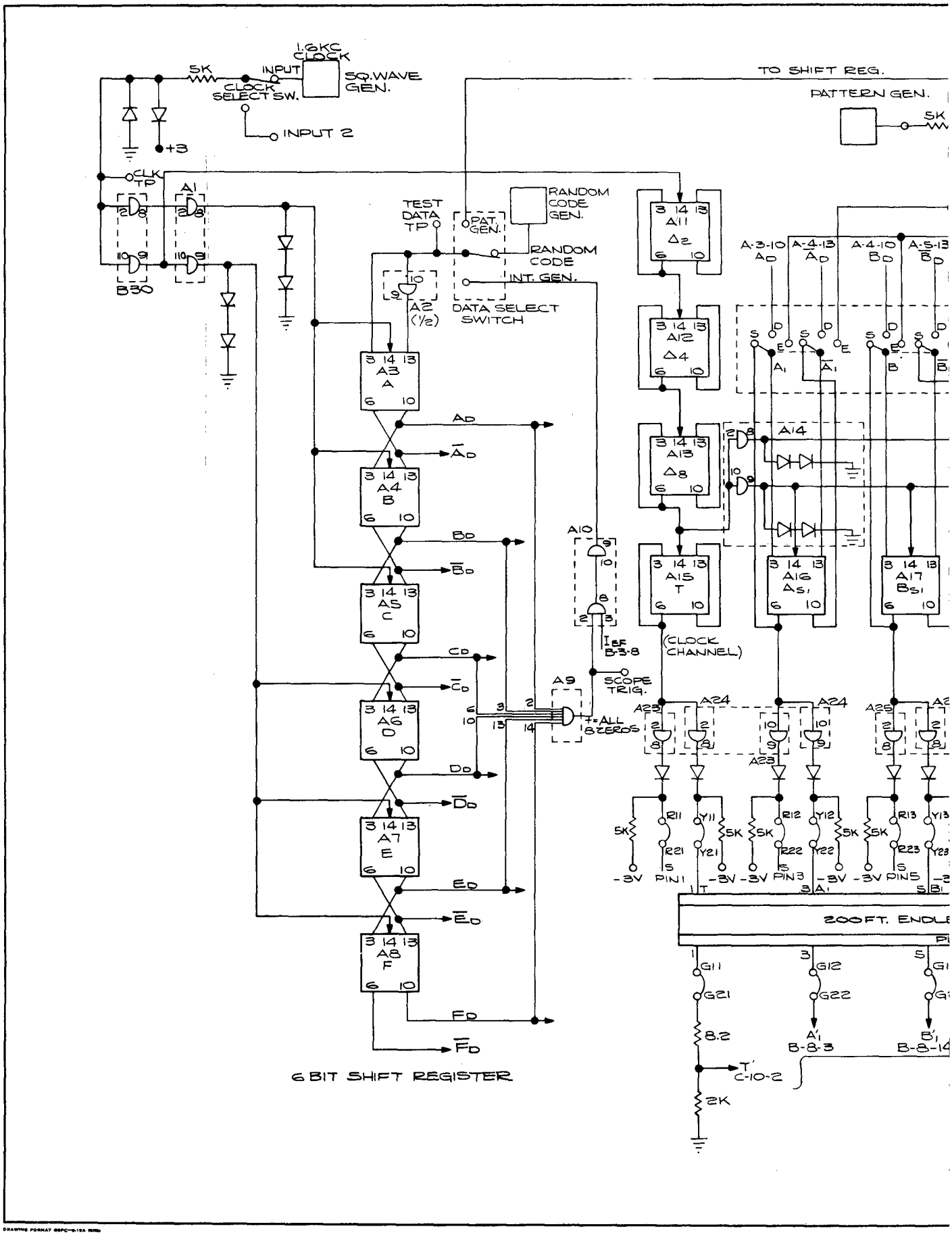
ACKNOWLEDGMENTS

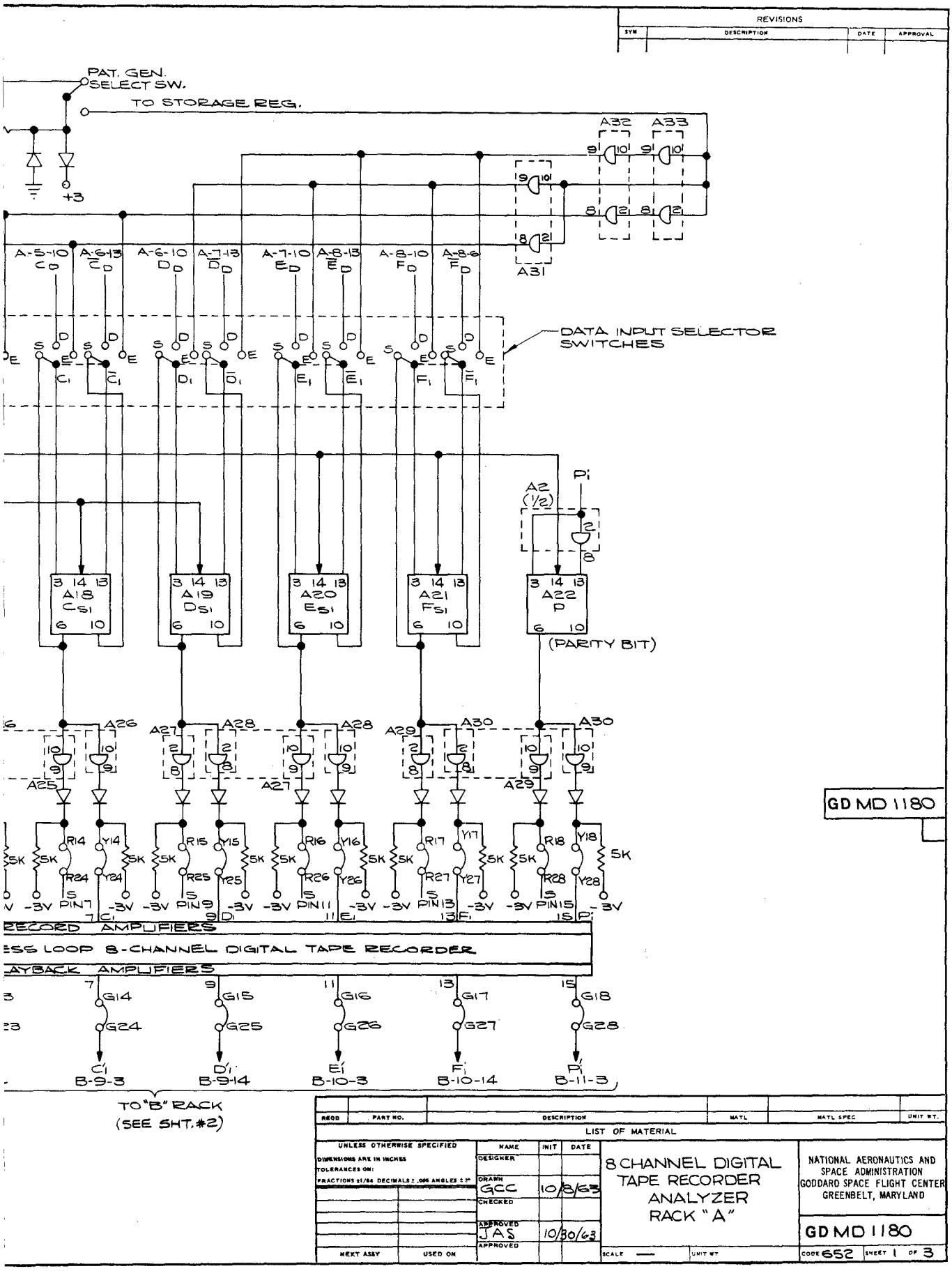
The author wishes to express his gratitude to Mr. Marvin S. Maxwell, Mr. Sebastian M. Costa, and Mrs. Marjorie R. Townsend for their assistance in preparing this paper.

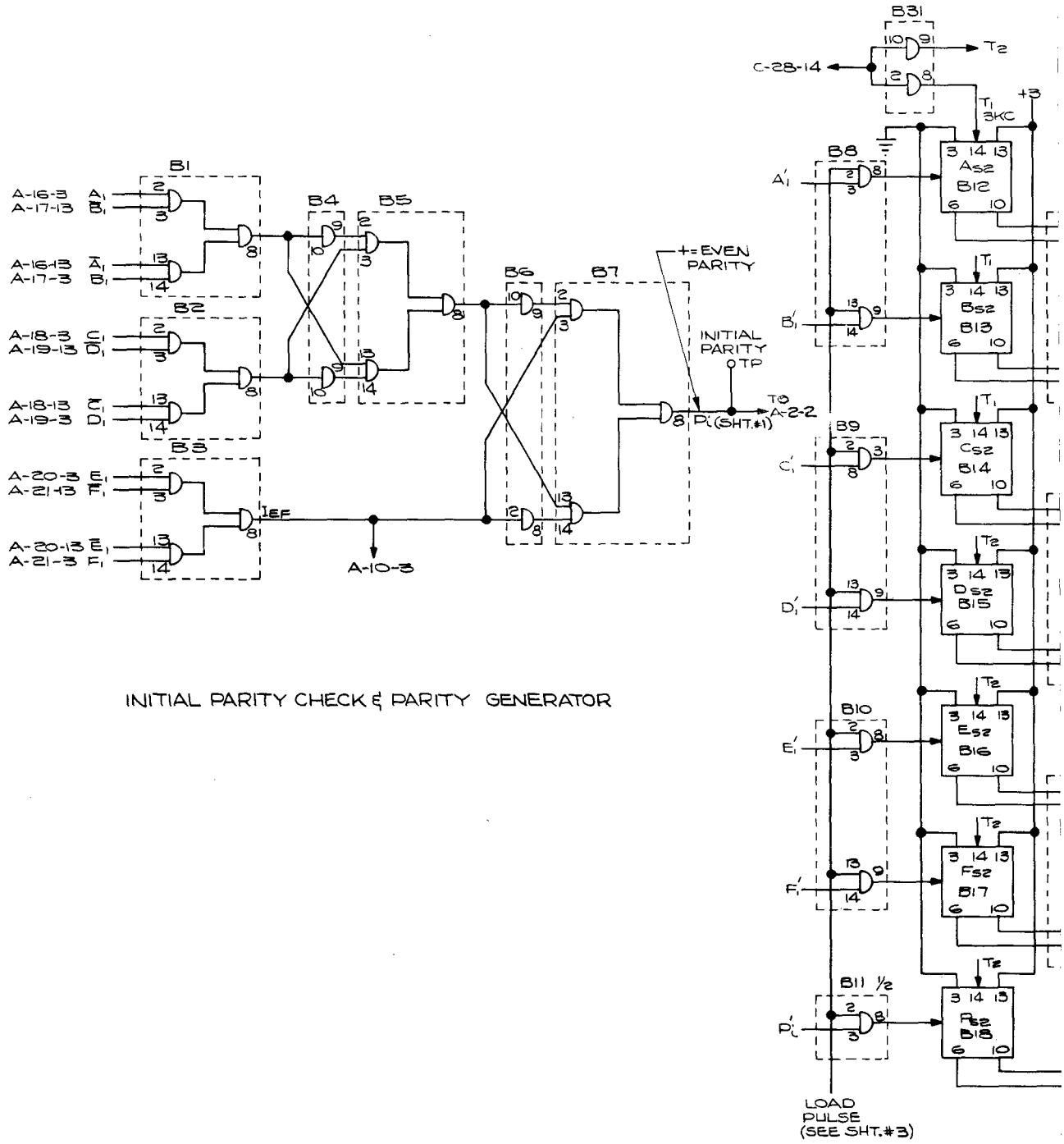
(Manuscript Received May 7, 1964.)

Appendix A

Complete Drawings and Component Listings


1.6KC CLOCK
5K
INPUT
SQ. WAVE GEN.
CLOCK SELECT SW.
INPUT 2
+3
TO SHIFT REG.
PATTERN GEN.
5K
CLK TP
A1
B30
TEST DATA TP
PAT. GEN.
RANDOM CODE GEN.
RANDOM CODE
INT. GEN.
DATA SELECT SWITCH
A2 (1/2)
A3 A
A4 B
A5 C
A6 D
A7 E
A8 F
A11 Δ2
A12 Δ4
A13 Δ8
A15 T
A16 As1
A17 Bs1
A14
A10
A9
SCOPE TRIG.
T=ALL 8 ZEROS
(CLOCK CHANNEL)
A23
A24
A25
-3V
PIN1
PIN3
PIN5
200 FT. ENDLE
G11
G12
G21
G22
8.2
2K
A'1 B-8-3
B'1 B-8-14
T' C-10-2
6 BIT SHIFT REGISTER

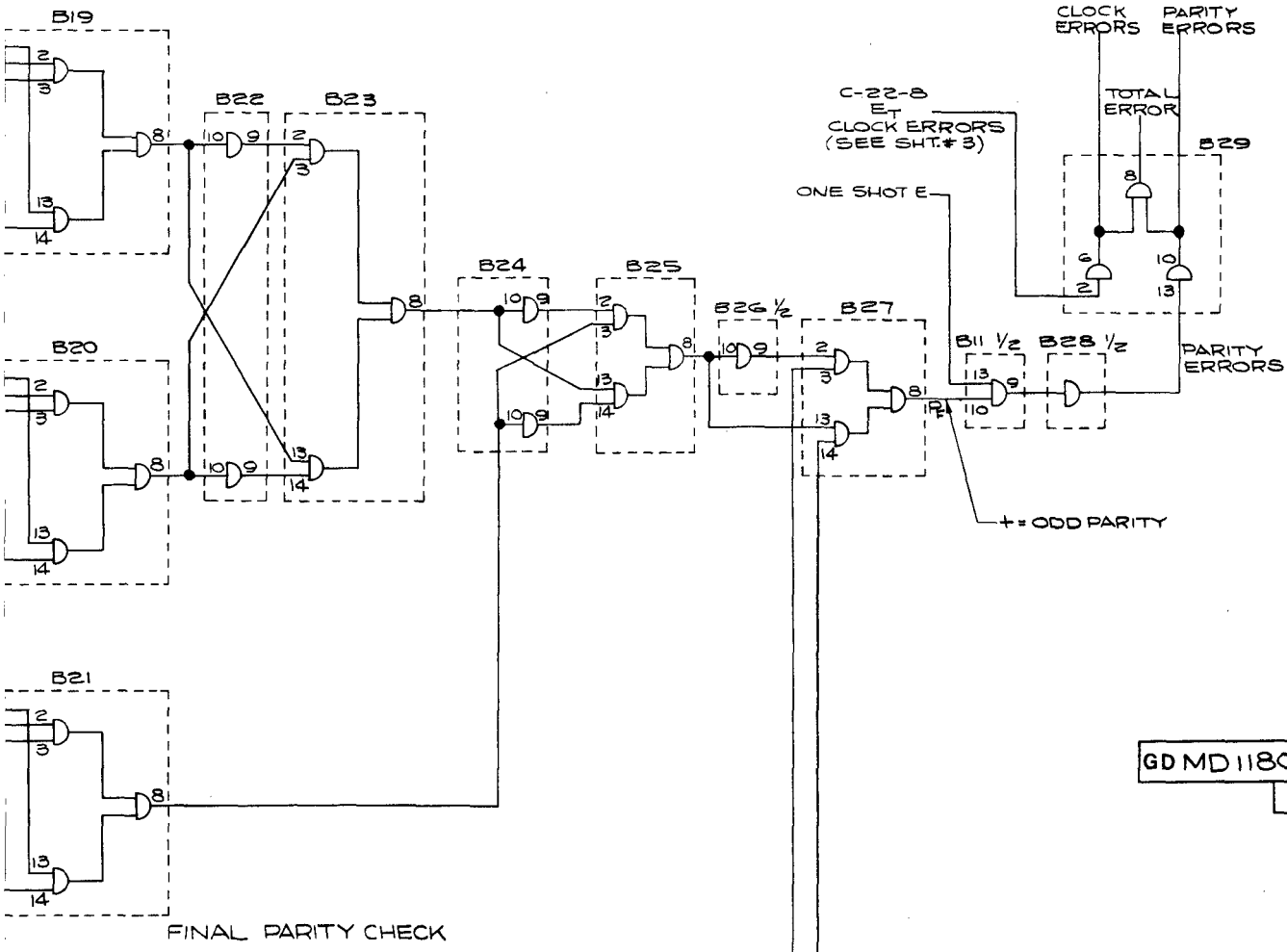

REVISIONS
SYM
DESCRIPTION
DATE
APPROVAL
PAT. GEN. SELECT SW.
TO STORAGE REG.
+3
A32
A33
A31
A-5-10 C_D
A-6-13 $\overline{C}_D$
A-6-10 D_D
A-7-13 $\overline{D}_D$
A-7-10 E_D
A-8-13 $\overline{E}_D$
A-8-10 F_D
A-8-6 $\overline{F}_D$
DATA INPUT SELECTOR SWITCHES
C_1
$\overline{C}_1$
D_1
$\overline{D}_1$
E_1
$\overline{E}_1$
F_1
$\overline{F}_1$
P_1
A2 (1/2)
A18 C_{S1}
A19 D_{S1}
A20 E_{S1}
A21 F_{S1}
A22 P
(PARITY BIT)
A25
A26
A27
A28
A29
A30
R14
Y14
R24
Y24
R15
Y15
R25
Y25
R16
Y16
R26
Y26
R17
Y17
R27
Y27
R18
Y18
R28
Y28
5K
-3V
PIN7
PIN9
PIN11
PIN13
PIN15
RECORD AMPLIFIERS
LOOP 8-CHANNEL DIGITAL TAPE RECORDER
PLAYBACK AMPLIFIERS
G14
G15
G16
G17
G18
G24
G25
G26
G27
G28
C_1'
D_1'
E_1'
F_1'
P_1'
B-9-3
B-9-14
B-10-3
B-10-14
B-11-3
TO "B" RACK (SEE SHT. #2)
GD MD 1180
REQD
PART NO.
DESCRIPTION
MATL
MATL SPEC
UNIT WT.
LIST OF MATERIAL
UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS ±1/64 DECIMALS ± .005 ANGLES ± 1°
NAME
INIT
DATE
DESIGNER
DRAWN GCC 10/8/63
CHECKED
APPROVED JAS 10/30/63
APPROVED
NEXT ASSY
USED ON
8 CHANNEL DIGITAL TAPE RECORDER ANALYZER RACK "A"
NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND
GD MD 1180
SCALE
UNIT WT
CODE 652
SHEET 1 OF 3



INITIAL PARITY CHECK & PARITY GENERATOR

7 BIT STORAGE REGISTER

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL

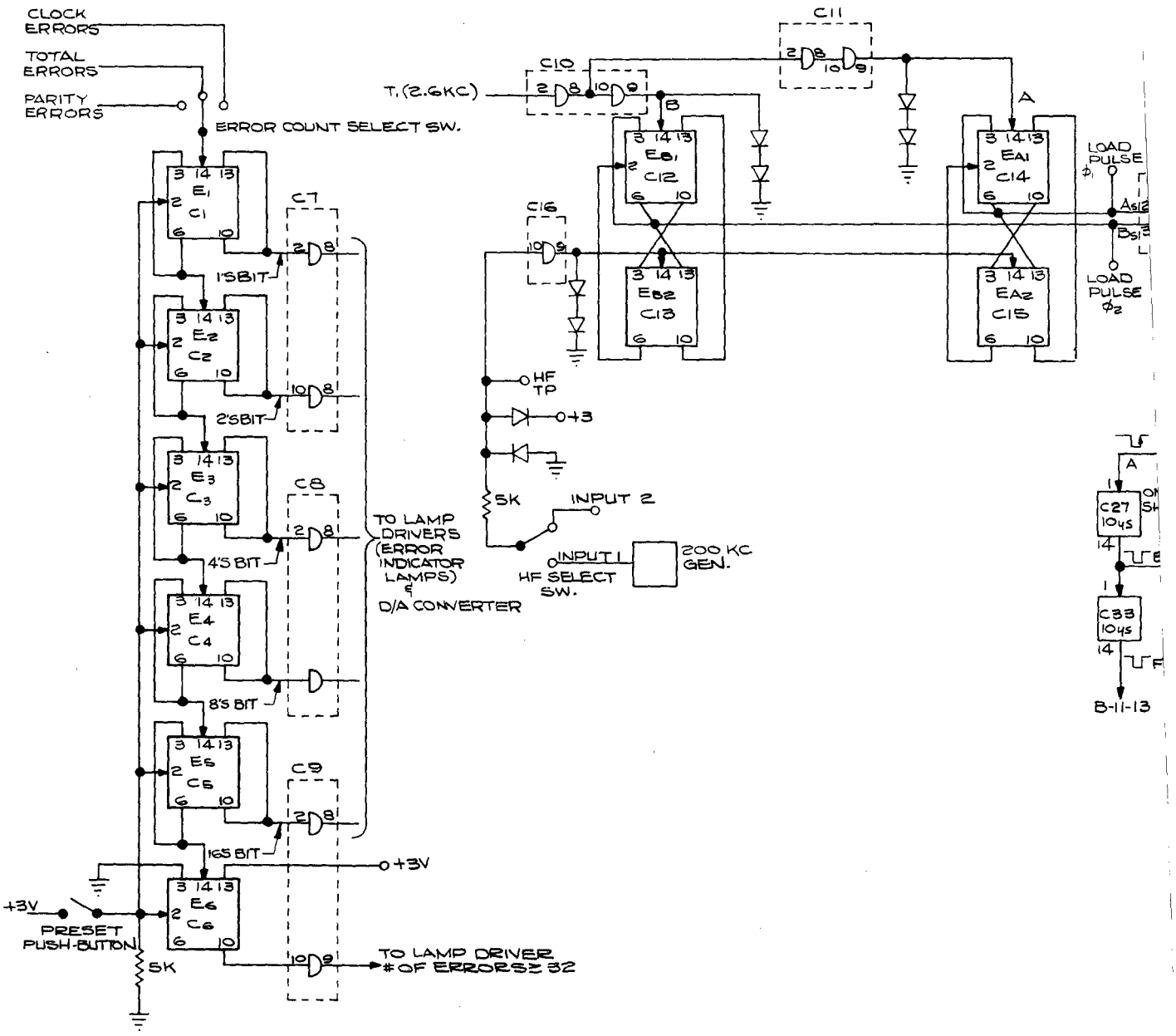


GD MD 1180

REQD	PART NO.	DESCRIPTION	MATL	MATL SPEC	UNIT WT.

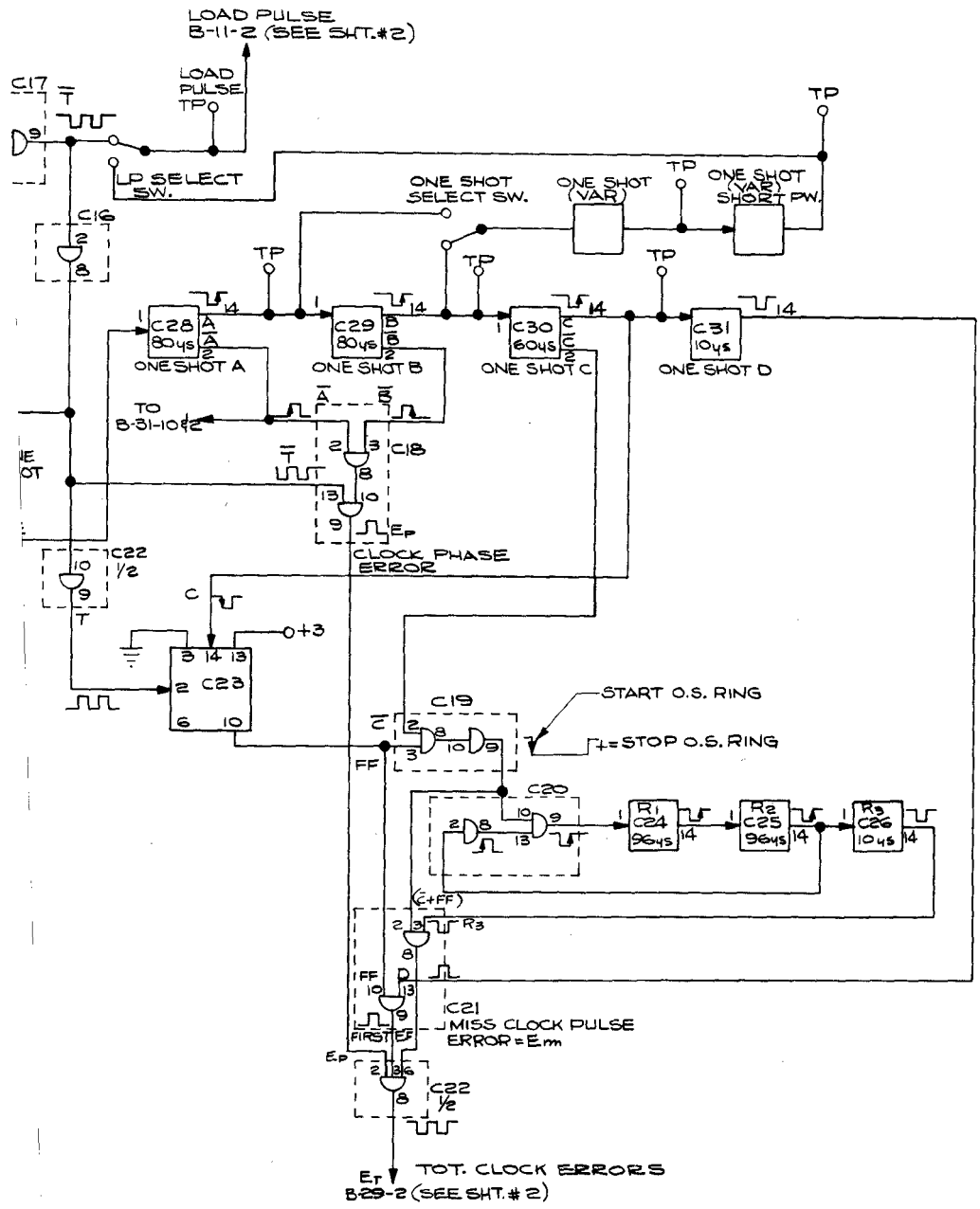
LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED	NAME	INIT	DATE		
DIMENSIONS ARE IN INCHES	DESIGNER			8 CHANNEL DIGITAL TAPE RECORDER ANALYZER RACK "B"	NATIONAL AERONAUTICS AND SPACE ADMINISTRATION GODDARD SPACE FLIGHT CENTER GREENBELT, MARYLAND
TOLERANCES ON:	DRAWN GCC		10/25/63		
FRACTIONS ±1/64 DECIMALS ±.005 ANGLES ±2°	CHECKED				
	APPROVED JAS		10/30/63		GD MD 1180
NEXT ASSY / USED ON	APPROVED			SCALE — / UNIT WT	CODE 652 / SHEET 2 OF 3



ERROR COUNTER

REVISIONS			
SYM	DESCRIPTION	DATE	APPROVAL



GD MD1180

REQD	PART NO.	DESCRIPTION	MATL	MATL SPEC	UNIT WT.

LIST OF MATERIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON:
FRACTIONS ±1/64 DECIMALS ± .005 ANGLES ± 2°

NAME	INIT	DATE
DESIGNER		
DRAWN GCC		10/28/63
CHECKED		
APPROVED JAS		10/30/63
APPROVED		

8 CHANNEL DIGITAL TAPE RECORDER ANALYZER RACK 'C'

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

GD MD1180

NEXT ASSY | USED ON | SCALE — | UNIT WT | CODE 652 | SHEET 3 OF 3

Component Listing*

Module Identification	Module Type	Module Identification	Module Type	Module Identification	Module Type
A-1	SN514	B-1	SN515	C-1	SN510
A-2	SN514	B-2	SN515	C-2	SN510
A-3	SN510	B-3	SN515	C-3	SN510
A-4	SN510	B-4	SN514	C-4	SN510
A-5	SN510	B-5	SN515	C-5	SN510
A-6	SN510	B-6	SN514	C-6	SN510
A-7	SN510	B-7	SN515	C-7	SN514
A-8	SN510	B-8	SN514	C-8	SN514
A-9	SN512	B-9	SN514	C-9	SN514
A-10	SN514	B-10	SN514	C-10	SN514
A-11	SN510	B-11	SN514	C-11	SN514
A-12	SN510	B-12	SN510	C-12	SN510
A-13	SN510	B-13	SN510	C-13	SN510
A-14	SN514	B-14	SN510	C-14	SN510
A-15	SN510	B-15	SN510	C-15	SN510
A-16	SN510	B-16	SN510	C-16	SN514
A-17	SN510	B-17	SN510	C-17	SN513
A-18	SN510	B-18	SN510	C-18	SN514
A-19	SN510	B-19	SN515	C-19	SN514
A-20	SN510	B-20	SN515	C-20	SN514
A-21	SN510	B-21	SN515	C-21	SN514
A-22	SN510	B-22	SN514	C-22	SN514
A-23	SN514	B-23	SN515	C-23	SN510
A-24	SN514	B-24	SN514	C-24	One-Shot 96 μsec $\{R_1\}$
A-25	SN514	B-25	SN515	C-25	One-Shot 96 μsec $\{R_2\}$
A-26	SN514	B-26	SN514	C-26	One-Shot 10 μsec $\{R_3\}$
A-27	SN514	B-27	SN515	C-27	One-Shot 10 μsec (E)
A-28	SN514	B-28	SN514	C-28	One-Shot 80 μsec (A)
A-29	SN514	B-29	SN515	C-29	One-Shot 80 μsec (B)
A-30	SN514	B-30	SN514	C-30	One-Shot 60 μsec (C)
A-31	SN514	B-31	SN514	C-31	One-Shot 10 μsec (D)
A-32	SN514	B-32	SN510	C-32	5 Lamp Drivers
A-33	SN514	B-33	SN510	C-33	One-Shot 10 μsec (F)

*1. Each module shown on the drawings is identified with a letter — number designation. The letter (A, B, or C) denotes the rack in which the module is located. The number (1 thru 33) denotes the particular socket in which the module is located.

2. Each module having a module type designation of 3 digits preceeded by an SN prefex is one of the Texas Instrument Series 51 micrologic modules. Additional information on this series of modules is available upon request. Any other module-type designation is a printed circuit card containing the circuitry described.

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—NATIONAL AERONAUTICS AND SPACE ACT OF 1958

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