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# HANDBOOK OF INSTRUCTIONS FOR MEC MODEL 76 COMPARATOR RECEIVING REGISTER

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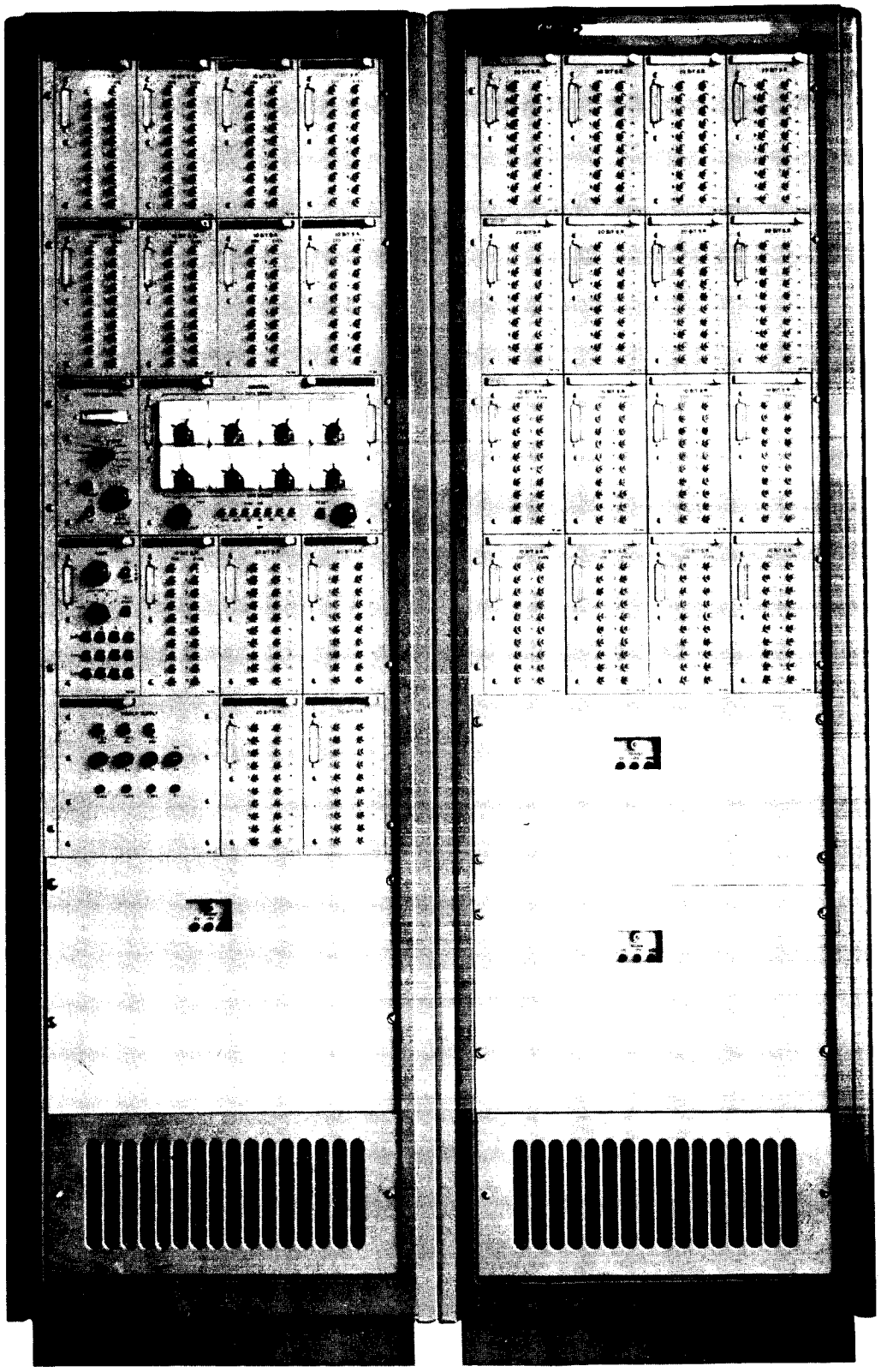


Figure 1-1. MEC Model 76 Comparator Receiving Register, Front View

# CHAPTER I

# INTRODUCTION

1-1. PURPOSE OF THE EQUIPMENT

The purpose of the Milgo Electronic Corporation (MEC) Model 76 Comparator Receiving Register is to receive a 408 bit serial word by means of 4 data lines (each data line presenting the same data) from a MEC Model 75 Data Receiver.* This data is processed and made available for a continuous readout. A complete word is received in 500 milliseconds. Also available from the output of the 75 Data Receiver are two control signals, "copy" and "EOW". The "copy" pulses are received one each millisecond and are used for shift register shifting purposes. The "EOW" pulse is presented at the end of each (408 bit) data word and is used for controlling the renewing of the new data to the outputs of the Comparator Receiving Register. This word is divided into three sections, "odd readout", "even readout" and "every readout".** The "odd readout" and "even readout" are renewed every 1000 milliseconds with the "odd readout" being renewed at the end of 500, 1500, 2500 etc. milliseconds, and the "even readout" being renewed at 1000, 2000, 3000 etc. milliseconds. The "every readout" is renewed every 500 milliseconds. There is a total of 171 "even readouts", 171"odd readouts" and 237 "every readouts". Each readout data line is available on MS plugs at the rear of the rack and will drive a load of 200 MA at -17 volts. A "1" is -17 volts and a "0" is 0 volts. These outputs are to be used for the input of D-A converters and to operate digital displays.

1-2. SCOPE OF THE MANUAL

This instruction manual describes the MEC Model 76 500 Bit Receiver, designed and manufactured by Milgo Electronic Corporation for International Business Machines, Federal Systems Division, Kingston, New York, in conjunction with Project Mercury.

1-3. PURPOSE OF THE MANUAL

1-3.1. This instruction manual is provided as an aid to better understanding the operation and theory behind the MEC Model 76 500 Bit Receiver and its associated equipment. It offers a complete technical explanation coupled with applicable illustrations, with an estimation of the interest and questions of the qualified technician.

1-3.2. It is strongly urged that the operator, or any person involved in the operation of this equipment, thoroughly read and fully understand the contents of this manual.

* In reference to unit title, COMPARATOR RECEIVING REGISTER and 500 BIT RECEIVER are interchangeable.

** In reference to frame bit terminology, the term, "every" and the term, "common" are interchangeable as used in conjunction with frame bit designations "odd" and "even".

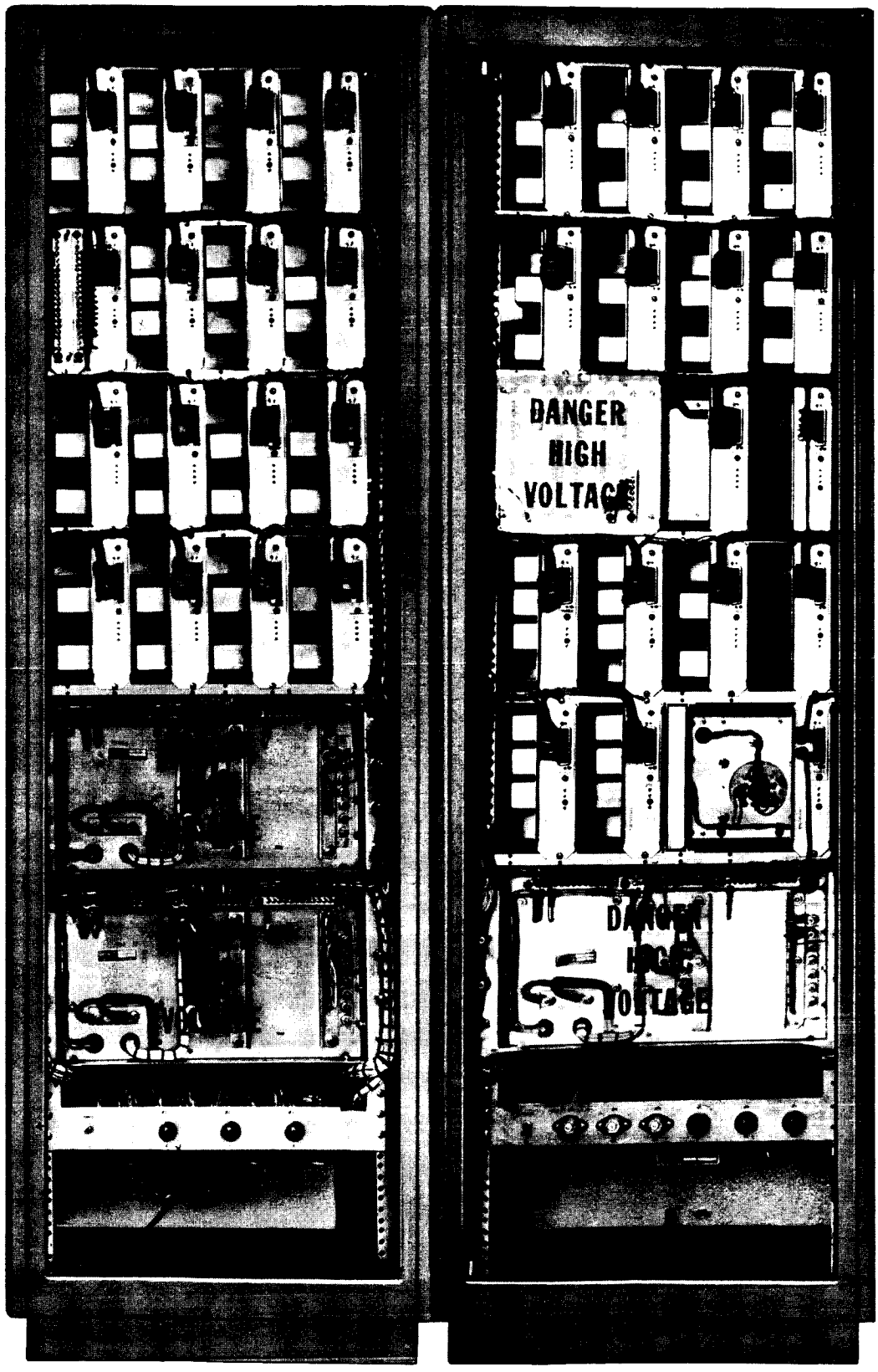



Figure 1-2. MEC Model 76 Comparator Receiving Register, Rear View

# CHAPTER II
# GENERAL DESCRIPTION

## 2-1. GENERAL

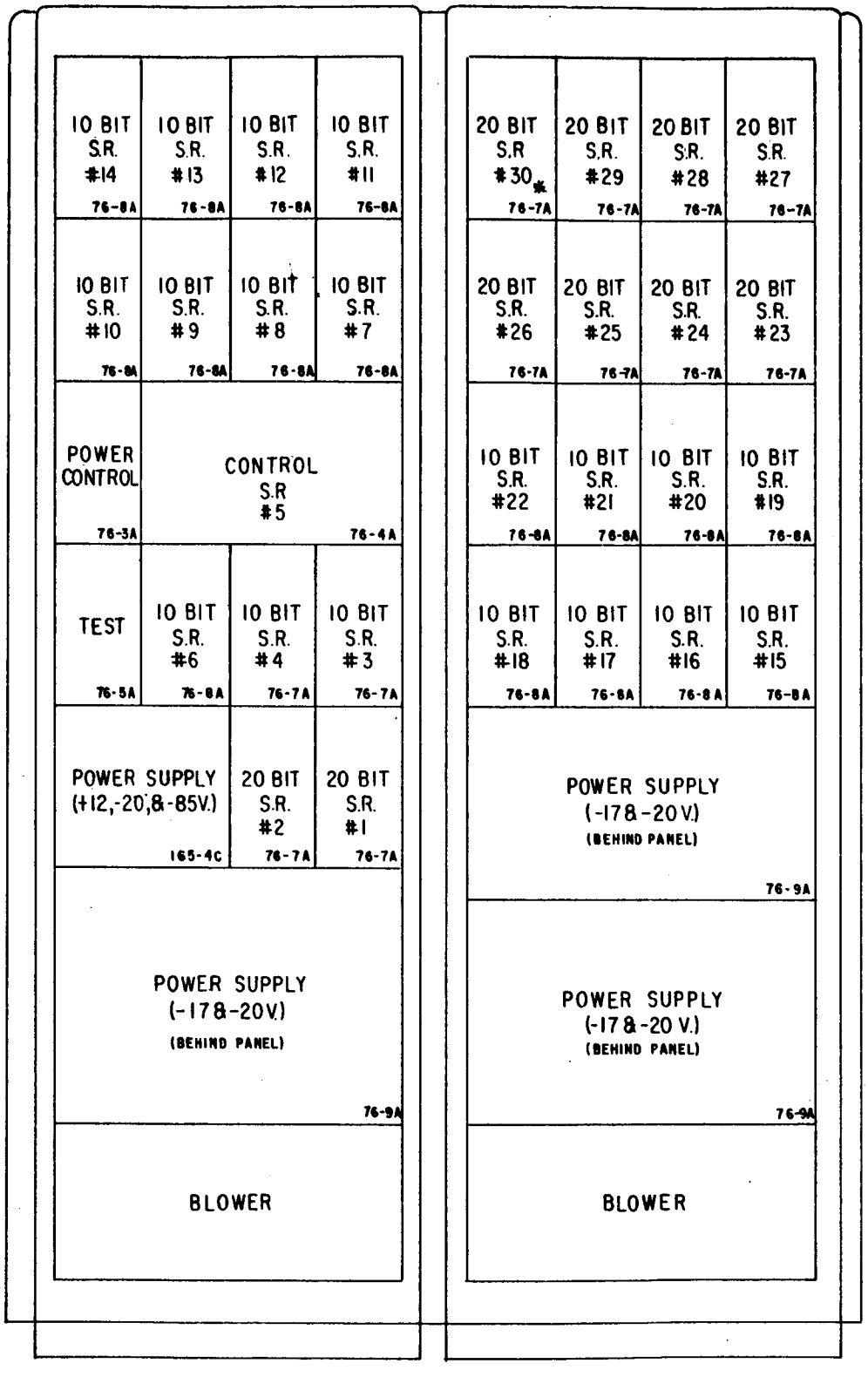
MEC Model 76 500 Bit Receiver receives a 408 bit data word from a MEC Model 75 Receiver. The data is received by means of four independent data lines, each line having the same data present. Two control inputs, Copy and EOW are also provided by means of four input lines. A comparison circuit selects three of the four data lines, compares them with each other, and a composite data bit is obtained on the basis of at least two of the three data lines being alike and correct. The reason for the redundancy is to provide a more reliable input of correct data (as it is remotely impossible for all inputs to be inoperative at same time). A comparison circuit within the 500 Bit Receiver will select 3 of the 4 input lines and make a 2 out of 3 comparison with a resultant which should have eliminated all data errors. The data under control of the Copy pulses is shifted through the 408 Bit Shift Register. Upon receipt of the EOW, bits #84 and #85 are compared to determine if the data word is an "odd" frame or an "even" frame. If the data is in an "odd" frame, then a portion of the data is put into parallel readout storage in one group of flip-flops ("odd" data storage) and if the data is an "even" frame, then the same portion of the data is put in storage in a different set of flip-flops ("even" data storage). A second portion of the received data is always put in the same storage group ("every" data storage). Each time a new data word is received, the old data is erased and the new data is inserted. Data remains in the parallel readout flip-flops at all times, except for approximately 100 microseconds out of 500 milliseconds when the new data is being inserted. The input data word is divided into 171 "even-odd" bits and 237 "every" bits. A control pulse for the D/A Converters is provided as "D/A hold". A new word is processed every 500 milliseconds.

## 2-2. PHYSICAL DESCRIPTION

2-2.1. The 500 Bit Receiver is housed in two standard Milgo type 1007-41 Racks which are 74 1/8" high, 23 9/16" wide and 22" deep. The two racks are set side by side and occupy a floor space of 48" by 22". To facilitate the opening of the rear doors there must be 24" clearance; no side clearance required. The individual chassis which make up the Receiver are of modular construction and are locked in place by a single screw type locking handle. The following chassis are utilized in the Receiver:

| QUANTITY | NOUN NAME | MODEL NO. |
|---|---|---|
| 1 | Power Control Chassis | 76-3A |
| 1 | Control Chassis | 76-4A |
| 1 | Test Chassis | 76-5A |
| 12 | 20 Bit Shift Register Chassis | 76-7A |
| 17 | 10 Bit Shift Register Chassis | 76-8A |
| 3 | Power Supply | 76-9A |
| 1 | Power Supply | 165-4C |

2-2.2. In one of the 20 Bit Shift Register Chassis there is a plug-in modification. This plug-in modification is illustrated in Figure 2-2. This particular 20 Bit Shift Register is located in the upper left hand corner of the right hand rack as shown in Figure 2-1.




* has plug-in modification

Figure 2-1. Chassis Arrangement

## 2-3. DATA INPUTS

There are four data inputs, four Copy inputs and four EOW inputs. Each of the data inputs, Copy inputs and EOW inputs receive the same information by means of four independent channels; this is for reliability purposes. This will be described in detail in Chapter 3, Theory of Operation. The data input pulse for a "1" is 0 volts and for a "0" is -14 to -20 volts. The width of the data "1" is 1 millisecond -20 microseconds. The Copy pulse is a positive pulse (from -20 volts to 0 volts) with a width of 400 microseconds. The EOW pulse is identical to a data "1" pulse. There is one requirement on the input pulses; the leading edge of the input pulse coming on the four independent lines must be within 300 microseconds between the first and the last pulse which arrive at the 500 Bit Receiver.

## 2-4. DATA OUTPUTS

Since the 500 Bit Receiver is used to receive data in serial form and to present it in a continuous parallel form there are many data outputs. These data outputs are divided into three categories, "every" output, "even" output, and "odd" output. There are 237 "every" outputs, 171 "even" outputs and 171 "odd" outputs; i. e., a total of 579 outputs. There is also one D-A "hold" output. The discussion on how "even" and "odd" outputs are derived will be discussed in Chapter 3, Theory of Operation.

## 2-5. POWER INPUT

The Power Input may be either 115vac ±10%, 60 cycles ±10%, single phase with an input current of less than 50 amperes or it may be 3 phase with an input of less than 15 amperes per phase. This power is connected to connector J98. If the input is a single phase input, pin A, B, and C are jumpered together for the "hot" input and pins D and E are jumpered together for the ground input. If a 3 phase wye connection input is used, one phase is connected to terminal A, the second phase to terminal B, the third phase to terminal C and the ground return connected to terminal D.

## 2-6 BLOWER

Each rack is equipped with a McLean Blower which is located in the lower portion of

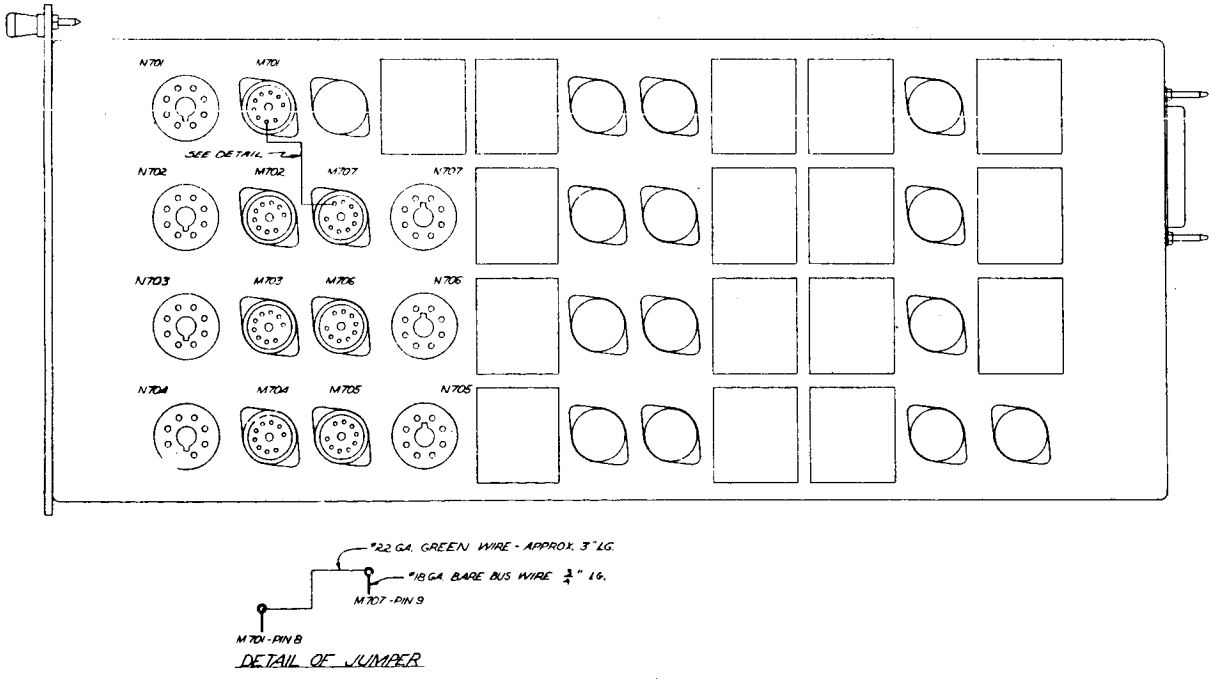



Figure 2-2. Plug-in Modification

each rack. The Blowers provide enough air circulation to maintain adequate cooling when the environment temperature is between 10 and 40 degrees centigrade. The Blowers should be operated to their maximum when the equipment is in operation.

# CHAPTER III

# THEORY OF OPERATION

## 3-1. INTRODUCTION

In this chapter, the 500 Bit Receiver, each Shift Register Chassis, the Control Chassis, the Test Chassis and the Power Control Chassis are described in detail as to their operation and function. The 165-4C Power Supply and the 76-9A Power Supply are described in full detail in Chapter 10, Appendix of this manual. Also found in the Appendix of this manual is a full description of each of the TN networks used within the racks and also a full description on the operation of the MN11 magnetic core used in a magnetic core shift register. The applicable sections of the Appendix should be consulted by the reader.

## 3-2. GENERAL THEORY (Figure 9-16)

The 500 Bit Receiver contains a 408 bit serial shift register which is made up of magnetic cores. The output of each core is applied to the appropriate gate on the input of a flip-flop which is used for the parallel outputs of the 500 Bit Receiver. The data is brought in in a serial format which is shifted down the 408 bit shift register. Then, at the proper time, the information is transferred into the continuous readout flip-flops which are found in each Shift Register Chassis. A portion of the output format requires that the data, in alternate words, be presented to two different sets of flip-flops. These flip-flops are provided in the 10 Bit Shift Registers. When proper signals are given to these Shift Registers, alternate words are stored in alternate sets of flip-flops. Consult paragraph 3-7 on the 10 Bit Shift Register for this operation. The remainder of the data word will be inserted into the same flip-flops each time a data word is received. These flip-flops are located in the 20 Bit Shift Registers and transfer the new data into the same group of flip-flops each time a new word is received. A second function of this Receiver is to make the two out of three comparison which is fully described in paragraph 3-3 on the Control Chassis. This two to three comparison is made so that a more reliable output may be resolved from the input data. The data is brought in on four independent data lines, and by proper selection by the operator with a selector switch, three of the lines are selected. A comparator network makes a two out of three comparison so that a single output line is made available in which this detected output has been resolved. This data is then shifted through a 408 Bit Shift Register, the driving signal being synchronized with a resolved copy pulse which is resolved in the same fashion as the data signals. When a complete data word has been put into storage, an EOW signal will be generated by the MEC Model 75 Receiver, which will signify to the 500 Bit Receiver to transfer the data from the series cores to the parallel flip-flop outputs. This EOW triggers the necessary circuits which perform the function of checking to see if the "even" frame bit or the "odd" frame bit (bits #85 and #84) is present (only one can be present at a time). If both bits are present, the data is rejected. If either the "even" frame or the "odd" frame bit is present, but not both, then this data is accepted and is put into the output storage flip-flops. The old word is erased 100 microseconds before the new word is put into storage. If both bits #84 and #85 are present, or if both of them are "0", the whole data frame is rejected and a new frame is shifted in. This prevents the presenting of erroneous data to the outputs of the 500 Bit Receiver. There are error detectors which the output reads into a voltmeter located on the front panel of the Control Chassis and these indicate the percentage of

errors found on any one of the input data lines and the error rate on any one of input EOW lines. A D-A hold signal is provided so that D-A Converters may hold the last data received during the transposition period from when the old data is erased and the new data is inserted. This transposition period should be on the average of 100 microseconds, but in no case should it ever be longer than 200 microseconds. The D-A hold signal will be at -17 volts during this transposition period for approximately 3 or 4 milliseconds. Since the bits #84 and #85 have the control operations in them and are somewhat in the middle of the data word, the 20 Bit and 10 Bit Shift Registers form a row on both sides of the Control Chassis (Figure 9-16). Data flows through N401, through comparator N410, and then into core M401. The data output from core M401 goes to Shift Register #30 through #6. The output of Shift Register #6 flows back into the Control Chassis to six magnetic cores (M460 through M465) which constitute Shift Register #5. The output of core M465 then goes back to the input of Shift Register #4 and is shifted down through Shift Registers #3 and #2, and then to Shift Register #1. This constitutes the serial data path. The parallel output of these Shift Registers are wired to the output plugs found in the rear bottom of the rack. There are a total of 237 "every" outputs, 171 "even" outputs, 171 "odd" outputs and 1 D-A hold output, making a total of 580 outputs. Each output can drive an output load of 200 milliamps of current at -17vdc. The parallel output of the Shift Registers are so designed that they may drive directly into D-A converters and directly illuminate digital display boards. The power necessary for the operation of the Shift Registers and also to produce the necessary current to drive the output requirement of the parallel outputs are provided by four Power Supplies. The small Power Supply (165-4C) is used for the necessary voltage for the operation of the Control Chassis, to produce the necessary voltage for reversed bias of the networks found in the complete system, and also to furnish the necessary voltage for indicator light operation. The three large Power Supplies (76-9A) are used to furnish the necessary voltage for the operation of the Shift Registers and also to produce enough current in order to drive the output lines. The output load of the three MEC Model 76-9A Power Supplies is equally divided by the connection of a group of Shift Registers to each. This will give an equally distributed load on the outputs of the three -17 volt 40 ampere Power Supplies.

## 3-3. CONTROL CHASSIS, MEC Model 76-4A (Figures 9-1, 9-2, and 9-3)

3-3.1 There are four independent input data lines which go through the Test Chassis through a normally closed set of relay contacts and then directly to pins 1, 2, 3, and 4 of input plug P401. Each input data line has the identical data as the next one. Four input data lines are utilized in order to increase the reliability of the data, since it has been received from a Receiver which receives the data by means of a long transmission line. The input data has the following specifications: a "1" is 0 volts, and is 1 millisecond -20 microseconds in width; a "O" is from -14 to -20 volts (i.e., a "0" is the absence of a pulse). These four data inputs are applied as the input to network N401 which consists of four clamped emitter followers. The outputs of network N401, are 0 volts for a "1" and -12 volts for a "0". Network N401 is transistor network 161 which is explained in detail in the Appendix under the heading TN161. The -12 volts is a "0" regardless whether the input was -14 volts or lower to a maximum of -20 volts. The four outputs of network N401 are applied to a selector switch S401A. Of the four inputs to S401A, one is rejected and therefore there are only three outputs from the switch. This is the switch in which the operator has the choice of selecting the three best input data lines out of the four possible choices. Each of the three outputs may be 0 volts or -12 volts. The three outputs from this selector switch are applied as follows: the first to resistor R414, the second to resistor R415, and the third to resistor R416. The summing junction of these three resistors is the input of pulse amplifier N410 (TN159 in Appendix). This pulse amplifier has a clamping action at -6 volts, as determined by a zener CR412 and resistor R439. If the three inputs to the three previously mentioned resistors are 0 volts, then the summing junction would seek to go to 0 volts. If one of the inputs was at -12 volts and the other two were at 0 volts the summing junction would seek to be at -4 volts, and if one of the inputs were at 0 volts and two of the inputs were at -12 volts the summing junction would seek to be at -8 volts. Since the limiting action was chosen at -6 volts, the pulse amplifier will produce a positive pulse if the input to pin 3 is more positive than -6 volts. So if two of the inputs are at 0 volts then the pulse amplifier will produce an output pulse on pin 8 of N410. If two of the inputs are at -12 volts there will be a "0" output or no pulse on pin 8, N410. If a "1" or 0 volts is on the output of N410, this is applied to pin 5 of core M401 through resistor R413 and diode CR405. In order that this data may be inserted into core M401, pin 4 must be at -20 volts so that there would be a

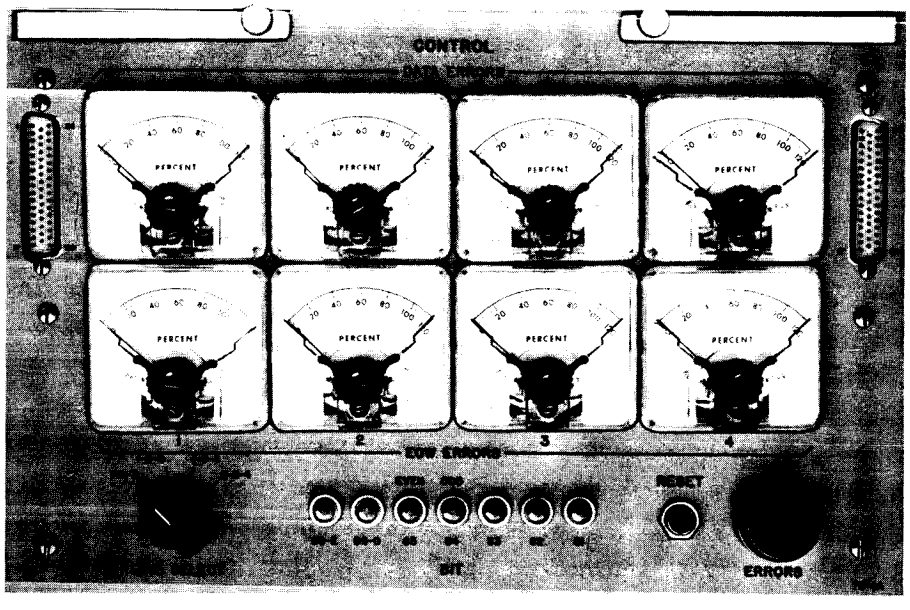



Figure 3-1. Control Chassis

current in the windings of the core. This current will only be present if the input to resistor R413 is near 0 volts and if pin 4 of core M401 is near -20 volts, at which time there will be 20 milliamps of current flowing in the windings of the core. If the gate pulse is not present, then pin 4 is at 0 volts and no current would flow when there was a "1" output from pulse amplifier N410. Diode CR405 prevents a reverse current from flowing when a "0" (-20 volts) is present on the output of the pulse amplifier N410. This gate is operated by the copy pulse after it is received and detected by the 500 Bit Receiver.

3-3.2 The copy pulse is received in the same way in which the data pulse was received. The copy pulse is applied to emitter follower N411 (TN161 in Appendix) through switch selector S401B and then is the input to pulse amplifier N412 (TN159 in Appendix) which operates in the same fashion in which the previously discussed data inputs operated. The output of pulse amplifier N412 triggers a 400 microsecond one-shot N413 (TN111 in Appendix) which is used to delay the detected copy pulse before the data is gated into core M401. This delay is in order to give enough time for the input data to arrive if there is some time displacement between any of the input data lines. The delayed output of N413 triggers one-shot N414 (TN111). One-shot N414 performs three functions:

a. It immediately opens the data gate to core M401 via emitter follower N416B.

b. It immediately triggers flip-flops N418 and N419 to the "1" condition (the input gate, consisting of resistors R423 and R424, to flip-flops N418 and N419 has been opened).

c. The delayed output triggers core driver N415.

This input gate, consisting of resistors R423 and R425, is open only during one of the pulses from N414 and the time is EOW time. The EOW time is discussed in detail later. At this time, this pulse from N414 does not operate on the two flip-flops. The delayed output of N414 has been delayed an additional 100 microseconds. Core driver N415 is basically a heavy duty power amplifier which produces a positive going pulse from -20 volts to 0 volts on pin 8 of N415. Magnetic cores M402 and M403 are used to determine the width of the core drive pulse of TN130B. The drive pulse will be formed each time a copy pulse has been detected, which normally will be one each millisecond. There are a total of 408 normal input data pulses which will be received on all four input data lines, each being received with a copy pulse. The copy pulse is used to generate a core drive pulse to shift the data through a magnetic core Shift Register. The magnetic core Shift Register consists of 410 cores. The data will be in only 408 of these cores. Of the remaining two cores, one is used for delay purposes and the other for data input purposes. When the total word (which is 408 bits long) has been received, detected, and put into storage, an EOW pulse will be received on each of the four input lines. The EOW pulse is applied to the four clamp emitter followers found in N420, then goes through switch S401C, and is then detected by pulse amplifier N417 in identically the same way as which the data was detected. When the EOW is detected, a positive pulse on pin 8 of N417 will be formed. This pulse will remain at 0 volts for at least 1 millisecond. When pin 8 of pulse amplifier N417, is at 0 volts the gate previously mentioned of resistors R423 and R424 is open, so that the copy pulse associated with the EOW pulse will trigger flip-flops N418, and N419 to the "1" condition. Pin 8 of flip-flop N418 will go from 0 volts to -17 volts (a "1") which is used as a D-A hold signal. Pin 8 of flip-flop N419 will produce a positive going pulse which will trigger one-shot N478 (through capacitor C496) and produce a positive pulse from -20 volts to 0 volts on pin 7 of the network. This pulse is used as an inhibit input to pulse amplifier N412. N412 is used to detect the incoming copy pulses. When pin 1 is at 0 volts it will be noted that the output stage of the pulse amplifier has no voltage across the transistor; therefore there can be no output pulse generated by this

pulse amplifier. This circuit is now operating as an inhibit "and" gate. This prevents the occurrence of an output pulse from pin 8 of pulse amplifier N412, during the time in which one-shot N478 is in the "1" condition; N478 in the "1" condition for approximately 2 milliseconds. This allows time for the EOW signal to do the necessary gating so that the previous incoming word may be transferred in paralled to the output flip-flop. The same output pulse from pin 8 of flip-flop N419 which triggered one-shot N478, also opens up a series of three "and" gates. These three "and" gates each consist of two resistors. The first consists of resistors R471 and R472, the second of resistors R477 and R478, and the third of resistors R487 and R488. These "and" gates will be open when the next core drive pulse appears. This core drive pulse will appear in 100 microseconds and is generated by the last copy pulse which went through the pulse amplifier N412. The copy pulse is delayed a total of 500 microseconds by N413 and N414. This core drive will happen exactly 100 microseconds after the three resistor "and" gates open by flip-flop N419. This delay is the delay created by one-shot N414. Because the three "and" gates are open, the core drive pulse triggers the one-shot N470 (whose delayed output triggers one-shot N471 in 500 microseconds) and drives any data which may be present in cores M460 and M461 through the "and" gate consisting of R471 and R472, and the "and" gate of R477 and R478. These two cores should have the "odd-even" frame data in them at this time. If the system is operating correctly one of the two cores will have a "1" and the other will have a "0". If the "1" is in core M460 it is considered an "even" frame; if the "1" is in core M461 it is considered an "odd" frame. There is a provision, as described later, to prevent erroneous data from being parallel transferred if both of these data bits have a "1" or if both of them have a "0". In either case it would be uncertain as to which is an "odd" frame or which is an "even" frame, therefore the data is not transferred but a new word is shifted in the Shift Registers. The operation of this circuit is as follows. When this core drive previously mentioned drove a "1" out of one of the two cores, in the first case out of core M460, it goes through capacitor C463 through the open "and" gate consisting of resistors R471 and R472 and triggers flip-flop N468 to the "1" condition. If there is no pulse in M461 there would be no pulse through the "and" gate consisting of resistors R477 and R478 and thus there would be no pulse to trigger flip-flop N469. Therefore it will remain in the "0" condition. To assure that flip-flop N469 will be in the "0" condition, another pulse of core M460 is coupled to the reset input of this flip-flop, pin 6. The 4 to 5 winding output of magnetic core MN11 has a 10 microsecond output on the auxiliary winding and has a 40 microsecond output on the pin 9 output; thus if both core M460 and M461 had a "1" in it and each "1" went through its associated "and" gates and triggered both flip-flops to the "1" condition the pin 9 output of these two cores would trigger both flip-flops back to the off or "0" condition. So it can be clearly seen that at this time in order for either flip-flop N468, or N469 to be in a "1" condition, a single "1" must be present in core M460 or M461 and not both. If either of the two cores has a "1" output, then one or the other of the two flip-flops will be in the "1" condition and the other in the "0" condition. In normal operation at the end of each incoming word this condition will alternate back and forth between the two flip-flops. If flip-flop N468 is in the "1" condition, then an "and" gate consisting of resistor R491 and resistor R492 will be open and the output of one-shot N471 which was triggered by the same core drive will now trigger one-shot N474. The reason that the same core drive which triggered N470 which in turn triggered N471 can go through this "and" gate, is that it was delayed a significant time (500 microseconds) by one-shot N470 so that the flip-flop and "and" gates have obtained a stable condition. The output of one-shot N474 serves for three functions: (a) it produces the "every reset" pulse, necessary for operation of the 10 Bit Shift Register, (b) it goes through an "or" gate consisting of diodes CR465 and CR466 and triggers one-shot N475 which produces the "every reset"; and (c) N474 also triggers one-shot N477 which produces the "even gate" pulse necessary for the 10 Bit Shift Registers. The output of one-shot N475 which developed the "every reset" also triggered one-shot N476 which produces the "every gate" pulse. It will be noted here that the reset pulses are 10 microseconds wide and the gate pulses are 200 microseconds wide. The reset pulses are used to reset the

parallel output flip-flops consisting of transistor networks TN144's (of the Shift Registers) into the "0" condition so that the new data can be inserted. These will be discussed when the operation of the Shift Register (consisting of cores M460 through M465) are described in Shift Register operation. This previously discussed pulse generation was caused when core M460 had a "1" in it at this time, but if it had a "0" and core M461 had the "1" in it, a little different operation would occur. Flip-flop N469 would have been in the "1" state and the "and" gate consisting of resistors R489 and R490 would be open and the other "and" gate consisting of resistors R491 and R492 would have been closed. In this case one-shot N472 would have been triggered which would have produced the "odd reset" pulse and also would have triggered one-shot N473, which produces the "odd gate" pulse. The output of one-shot N472 would have also triggered one-shot N475 through the "or" gate consisting of diodes CR465 and CR466, which would have produced the "every reset" pulse and also have triggered one-shot N476 which would have produced the "every gate" pulse. It should be noted here that in one case, "odd" and "every" set of pulses were developed; in the other case an "even" and "every" set of gate pulses were produced. In both cases there was a total of four pulses produced, two resets and two gates. One set of resets and gates are used for the 20 Bit Shift Register and the other for the 10 Bit Shift Registers. The reason for an "even" gate and an "odd" gate, is so that it can be determined in the 10 Bit Shift Register to exactly which set of output flip-flops to transfer the new data. If the outputs of cores M460 and M461 had both been a "0" or both been a "1", the flip-flops N468 and N469 would have both been in the "0" condition and both "and" gates associated with the flip-flops would have been closed. Therefore, there would have been no reset and gate pulses produced. This circuitry prevents the insertion of erroneous data into the parallel output flip-flop. The only way in which both of these cores could have the same information is when an error is produced somewhere between the remote Computer developing the data and to the complete Transmission System. Diodes CR494 and CR495, and resistor R4148 form a test circuit operated by the ODD NORM EVEN switch located on the Test Chassis. When this switch is in the EVEN position, +12 volts is applied to pin 33 of P401. This voltage forces both flip-flops N468 and N469 to the "1" condition and also prevents one-shot N473 from producing a pulse by clamping the collector of transistor Q1 to a positive voltage and preventing one-shot action. This is to prevent the operation of the #84 and #85 bit comparison, thus allowing an all "1"s and an all "0"s test pattern. Diodes CR493 and CR492, and resistor R4147 operate in the same manner for the ODD test pattern. This is active in test operation only. One of the outputs of N471 was previously discussed, but it has a delayed output (pin 5). This delayed output has somewhere from 3 to 4 milliseconds of delay which produces a positive going pulse which is the delayed portion of the pulse and will trigger flip-flop N418 back to the "0" condition. This will restore the D-A hold signal back to 0 volts. The positive going signal pulse from N471 which caused the gate and reset pulses to open also triggered flip-flop N419 back to the "0" condition so that it would be prepared for the next EOW pulse which would arrive in 500 milliseconds. This same pulse which triggered flip-flop N419 to the "0" condition also triggers one-shot N414 in order to produce one more core drive pulse. This core drive pulse will be delayed 100 microseconds from the time which the "even" or "odd" and "every" gate were opened. The gates were open the same time in which N414 was triggered, therefore in the middle of the 200 microsecond gate "every" gate, "even" gate or "odd" gate, there will come a core drive pulse. This core drive pulse will then drive the data from the auxiliary windings of the magnetic cores in all of the Shift Registers of the system so that they may insert data into the parallel flip-flops. The operation of cores M460 through M465 which are inserting their data into flip-flops N460 through N466 operate the same as in the operation of the 20 Bit and the 10 Bit Shift Registers and are completely described in paragraphs 3-6 and 3-7, and will not be repeated here.

### 3-3.3 Error Detection

3-3.3.1 General - The third section of the Control Chassis consisting of the

## 3-4. TEST CHASSIS, MEC Model 76-5A (Figures 9-4 and 9-5)

The purpose of the Test Chassis is to substitute for the input signals, a test signal so that the operation of the Model 76 500 Bit Receiver may be checked without the need of external equipment. Relays K501, K502, K503 disconnect the data, copy and EOW inputs from the external source and substitute for them a controlled test pattern. This test pattern is generated completely within this chassis by self contained oscillator and pulse shaping circuits. Switch S501 controls the operation of this chassis. In the first position, OPERATE, the previous relays mentioned are de-energized and the normal input signals flow through this chassis into the Control Chassis and the operation of the Test Chassis is not used. When the test switch is in any of the rest of the positions, the Test Chassis is substituting test signals for the normal data input signals. Switch S515 is used in order to put a circuit in the Control Chassis so that it will not reject the test data when certain test patterns are presented. The operation of this circuit will be described when the Control Chassis is being described. The only function of the switch in this chassis is that it gives a +12 volt signal to one of two output lines (to pins 32 and 33 of P501). When S501 is in any position 2 through 5 (A, B, C or D) oscillator N501 will produce a output pulse every millisecond. The output of N501, pin 8 is a rectangular pulse which is spaced 1 millisecond apart. The adjustment of this time may be accomplished by the adjustment of L501, so that this time interval can be as closely to 1 millisecond as practicable adjusted. Switch S514, a pushbutton switch, is a start pushbutton to generate the necessary pulse to guarantee that oscillator N501 will start and to give one-shot N507 an initial input pulse. The output of N501 is coupled through a one-shot N502 producing a positive 10 microsecond pulse on pin 7, and a negative 10 microsecond pulse on pin 5. The positive pulse on pin 7 is coupled to one-shot N506 producing another negative 10 microsecond pulse. The negative going pulse on pin 5 of N502 triggers flip-flop N503. Since flip-flop N503 requires a positive pulse to trigger, it therefore gives a 10 microsecond delay from the negative going pulse from pin 5, as the positive going edge

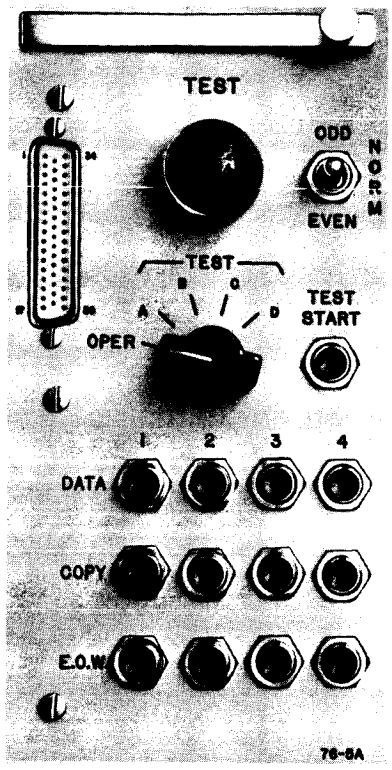



Figure 3-2. Test Chassis

of this pulse is used for the trigger of flip-flop N503. N503 is a counting flip-flop, which when receiving two input pulses produces 1 output pulse on both pin 5 and pin 8. The output pulses from pin 5 and pin 8 are opposite in polarity. The output of pin 8 is coupled to flip-flop N504 producing the test data pulse. Since the positive going edge of the negative pulse on pin 5 of N502 triggered N503 and thereby dividing it by 2, which in turn triggered and turned on flip-flop N504, it is then cut off by the next positive going edge of the pulse on pin 7 of N502 which is coupled to the off side of flip-flop N504. This permits N504 to be a "1", for 1 millisecond -10 microseconds, then remaining off for 1 millisecond, and then on for 1 millisecond, etc. This is producing alternate "1"s and "0"s as it is in the "1" position for one millisecond and for the "0" condition for one millisecond. This alternate "1"s and "0"s is coupled to the data input lines to switch S501C and through pushbutton S502 to S505. When S501C is in position 2 or 3, there is an alternate "1" and "0" pattern being sent on the data line. When in position 4 and position 5, it is either all "0"s or all "1"s. Since 0 volts is a "1" and -20 volts is a "0", it can be seen that the four test patterns are generated by this switch. The purpose of switch S502 through S505 is to introduce errors in the data lines by the use of a pushbutton. When any one of the four pushbuttons is pushed, there is automatically all "0"s being sent to the Control Chassis. This introduces a test giving an error data to the comparator circuits as described in the Control Chassis. The output pulse of N506 triggers one-shot N505, 10 microseconds after one-shot N502 was triggered. The output of one-shot N505 produces the necessary copy pulses to substitute for the incoming normal copy inputs. The output of this one-shot is 100 microseconds in length and is coupled to all four copy lines, through switches S506 through S509. When any one of the pushbuttons S506 to S509 is pushed, it prevents a copy pulse from being sent to the Control Chassis. This introduces an absence of copy pulse to the Control Chassis, which will be recognized at the Control Chassis as an error. As described later, it is required that 2 out of the 4 copy pulses be present for operation. Therefore, this gives a way in which a test can be performed to see if this circuit is working properly. If two of these pushbuttons are pushed, operation should go as usual. But if three of them are pushed, operation should cease. Pushbutton S514B is provided so that when pushed it generates a pulse to start one-shot N507 into operation. The output of N507 is coupled to the input of N508 and the output of N508 is coupled to flip-flop N509 through capacitor C517. The other input of flip-flop N509 is provided from the output of flip-flop N508 which is flipping back and forth between the "0" and "1" condition at a 2 millisecond rate. This produces the off signal for N509. When flip-flop N509 is in the "1" condition, as generated by the output of one-shot N508, an "and" gate is opened from pin 5 of flip-flop N509 to -20 volts by resistors R509 and R510. This conditions pin 6 input (the off input) so that it could be triggered by the next pulse received from flip-flop N503. The output of this flip-flop is coupled by capacitor C518 to one-shot N510. The positive pulse output of this one-shot is coupled to EOW lines and the delayed output also returns through CR504 to the input of one-shot N507 in order to repeat the cycle as just discussed. The time required for this cycle is approximately 500 milliseconds and this time is determined by the length of one-shot N507 and N508, which are controlled by capacitors C514 and C515. The pin 7 output is coupled to switches S510 to S513 to all four EOW lines. If any of the pushbuttons are pushed it will produce an error in one of the EOW lines by not giving an EOW signal. This is used in order to test the comparison circuit as described in the Control Chassis. K501, K502,and K503 are energized in any position of switch S501 except in the OPERATE position. If these relays are energized, an indicator (I501) on the front panel will be lit to indicate that the unit is in test operation. Switch S501D is to prevent the "odd", "even", "normal" test condition to have any significance except when in a "test" mode of operation. This is done by only giving an input voltage to S515 when in test positions 2 through 5. It should be noted that the distance between test EOW pulses on pin 8 of test jack 501 is not critical, provided they are at least 410 milliseconds apart and should not be greater than 1 second apart. The distance between the oscillator pulses as shown on test jack 501 (pin 1 or pin 2) should have an interval between them of approximately 1 millisecond. This time is not critical.

## 3-4. TEST CHASSIS, MEC Model 76-5A (Figures 9-4 and 9-5)

The purpose of the Test Chassis is to substitute for the input signals, a test signal so that the operation of the Model 76 500 Bit Receiver may be checked without the need of external equipment. Relays K501, K502, K503 disconnect the data, copy and EOW inputs from the external source and substitute for them a controlled test pattern. This test pattern is generated completely within this chassis by self contained oscillator and pulse shaping circuits. Switch S501 controls the operation of this chassis. In the first position, OPERATE, the previous relays mentioned are de-energized and the normal input signals flow through this chassis into the Control Chassis and the operation of the Test Chassis is not used. When the test switch is in any of the rest of the positions, the Test Chassis is substituting test signals for the normal data input signals. Switch S515 is used in order to put a circuit in the Control Chassis so that it will not reject the test data when certain test patterns are presented. The operation of this circuit will be described when the Control Chassis is being described. The only function of the switch in this chassis is that it gives a +12 volt signal to one of two output lines (to pins 32 and 33 of P501). When S501 is in any position 2 through 5 (A, B, C or D) oscillator N501 will produce a output pulse every millisecond. The output of N501, pin 8 is a rectangular pulse which is spaced 1 millisecond apart. The adjustment of this time may be accomplished by the adjustment of L501, so that this time interval can be as closely to 1 millisecond as practicable adjusted. Switch S514, a pushbutton switch, is a start pushbutton to generate the necessary pulse to guarantee that oscillator N501 will start and to give one-shot N507 an initial input pulse. The output of N501 is coupled through a one-shot N502 producing a positive 10 microsecond pulse on pin 7, and a negative 10 microsecond pulse on pin 5. The positive pulse on pin 7 is coupled to one-shot N506 producing another negative 10 microsecond pulse. The negative going pulse on pin 5 of N502 triggers flip-flop N503. Since flip-flop N503 requires a positive pulse to trigger, it therefore gives a 10 microsecond delay from the negative going pulse from pin 5, as the positive going edge

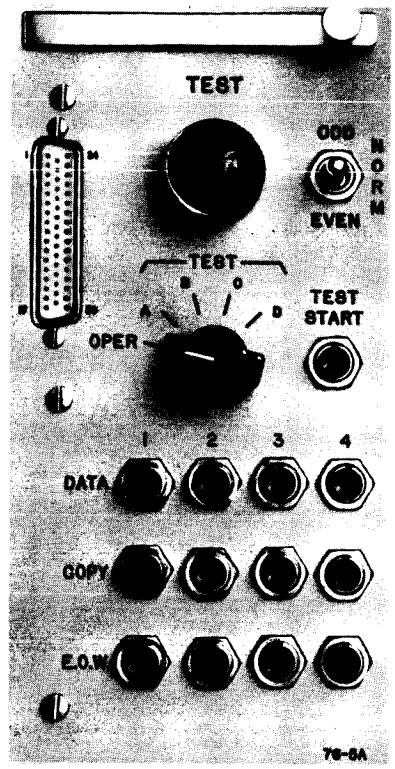



Figure 3-2. Test Chassis

of this pulse is used for the trigger of flip-flop N503. N503 is a counting flip-flop, which when receiving two input pulses produces 1 output pulse on both pin 5 and pin 8. The output pulses from pin 5 and pin 8 are opposite in polarity. The output of pin 8 is coupled to flip-flop N504 producing the test data pulse. Since the positive going edge of the negative pulse on pin 5 of N502 triggered N503 and thereby dividing it by 2, which in turn triggered and turned on flip-flop N504, it is then cut off by the next positive going edge of the pulse on pin 7 of N502 which is coupled to the off side of flip-flop N504. This permits N504 to be a "1", for 1 milliseconds -10 microseconds, then remaining off for 1 millisecond, and then on for 1 millisecond, etc. This is producing alternate "1"s and "0"s as it is in the "1" position for one millisecond and for the "0" condition for one millisecond. This alternate "1"s and "0"s is coupled to the data input lines to switch S501C and through pushbutton S502 to S505. When S501C is in position 2 or 3, there is a alternate "1" and "0" pattern being sent on the data line. When in position 4 and position 5, it is either all "0"s or all "1"s. Since 0 volts is a "1" and -20 volts is a "0", it can be seen that the four test patterns are generated by this switch. The purpose of switch S502 through S505 is to introduce errors in the data lines by the use of a pushbutton. When any one of the four pushbuttons is pushed, there is automatically all "0"s being sent to the Control Chassis. This introduces a test giving an error data to the comparator circuits as described in the Control Chassis. The output pulse of N506 triggers one-shot N505, 10 microseconds after one-shot N502 was triggered. The output of one-shot N505 produces the necessary copy pulses to substitute for the incoming normal copy inputs. The output of this one-shot is 100 microseconds in length and is coupled to all four copy lines, through switches S506 through S509. When any one of the pushbuttons S506 to S509 is pushed, it prevents a copy pulse from being sent to the Control Chassis. This introduces an absence of copy pulse to the Control Chassis, which will be recognized at the Control Chassis as an error. As described later, it is required that 2 out of the 4 copy pulses be present for operation. Therefore, this gives a way in which a test can be performed to see if this circuit is working properly. If two of these pushbuttons are pushed, operation should go as usual. But if three of them are pushed, operation should cease. Pushbutton S514B is provided so that when pushed it generates a pulse to start one-shot N507 into operation. The output of N507 is coupled to the input of N508 and the output of N508 is coupled to flip-flop N509 through capacitor C517. The other input of flip-flop N509 is provided from the output of flip-flop N508 which is flipping back and forth between the "0" and "1" condition at a 2 millisecond rate. This produces the off signal for N509. When flip-flop N507 is in the "1" condition, as generated by the output of one-shot N508, an "and" gate is opened from pin 5 of flip-flop N509 to -20 volts by resistors R509 and R510. This conditions pin 6 input (the off input) so that it could be triggered by the next pulse received from flip-flop N503. The output of this flip-flop is coupled by capacitor C518 to one-shot N510. The positive pulse output of this one-shot is coupled to EOW lines and the delayed output also returns through CR504 to the input of one-shot N507 in order to repeat the cycle as just discussed. The time required for this cycle is approximately 500 milliseconds and this time is determined by the length of one-shot N507 and N508, which are controlled by capacitors C514 and C515. The pin 7 output is coupled to switches S510 to S513 to all four EOW lines. If any of the pushbuttons are pushed it will produce an error in one of the EOW lines by not giving a EOW signal. This is used in order to test the comparison circuit as described in the Control Chassis. K501, K502 and K503 are energized in any position of switch S501 except in the OPERATE position. If these relays are energized, an indicator (I501) on the front panel will be lit to indicate that the unit is in test operation. Switch S501D is to prevent the "odd", "even", "normal" test condition to have any significance except when in a "test" mode of operation. This is done by only giving a input voltage to S515 when in test position 2 through 5. It should be noted that the distance between test EOW pulses on pin 8 of test jack 501 are not critical, provided they are at least 410 milliseconds apart and should not be greater than 1 second apart. The distance between the oscillator pulses as shown on test jack 501 (pin 1 or pin 2) should have an interval between them of approximately 1 millisecond. This time is not critical.

## 3-5. POWER CONTROL CHASSIS, MEC Model 76-3A (Figures 9-6 and 9-7)

The function of the Power Control Chassis is to turn on and off the AC power to the rack, to monitor the output of each power supply, and to indicate by visual means if the +12 volt Power Supply should fail. The power on-off is controlled by the switch S301 which is an on-off switch controlling a power contactor which is located in the base of the rack. This power contactor has a low current coil. The current on the coil is controlled by switch S301. The current to the Power Supply transformers goes through the contactor contacts. Indicator DS301 indicates that the power has been turned on by the contactor. I301 and relay K301 are used to indicate if the +12 volt Power Supply has failed and K301 is energized by the presence of +12 volts. If the +12 volts drops down to less than 6 volts, this relay will drop out and the contacts, pins 1 and 2 of the relay will close, thus turning on indicator I301, which is a 110 volt a-c bulb connected across the a-c line when relay K301 is de-energized. If +12 volts is present, the relay is energized and contacts 1 and 2 are open and the light is off. Switch S302 moves the terminals of the indicating meter to read the output voltage of the various power supplies voltages. Each of the four Power Supplies is designated by A, B, C, or D with the output voltage of each Power Supply being available on the selector switch. The series meter resistors are so chosen so that regardless of the voltage from the Power Supply, the meter will indicate a reading of 10 on the scale. The Power Supply adjustments found on the front panel of each Power Supply should be adjusted within ±2% of the 10 reading on meter M301. Position 2 of this switch allows one phase of the input a-c power to be metered. This position of the switch indicates the a-c input voltage which a normal line should read 10 and should not vary more than ±10% or should not vary more than the readings from 9 to 11 on indicator meter M301. CR301 is used to rectify the a-c voltage so that it may be used on a d-c meter.

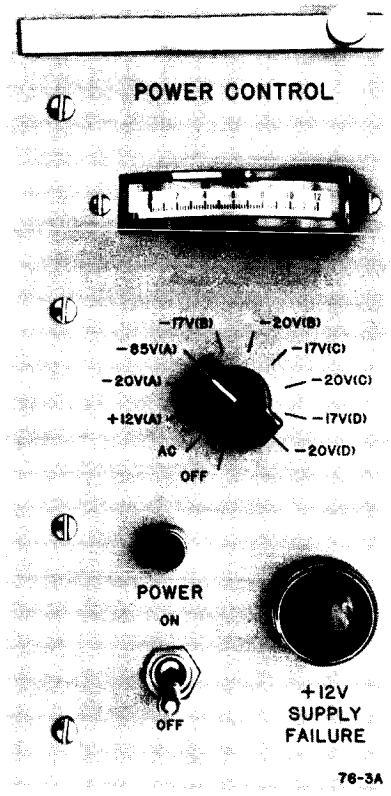



Figure 3-3. Power Control Chassis

## 3-6. 20 BIT SHIFT REGISTER, MEC Model 76-7A (Figures 9-8 through 9-11)

3-6.1. General - The function of the 20 Bit Shift Register is to accumulate data in serial form and transfer it into a parallel form. The data is received serially and stored in 20 magnetic cores (M701 through M720). Upon command, the data is read into 20 flip-flops N701 through N720 and will remain there while new data is being shifted through the cores M701 through M720.

3-6.2. Detailed Description - In the Control Chassis two pulses are derived from the EOW pulse; a reset trigger "every reset" from -20 volts to 0 volts with a width of 10 microseconds and a read gate "every" gate, from 20 volts to 0 volts with a width of 200 microseconds. The flip-flop reset trigger is capacity coupled through C701 to pin 3 of one-shot N723, with an emitter follower output. As previously mentioned, the theory of operation of all TN's used in this equipment is explained in detail in the Appendix. When pin 3 of N723 goes positive (from -20 volts to 0 volts) the output pin 7 goes positive (from -20 volts to 0 volts with a width of approximately 5 microseconds). Pin 7 of N723 is capacity coupled through C702 to pin 5 of flip-flops N701 through N720. Pin 5 of N701 through N720 is biased at -10 volts by R721 and R722. Therefore, as pin 7 of N723 goes positive (from -20 volts to 0 volts), pin 5 of all the flip-flops goes positive(from -10 volts to about +7 volts), resetting all the flip-flops to the "0" state. The states of the flip-flops (TN144) are defined as follows: When pin 8 is at 0 volts the flip-flop is in a "0" state, and conversely when pin 8 is at -17 volts the flip-flop is in a "1" state. At the same time that the flip-flop reset trigger enters the Shift Register, a read gate (from -20 volts to 0 volts, width 200 microseconds) enters pin 2 of an emitter follower N722. The output of N722

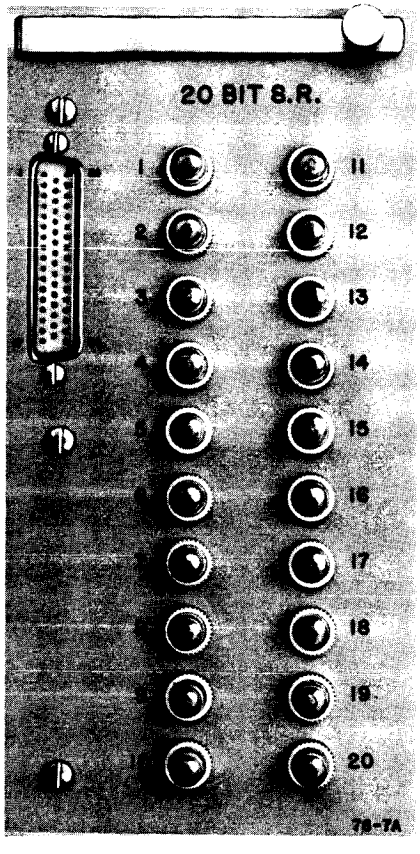



Figure 3-4. 20 Bit Shift Register

goes to pin 5 of all the cores M701 through M720, and is called the flip-flop-gate. When pin 2 of N722 goes positive (-20 volts to 0 volts, width 200 microseconds), pin 5 of all the cores goes positive (from -20 volts to -2 volts, width 200 microseconds). R727 and R728 are used to give a 2 volt noise bias when the gate is open. Since the gate raises pin 5 of M701 through M720, pin 4 of M701 through M720 rises to -2 volts and the flip-flops will not trigger. A voltage pulse equal to or greater than 0 volts must be present at pin 3 of the flip-flops in order for a change of state to occur. The next shift pulse (from -20 volts to 0 volts, width 40 microseconds) will cause the states of the cores to be read out into the flip-flops. This shift pulse will be 100 microseconds from the leading edge of the flip-flop gate. Since the flip-flop gate is 200 microseconds wide, this shift pulse will cause the readout from the core to be approximately in the middle of the gate. Assuming that there was a "1" in the core, a 10 microsecond pulse, of 5 to 8 volts in amplitude will be super-imposed on the flip-flop gate at pin 4 of the cores. This causes pin 3 of the flip-flop to go positive enough to set the state of the flip-flop to a "1". If there was a "0" in the core, only the flip-flop gate will be present at pin 4 of the core; consequently pin 3 of the flip-flop will go positive to only -2 volts, which is insufficient to change the state of the flip-flop. Since the flip-flop is initially reset to the "0" state, and this state remains unchanged if the core is in the "0" state, effectively one may say that the data in the core has been transferred to the flip-flop. The states of the cores are determined by the data which is read in serially. The serial data read in and the core shift pulses, occur at the same time and their repetition rate is 1000 pulses per second. Pin 8 of M701 is the data input. Pin 9 of M701 is directly coupled to pin 8 of M702; pin 9 of M702 is directly coupled to pin 8 of M703. This is repeated from M703 through M720 and constitutes the serial read in arrangement. Since all pin 5's of the cores are connected together, the flip-flop gate occurs at all cores simultaneously (at the proper time), and the data is read out on pin 4 of the cores to pin 3 of the flip-flops, in parallel. Operation of the core string is explained in detail in the Appendix. N721 is a core driver operating with a blocking oscillator core (M721). The data in the flip-flops is read out continuously except for approximately 100 microseconds. This is the time between reset and when the new data is read out of the cores. Each flip-flop N701 through N720 has an indicator light associated with it, DS701 through DS720 respectively, to indicate the states of flip-flops. When a flip-flop is in the "1" state its respective indicator will be on, and when a flip-flop is in the "0" state its respective indicator will be off. The lights have been reversed bias at -2 volts by CR701 through CR703 and R723 to insure that the lights will be off when the flip-flops are in the "0" state. C704, C705, and C707 are used as filter capacitors between the power voltages.

3-6.3. The 20 Bit Shift Register has a building capacity, in that any number of them can be connected in series to facilitate any number of bits in a word.

## 3-7. 10 BIT SHIFT REGISTER, MEC Model 76-8A (Figures 9-12, 9-13 and 9-14)

3-7.1. General - The function of the 10 Bit Shift Register is to receive two serial groups of 10 bits of data alternately. The groups are called "odd" and "even". The Register receives an "odd" or "even" group serially (M801 through M810) and shifts the group in parallel (depending on whether it is an "odd" or "even" group) to its respective set of flip-flops for independent output presentation. The odd set of flip-flops are N801, 3, 5, ...19, and the even set are N802, 4, 6, ...20. The data will remain in the flip-flops for accessibility until they are reset for acquisition of new data, and this time is approximately 100 microseconds, and not longer than 200 microseconds. The states of the flip-flops N801 through N820 are indicated by their respective neon indicators DS801 through DS820 on the front panel. When a flip flop is in a "1" state (a "1" state being the condition when pin 8 is at -17 volts), its associated indicator is on, and conversely when a flip-flop is in the "0" state (a "0" state being the condition when pin 8 is at 0 volts), its indicator is off. The indicators have been reversed bias at -2 volts by CR801 through CR803 and R865 to insure that the indicators will be off when the flip-flops are in the "0" state. C825, C826, and C827 are used as filter capacitors between the power voltages.

3-7.2 Detailed Description - The command pulses are developed in the Control Chassis. They are as follows: "Odd reset" and"even reset" triggers (from -20 volts to 0 volts, width 10 microseconds), "odd" flip-flop gate and "even" flip-flop gate (from -20 volts to 0 volts, width 200 microseconds), and core shift (from -20 volts to 0 volts, width 40 microseconds), 1000 cps. The "odd reset" trigger coming from the Control Chassis

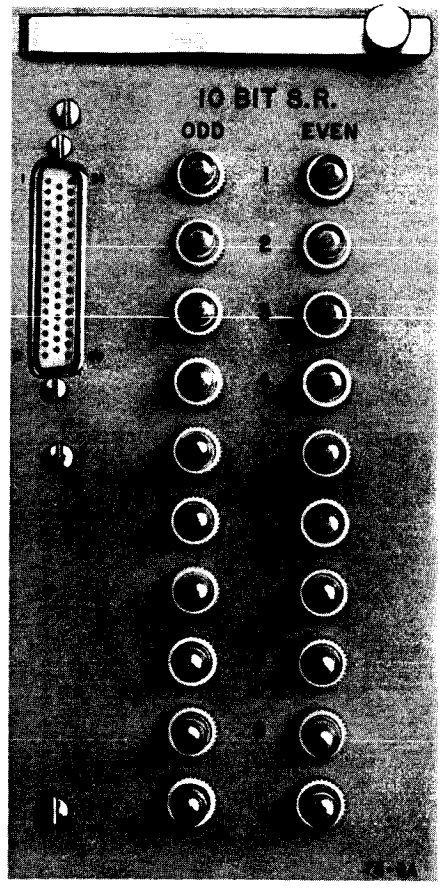



Figure 3-5. 10 Bit Shift Register

is capacity coupled through C829 to pin 3 of a one-shot N823. When pin 3 of N823 goes positive, then pin 7 of N823, the output, goes positive (from -20 volts to 0 volts, width 10 microseconds). This output ("odd reset") is capacity coupled through C824 to pin 5 of all the odd numbered flip-flops N801, 3, 5, ...19. Pin 5 of all the odd numbered flip-flops is biased in a quiescent condition at 7 volts by R851 and R862. Therefore, when pin 7 of N823 goes positive from (-20 volts to 0 volts 10 microseconds) pin 5 of all odd numbered flip-flops goes positive (from -7 volts to +10 volts, 10 microseconds) resetting the odd numbered flip-flops to the "0" state. At the same time that the "odd reset" trigger pulse enters the chassis, the "odd" flip-flop gate is received. The "odd" flip-flop gate is resistance coupled through R866 to pin 2 of N824 (TN58 consisting of two emitter followers). When pin 2 of the emitter follower N824 goes positive (from -20 volts to 0 volts, width 200 microseconds) and is directly coupled to R841 through R850 which is part of the " odd and" gates. There is an "odd" and "even and" gate associated with every magnetic core (M801 through M810), and these "and" gates are coupled to their respective flip-flops. The "odd" gate (output from pin 3 of the emitter follower) raises the voltage of pin 3 of all odd numbered flip-flops from -20 volts to -2 volts for 200 microseconds. This alone is not sufficient to trigger the flip-flops. The next shift pulse (from -20 volts to 0 volts, width 40 microseconds) will be 100 microseconds from the leading edge of the "odd" gate. Since the "odd" gate is 200 microseconds wide, this shift pulse will cause the read out from a core to be approximately in the middle of the gate (if there is a "1" present in the core). Assuming that there is a "1" in the core, a 10 microsecond pulse of 5 to 8 volts amplitude will be present at pin 4 of the cores. Pin 4 of the cores is capacity coupled through C801, 3, 5, ...19 to "odd and" gates and through C802, 4, 6 ...20 to "even and" gates. Therefore, the 5 to 8 volt pulses at pin 4 will be super-imposed on the "odd gate" and pin 3 of the odd numbered flip-flops will go positive enough (above 0 volts) to trigger the odd numbered flip-flops and a "1" state will be set. Both conditions have been satisfied at the "odd and" gates, therefore, only the odd numbered flip-flop will be triggered and the even numbered flip-flop will not be affected. The operation (a core string and core driver N821 with M811) is explained in detail in the Appendix. If there was a "0" in a core, when the shift pulse occurred, the odd numbered flip-flop will not change state because of the "odd and" gate and the 5 to 8 volt pulse from a core and the "odd" gate must be present at the same time in order for an odd numbered flip-flop to trigger. Therefore, at the time of the coincidence of the "odd" gate and shift pulse, all data in the cores is read out in parallel to the odd numbered flip-flop only. The next shift pulse occurs after the trailing edge of the "odd" gate and new data (1000 PPS) commences to be read in serially. Pin 8 of M801 is the data input. Pin 9 of M801 is directly coupled to pin 8 of M802 and pin 9 of M802 is directly coupled to pin 8 of M803. This is continued on to M810 and pin 9 of M810 is data output in the event another Shift Register is used. Many of these Shift Registers may be coupled together in a serial form to facilitate any number of bits in a word.

3-7.3. After the last bit of new data has been received by the cores, an "even reset" trigger (from -20 volts to 0 volts, width 10 microseconds) enters the chassis, and is capacity coupled through C828 to pin 3 of a one-shot N822. When pin 3 goes positive (from -20 volts to 0 volts, width 10 microseconds) the output pin 7 goes positive (from -20 volts to 0 volts, width 10 microseconds) and is capacity coupled through C823 to pin 5 of all the even numbered flip-flops (N802, 4, 6....20). Pin 5 is biased in a quiescent condition at -7 volts by R863 and R864. Therefore, when pin 7 of N822 goes positive (from -20 volts to 0 volts, width 10 microseconds) pin 5 of all the even numbered flip-flops goes positive (from -7 volts to above 0 volts, 10 microseconds) resetting the even numbered flip-flops to the "0" state. At the same time that the "even reset" trigger pulse enters the chassis, the even flip-flop gate is received. The even flip-flop gate is resistance coupled through R867 to pin 7 of an emitter follower (N824). When pin 7 goes positive (from -20 volts to 0 volts, width 200 microseconds), the output pin 5, (called even gate), goes positive (from -20 volts to 0 volts, width 200 microseconds) and is directly coupled to R851 through R860 which is part of the even "and" gates. The even "and" gates are coupled to pin 3 of the even flip-

flops. Therefore when pin 6 of N824 goes positive, all pin 3's of the even flip-flops go positive (from -20 volts to -2 volts, width 200 microseconds). This will not trigger the flip-flops since a pulse equal to or greater than 0 volts is necessary. The "even and" gate requires an additional input in order to trigger the even flip-flops and this input will come from the cores if there is a "1" present in the cores. The first shift pulse that occurs after the "even" gate will be 100 microseconds from the leading edge of the "even" gate. Since the "even" gate is 200 microseconds wide, this shift pulse will cause the readout from a core to be approximately in the middle of the gate (if there is a "1" present in the core). Assuming that there was a "1" in the core, a 10 microsecond pulse, 5 to 8 volts will be present at pin 4 of the core. Pin 4 of the cores is capacity coupled to the Odd and Even "and" gates. Therefore, the output from the core (5 to 8 volt pulse) will be superimposed on the "even" gate and pin 3 of the even flip-flops will go positive enough (above 0 volts) to trigger the even flip-flops and a "1" state will be set. Both conditions have satisfied at the "even and" gate, and only the even flip-flops can be set. The odd flip-flops will not be affected by the output from the cores. If there was a "0" in a core when the shift pulse occurred, the even flip-flop will not change state because the "even and" gate and the 5 to 8 volt pulse from a core and the "even and" gate must be present at the same time in order for an even flip-flop to trigger. Therefore, at the time of coincidence of the Even Gate and shift pulse, all data in the cores is read out in parallel to the even flip-flops only. The next shift pulse occurs after the trailing edge of the "even gate", and new data commences to be read in. The next gate will be the "odd gate", occurring after the last bit of this new data has been received. This completes one cycle of operation, the length of a cycle being determined by the system.

## 3-8. AC POWER INPUT DESCRIPTION

Since the input a-c current of this rack is in the order of a maximum of 40 amps, it was chosen that a power contactor be used to switch the input a-c power. The contactor used in this application is a 3 pole contactor. The magnetic coil for the contactor is operated by a switch in the Power Control Chassis which allows 110 volts a-c to flow through the contactor's coil. This closes the contactor in which the 3 poles are connected one each to the input of each of the three large -17 volt d-c Power Supplies. One blower is connected to one pole of the contactor, the second blower is connected to the second pole of the contactor and the small 165-4C Power Supply is connected to the third set of contacts. This basically gives a balance power load to the three sets of contacts. The inputs of these three sets of contacts go through fuses to the input power connector plug which allows the connection of a balance 3 phase wye connection input from the power lines. The input should be balanced within a small percentage. If it is desired to use this equipment from a single phase input, the three input pins may be connected together and connected to a single phase input. If this equipment is working on a single phase input, it can be expected that 40 amps of power will flow through the conductors going to the rack, therefore they should be of sufficient size or approximately #6 wire for input power connection. The method of connection is described in the installation section. This contactor is fastened to the side of the plug connecting bracket found in the rear bottom of the rack. The three indicator lights found in each rack indicate if power is on, that is, that the contactor is closed. There is one light for each contactor connection so that indication may be had to indicate if any one of the three input line fuses might be blown. If one indicator light is out it may be assumed that its adjoining fuse may be also defected. A Power Off Switch is located in the bottom rear of each rack in order to turn off the a-c power to the rack for servicing the racks and not having a-c flowing through the rack. Even though this switch is disconnected care should be taken when doing service work near the contactor or near the fuse terminals.

# CHAPTER IV

# OPERATION

## 4-1. GENERAL

The operation of the 500 Bit Receiver is quite simple and requires very little controlling operation from the operator. Before operating in the OPERATION mode, check the system in the Test mode. This will set up all adjustments necessary for operation.

## 4-2. TEST OPERATION

Turn on the power switch found in the lower portion of the Power Control Chassis and the indicator should light directly above this switch. If it does not light, then the operator should check in the rear of the two racks to see if the safety power switches are in the ON position. If they are in the ON position input power should be checked to see where the trouble is. With the 500 Bit Receiver, power on and the power indicator light lit, the +12 volt supply failure light should not be on. If this light is on, turn the equipment off until the +12 volt supply is repaired. With the power switch on and after a few seconds of stabilization time, the voltages of the power supplies should be checked. There is a total of four Power Supplies and a total of nine voltages to be checked. These voltages are shown on the meter selection switch on the Power Control Chassis and their voltage is indicated by the meter above the switch. The input series resistors to the voltmeter are chosen so that a 10 reading on the meter is required for each voltage. Out of the nine voltages which come out of the Power Supplies, six of these are adjustable, by adjustment potentiometers found on the front of the chassis. Three of the potentiometers are found on the small Power Supply in the left hand rack; the other three are found in the little windows on the large panels which a large Power Supply is mounted behind. These adjustments should be adjusted until the six Power Supplies are reading at 10 ±2%. It is not expected that the voltages from these Power Supplies will drift except in an extremely long term time and this adjustment may not be necessary except at long time intervals, but should be checked from time to time so that if one Power Supply has drifted a few volts, it can be restored by its adjustment to normal operation. Once it has been determined that all Power Supplies are operating, then the unit can be put into one of its many test conditions so that a complete unit test can be performed. It only takes about 5 minutes to perform this complete unit test, and it is desirable that this be done at intervals of at least once per day. The test is as follows. Put the OPERATE TEST switch found in the Test Chassis into position A on the test switch. Throw the NORMAL EVEN ODD switch to NORMAL, then to EVEN, and then back to NORMAL. This will turn on the following lights with the particular pattern of "on" lights shown in Table 1. Put the NORMAL EVEN ODD switch into the EVEN position. Table 2 shows the light conditions at this time. Then put the switch into the ODD position and the condition of the lights will be as shown in Table 3. Rotate the test switch to pattern B and repeat the performance of the NORMAL ODD EVEN switch through its three positions (NORMAL, ODD, and EVEN), and consult Tables 4, 5, and 6. Do the same thing for the test positions C and D, and Tables 7 through 11 will give the expected light patterns in these test positions. Put the NORMAL EVEN ODD switch back into the NORMAL position, and rotate the test switch to the A position. This will restore the light pattern to the condition as shown in Table 1. Push each of the pushbuttons marked DATA. When each pushbutton is pushed, the meter associated with the pushbutton which is in the same physical order will indicate 100% of errors. An adjustment potentiometer located in the Control Chassis (consult the schematic for the correct one), may be adjusted to indicate the desired meter reading at this time. Pushbutton #2

enters reading on meter 2. Pushbutton 3 should give an indication on meter 3 and likewise for pushbutton 4. For the EOW test, the operation of the pushbutton will give meter indications of the bottom row of meters in the same way. The operation of any one of the copy pushbuttons should not cause any change in either the meter readings or the lights, but if three of the copy pushbuttons are pushed at the same time, operation of the system should cease to operate. If the limit pointers, which are adjusted on the front of the meters, are in the position so that the meter needle can contact them, when one of the error developing pushbuttons is pushed the meter will come in contact with this limit switch, and will cause the error indicator on the front panel of the Control Chassis to light. When the pushbutton causing the error is released the light will remain lit but when the RESET pushbutton is pushed, the light should go out and remain out until another error is inserted. This constitutes the end of the test phase of the 500 Bit Receiver. To put the Receiver into the OPERATE mode, only one switch needs to be switched and that is the selector switch on the Test Chassis and when placed in the OPERATE position the 500 Bit Receiver will automatically go into an OPERATE mode.

## 4-3. OPERATE MODE

When the 500 Bit Receiver is in the Operate Mode only two switches need be utilized. The OPERATE test switch must be placed in the OPERATE position, and LINE SELECT switch placed in the line selecting position desired. The choice of which line chosen should be based on the operator's observance of the error indicating meters. If for instance meter #2 is showing more errors than any of the other meters, it can be assumed that line #2 has the most errors of the four lines, and therefore should not be used. The selector switch in this case should therefore be in the third position in which lines 1, 3, and 4 are being used. If for instance line #3 is a bad line, then the selector switch should be in the second position in which lines 1, 2, and 4 are used, and so on. The operator can choose the line in which he is receiving the best data. This selection should be based on the indications of the error detecting meters. If during an operation an excessive amount of errors has caused the error indicator to light, the operator may push the reset button to restore this circuit into normal operation, so that he may know when the next large group of errors has been received. In normal operation it is not expected that a large percentage of errors will be present. It is therefore not expected that the error light will light. If one line goes bad or some part of the unit on which it is used goes dead (either on the transmission end or the receiving end of this line), the meter will indicate a high percentage of errors and the light will light. The indicators on the Shift Register, and the indicators on the Control Chassis, indicate the output conditions of each flip-flop and will be lit when a "1" is present. The operator can note that there are two special bits, numbers 84 and 85, marked EVEN and ODD, located on the Control Chassis. In normal operation these two special bits should alternate back and forth at half-second intervals; that is, #84 should be on for 1/2 second, and #85 for 1/2 second; #84 for the third half-second, and #85 for the next 1/2 second, and so on. If both these lights stay on all the time or stay off all the time, the operator knows that the system is not receiving the data as it should. The operation theory of the Control Chassis should be consulted. If during an operation the operator notices that a whole group of Shift Registers has developed an all "1" or an all "0" pattern, the power supply voltages should be checked. If one of the Power Supplies should go too high in voltage or too low in voltage, malfunction will exist. This can be corrected most of the time by proper adjustment of the Power Supply voltage.

TABLE 4-1

| | |
|---|---|
| Test Switch: | Pattern A |
| Normal-Odd-Even: | Normal |
| 10 Bit S. R. Lights On: | 1, 3, 5, 7, & 9 |
| 20 Bit S. R. Lights On: | 1, 3, 5, 7, 9, 11, 13, 15, 17, & 19 |

TABLE 4-2

| | |
|---|---|
| Test Switch: | Pattern A |
| Normal-Odd-Even: | Even |
| 10 Bit S. R. Lights On: | 1, 3, 5, 7, & 9 Even |
| 20 Bit S. R. Lights On: | 1, 3, 5, 7, 9, 11, 13, 15, 17, & 19 |

TABLE 4-3

| | |
|---|---|
| Test Switch: | Pattern A |
| Normal-Odd-Even: | Odd |
| 10 Bit S. R. Lights On: | 1, 3, 5, 7, & 9 Odd |
| 20 Bit S. R. Lights On: | 1, 3, 5, 7, 9, 11, 13, 15, 17, & 19 |

TABLE 4-4

| | |
|---|---|
| Test Switch: | Pattern B |
| Normal-Odd-Even: | Normal |
| 10 Bit S. R. Lights On: | 2, 4, 6, 8, & 10 |
| 20 Bit S. R. Lights On: | 2, 4, 6, 8, 10, 12, 14, 16, 18, & 20 |

TABLE 4-5

| | |
|---|---|
| Test Switch: | Pattern B |
| Normal-Odd-Even: | Even |
| 10 Bit S. R. Lights On: | 2, 4, 6, 8, & 10 Even |
| 20 Bit S. R. Lights On: | 2, 4, 6, 8, 10, 12, 14, 16, 18, & 20 |

TABLE 4-6

| | |
|---|---|
| Test Switch: | Pattern B |
| Normal-Odd-Fven: | Odd |
| 10 Bit S. R. Lights On: | 2, 4, 6, 8, & 10 Odd |
| 20 Bit S. R. Lights On: | 2, 4, 6, 8, 10, 12, 14, 16, 18, & 20 |

TABLE 4-7

| | |
|---|---|
| Test Switch: | Pattern C |
| Normal-Odd-Even: | Normal |
| 10 Bit S. R. Lights On: | See Note After Table #11 |
| 20 Bit S. R. Lights On: | See Note After Table #11 |

TABLE 4-8

| | |
|---|---|
| Test Switch: | Pattern C |
| Normal-Odd-Even: | Even |
| 10 Bit S. R. Lights On: | All Even Lights |
| 20 Bit S. R. Lights On: | All lights |

TABLE 4-9

| | |
|---|---|
| Test Switch: | Pattern C |
| Normal-Odd-Even | Odd |
| 10 Bit S. R. Lights On: | All Odd Lights |
| 20 Bit S. R. Lights On: | All lights |

TABLE 4-10

| | |
|---|---|
| Test Switch: | Pattern D |
| Normal-Odd-Even | Normal |
| 10 Bit S. R. Lights On: | See Note After Table #11 |
| 20 Bit S. R. Lights On: | See Note After Table #11 |

TABLE 4-11

| | |
|---|---|
| Test Switch: | Pattern D |
| Normal-Odd-Even: | Odd or Even |
| 10 Bit S. R. Lights On: | None |
| 20 Bit S. R. Lights On: | None |

NOTE: The last pattern which was given by the lights will remain because the odd-even check of bits #84 & #85 will reject this test pattern.

# CHAPTER V
# INSTALLATION

## 5-1 GENERAL

The two racks are set side by side over a false floor. A trim strip is installed between them. Connect the input and output plugs in the jacks provided at the lower portion of the rack. The power input plug and the data input plug are keyed so that no mistakes can be made in the installation in these two plugs. There are 14 output plug connections. No keying exists on the plugs or jacks; therefore care must be exercised to insure that the correct connections are made. These external cables are connected to the rack and are routed under the floor to other external equipment. Consult tables in this section for connection of the input and output plugs. The wire size of the data input and data output connectors are not critical. The only wire sizes which are critical are the power input connectors which should be as follows. If the rack is to be operated on single phase equipment the wire size of this equipment should be #6 Conductor. If the equipment is to be operated on 3 phase power the input wire size may be #12. Consult the wire list for terminal connections. For safety purposes the rack should be connected to a rack earth ground. Each 0 volt bus bar found on the rear of the three 76-9A power supplies MUST be grounded to the system's digital ground with number 8 Conductor. This wire is wired from the 0 volt bus bar found on the rear of these power supplies directly to the digital bus bar found under the false floor. There is a requirement for three such conductors, one for each power supply.

## 5-2 TABLES

TABLE 5-1
A-C Power Input (J98)

| Terminal | Identification | A W G |
|---|---|---|
| A | AC Ø 1 Hot | ** |
| B | AC Ø 2 Hot | ** |
| C | AC Ø 3 Hot | ** |
| D | AC Common | ** |
| E | AC Common | ** |
| F | Signal Ground | #18 |
| G | Rack Ground | #12 |

TABLE 5-2
Data Input (J99)

| Terminal | Identification | A W G |
|---|---|---|
| A | Data #1 Input | * |
| B | Data #2 Input | * |
| C | Data #3 Input | * |
| D | Data #4 Input | * |
| E | Copy #1 Input | * |
| F | Copy #2 Input | * |
| G | Copy #3 Input | * |
| H | Copy #4 Input | * |
| J | EOW #1 Input | * |
| K | EOW #2 Input | * |
| L | EOW #3 Input | * |
| M | EOW #4 Input | * |
| N | | |
| P | | |
| Q | | |
| R | | |
| S | | |
| T | | |
| U | | |
| V | | |
| W | | |
| X | | |
| Y | Signal Ground | #20 |
| Z | Rack Ground | #20 |

* Shielded #22 or RG174 Coax
** See above paragraph.

## TABLE 5-3

### Data Output (J101)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #1 Every | * |
| A | Bit #2 Every | * |
| 2 | Bit #3 Every | * |
| B | Bit #4 Every | * |
| 3 | Bit #5 Every | * |
| C | Bit #6 Every | * |
| 4 | Bit #7 Every | * |
| D | Bit #8 Every | * |
| 5 | Bit #9 Every | * |
| E | Bit #10 Every | * |
| 6 | Bit #11 Every | * |
| F | Bit #12 Every | * |
| 7 | Bit #13 Every | * |
| G | Bit #14 Every | * |
| 8 | Bit #15 Every | * |
| H | Bit #16 Every | * |
| 9 | Bit #17 Every | * |
| I | Bit #18 Every | * |
| 10 | Bit #19 Every | * |
| J | Bit #20 Every | * |
| 11 | Bit #21 Every | * |
| K | Bit #22 Every | * |
| 12 | Bit #23 Every | * |
| L | Bit #24 Every | * |
| 13 | Bit #25 Every | * |
| M | Bit #26 Every | * |
| 14 | Bit #27 Every | * |
| N | Bit #28 Every | * |
| 15 | Bit #29 Every | * |
| O | Bit #30 Every | * |
| 16 | Bit #31 Every | * |
| P | Bit #32 Every | * |
| 17 | Bit #33 Every | * |
| Q | Bit #34 Every | * |
| 18 | Bit #35 Every | * |
| R | Bit #36 Every | * |
| 19 | Bit #37 Every | * |
| S | Bit #38 Every | * |
| 20 | Bit #39 Every | * |
| T | Bit #40 Every | * |
| 21 | Bit #41 Every | * |
| U | Bit #42 Every | * |
| 22 | | |
| V | | |
| 23 | | |
| W | | |
| 24 | D-A Hold | * |
| X | | |
| 25 | | |
| Y | | |
| +4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

## TABLE 5-4

### Data Output (J102)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #43 Every | * |
| A | Bit #44 Every | * |
| 2 | Bit #45 Every | * |
| B | Bit #46 Every | * |
| 3 | Bit #47 Every | * |
| C | Bit #48 Every | * |
| 4 | Bit #49 Every | * |
| D | Bit #50 Every | * |
| 5 | Bit #51 Every | * |
| E | Bit #52 Every | * |
| 6 | Bit #53 Every | * |
| F | Bit #54 Every | * |
| 7 | Bit #55 Every | * |
| G | Bit #56 Every | * |
| 8 | Bit #57 Every | * |
| H | Bit #58 Every | * |
| 9 | Bit #59 Every | * |
| I | Bit #60 Every | * |
| 10 | Bit #61 Every | * |
| J | Bit #62 Every | * |
| 11 | Bit #63 Every | * |
| K | Bit #64 Every | * |
| 12 | Bit #65 Every | * |
| L | Bit #66 Every | * |
| 13 | Bit #67 Every | * |
| M | Bit #68 Every | * |
| 14 | Bit #69 Every | * |
| N | Bit #70 Every | * |
| 15 | Bit #71 Every | * |
| 0 | Bit #72 Every | * |
| 16 | Bit #73 Every | * |
| P | Bit #74 Every | * |
| 17 | Bit #75 Every | * |
| Q | Bit #76 Every | * |
| 18 | Bit #77 Every | * |
| R | Bit #78 Every | * |
| 19 | Bit #79 Every | * |
| S | Bit #80 Every | * |
| 20 | Bit #81 Every | * |
| T | Bit #82 Every | * |
| 21 | Bit #83 Every | * |
| U | Bit #84 Every | * |
| 22 | Bit #85 Every | * |
| V | | |
| 23 | | |
| W | | |
| 24 | | |
| X | | |
| 25 | | |
| Y | | |
| +4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

* Low Capacitance Shielded #22 Wire

TABLE 5-5

Data Output (J103)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #86 Odd | * |
| A | Bit #87 Odd | * |
| 2 | Bit #88 Odd | * |
| B | Bit #89 Odd | * |
| 3 | Bit #90 Odd | * |
| C | Bit #91 Odd | * |
| 4 | Bit #92 Odd | * |
| D | Bit #93 Odd | * |
| 5 | Bit #94 Odd | * |
| E | Bit #95 Odd | * |
| 6 | Bit #96 Odd | * |
| F | Bit #97 Odd | * |
| 7 | Bit #98 Odd | * |
| G | Bit #99 Odd | * |
| 8 | Bit #100 Odd | * |
| H | Bit #101 Odd | * |
| 9 | Bit #102 Odd | * |
| I | Bit #103 Odd | * |
| 10 | Bit #104 Odd | * |
| J | Bit #105 Odd | * |
| 11 | Bit #106 Odd | * |
| K | Bit #107 Odd | * |
| 12 | Bit #108 Odd | * |
| L | Bit #109 Odd | * |
| 13 | Bit #110 Odd | * |
| M | | |
| 14 | | |
| N | | |
| 15 | | |
| 0 | | |
| 16 | | |
| P | | |
| 17 | | |
| Q | | |
| 18 | | |
| R | | |
| 19 | | |
| S | | |
| 20 | | |
| T | | |
| 21 | | |
| U | | |
| 22 | | |
| V | | |
| 23 | | |
| W | | |
| 24 | | |
| X | | |
| 25 | | |
| Y | | |
| +4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

TABLE 5-6

Data Output (J104)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #111 Odd | * |
| A | Bit #112 Odd | * |
| 2 | Bit #113 Odd | * |
| B | Bit #114 Odd | * |
| 3 | Bit #115 Odd | * |
| C | Bit #116 Odd | * |
| 4 | Bit #117 Odd | * |
| D | Bit #118 Odd | * |
| 5 | Bit #119 Odd | * |
| E | Bit #120 Odd | * |
| 6 | Bit #121 Odd | * |
| F | Bit #122 Odd | * |
| 7 | Bit #123 Odd | * |
| G | Bit #124 Odd | * |
| 8 | Bit #125 Odd | * |
| H | Bit #126 Odd | * |
| 9 | Bit #127 Odd | * |
| I | Bit #128 Odd | * |
| 10 | Bit #129 Odd | * |
| J | Bit #130 Odd | * |
| 11 | Bit #131 Odd | * |
| K | Bit #132 Odd | * |
| 12 | Bit #133 Odd | * |
| L | Bit #134 Odd | * |
| 13 | Bit #135 Odd | * |
| M | Bit #136 Odd | * |
| 14 | Bit #137 Odd | * |
| N | Bit #138 Odd | * |
| 15 | Bit #139 Odd | * |
| 0 | Bit #140 Odd | * |
| 16 | Bit #141 Odd | * |
| P | Bit #142 Odd | * |
| 17 | Bit #143 Odd | * |
| Q | Bit #144 Odd | * |
| 18 | Bit #145 Odd | * |
| R | Bit #146 Odd | * |
| 19 | Bit #147 Odd | * |
| S | Bit #148 Odd | * |
| 20 | Bit #149 Odd | * |
| T | Bit #150 Odd | * |
| 21 | Bit #151 Odd | * |
| U | Bit #152 Odd | * |
| 22 | Bit #153 Odd | * |
| V | Bit #154 Odd | * |
| 23 | Bit #155 Odd | * |
| W | Bit #156 Odd | * |
| 24 | Bit #157 Odd | * |
| X | Bit #158 Odd | * |
| 25 | | |
| Y | | |
| +4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

*Low Capacitance Shielded #22 Wire

TABLE 5-7

Data Output (J105)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | | |
| A | | |
| 2 | Bit #161 Odd | * |
| B | Bit #162 Odd | * |
| 3 | Bit #163 Odd | * |
| C | Bit #164 Odd | * |
| 4 | Bit #165 Odd | * |
| D | Bit #166 Odd | * |
| 5 | Bit #167 Odd | * |
| E | Bit #168 Odd | * |
| 6 | Bit #169 Odd | * |
| F | Bit #170 Odd | * |
| 7 | Bit #171 Odd | * |
| G | Bit #172 Odd | * |
| 8 | Bit #173 Odd | * |
| H | Bit #174 Odd | * |
| 9 | Bit #175 Odd | * |
| I | Bit #176 Odd | * |
| 10 | Bit #177 Odd | * |
| J | Bit #178 Odd | * |
| 11 | Bit #179 Odd | * |
| K | Bit #180 Odd | * |
| 12 | Bit #181 Odd | * |
| L | Bit #182 Odd | * |
| 13 | Bit #183 Odd | * |
| M | Bit #184 Odd | * |
| 14 | Bit #185 Odd | * |
| N | Bit #186 Odd | * |
| 15 | Bit #187 Odd | * |
| 0 | Bit #188 Odd | * |
| 16 | Bit #189 Odd | * |
| P | Bit #190 Odd | * |
| 17 | Bit #191 Odd | * |
| Q | Bit #192 Odd | * |
| 18 | Bit #193 Odd | * |
| R | Bit #194 Odd | * |
| 19 | Bit #195 Odd | * |
| S | Bit #196 Odd | * |
| 20 | Bit #197 Odd | * |
| T | Bit #198 Odd | * |
| 21 | Bit #199 Odd | * |
| U | Bit #200 Odd | * |
| 22 | Bit #201 Odd | * |
| V | Bit #202 Odd | * |
| 23 | Bit #203 Odd | * |
| W | Bit #204 Odd | * |
| 24 | Bit #205 Odd | * |
| X | Bit #206 Odd | * |
| 25 | | |
| Y | | |
| +4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

TABLE 5-8

Data Output (J106)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #207 Odd | * |
| A | Bit #208 Odd | * |
| 2 | Bit #209 Odd | * |
| B | Bit #210 Odd | * |
| 3 | Bit #211 Odd | * |
| C | Bit #212 Odd | * |
| 4 | Bit #213 Odd | * |
| D | Bit #214 Odd | * |
| 5 | Bit #215 Odd | * |
| E | Bit #216 Odd | * |
| 6 | Bit #217 Odd | * |
| F | Bit #218 Odd | * |
| 7 | Bit #219 Odd | * |
| G | Bit #220 Odd | * |
| 8 | Bit #221 Odd | * |
| H | Bit #222 Odd | * |
| 9 | Bit #223 Odd | * |
| I | Bit #224 Odd | * |
| 10 | Bit #225 Odd | * |
| J | Bit #226 Odd | * |
| 11 | Bit #227 Odd | * |
| K | Bit #228 Odd | * |
| 12 | Bit #229 Odd | * |
| L | Bit #230 Odd | * |
| 13 | Bit #231 Odd | * |
| M | Bit #232 Odd | * |
| 14 | Bit #233 Odd | * |
| N | Bit #234 Odd | * |
| 15 | Bit #235 Odd | * |
| 0 | Bit #236 Odd | * |
| 16 | Bit #237 Odd | * |
| P | Bit #238 Odd | * |
| 17 | Bit #239 Odd | * |
| Q | Bit #240 Odd | * |
| 18 | Bit #241 Odd | * |
| R | Bit #242 Odd | * |
| 19 | Bit #243 Odd | * |
| S | Bit #244 Odd | * |
| 20 | Bit #245 Odd | * |
| T | Bit #246 Odd | * |
| 21 | Bit #247 Odd | * |
| U | Bit #248 Odd | * |
| 22 | Bit #249 Odd | * |
| V | Bit #250 Odd | * |
| 23 | Bit #251 Odd | * |
| W | Bit #252 Odd | * |
| 24 | Bit #253 Odd | * |
| X | Bit #254 Odd | * |
| 25 | Bit #255 Odd | * |
| Y | Bit #256 Odd | * |
| +4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

*Low Capacitance Shielded #22 Wire

## TABLE 5-9

Data Output (J107)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #86 Even | * |
| A | Bit #87 Even | * |
| 2 | Bit #88 Even | * |
| B | Bit #89 Even | * |
| 3 | Bit #90 Even | * |
| C | Bit #91 Even | * |
| 4 | Bit #92 Even | * |
| D | Bit #93 Even | * |
| 5 | Bit #94 Even | * |
| E | Bit #95 Even | * |
| 6 | Bit #96 Even | * |
| F | Bit #97 Even | * |
| 7 | Bit #98 Even | * |
| G | Bit #99 Even | * |
| 8 | Bit #100 Even | * |
| H | Bit #101 Even | * |
| 9 | Bit #102 Even | * |
| I | Bit #103 Even | * |
| 10 | Bit #104 Even | * |
| J | Bit #105 Even | * |
| 11 | Bit #106 Even | * |
| K | Bit #107 Even | * |
| 12 | Bit #108 Even | * |
| L | Bit #109 Even | * |
| 13 | Bit #110 Even | * |
| M | Bit #111 Even | * |
| 14 | Bit #112 Even | * |
| N | Bit #113 Even | * |
| 15 | Bit #114 Even | * |
| 0 | Bit #115 Even | * |
| 16 | Bit #116 Even | * |
| P | Bit #117 Even | * |
| 17 | Bit #118 Even | * |
| Q | Bit #119 Even | * |
| 18 | Bit #120 Even | * |
| R | Bit #121 Even | * |
| 19 | Bit #122 Even | * |
| S | Bit #123 Even | * |
| 20 | Bit #124 Even | * |
| T | Bit #125 Even | * |
| 21 | Bit #126 Even | * |
| U | | |
| 22 | | |
| V | | |
| 23 | | |
| W | | |
| 24 | | |
| X | | |
| 25 | | |
| Y | | |
| +4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

## TABLE 5-10

Data Output (J108)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #127 Even | * |
| A | Bit #128 Even | * |
| 2 | Bit #129 Even | * |
| B | Bit #130 Even | * |
| 3 | Bit #131 Even | * |
| C | Bit #132 Even | * |
| 4 | Bit #133 Even | * |
| D | Bit #134 Even | * |
| 5 | Bit #135 Even | * |
| E | Bit #136 Even | * |
| 6 | Bit #137 Even | * |
| F | Bit #138 Even | * |
| 7 | Bit #139 Even | * |
| G | Bit #140 Even | * |
| 8 | Bit #141 Even | * |
| H | Bit #142 Even | * |
| 9 | Bit #143 Even | * |
| I | Bit #144 Even | * |
| 10 | Bit #145 Even | * |
| J | Bit #146 Even | * |
| 11 | Bit #147 Even | * |
| K | Bit #148 Even | * |
| 12 | Bit #149 Even | * |
| L | Bit #150 Even | * |
| 13 | Bit #151 Even | * |
| M | Bit #152 Even | * |
| 14 | Bit #153 Even | * |
| N | Bit #154 Even | * |
| 15 | Bit #155 Even | * |
| 0 | Bit #156 Even | * |
| 16 | Bit #157 Even | * |
| P | Bit #158 Even | * |
| 17 | Bit #159 Even | * |
| Q | Bit #160 Even | * |
| 18 | Bit #161 Even | * |
| R | Bit #162 Even | * |
| 19 | Bit #163 Even | * |
| S | Bit #164 Even | * |
| 20 | Bit #165 Even | * |
| T | Bit #166 Even | * |
| 21 | Bit #167 Even | * |
| U | | |
| 22 | | |
| V | | |
| 23 | | |
| W | | |
| 24 | | |
| X | | |
| 25 | | |
| Y | | |
| +4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

*Low Capacitance Shielded #22 Wire

## TABLE 5-11

### Data Output (J107)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #168 Even | * |
| A | Bit #169 Even | * |
| 2 | Bit #170 Even | * |
| B | Bit #171 Even | * |
| 3 | Bit #172 Even | * |
| C | Bit #173 Even | * |
| 4 | Bit #174 Even | * |
| D | Bit #175 Even | * |
| 5 | Bit #176 Even | * |
| E | Bit #177 Even | * |
| 6 | Bit #178 Even | * |
| F | Bit #179 Even | * |
| 7 | Bit #180 Even | * |
| G | Bit #181 Even | * |
| 8 | Bit #182 Even | * |
| H | Bit #183 Even | * |
| 9 | Bit #184 Even | * |
| I | Bit #185 Even | * |
| 10 | Bit #186 Even | * |
| J | Bit #187 Even | * |
| 11 | Bit #188 Even | * |
| K | Bit #189 Even | * |
| 12 | Bit #190 Even | * |
| L | Bit #191 Even | * |
| 13 | Bit #192 Even | * |
| M | Bit #193 Even | * |
| 14 | Bit #194 Even | * |
| N | Bit #195 Even | * |
| 15 | Bit #196 Even | * |
| 0 | Bit #197 Even | * |
| 16 | Bit #198 Even | * |
| P | Bit #199 Even | * |
| 17 | Bit #200 Even | * |
| Q | Bit #201 Even | * |
| 18 | Bit #202 Even | * |
| R | Bit #203 Even | * |
| 19 | Bit #204 Even | * |
| S | Bit #205 Even | * |
| 20 | Bit #206 Even | * |
| T | Bit #207 Even | * |
| 21 | Bit #208 Even | * |
| U | | |
| 22 | | |
| V | | |
| 23 | | |
| W | | |
| 24 | | |
| X | | |
| 25 | | |
| Y | | |
| +4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

*Low Capacitance Shielded #22 Wire

TABLE 5-12

Data Output (J110)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #209 Even | * |
| A | Bit #210 Even | * |
| 2 | Bit #211 Even | * |
| B | Bit #212 Even | * |
| 3 | Bit #213 Even | * |
| C | Bit #214 Even | * |
| 4 | Bit #215 Even | * |
| D | Bit #216 Even | * |
| 5 | Bit #217 Even | * |
| E | Bit #218 Even | * |
| 6 | Bit #219 Even | * |
| F | Bit #220 Even | * |
| 7 | Bit #221 Even | * |
| G | Bit #222 Even | * |
| 8 | Bit #223 Even | * |
| H | Bit #224 Even | * |
| 9 | Bit #225 Even | * |
| I | Bit #226 Even | * |
| 10 | Bit #227 Even | * |
| J | Bit #228 Even | * |
| 11 | Bit #229 Even | * |
| K | Bit #230 Even | * |
| 12 | Bit #231 Even | * |
| L | Bit #232 Even | * |
| 13 | Bit #233 Even | * |
| M | Bit #234 Even | * |
| 14 | Bit #235 Even | * |
| N | Bit #236 Even | * |
| 15 | Bit #237 Even | * |
| 0 | Bit #238 Even | * |
| 16 | Bit #239 Even | * |
| P | Bit #240 Even | * |
| 17 | Bit #241 Even | * |
| Q | Bit #242 Even | * |
| 18 | Bit #243 Even | * |
| R | Bit #244 Even | * |
| 19 | Bit #245 Even | * |
| S | Bit #246 Even | * |
| 20 | Bit #247 Even | * |
| T | Bit #248 Even | * |
| 21 | Bit #249 Even | * |
| U | Bit #250 Even | * |
| 22 | Bit #251 Even | * |
| V | Bit #252 Even | * |
| 23 | Bit #253 Even | * |
| W | Bit #254 Even | * |
| 24 | Bit #255 Even | * |
| X | Bit #256 Even | * |
| 25 | | |
| Y | | |
| +4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

TABLE 5-13

Data Output (J111)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #257 Every | * |
| A | Bit #258 Every | * |
| 2 | Bit #259 Every | * |
| B | Bit #260 Every | * |
| 3 | Bit #261 Every | * |
| C | Bit #262 Every | * |
| 4 | Bit #263 Every | * |
| D | Bit #264 Every | * |
| 5 | Bit #265 Every | * |
| E | Bit #266 Every | * |
| 6 | Bit #267 Every | * |
| F | Bit #268 Every | * |
| 7 | Bit #269 Every | * |
| G | Bit #270 Every | * |
| 8 | Bit #271 Every | * |
| H | Bit #272 Every | * |
| 9 | Bit #273 Every | * |
| I | Bit #274 Every | * |
| 10 | Bit #275 Every | * |
| J | Bit #276 Every | * |
| 11 | Bit #277 Every | * |
| K | Bit #278 Every | * |
| 12 | Bit #279 Every | * |
| L | Bit #280 Every | * |
| 13 | Bit #281 Every | * |
| M | Bit #282 Every | * |
| 14 | Bit #283 Every | * |
| N | Bit #284 Every | * |
| 15 | Bit #285 Every | * |
| O | Bit #286 Every | * |
| 16 | Bit #287 Every | * |
| P | Bit #288 Every | * |
| 17 | Bit #289 Every | * |
| Q | Bit #290 Every | * |
| 18 | Bit #291 Every | * |
| R | Bit #292 Every | * |
| 19 | Bit #293 Every | * |
| S | Bit #294 Every | * |
| 20 | Bit #295 Every | * |
| T | Bit #296 Every | * |
| 21 | Bit #297 Every | * |
| U | Bit #298 Every | * |
| 22 | Bit #298 Every | * |
| V | | |
| 23 | | |
| W | | |
| 24 | | |
| X | | |
| 25 | | |
| Y | | |
| +4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

*Low Capacitance Shielded #22 Wire

## TABLE 5-14

Data Output (J112)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #299 Every | * |
| A | Bit #300 Every | * |
| 2 | Bit #301 Every | * |
| B | Bit #302 Every | * |
| 3 | Bit #303 Every | * |
| C | Bit #304 Every | * |
| 4 | Bit #305 Every | * |
| D | Bit #306 Every | * |
| 5 | Bit #307 Every | * |
| E | Bit #308 Every | * |
| 6 | Bit #309 Every | * |
| F | Bit #310 Every | * |
| 7 | Bit #311 Every | * |
| G | Bit #312 Every | * |
| 8 | Bit #313 Every | * |
| H | Bit #314 Every | * |
| 9 | Bit #315 Every | * |
| I | Bit #316 Every | * |
| 10 | Bit #317 Every | * |
| J | Bit #318 Every | * |
| 11 | Bit #329 Every | * |
| K | Bit #330 Every | * |
| 12 | Bit #331 Every | * |
| L | Bit #332 Every | * |
| 13 | Bit #333 Every | * |
| M | Bit #334 Every | * |
| 14 | Bit #335 Every | * |
| N | Bit #336 Every | * |
| 15 | Bit #337 Every | * |
| O | Bit #338 Every | * |
| 16 | Bit #340 Every | * |
| P | Bit #341 Every | * |
| 17 | Bit #342 Every | * |
| Q | Bit #343 Every | * |
| 18 | Bit #344 Every | * |
| R | Bit #345 Every | * |
| 19 | Bit #346 Every | * |
| S | Bit #347 Every | * |
| 20 | Bit #348 Every | * |
| T | Bit #349 Every | * |
| 21 | Bit #350 Every | * |
| U | Bit #351 Every | * |
| 22 | Bit #352 Every | * |
| V | Bit #353 Every | * |
| 23 | Bit #354 Every | * |
| W | Bit #355 Every | * |
| 24 | Bit #356 Every | * |
| X | Bit #357 Every | * |
| 25 | Bit #358 Every | * |
| Y | Bit #359 Every | * |
| =4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

## TABLE 5-15

Data Output (J113)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #319 Every | * |
| A | Bit #320 Every | * |
| 2 | Bit #321 Every | * |
| B | Bit #322 Every | * |
| 3 | Bit #323 Every | * |
| C | Bit #324 Every | * |
| 4 | Bit #325 Every | * |
| D | Bit #326 Every | * |
| 5 | Bit #327 Every | * |
| E | Bit #328 Every | * |
| 6 | | |
| F | | |
| 7 | | |
| G | | |
| 8 | | |
| H | | |
| 9 | | |
| I | | |
| 10 | | |
| J | | |
| 11 | Bit #360 Every | * |
| K | Bit #361 Every | * |
| 12 | Bit #362 Every | * |
| L | Bit #363 Every | * |
| 13 | Bit #364 Every | * |
| M | Bit #365 Every | * |
| 14 | Bit #366 Every | * |
| N | Bit #367 Every | * |
| 15 | Bit #368 Every | * |
| O | Bit #369 Every | * |
| 16 | Bit #370 Every | * |
| P | Bit #371 Every | * |
| 17 | Bit #372 Every | * |
| Q | Bit #373 Every | * |
| 18 | Bit #374 Every | * |
| R | Bit #375 Every | * |
| 19 | Bit #376 Every | * |
| S | Bit #377 Every | * |
| 20 | Bit #378 Every | * |
| T | Bit #379 Every | * |
| 21 | Bit #159 Odd | * |
| U | Bit #160 Odd | * |
| 22 | | |
| V | | |
| 23 | | |
| W | | |
| 24 | | |
| X | | |
| 25 | | |
| Y | | |
| =4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

*Low Capacitance Shielded #22 Wire

## TABLE 5-16

Data Output (J114)

| Terminal | Identification | A W G |
|---|---|---|
| 1 | Bit #339 Every | * |
| A | Bit #380 Every | * |
| 2 | Bit #402 Every | * |
| B | Bit #403 Every | * |
| 3 | Bit #404 Every | * |
| C | Bit #405 Every | * |
| 4 | Bit #406 Every | * |
| D | Bit #407 Every | * |
| 5 | Bit #408 Every | * |
| E | | |
| 6 | | |
| F | | |
| 7 | | |
| G | | |
| 8 | | |
| H | | |
| 9 | | |
| I | | |
| 10 | | |
| J | | |
| 11 | Bit #381 Every | * |
| K | Bit #382 Every | * |
| 12 | Bit #383 Every | * |
| L | Bit #384 Every | * |
| 13 | Bit #385 Every | * |
| M | Bit #386 Every | * |
| 14 | Bit #387 Every | * |
| N | Bit #388 Every | * |
| 15 | Bit #389 Every | * |
| O | Bit #390 Every | * |
| 16 | Bit #391 Every | |
| P | Bit #392 Every | * |
| 17 | Bit #393 Every | * |
| Q | Bit #394 Every | * |
| 18 | Bit #395 Every | * |
| R | Bit #396 Every | * |
| 19 | Bit #397 Every | * |
| S | Bit #398 Every | * |
| 20 | Bit #399 Every | * |
| T | Bit #400 Every | * |
| 21 | Bit #401 Every | * |
| U | | |
| 22 | | |
| V | | |
| 23 | | |
| W | | |
| 24 | | |
| X | | |
| 25 | | |
| Y | | |
| =4.5 | Shield of Above Cable | |
| -4.5 | Shield of Above Cable | |

*Low Capacitance Shielded #22 Wire

# CHAPTER VI
# MAINTENANCE

## 6-1. GENERAL

Since the 500 Bit Receiver is made up of semiconductor circuits and magnetic core circuits it should operate over long periods of time with no maintenance. When in the OPERATE mode, several conditions are dependent on external signals which are required for the 500 Bit Receiver to operate properly. If operation is faulty in OPERATE only, check the following input signals.

6-1.1. Data Input - There are four input data lines each which must be receiving data.

6-1.2. Copy Input Line - There are four copy input lines in which a copy pulse once each 1 millisecond must be received for operation. The copy pulse should go from -20 volts to 0 volts and remain 400 microseconds.

6-1.3. EOW Pulse - There must be on each EOW line an EOW pulse which is approximately 1 millisecond wide with an amplitude from -20 volts to 0 volts. These EOW pulses are expected to arrive once each 500 milliseconds. The leading edge of the four EOW pulses should not vary more than a total of 400 microseconds from the leading edge of the most advanced to the leading edge of the most retarded pulse.

## 6-2. CORRECTIVE MAINTENANCE

If a normal check of inputs and outputs indicate malfunction reference to the system block diagram (Figure 9-16) and the various chassis schematics figures 9-1 through 9-14, and the waveforms in figure 9-15 with a full understanding of the section of Theory of Operation; one should be able to quickly locate the trouble.

## 6-3. PREVENTIVE MAINTENANCE

Since the Data Transmitter is made up largely of semiconductors and magnetic cores it should operate over long periods of time with little or no maintenance. There are no critical adjustments to be made except that occasionally the output voltage of the four power supplies should be checked to see if the voltage is within operation limits as read on the voltage meter on the Power Control Panel. These voltages may be checked by rotating the selection switch and reading the voltage of each power supply on the meter. A normal reading should be 10 on the meter and should not vary more than 2%.

## 6-4. PERIODICAL MAINTENANCE

6-4.1. Mechanical Maintenance - The dust filter in front of each blower must be cleaned once a week OR MORE often when in a dusty location. Remove the two cap nuts, one on each side of the chrome grill at the bottom of the rack. Remove the grill. The filter can now be removed for cleaning. This filter can easily be cleaned with the aid of a vacuum cleaner. Replace the filter with the reverse procedure.

6-4.2. Electrical Maintenance - No special considerations are needed for maintenance of this equipment. However, normal failures of individual components may be expected and can be located through normal maintenance operations. Values of all major component parts used in the chassis are indicated in CHAPTER V11, PARTS LIST. The indicators located on the front panels of the chassis give indication of malfunction in most cases. By observing these indicators during normal operation, it is possible to determine quickly in which chassis the trouble is located, and in which portion of the chassis the trouble is contained.

# CHAPTER VII

# PARTS LIST

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 4-1 | | | | MEC 76-4A | ASSEMBLY, CONTROL | 1 | |
| 4-2 | C401<br>C403<br>C405<br>C407<br>C471 | | | Cornell-Dubilier PM4S5 | CAPACITOR, Fixed Mylar, .05mf, 400vdc | 5 | |
| 4-3 | C473 | | | Cornell-Dubilier PM2P5 | CAPACITOR, Fixed Mylar, .5mf, 200vdc | 1 | |
| 4-4 | C402<br>C404<br>C406<br>C408<br>C414<br>C416<br>C418<br>C420<br>C422<br>C468 | | | Fansteel F308-1 | CAPACITOR, (Blu-Cap) 100mf, 30vdc | 10 | |
| 4-5 | C476<br>C480<br>C481 | | | Cornell-Dubilier PM4S2 | CAPACITOR, Fixed Mylar, .02mf, 400vdc | 3 | |
| 4-6 | C409 | | | Cornell-Dubilier PM4S4 | CAPACITOR, Fixed Mylar, .04mf, 600vdc | 1 | |
| 4-7 | C412<br>C423<br>C469<br>C470 | | | Elmenco CM-19B-222K | CAPACITOR Fixed Mica, 2200mmf, 500vdc | 4 | |
| 4-8 | C421 | | | Fansteel F110-1 | CAPACITOR, (Blu-Cap) 10mf, 25vdc | 1 | |
| 4-9 | C460<br>C461<br>C482-<br>C489<br>C472<br>C474<br>C477<br>C411<br>C492<br>C493<br>C494<br>C495<br>C496 | | | Elmenco CM-19B-102K | CAPACITOR, Fixed Mica, 1000mmf, 500vdc | 19 | |
| 4-10 | C462<br>C410 | | | Cornell-Dubilier PM4S1 | CAPACITOR Fixed Mylar, .01mf, 400vdc | 2 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 4-11 | C413, 13A<br>C415, 15A<br>C417, 17A<br>C419, 19A | | | Cornell-Dubilier<br>PM4P1 | CAPACITOR, Fixed Mylar, .1mf, 400vdc | 8 | |
| 4-12 | C475<br>C478<br>C479 | | | Elmenco<br>CM-19B-681K | CAPACITOR, Fixed Mica, 680mf, 500vdc | 3 | |
| 4-13 | C463-<br>C467 | | | Elmenco<br>CM-19B-202K | CAPACITOR, Fixed Mica, 2000mf, 500vdc | 5 | |
| 4-14 | C497 | | | Cornell-Dubilier<br>PM2P25 | CAPACITOR, Fixed Mylar, .25mf, 200vdc | 1 | |
| 4-15 | C490 | | | Elmenco<br>CM-19B-331K | CAPACITOR Fixed Mica, 330mmf, 500vdc | 1 | |
| 4-16 | CR401-<br>CR404<br>CR407-<br>CR410<br>CR460<br>CR461<br>CR467-<br>CR469 | | | G.E.<br>1N1692 | DIODE | 13 | |
| 4-17 | CR405<br>CR462-<br>CR466<br>CR496<br>CR497<br>CR496<br>CR499<br>CR470-<br>CR495 | | | Transitron<br>T12G or<br>Clevite<br>CTP-503 | DIODE | 36 | |
| 4-18 | CR411<br>CR413 | | | Pacific<br>Semi-Conductor<br>IN703 | DIODE | 2 | |
| 4-19 | CR412 | | | International<br>Rectifier<br>1Z6.2T5 | DIODE | 1 | |
| 4-20 | DS460-<br>DS466 | | | MEC<br>16-102 | INDICATOR | 7 | |
| 4-21 | L401 | | | Dialight Corp.<br>6S6 | LAMP, Incandescent, Candelabra Base, 24V, Clear | 1 | |
| 4-22 | M401<br>M460-<br>M465 | | | MEC<br>MN11 | CORE, Magnetic | 7 | |
| 4-23 | M402<br>M403 | | | MEC<br>MN12 | CORE Magnetic | 2 | |
| 4-24 | N401<br>N411<br>N420 | | | MEC<br>TN161 | TRANSISTOR NETWORK | 3 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 4-25 | N402<br>N404<br>N406<br>N408<br>N421<br>N423<br>N425<br>N427 | | | MEC<br>TN162 | TRANSISTOR NETWORK | 8 | |
| 4-26 | N403<br>N405<br>N407<br>N409<br>N422<br>N424<br>N426<br>N428<br>N470-<br>N478<br>N413<br>N414 | | | MEC<br>TN138B | TRANSISTOR NETWORK | 19 | |
| 4-27 | N410<br>N412<br>N417 | | | MEC<br>TN159 | TRANSISTOR NETWORK | 3 | |
| 4-28 | N415 | | | MEC<br>TN130B | TRANSISTOR NETWORK | 1 | |
| 4-29 | N416 | | | MEC<br>TN57 | TRANSISTOR NETWORK | 1 | |
| 4-30 | N419<br>N468<br>N469 | | | MEC<br>TN28 | TRANSISTOR NETWORK | 3 | |
| 4-31 | N460-<br>N466<br>N418 | | | MEC<br>TN144 | TRANSISTOR NETWORK | 8 | |
| 4-32 | P401 | | | Cannon<br>DD-50P | PLUG, Male 50 Pin Contact, 5 Amp Rating | 1 | |
| 4-33 | R413<br>R436<br>R441<br>R444<br>R447<br>R450 | | | MIL<br>RC20GF102K | RESISTOR Fixed Composition 1K, 10%, ½W | 6 | |
| 4-34 | R401<br>R404<br>R407<br>R410<br>R428-<br>R435<br>R440<br>R443<br>R446<br>R449 | | | MIL<br>RC20GF101K | RESISTOR, Fixed Composition, 100 ohm, 10%, ½W | 16 | |
| 4-35 | R402<br>R405<br>R408<br>R411 | | | MIL<br>RC20GF153K | RESISTOR, Fixed Composition, 15K, 10%, ½W | 4 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 4-36 | R403<br>R406<br>R409<br>R412<br>R442<br>R445<br>R448<br>R451 | | | Allen Bradley<br>JLU-1031 of<br>JA1L040S103UC | POTENTIOMETER. 10K, 10%, 2W, Linear Taper | 8 | |
| 4-37 | R414-<br>R422<br>R472<br>R473<br>R476<br>R478<br>R480 | | | MIL<br>RC20GF113J | RESISTOR Fixed Composition, 11K, 5%, ½W | 14 | |
| 4-38 | R423<br>R427<br>R481<br>R483<br>R487<br>R489<br>R491<br>R4117<br>R4121<br>R4113<br>R4125<br>R4129<br>R4133<br>R4137<br>R4141 | | | MIL<br>RC20GF332K | RESISTOR. Fixed Composition, 3.3K, 10%, ½W | 15 | |
| 4-39 | R424<br>R488<br>R490<br>R492 | | | MIL<br>RC20GF333K | RESISTOR FIXED Composition, 33K, 10%, ½W | 4 | |
| 4-40 | R426<br>R468-<br>R470<br>R4101-<br>R4112<br>R496<br>R497<br>R482<br>R484<br>R452<br>R453<br>R4151 | | | MIL<br>RC20GF103K | RESISTOR. Fixed Composition, 10K, 10%, ½W | 23 | |
| 4-41 | R437 | | | MIL<br>RC20GF104K | RESISTOR Fixed Composition, 100K, 10%, ½W | 1 | |
| 4-42 | R438 | | | MIL<br>RC20GF202K | RESISTOR. Fixed Composition, 2K, 10%, ½W | 2 | |
| 4-43 | R439 | | | MIL<br>RC32GF431J | RESISTOR. Fixed Composition, 430 ohm, 5%, 1W | 1 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 4-44 | R460-<br>R466<br>R4114<br>R4118<br>R4122<br>R4126<br>R4130<br>R4134<br>R4138<br>R4142 | | | MIL<br>RC20GF273K | RESISTOR, Fixed Composition, 27K, 10%, ½W | 15 | |
| 4-45 | R493 | | | MIL<br>RC20GF223K | RESISTOR, Fixed Composition, 22K, 10%, ½W | 1 | |
| 4-46 | R494 | | | MIL<br>RC20GF182K | RESISTOR, Fixed Composition, 1.8K, 10%, ½W | 1 | |
| 4-47 | R495<br>R498<br>R4115<br>R4119<br>R4123<br>R4127<br>R4132<br>R4136<br>R4140<br>R4144<br>R4149<br>R4150 | | | MIL<br>RC20GF473K | RESISTOR, Fixed Composition, 47K, 10%, ½W | 12 | |
| 4-48 | R471<br>R474<br>R475<br>R477<br>R479 | | | MIL<br>RC20GF104K | RESISTOR, FIXED Composition, 100K, 10%, ½W | 5 | |
| 4-49 | R4116<br>R4120<br>R4124<br>R4128<br>R4131<br>R4135<br>R4139<br>R4143 | | | MIL<br>RC20GF472K | RESISTOR, Fixed Composition, 4.7K, 10%, ½W | 8 | |
| 4-50 | R4147<br>R4148 | | | MIL<br>RC32GF821K | RESISTOR, Fixed Composition, 820 ohms, 10%, ½W | 2 | |
| 4-51 | S401 | | | Centralab<br>PA2029 | SWITCH, Rotary | 1 | |
| 4-52 | S402 | | | Micro<br>2PB11 | SWITCH, Pushbutton | 1 | |
| 4-53 | TJ401<br>TJ402 | | | Cannon<br>DD50S | CONNECTOR, Female, 50 Pin Contact, 5 Amp Rating | 2 | |
| 4-54 | VM401-<br>VM408 | | | Assembly Prod.<br>261-C | METER, Relay (Clear Plastic) | 8 | |
| 4-55 | XI401 | | | Dialight Corp.<br>514001-111 | INDICATOR HOLDER | 1 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 4-56 | XM401-<br>XM403<br>XM460-<br>XM465 | | | Amphenol<br>TS103P02 | SOCKET, 9 Pin Miniature | 9 | |
| 4-57 | XN401<br>XN411<br>XN420 | | | Amphenol<br>77-MIP-11T | SOCKET, 11 Pin | 3 | |
| 4-58 | XN402-<br>XN410<br>XN412-<br>XN419<br>XN460-<br>XN466<br>XN468-<br>XN478<br>XN421-<br>XN428 | | | JAN<br>TS101P01 | SOCKET Octal, Mica Filled | 46 | |
| 4-59 | | | | Whitso<br>K105 | KNOB | 1 | |
| 3-1 | | | | MEC<br>76-3A | ASSEMBLY, POWER CONTROL | 1 | |
| 3-2 | CR301 | | | G. E.<br>IN1695 | DIODE | 1 | |
| 3-3 | CR302 | | | Transitron<br>T12G or<br>Clevite<br>CTP-503 | DIODE | 1 | |
| 3-4 | DS301 | | | Eldema<br>1CG12-4535 | LAMP, Neon to Spec. 21C-3864-7 | 1 | |
| 3-5 | I301 | | | Dialight Corp.<br>S-6 | LAMP, Incandescent, Candelabra Base, 110V Clear | 1 | |
| 3-6 | K301 | | | C. P. Clare<br>RP-3718-G76 | RELAY, 2 Form c (Type 7) to MEC Spec. Dwg. B1501F1A7 | 1 | |
| 3-7 | P301 | | | Cannon<br>DD-50P | PLUG | 1 | |
| 3-8 | R301 | | | MIL<br>RC20GF393K | RESISTOR, Fixed composition, 39K ±10% 1/2W | 1 | |
| 3-9 | R302 | | | Phaostron<br>CA4RS-1/2 | RESISTOR, Precision, 54K ±1% 1/2W | 1 | |
| 3-10 | R303 | | | Phaostron<br>CA4RS-1/2 | RESISTOR, Precision, 12K ±1% 1/2W | 1 | |
| 3-11 | R304<br>R307<br>R309<br>R311 | | | Phaostron<br>CA4RS-1/2 | RESISTOR, Precision, 20K ±1% 1/2W | 4 | |
| 3-12 | R305 | | | Phaostron<br>CA4RS-1/2 | RESISTOR, Precision, 85K ±1% 1/2W | 1 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 3-13 | R306<br>R308<br>R310 | | | Phaostron<br>CA4RS-1/2 | RESISTOR, Precision, 17K ±1% 1/2W | 3 | |
| 3-14 | S301 | | | Carling<br>2GL63-73 | SWITCH, Toggle | 1 | |
| 3-15 | S302 | | | Centralab<br>PA-2003 | SWITCH, Rotary | 1 | |
| 3-16 | VM301 | | | Beede<br>E-25 | METER | 1 | |
| 3-17 | XI301 | | | Dialight Corp.<br>514001-111 | INDICATOR HOLDER | 1 | |
| 3-18 | XK301 | | | JAN<br>TS101P01 | SOCKET, Octal, Mica filled | 1 | |
| 3-19 | XD301 | | | Eldema<br>11H4593 | INDICATOR HOLDER | 1 | |
| 3-20 | | | | Whitso<br>K-105 | KNOB | 1 | |
| 3-21 | | | | Eldema<br>11H4119 | LENS, Cap. (Red) | 1 | |
| 5-1 | | | | MEC<br>76-5A | ASSEMBLY, TEST | 1 | |
| 5-2 | C501 | | | Fansteel<br>F110-1 | CAPACITOR, (Blu-Cap) 10μf 25 vdc | 1 | |
| 5-3 | C502 | | | Fansteel<br>F308-1 | CAPACITOR, (Blu-Cap) 100μf 30 vdc | 1 | |
| 5-4 | C504 | | | Cornell Dubilier<br>PM4S5 | CAPACITOR, Fixed, Mylar, .05μf 400 vdc | 1 | |
| 5-5 | C505 | | | Cornell Dubilier<br>PM4P25 | CAPACITOR, Fixed, Mylar, .25μf 400 vdc | 1 | |
| 5-6 | C506<br>C510 | | | MIL<br>CM-19B-681K | CAPACITOR, Fixed Mica, 680μμf ±10% 500 vdc | 2 | |
| 5-7 | C508<br>C509<br>C517 | | | MIL<br>CM-19B-222K | CAPACITOR, Fixed Mica, 2200μμf ±10% 500 vdc | 3 | |
| 5-8 | C511<br>C518<br>C507 | | | MIL<br>CM-19B-102K | CAPACITOR, Fixed Mica, 1000μf ±10% 500 vdc | 3 | |
| 5-9 | C512 | | | Cornell Dubilier<br>PM4S1 | CAPACITOR, Fixed Mylar, .01μf 400 vdc | 1 | |
| 5-10 | C513<br>C519 | | | Cornell Dubilier<br>PM4P1 | CAPACITOR, Fixed Mylar, .1μf 400 vdc | 2 | |
| 5-11 | C514<br>C515 | | | G.E.<br>29F610 | CAPACITOR, Tantalytic, 8μf 30 vdc | 2 | |
| 5-12 | CR501<br>CR503-<br>CR505 | | | Transitron<br>T12G or<br>Clevite<br>CTP-503 | DIODE | 4 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 5-13 | CR502 | | | Hoffman IN703 | DIODE (Zener) | 1 | |
| 5-14 | I501 | | | Dialight Corp. S-6 | LAMP, Incandescent, Candelabra Base, 24V, Clear | 1 | |
| 5-15 | K501-K503 | | | C.P. Clare RP4461-G28 | RELAY, Type J, 4 Form c (Type 2) | 3 | |
| 5-16 | L501 | | | U.T.C. HVC-6 | INDUCTOR | 1 | |
| 5-17 | N501 | | | MEC TN-134 | TRANSISTOR NETWORK | 1 | |
| 5-18 | N502 N506 | | | MEC TN-111 | TRANSISTOR NETWORK | 2 | |
| 5-19 | N503 N509 | | | MEC TN-90B | TRANSISTOR NETWORK | 2 | |
| 5-20 | N504 | | | MEC TN-154 | TRANSISTOR NETWORK | 1 | |
| 5-21 | N505 N510 | | | MEC TN-138 | TRANSISTOR NETWORK | 2 | |
| 5-22 | N507 N508 | | | MEC TN-158 | TRANSISTOR NETWORK | 2 | |
| 5-23 | P501 | | | Cannon DD-50P | PLUG | 1 | |
| 5-24 | R502 R503 R506-R508 R511 R512 | | | MIL RC20GF103K | RESISTOR, Fixed composition, 10K ±10% 1/2W | 7 | |
| 5-25 | R509 | | | MIL RC20GF333K | RESISTOR, Fixed composition, 33K ±10% 1/2W | 1 | |
| 5-26 | R510 R501 | | | MIL RC20GF332K | RESISTOR, Fixed composition, 3.3K ±10% 1/2W | 2 | |
| 5-27 | R505 | | | MIL RC20GF202K | RESISTOR, Fixed composition, 2000Ω ±10% 1/2W | 1 | |
| 5-28 | S501 | | | Centralab PA-2011 | SWITCH, Rotary | 1 | |
| 5-29 | S502-S514 | | | Micro 2PB11 | SWITCH | 13 | |
| 5-30 | S515 | | | Carling 2GM63-73 | SWITCH, Toggle | 1 | |
| 5-31 | TJ501 | | | Cannon DD-50S | CONNECTOR | 1 | |
| 5-32 | XI501 | | | Dialight Corp. 514001-111 | INDICATOR HOLDER | 1 | |
| 5-33 | XN501-XN510 | | | JAN TS101P01 | SOCKET, Octal, Mica filled | 10 | |
| 5-34 | XK501-XK503 | | | Eby 9759-5 | SOCKET, 14 Pin Miniature, (Bottom Mounted) | 3 | |
| 5-35 | | | | Whitso K-105 | KNOB | 1 | |
| 5-36 | C516 | | | MIL CM-19B-331K | CAPACITOR, Molded Mica, 330μμf 500 vdc ±10% | 1 | |

| 1 ITEM NO. | 2 REFER. DESIG-NATOR | 3 CLASS | 3 STOCK NO. | 4 MFG. AND PART NO. | 5 DESCRIPTION 1 2 3 4 5 6 7 | 6 UNIT PER ASSY. | 7 PROCURE-MENT CODE |
|---|---|---|---|---|---|---|---|
| 7-1 | | | | MEC 76-7A | ASSEMBLY, 20-BIT SHIFT REGISTER | 1 | |
| 7-2 | C701 | | | MIL CM-19B-102K | CAPACITOR, Fixed Mica, 1000μμf 500vdc±10% | 1 | |
| 7-3 | C702 | | | Cornell Dubilier PM4S1 | CAPACITOR, Fixed, Mylar, .01μf 400 vdc | 1 | |
| 7-4 | C703 | | | MIL CM-19B-471K | CAPACITOR, Fixed, Mica, 470μμf 500 vdc ±10% | 1 | |
| 7-5 | C704 | | | Fansteel F110-1 | CAPACITOR, (Blu-Cap) 10μf 25 vdc Insulated Case. | 1 | |
| 7-6 | C705 C707 | | | Fansteel F308-1 | CAPACITOR, (Blu-Cap) 100μf 30 vdc Insulated Case. | 2 | |
| 7-7 | C706 | | | Cornell Dubilier PM4S5 | CAPACITOR, Fixed Mylar, .05μf 400 vdc | 1 | |
| 7-8 | CR701-CR703 | | | G.E. IN1692 | DIODE | 3 | |
| 7-9 | CR704 | | | Transitron T12G or Clevite CTP-503 | DIODE | 1 | |
| 7-10 | DS701-DS720 | | | MEC 16-102 | INDICATOR | 20 | |
| 7-11 | M701-M720 | | | MEC MN-11 | CORE, Magnetic | 20 | |
| 7-12 | M721 | | | MEC MN-13 | CORE, Magnetic | 1 | |
| 7-13 | N701-N720 | | | MEC TN-144 | TRANSISTOR NETWORK | 20 | |
| 7-14 | N721 | | | MEC TN-130B | TRANSISTOR NETWORK | 1 | |
| 7-15 | N722 | | | MEC TN-58 | TRANSISTOR NETWORK | 1 | |
| 7-16 | N723 | | | MEC TN-138B | TRANSISTOR NETWORK | 1 | |
| 7-17 | P701 | | | Cannon DD-50P | PLUG | 1 | |
| 7-18 | R701-R720 | | | MIL RC20GF273K | RESISTOR, Fixed composition, 27K ±10% 1/2W | 20 | |
| 7-19 | R721 R722 | | | MIL RC20GF103K | RESISTOR, Fixed composition, 10K ±10% 1/2W | 2 | |
| 7-20 | R723 | | | MIL RC20GF182K | RESISTOR, Fixed composition, 1.8K ±10% 1/2W | 1 | |
| 7-21 | R724 | | | MIL RC20GF332K | RESISTOR, Fixed composition, 3.3K ±10% 1/2W | 1 | |
| 7-22 | R725 | | | MIL RC20GF163J | RESISTOR, Fixed composition, 16K ±5% 1/2W | 1 | |
| 7-23 | R726 R728 | | | MIL RC20GF102J | RESISTOR, Fixed composition, 1K ±5% 1/2W | 2 | |
| 7-24 | R727 | | | MIL RC20GF161J | RESISTOR, Fixed composition, 160Ω ±5% 1/2W | 1 | |
| 7-25 | TJ701 | | | Cannon DD-50S | CONNECTOR | 1 | |
| 7-26 | XM701-XM721 | | | JAN TS103P02 | SOCKET, 9 Pin Miniature, Mica filled | 21 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 7-27 | XN701-XN723 | | | JAN TS101P01 | SOCKET, Octal, Mica filled | 23 | |
| 8-1 | | | | MEC 76-8A | ASSEMBLY, 10-BIT SHIFT REGISTER | 1 | |
| 8-2 | C801-C822 | | | MIL CM-19B-102K | CAPACITOR, Fixed Mica, 1000$\mu\mu$f ±10% 500 vdc | 22 | |
| 8-3 | C823 C824 | | | Cornell Dubilier PM4S1 | CAPACITOR, Fixed, Mylar, .01$\mu$f 400 vdc | 2 | |
| 8-4 | C825 | | | Fansteel F110-1 | CAPACITOR, (Blu-Cap) 10$\mu$f 25 vdc Insulated Case. | 1 | |
| 8-5 | C826 C827 | | | Fansteel F308-1 | CAPACITOR, (Blu-Cap) 100$\mu$f 30 vdc | 2 | |
| 8-6 | C828 C829 | | | MIL CM-19B-331K | CAPACITOR, Fixed, Mica, 330$\mu\mu$f ±10% 500 vdc | 2 | |
| 8-7 | CR801-CR803 | | | G.E. IN1692 | DIODE | 3 | |
| 8-8 | CR804 | | | Clevite CTP-503 | DIODE | 1 | |
| 8-9 | DS801-DS820 | | | MEC 16-102 | INDICATOR | 20 | |
| 8-10 | M801-M810 | | | MEC MN-11 | CORE, Magnetic | 10 | |
| 8-11 | M811 | | | MEC MN-13 | CORE, Magnetic | 1 | |
| 8-12 | N801-N820 | | | MEC TN-144 | TRANSISTOR NETWORK | 20 | |
| 8-13 | N821 | | | MEC TN-130B | TRANSISTOR NETWORK | 1 | |
| 8-14 | N822 M823 | | | MEC TN-138B | TRANSISTOR NETWORK | 2 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 8-15 | N824 | | | MEC TN-58 | TRANSISTOR NETWORK | 1 | |
| 8-16 | P801 | | | Cannon DD-50P | PLUG | 1 | |
| 8-17 | R801 | | | MIL RC20GF273K | RESISTOR, Fixed composition, 27K ±10% 1/2W | 20 | |
| 8-18 | R861-R864 | | | MIL RC20GF103K | RESISTOR, Fixed composition, 10K ±10% 1/2W | 4 | |
| 8-19 | R841-R860 | | | MIL RC20GF113J | RESISTOR, Fixed composition, 11K ±5% 1/2W | 20 | |
| 8-20 | R865 | | | MIL RC20GF182K | RESISTOR, Fixed composition, 1800Ω ±10% 1/2W | 1 | |
| 8-21 | R866 R867 | | | MIL RC20GF102K | RESISTOR, Fixed composition, 1K ±10% 1/2W | 2 | |
| 8-22 | R868 | | | MIL RC20GF332K | RESISTOR, Fixed composition, 3.3K ±10% 1/2W | 1 | |
| 8-23 | R869 | | | MIL RC20GF163J | RESISTOR, Fixed composition, 16K ±5% 1/2W | 1 | |
| 8-24 | TJ801 | | | Cannon DD-50S | CONNECTOR | 1 | |
| 8-25 | R821-R840 | | | MIL RC20GF104K | RESISTOR, Fixed composition, 100K ±10% 1/2W | 20 | |
| 8-26 | XM801-XM811 | | | JAN TS103P02 | SOCKET, 9 Pin Miniature, Mica filled | 11 | |
| 8-27 | XN801-XN824 | | | JAN TS101P01 | SOCKET, Octal, Mica filled | 24 | |
| 4-1 | | | | MEC 165-4C | ASSEMBLY, POWER SUPPLY | 1 | |
| 4-2 | C401 C402 C421-C423 | | | Mallory 20-71937 | CAPACITOR, Computer Grade, 4000μf 60 vdc, 2-1/16 x 4-1/2, Alum. can with acetate sleeve. | 5 | |
| 4-3 | C403 C425 C443 C444 | | | Cornell Dubilier PM4S1 | CAPACITOR, Fixed, Mylar, .01μf 400 vdc | 4 | |
| 4-4 | C424 | | | Cornell Dubilier PM4P1 | CAPACITOR, Fixed, Mylar, .1μf 400 vdc | 1 | |
| 4-5 | C404 C426 | | | Fansteel F308-1 | CAPACITOR, Blu-cap, 100μf 30 vdc | 2 | |
| 4-6 | C441 C442 | | | Mallory 20-71855 | CAPACITOR, Computer Grade, 2000μf 100 vdc, 2-1/16 x 4-1/2, Alum. can with acetate sleeve. | 2 | |
| 4-7 | C445 | | | Fansteel F316-1 | CAPACITOR, Blu-cap, 30μf 100 vdc | 1 | |
| 4-8 | CR401 CR421 | | | G.E. 4JA211AB1AC2 | RECTIFIER | 3 | |
| 4-9 | CR402 CR422 | | | International Rectifier IN1519 | DIODE, Zener (1Z4.7) | 2 | |
| 4-10 | CR442 | | | International Rectifier IN1524 | DIODE, Zener (1Z12) | 1 | |
| 4-11 | F401 F403 | | | Bussmann AGC | FUSE, 1 Amp | 2 | |
| 4-12 | F402 | | | Bussmann AGC | FUSE, 3 Amp | 1 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 4-13 | F404 | | | Bussmann MDX | FUSE, Fusetron, Slo-Blow, 3 Amp. | 1 | |
| 4-14 | P401 | | | Cannon DD-50P | PLUG | 1 | |
| 4-15 | Q423 Q442 | | | Delco 2N553 | TRANSISTOR, (Mount with Parts #100 & #101) | 2 | |
| 4-16 | Q401 Q421 Q441 Q422 | | | Delco 2N443 | TRANSISTOR, (Lug type Leads) | 4 | |
| 4-17 | Q402 Q403 Q424 Q443 | | | G. E. 2N525 | TRANSISTOR | 4 | |
| 4-18 | Q404 Q425 Q444 | | | Sylvania 2N377A | TRANSISTOR | 3 | |
| 4-19 | R401, R402 R421A R421B R441 R442 | | | Ward Leonard 5X1 | RESISTOR, Axiohm, 1Ω 5W | 6 | |
| 4-20 | R403 R443 | | | Ward Leonard 5X2 | RESISTOR, Axiohm, 2Ω 5W | 2 | |
| 4-21 | R404 R425 R444 | | | MIL RC42GF102K | RESISTOR, Fixed composition, 1K ±10% 2W | 3 | |
| 4-22 | R405 | | | MIL RC42GF151K | RESISTOR, Fixed composition, 150Ω ±10% 2W | 1 | |
| 4-23 | R406 | | | MIL RC20GF681K | RESISTOR, Fixed composition, 680Ω ±10% 1/2W | 1 | |
| 4-24 | R407 R428 R447 | | | MIL RC20GF101K | RESISTOR, Fixed composition, 100Ω ±10% 1/2W | 3 | |
| 4-25 | R408 | | | MIL RC20GF122K | RESISTOR, Fixed composition, 1.2K ±10% 1/2W | 1 | |
| 4-26 | R409 R430 R449 | | | MIL RC20GF822K | RESISTOR, Fixed composition, 8.2K ±10% 1/2W | 3 | |
| 4-27 | R410 R431 R450 | | | MIL RC20GF621J | RESISTOR, Fixed composition, 620Ω ±5% 1/2W | 3 | |
| 4-28 | R411 R432 | | | MIL RC20GF472K | RESISTOR, Fixed composition, 4.7K ±10% 1/2W | 2 | |
| 4-29 | R412 | | | MIL RC32GF121K | RESISTOR, Fixed composition, 120Ω ±10% 1W | 1 | |
| 4-30 | R414 R435 | | | Chicago Tel. RA20LASB250A | POTENTIOMETER, 25Ω 2W | 2 | |
| 4-31 | R415 | | | MIL RC32GF820J | RESISTOR, Fixed composition, 82Ω ±5% 1W | 1 | |
| 4-32 | R413 | | | MIL RC42GF131J | RESISTOR, Fixed composition, 130Ω ±5% 2W | 1 | |
| 4-33 | R422 | | | Ward Leonard 10F1 | RESISTOR, Fixed, Wire wound, 1Ω 10W | 1 | |
| 4-34 | R423 R424 | | | Ward Leonard 10F2 | RESISTOR, Fixed, Wire wound, 2Ω 10W | 2 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 4-35 | R426<br>R437 | | | Ward Leonard<br>10F150 | RESISTOR, Fixed, Wire wound, 150Ω 10W | 2 | |
| 4-36 | R427<br>R446 | | | MIL<br>RC32GF681K | RESISTOR, Fixed composition, 680Ω ±10% 1W | 2 | |
| 4-37 | R429<br>R448 | | | MIL<br>RC32GF122K | RESISTOR, Fixed composition, 1.2K ±10% 1W | 2 | |
| 4-38 | R433<br>R416 | | | MIL<br>RC42GF271K | RESISTOR, Fixed composition, 270Ω ±10% 2W | 2 | |
| 4-39 | R436 | | | MIL<br>RC32GF510J | RESISTOR, Fixed composition, 51Ω ±5% 1W | 1 | |
| 4-40 | R434 | | | MIL<br>RC42GF181J | RESISTOR, Fixed composition, 180Ω ±5% 2W | 1 | |
| 4-41 | R451 | | | MIL<br>RC42GF302J | RESISTOR, Fixed composition, 3K ±5% 2W | 1 | |
| 4-42 | R453 | | | Allen Bradley<br>JLU-1011 or<br>JA1L040S101UC | POTENTIOMETER, 100Ω 2W, Linear Taper | 1 | |
| 4-43 | R454 | | | MIL<br>RC42GF272J | RESISTOR, Fixed composition, 2.7K ±5% 2W | 1 | |
| 4-44 | R455 | | | Ward Leonard<br>5X500 | RESISTOR, Fixed, Axiohm, 500Ω 5W | 1 | |
| 4-45 | R452 | | | MIL<br>RC32GF561J | RESISTOR, Fixed composition, 560Ω ±5% 1W | 1 | |
| 4-46 | R445 | | | Ward Leonard<br>10F250 | RESISTOR, Fixed, Wire wound, 250Ω 10W | 1 | |
| 4-47 | T401 | | | TTI 5486 | TRANSFORMER | 1 | |
| 4-48 | TJ401-<br>TJ404 | | | H.H. Smith<br>221 | JACK, Midget Banana (Black) | 4 | |
| 4-49 | XF401-<br>XF404 | | | Bussmann<br>HKP | FUSEHOLDER | 4 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 9-1 | | | | MEC 76-9A | ASSEMBLY, POWER SUPPLY (-17V and -20V) | 1 | |
| 9-2 | C901-C905 C906 | | | Mallory 20-71937 | CAPACITOR, Computer Grade, 4000$\mu$f 60 vdc 2-1/16 x 4-1/2, Alum. can with Acetate Sleeve. | 6 | |
| 9-3 | C907 | | | Cornell Dubilier PM4P5 | CAPACITOR, Fixed, Mylar, .5$\mu$f 400 vdc | 1 | |
| 9-4 | C908 | | | Mallory 20-71844 | CAPACITOR, Computer Grade, 15,000$\mu$f 15 vdc 2-9/16 x 4-1/2 Alum. can with Acetate Sleeve | 1 | |
| 9-5 | CR901 CR902 | | | G. E. ZJ50B(C60) | DIODE, 100 V | 2 | |
| 9-6 | CR903 | | | Westinghouse IN1200 | DIODE, | 1 | |
| 9-7 | CR904-CR907 CR909-CR911 | | | G. E. IN1692 | DIODE | 7 | |
| 9-8 | CR908 | | | G. E. 4JA211BB1AC1 | RECTIFIER | 1 | |
| 9-9 | L901 | | | Sterling Trans. T3891 | CHOKE | 1 | |
| 9-10 | N901 | | | MEC TN-160 | TRANSISTOR NETWORK | 1 | |
| 9-11 | Q901 | | | Delco 2N443 | TRANSISTOR, (Lug type Leads) | 1 | |
| 9-12 | R901 | | | MIL RC20GF622J | RESISTOR, Fixed composition, 6.2K ±5% 1/2W | 1 | |
| 9-13 | R902 | | | Ohmite CLU-1521 or JA1L040S152UC | POTENTIOMETER, 1.5K 2W, Linear Taper | 1 | |
| 9-14 | R903 | | | MIL RC20GF621J | RESISTOR, Fixed composition, 620Ω ±5% 1/2W | 1 | |
| 9-15 | R904 | | | MIL RC20GF331K | RESISTOR, Fixed composition, 330Ω ±10% 1/2W | 1 | |
| 9-16 | R905 | | | Ohmite 0600A | RESISTOR, Fixed, Wire wound, 5Ω 100W (with Mounting Bracket #12) | 1 | |
| 9-17 | R906 | | | MIL RC42GF332K | RESISTOR, Fixed composition, 3.3K ±10% 2W | 1 | |
| 9-18 | R907-R909 | | | Ward Leonard 20F1 | RESISTOR, Fixed, Wire wound, 1Ω 20W | 3 | |
| 9-19 | R910 | | | MIL RC20GF101K | RESISTOR, Fixed composition, 100Ω ±10% 1/2W | 1 | |
| 9-20 | T901 | | | Industrial Trans. MP-8610 | TRANSFORMER | 1 | |
| 9-21 | T902 | | | Sterling Trans. T-3890 | TRANSFORMER | 1 | |
| 9-22 | T903 | | | Chicago Trans. FMS-6 | TRANSFORMER | 1 | |
| 9-23 | TJ901-TJ903 | | | H.H. Smith 221 | JACK, Midget Banana (Black) | 3 | |
| 9-24 | XN901 | | | Amphenol 77-MIP-11T | SOCKET, 11 Pin | 1 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 1-1 | | | | MEC 76-1ABA | Assembly, Connector Bracket | 1 | |
| 1-2 | I4-I6 | | | Dialight Corp 6S6 | Lamp, Incandescent, Candelabra Base 125V Clear | 3 | |
| 1-3 | J105 J106 J109 J114 | | | Amphenol 97-3102A-36-404P | Connector | 8 | |
| 1-4 | S2 | | | Carling 2GM63-73 | Switch, Toggle DPDT | 1 | |
| 1-5 | TB2 | | | Cinch Jones 2-140 | Terminal Strip | 1 | |
| 1-6 | XI1-XI3 | | | Dialight Corp 514001-111 | Indicator Holder | 3 | |
| 1-1 | | | | MEC 76-1AAA | Assembly, Connector Bracket | 1 | |
| 1-2 | F1-F3 | | | Bussmann BAN | Fuse, 15 Amp | 3 | |
| 1-3 | I1-I3 | | | Dialight Corp 6S6 | Lamp, Incandescent, Candelabra Base 125V, Clear | 3 | |
| 1-4 | J101-J104 J107 J108 | | | Amphenol 97-3102A-36-404P | Connector | 6 | |
| 1-5 | J40 | | | Cannon MS3102A-48-5P | Connector | 1 | |
| 1-6 | J98 | | | Cannon MS3102A-24-10P | Connector | 1 | |
| 1-7 | J99 | | | Cannon MS3102A-24-28P | Connector | 1 | |
| 1-8 | S1 | | | Carling 2GM63-73 | Switch, Toggle, DPDT | 1 | |
| 1-9 | TB1 | | | Cinch Jones 2-140 | Terminal Strip | 1 | |
| 1-10 | XF1-XF3 | | | Bussmann HPC | Fuse Holder | 3 | |

| 1 | 2 | 3 | | 4 | 5 | 6 | 7 |
|---|---|---|---|---|---|---|---|
| ITEM NO. | REFER. DESIG-NATOR | CLASS | STOCK NO. | MFG. AND PART NO. | DESCRIPTION 1 2 3 4 5 6 7 | UNIT PER ASSY. | PROCURE-MENT CODE |
| 1-11 | XI1-XI3 | | | Dialight Corp 514001-111 | Indicator Holder | 3 | |
| 1-12 | | | | Allen Bradley 702AOD92 | Contactor | 1 | |
| 1 | | | | McLean 2EB508C | ASSEMBLY: BLOWER | 1 | |

# CHAPTER VIII

# WIRE LIST

INDEX

| WIRE NO. | REFERENCE | LIST | PAGE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | J1 | 50-51 | 8-27 | 20 Bit SR Bits 337-356 | | |
| | J2 | 52-53 | 8-28 | 20 Bit SR Bits 357-376 | | |
| | J3 | 54-56 | 8-29&30 | 20 Bit SR Bits 377-396 | | |
| | J4 | 57-59 | 8-30&31 | 20 Bit SR Bits 397-408 | | |
| | J5 | 60-62 | 8-32&33 | 20 Bit SR Bits 257-276 | | |
| | J6 | 63-65 | 8-33&34 | 20 Bit SR Bits 277-296 | | |
| | J7 | 66-68 | 8-35&36 | 20 Bit SR Bits 297-316 | | |
| | J8 | 69-71 | 8-36&37 | 20 Bit SR Bits 317-336 | | |
| | J9 | 72-74 | 8-38&39 | 10 Bit SR Bits 217-226 | | |
| | J10 | 75-77 | 8-39&40 | 10 Bit SR Bits 227-236 | | |
| | J11 | 78-80 | 8-41&42 | 10 Bit SR Bits 237-246 | | |
| | J12 | 81-82 | 8-42&43 | 10 Bit SR Bits 247-256 | | |
| | J13 | 83-85 | 8-43&44 | 10 Bit SR Bits 177-186 | | |
| | J14 | 86-88 | 8-45&46 | 10 Bit SR Bits 187-196 | | |
| | J15 | 89-91 | 8-46&47 | 10 Bit SR Bits 197-206 | | |
| | J16 | 92-94 | 8-48&49 | 10 Bit SR Bits 207-216 | | |

NOTES:

LIST 1

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| WIRE NO. | REFERENCE | LIST | PAGE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | J20 | 95-97 | 8-49&50 | 10 Bit SR Bits 137-146 | | |
| | J21 | 98-100 | 8-51&52 | 10 Bit SR Bits 147-156 | | |
| | J22 | 101-103 | 8-52&53 | 10 Bit SR Bits 157-166 | | |
| | J23 | 104-105 | 8-54 | 10 Bit SR Bits 167-176 | | |
| | J24 | 106-108 | 8-55&56 | 10 Bit SR Bits 97-106 | | |
| | J25 | 109-111 | 8-56&57 | 10 Bit SR Bits 107-116 | | |
| | J26 | 112-114 | 8-58&59 | 10 Bit SR Bits 117-126 | | |
| | J27 | 115-117 | 8-59&60 | 10 Bit SR Bits 127-136 | | |
| | J28 | (NOT USED) | | | | |
| | J29 | 118-120 | 8-61&62 | Control Bit 81-86 | | |
| | J30 | 121-122 | 8-62&63 | Power Control | | |
| | J31 | 123-125 | 8-63&64 | 20 Bit SR Bit 41-60 | | |
| | J32 | 126-128 | 8-65&66 | 20 Bit SR Bit 61-80 | | |
| | J33 | 129-131 | 8-66&67 | 10 Bit SR Bit 87-96 | | |
| | J34 | 132-133 | 8-68 | TEST | | |
| | J35 | 134-136 | 8-69&70 | 20 Bit SR Bits 1-20 | | |
| | J36 | 137-139 | 8-70&71 | 20 Bit SR Bits 21-40 | | |
| | J37 | 140-141 | 8-72 | Power Supply | | |
| | J40 | 142-146 | 8-73,74&75 | Inter Rack | | |
| | P40 | 147-151 | 8-75,76&77 | Inter Rack | | |

NOTES:

LIST 2

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| WIRE NO. | REFERENCE | LIST | PAGE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | J98 | 6 | 8-5 | Power Input | | |
| | J99 | 7 | 8-6 | Data Input | | |
| | J101 | 8-10 | 8-6&7 | Outputs Bits 1-42 Every | | |
| | J102 | 11-13 | 8-8&9 | Outputs Bits 43-85 Every | | |
| | J103 | 14-16 | 8-9&10 | Outputs Bits 86-110 Odd | | |
| | J104 | 17-19 | 8-10&11 | Outputs Bits 111-158 Odd | | |
| | J105 | 20-22 | 8-12&13 | Outputs Bits 161-206 Odd | | |
| | J106 | 23-25 | 8-13&14 | Outputs Bits 207-256 Odd | | |
| | J107 | 26-28 | 8-15&16 | Outputs Bits 86-126 Even | | |
| | J108 | 29-31 | 8-16&17 | Outputs Bits 127-167 Even | | |
| | J109 | 32-34 | 8-18&19 | Outputs Bits 168-208 Even | | |
| | J110 | 35-37 | 8-19&20 | Outputs Bits 209-256 Even | | |
| | J111 | 38-40 | 8-21&22 | Outputs Bits 257-298 Every | | |
| | J112 | 41-43 | 8-22&23 | Outputs Bits 299-318 Every<br>Outputs Bits 329-359 except 339 Every | | |
| | J113 | 44-46 | 8-24&25 | Outputs Bits 159-160<br>319-328 Every<br>360-379 | | |
| | J114 | 47-49 | 8-25&26 | Outputs Bits 381-408 Every<br>339, 380 Every | | |

NOTES:

LIST 3

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| WIRE NO. | REFERENCE | LIST | PAGE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +12V(A) | 152-153 | 8-78 | | | |
| | OV(A) | 154 | 8-79 | | | |
| | -20V(A) | 155 | 8-79 | | | |
| | -85V(A) | 156-157 | 8-80 | | | |
| | OV(B) | 158 | 8-81 | | | |
| | -17V(B) | 159 | 8-81 | | | |
| | -20V(B) | 160 | 8-82 | | | |
| | OV(C) | 161 | 8-82 | | | |
| | -17V(C) | 162 | 8-83 | | | |
| | -20V(C) | 163 | 8-83 | | | |
| | OV(D) | 164 | 8-84 | | | |
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| | -20V(D) | 167-168 | 8-85&86 | | | |

NOTES:

LIST 4

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| WIRE NO. | REFERENCE | LIST | PAGE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
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| | F1 | 170 | | | | |
| | F2 | 170 | | | | |
| | F3 | 170 | | | | |
| | I1 | 171 | | | | |
| | I2 | 171 | | | | |
| | I3 | 171 | | | | |
| | I4 | 172 | | | | |
| | I5 | 172 | | | | |
| | I6 | 172 | | | | |
| | TB1 | 173 | | | | |
| | TB2 | 174 | | | | |
| | T902 (B Supply) | 175 | | | | |
| | T902 (C Supply) | 176 | | | | |
| | T902 (D Supply) | 177 | | | | |
| | SW1 | 178 | | | | |
| | SW2 | 179 | | | | |

NOTES:

LIST 5

J98

AC INPUT

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | A | F1-1 | jumper | AC Ø1 Input | 12 | BR |
| | B | F2-1 | | AC Ø2 Input | 12 | BR |
| | C | F3-1 | | AC Ø3 Input | 12 | BR |
| | D | | | AC Common | | |
| | | J40-CD | | | 12 | W |
| | | J40-CD | | | 12 | W |
| | | T902-1 (B Supply) | | | 12 | W |
| | | TB1-1 | | | 16 | W |
| | | I1-1 | jumper | AC Common | 22 | W |
| | E | | | | | |
| | F | OV(A)-2 | | OV (Signal Ground) | 18 | BK |
| | G | Rack | | Rack Ground | 12 | BK |

NOTES:

LIST 6

J99
DATA INPUT

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | A | J34-1 | 1 | Data #1 Input | | V |
| | B | J34-2 | | Data #2 Input | | G |
| | C | J34-3 | | Data #3 Input | | Y |
| | D | J34-4 | | Data #4 Input | | O |
| | E | J34-5 | | Copy #1 Input | | V |
| | F | J34-6 | | Copy #2 Input | | G |
| | G | J34-7 | | Copy #3 Input | | Y |
| | H | J34-8 | | Copy #4 Input | | O |
| | J | J34-9 | | EOW #1 Input | | V |
| | K | J34-10 | | EOW #2 Input | | G |
| | L | J34-11 | | EOW #3 Input | | Y |
| | M | J34-12 | 1 | EOW #4 Input | | O |
| | N | | | | | |
| | P | | | | | |
| | Q | | | | | |
| | R | | | | | |
| | S | | | | | |
| | T | | | | | |
| | U | | | | | |
| | V | | | | | |
| | W | | | | | |
| | X | | | | | |
| | Y | OV(A)-20 | | OV (Signal Gnd) | 20 | BK |
| | Z | Rack | | Rack Ground | 20 | BK |

NOTES: ALL WIRES 22 GUAGE UNLESS OTHERWISE NOTED

24-28P

LIST 7

J101

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J35-20 | 2 | Bit #1 Output Every | * | O |
| | A | J35-19 | | #2 | | Y |
| | 2 | J35-18 | | #3 | | G |
| | B | J35-17 | | #4 | | BL |
| | 3 | J35-16 | | #5 | | V |
| | C | J35-15 | | #6 | | W/O |
| | 4 | J35-14 | | #7 | | W/Y |
| | D | J35-13 | | #8 | | W/G |
| | 5 | J35-12 | | #9 | | W/BL |
| | E | J35-11 | | #10 | | W/V |
| | 6 | J35-10 | | #11 | | O |
| | F | J35-9 | | #12 | | Y |
| | 7 | J35-8 | | #13 | | G |
| | G | J35-7 | | #14 | | BL |
| | 8 | J35-6 | | #15 | | V |
| | H | J35-5 | | #16 | | W/O |
| | 9 | J35-4 | | #17 | | W/Y |
| | I | J35-3 | | #18 | | W/G |
| | 10 | J35-2 | | #19 | | W/BL |
| | J | J35-1 | | #20 | | W/V |
| | 11 | J36-20 | | #21 | | O |
| | K | J36-19 | | #22 | | Y |
| | 12 | J36-18 | | #23 | | G |
| | L | J36-17 | | #24 | | BL |
| | 13 | J36-16 | 2 | Bit #25 Output Every | | V |

NOTES: (*) #22 unless otherwise specified.

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LIST 8

J101

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | M | J36-15 | 2 | Bit #26 Output Every | * | W/O |
| | 14 | J36-14 | | #27 | | W/Y |
| | N | J36-13 | | #28 | | W/G |
| | 15 | J36-12 | | #29 | | W/BL |
| | O | J36-11 | | #30 | | W/V |
| | 16 | J36-10 | | #31 | | O |
| | P | J36-9 | | #32 | | Y |
| | 17 | J36-8 | | #33 | | G |
| | Q | J36-7 | | #34 | | BL |
| | 18 | J36-6 | | #35 | | V |
| | R | J36-5 | | #36 | | W/O |
| | 19 | J36-4 | | #37 | | W/Y |
| | S | J36-3 | | #38 | | W/G |
| | 20 | J36-2 | | #39 | | W/BL |
| | T | J36-1 | | #40 | | W/V |
| | 21 | J31-20 | | #41 | | O |
| | U | J31-19 | 2 | Bit #42 Output Every | | Y |
| | 22 | | | | | |
| | V | | | | | |
| | 23 | | | | | |
| | W | | | | | |
| | 24 | J29-13 | 1 | D/A Hold | | BL |
| | X | | | | | |
| | 25 | | | | | |
| | Y | | | | | |

NOTES:

(*) #22 unless otherwise specified.

LIST 9

J101

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | | | Shield | 20 | BK |
| | -4.5 | | | Shield | 20 | BK |

NOTE: All Black wires from pins (+4.5 and -4.5) on J101, J102, J103, J104, J107 and J108 are to be connected together and a single #14 Black is to connect to Rack.

All Black wires from pins (+4.5 and -4.5) on J105, J106, J109, J110, J111, J112, J113 and J114 are to be connected together and a single #14 Black is to connect to Rack.

NOTES:

LIST 10

J102

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J31-18 | 2 | Bit #43 Output Every | * | O |
| | A | J31-17 | | #44 | | Y |
| | 2 | J31-16 | | #45 | | G |
| | B | J31-15 | | #46 | | BL |
| | 3 | J31-14 | | #47 | | V |
| | C | J31-13 | | #48 | | W/O |
| | 4 | J31-12 | | #49 | | W/Y |
| | D | J31-11 | | #50 | | W/G |
| | 5 | J31-10 | | #51 | | W/BL |
| | E | J31-9 | | #52 | | W/V |
| | 6 | J31-8 | | #53 | | O |
| | F | J31-7 | | #54 | | Y |
| | 7 | J31-6 | | #55 | | G |
| | G | J31-5 | | #56 | | BL |
| | 8 | J31-4 | | #57 | | V |
| | H | J31-3 | | #58 | | W/O |
| | 9 | J31-2 | | #59 | | W/Y |
| | I | J31-1 | | #60 | | W/G |
| | 10 | J32-20 | | #61 | | W/BL |
| | J | J32-19 | | #62 | | W/V |
| | 11 | J32-18 | | #63 | | O |
| | K | J32-17 | | #64 | | Y |
| | 12 | J32-16 | | #65 | | G |
| | L | J32-15 | | #66 | | BL |
| | 13 | J32-14 | 2 | Bit #67 Output Every | | V |

NOTES: (*) #22 unless otherwise specified.

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LIST 11

J102

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | M | J32-13 | 2 | Bit #68 Output Every | * | W/O |
| | 14 | J32-12 | | #69 | | W/Y |
| | N | J32-11 | | #70 | | W/G |
| | 15 | J32-10 | | #71 | | W/BL |
| | O | J32-9 | | #72 | | W/V |
| | 16 | J32-8 | | #73 | | O |
| | P | J32-7 | | #74 | | Y |
| | 17 | J32-6 | | #75 | | G |
| | Q | J32-5 | | #76 | | BL |
| | 18 | J32-4 | | #77 | | V |
| | R | J32-3 | | #78 | | W/O |
| | 19 | J32-2 | | #79 | | W/Y |
| | S | J32-1 | 2 | #80 | | W/G |
| | 20 | J29-40 | 1 | #81 | | W/BL |
| | T | J29-39 | | #82 | | W/V |
| | 21 | J29-38 | | #83 | | O |
| | U | J29-37 | 1 | #84 | | Y |
| | 22 | J29-36 | | Bit #85 Output Every | | G |
| | V | | | | | |
| | 23 | | | | | |
| | W | | | | | |
| | 24 | | | | | |
| | X | | | | | |
| | 25 | | | | | |
| | Y | | | | | |

NOTES: (*) #22 unless otherwise specified.

LIST 12

J102

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10 | | Shield | 20 | BK |

NOTES:

LIST 13

J103

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J29-35 | 1 | Bit #86 Output Odd | * | O |
| | A | J33-19 | | #87 | | W/Y |
| | 2 | J33-17 | | #88 | | W/G |
| | B | J33-15 | | #89 | | W/BL |
| | 3 | J33-13 | | #90 | | W/V |
| | C | J33-11 | | #91 | | O |
| | 4 | J33-9 | | #92 | | Y |
| | D | J33-7 | | #93 | | G |
| | 5 | J33-5 | | #94 | | BL |
| | E | J33-3 | | #95 | | V |
| | 6 | J33-1 | 1 | #96 | | W/O |
| | F | J24-19 | 2 | #97 | | W/Y |
| | 7 | J24-17 | | #98 | | W/G |
| | G | J24-15 | | #99 | | W/BL |
| | 8 | J24-13 | | #100 | | W/V |
| | H | J24-11 | | #101 | | O |
| | 9 | J24-9 | | #102 | | Y |
| | I | J24-7 | | #103 | | G |
| | 10 | J24-5 | | #104 | | BL |
| | J | J24-3 | | #105 | | V |
| | 11 | J24-1 | | #106 | | W/O |
| | K | J25-19 | | #107 | | W/Y |
| | 12 | J25-17 | | #108 | | W/G |
| | L | J25-15 | | #109 | | W/BL |
| | 13 | J25-13 | 2 | Bit #110 Output Odd | | W/V |

NOTES: (*) #22 unless otherwise specified.
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LIST 14

J103

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10 | | Shield | 20 | BK |

NOTES:

LIST 16

J104

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J25-11 | 2 | Bit #111 Output Odd | * | O |
| | A | J25-9 | | #112 | | Y |
| | 2 | J25-7 | | #113 | | G |
| | B | J25-5 | 2 | #114 | | BL |
| | 3 | J25-3 | 1 | #115 | | V |
| | C | J25-1 | | #116 | | W/O |
| | 4 | J26-19 | | #117 | | W/Y |
| | D | J26-17 | | #118 | | W/G |
| | 5 | J26-15 | | #119 | | W/BL |
| | E | J26-13 | | #120 | | W/V |
| | 6 | J26-11 | | #121 | | O |
| | F | J26-9 | | #122 | | Y |
| | 7 | J26-7 | | #123 | | G |
| | G | J26-5 | | #124 | | BL |
| | 8 | J26-3 | | #125 | | W/V |
| | H | J26-1 | | #126 | | W/O |
| | 9 | J27-19 | | #127 | | W/Y |
| | I | J27-17 | | #128 | | W/G |
| | 10 | J27-15 | | #129 | | W/BL |
| | J | J27-13 | | #130 | | W/V |
| | 11 | J27-11 | | #131 | | O |
| | K | J27-9 | | #132 | | Y |
| | 12 | J27-7 | | #133 | | G |
| | L | J27-5 | | #134 | | BL |
| | 13 | J27-3 | 1 | Bit #135 Output Odd | | V |

NOTES: (*) #22 unless otherwise specified.

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LIST 17

J104

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | M | J27-1 | 2 | Bit #136 Output Odd | * | W/O |
| | 14 | J20-19 | | #137 | | W/Y |
| | N | J20-17 | | #138 | | W/G |
| | 15 | J20-15 | | #139 | | W/BL |
| | O | J20-13 | | #140 | | W/V |
| | 16 | J20-11 | | #141 | | O |
| | P | J20-9 | | #142 | | Y |
| | 17 | J20-7 | | #143 | | G |
| | Q | J20-5 | | #144 | | BL |
| | 18 | J20-3 | | #145 | | V/ |
| | R | J20-1 | | #146 | | W/O |
| | 19 | J21-19 | | #147 | | W/Y |
| | S | J21-17 | | #148 | | W/G |
| | 20 | J21-15 | | #149 | | W/BL |
| | T | J21-13 | | #150 | | W/V |
| | 21 | J21-11 | | #151 | | O |
| | U | J21-9 | | #152 | | Y |
| | 22 | J21-7 | | #153 | | G |
| | V | J21-5 | | #154 | | BL |
| | 23 | J21-3 | | #155 | | V/ |
| | W | J21-1 | 2 | #156 | | W/O |
| | 24 | J22-19 | 1 | #157 | | W/Y |
| | X | J22-17 | 1 | Bit #158 Output Odd | | W/G |
| | 25 | | | | | |
| | Y | | | | | |

NOTES: (*) All wires #22 unless otherwise specified

LIST 18

J104

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10. | | Shield | 20 | BK |

NOTES:

LIST 19

J105

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | A | | | | | |
| | 2 | P40-A | 5 | Bit #161 Output Odd | * | G |
| | B | P40-B | | #162 | | BL |
| | 3 | P40-C | | #163 | | V |
| | C | P40-D | | #164 | | W/O |
| | 4 | P40-E | | #165 | | W/Y |
| | D | P40-F | | #166 | | W/G |
| | 5 | P40-G | | #167 | | W/BL |
| | E | P40-H | | #168 | | W/V |
| | 6 | P40-J | | #169 | | O |
| | F | P40-K | | #170 | | Y |
| | 7 | P40-L | | #171 | | G |
| | G | P40-M | | #172 | | BL |
| | 8 | P40-N | | #173 | | V |
| | H | P40-P | | #174 | | W/O |
| | 9 | P40-Q | | #175 | | W/Y |
| | I | P40-R | 5 | #176 | | W/G |
| | 10 | J13-19 | 4 | #177 | | W/BL |
| | J | J13-17 | | #178 | | W/V |
| | 11 | J13-15 | | #179 | | O |
| | K | J13-13 | | #180 | | Y |
| | 12 | J13-11 | | #181 | | G |
| | L | J13-9 | | #182 | | BL |
| | 13 | J13-7 | 4 | Bit #183 Output Odd | | V |

NOTES: (*) #22 unless otherwise specified.

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LIST 20

J105

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | M | J13-5 | 4 | Bit #184 Output Odd | * | W/O |
| | 14 | J13-3 | | #185 | | W/Y |
| | N | J13-1 | | #186 | | W/G |
| | 15 | J14-19 | | #187 | | W/BL |
| | O | J14-17 | | #188 | | W/V |
| | 16 | J14-15 | | #189 | | O |
| | P | J14-13 | | #190 | | Y |
| | 17 | J14-11 | | #191 | | G |
| | Q | J14-9 | | #192 | | BL |
| | 18 | J14-7 | | #193 | | V |
| | R | J14-5 | | #194 | | W/O |
| | 19 | J14-3 | | #195 | | W/Y |
| | S | J14-1 | 4 | #196 | | W/G |
| | 20 | J15-19 | 3 | #197 | | W/BL |
| | T | J15-17 | | #198 | | W/V |
| | 21 | J15-15 | | #199 | | O |
| | U | J15-13 | | #200 | | Y |
| | 22 | J15-11 | | #201 | | G |
| | V | J15-9 | | #202 | | BL |
| | 23 | J15-7 | | #203 | | V |
| | W | J15-5 | | #204 | | W/O |
| | 24 | J15-3 | | #205 | | W/Y |
| | X | J15-1 | 3 | Bit #206 Output Odd | | W/G |
| | 25 | | | | | |
| | Y | | | | | |

NOTES: (*) All wires #22 unless otherwise specified

LIST 21

J105

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10. | | Shield | 20 | BK |

NOTES:

LIST 22

J106

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J16-19 | 3 | Bit #207 Output Odd | * | O |
| | A | J16-17 | | #208 | | Y |
| | 2 | J16-15 | | #209 | | G |
| | B | J16-13 | | #210 | | BL |
| | 3 | J16-11 | | #211 | | V |
| | C | J16-9 | | #212 | | W/O |
| | 4 | J16-7 | | #213 | | W/Y |
| | D | J16-5 | | #214 | | W/G |
| | 5 | J16-3 | | #215 | | W/BL |
| | E | J16-1 | 3 | #216 | | W/V |
| | 6 | J9-19 | 4 | #217 | | O |
| | F | J9-17 | | #218 | | Y |
| | 7 | J9-15 | | #219 | | G |
| | G | J9-13 | | #220 | | BL |
| | 8 | J9-11 | | #221 | | V |
| | H | J9-9 | | #222 | | W/O |
| | 9 | J9-7 | | #223 | | W/Y |
| | I | J9-5 | | #224 | | W/G |
| | 10 | J9-3 | | #225 | | W/BL |
| | J | J9-1 | | #226 | | W/V |
| | 11 | J10-19 | | #227 | | O |
| | K | J10-17 | | #228 | | Y |
| | 12 | J10-15 | | #229 | | G |
| | L | J10-13 | | #230 | | BL |
| | 13 | J10-11 | 4 | Bit #231 Output Odd | | V |

NOTES: (*) #22 unless otherwise specified.

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LIST 23

J106

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | M | J10-9 | 4 | Bit #232 Output Odd | * | W/O |
| | 14 | J10-7 | | #233 | | W/Y |
| | N | J10-5 | | #234 | | W/G |
| | 15 | J10-3 | | #235 | | W/BL |
| | O | J10-1 | 4 | #236 | | W/V |
| | 16 | J11-19 | 3 | #237 | | O |
| | P | J11-17 | | #238 | | Y |
| | 17 | J11-15 | | #239 | | G |
| | Q | J11-13 | | #240 | | BL |
| | 18 | J11-11 | | #241 | | V |
| | R | J11-9 | | #242 | | W/O |
| | 19 | J11-7 | | #243 | | W/Y |
| | S | J11-5 | | #244 | | W/G |
| | 20 | J11-3 | | #245 | | W/BL |
| | T | J11-1 | | #246 | | W/V |
| | 21 | J12-19 | | #247 | | O |
| | U | J12-17 | | #248 | | Y |
| | 22 | J12-15 | | #249 | | G |
| | V | J12-13 | | #250 | | BL |
| | 23 | J12-11 | | #251 | | V |
| | W | J12-9 | | #252 | | W/O |
| | 24 | J12-7 | | #253 | | W/Y |
| | X | J12-5 | | #254 | | W/G |
| | 25 | J12-3 | | #255 | | W/BL |
| | Y | J12-1 | 3 | Bit #256 Output Odd | | W/V |

NOTES: (*) #22 unless otherwise specified.

LIST 24

J106

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10 | | Shield | 20 | BK |

NOTES:

LIST 25

J107

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J29-34 | 1 | Bit #86 Output Even | * | W/O |
| | A | J33-20 | | #87 | | Y |
| | 2 | J33-18 | | #88 | | G |
| | B | J33-16 | | #89 | | BL |
| | 3 | J33-14 | | #90 | | V |
| | C | J33-12 | | #91 | | W/O |
| | 4 | J33-10 | | #92 | | W/Y |
| | D | J33-8 | | #93 | | W/G |
| | 5 | J33-6 | | #94 | | W/BL |
| | E | J33-4 | | #95 | | W/V |
| | 6 | J33-2 | | #96 | | O |
| | F | J24-20 | | #97 | | Y |
| | 7 | J24-18 | | #98 | | G |
| | G | J24-16 | | #99 | | BL |
| | 8 | J24-14 | | #100 | | V |
| | H | J24-12 | | #101 | | W/O |
| | 9 | J24-10 | | #102 | | W/Y |
| | I | J24-8 | | #103 | | W/G |
| | 10 | J24-6 | | #104 | | W/BL |
| | J | J24-4 | | #105 | | W/V |
| | 11 | J24-2 | 1 | #106 | | O |
| | K | J25-20 | 2 | #107 | | Y |
| | 12 | J25-18 | | #108 | | G |
| | L | J25-16 | | #109 | | BL |
| | 13 | J25-14 | 2 | Bit #110 Output Even | | V |

NOTES: (*) #22 unless otherwise specified.

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LIST 26

J107

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | M | J25-12 | 2 | Bit #111 Output Even | * | W/O |
| | 14 | J25-10 | | #112 | | W/Y |
| | N | J25-8 | | #113 | | W/G |
| | 15 | J25-6 | | #114 | | W/BL |
| | O | J25-4 | | #115 | | W/V |
| | 16 | J25-2 | 2 | #116 | | O |
| | P | J26-20 | 1 | #117 | | Y |
| | 17 | J26-18 | | #118 | | G |
| | Q | J26-16 | | #119 | | BL |
| | 18 | J26-14 | | #120 | | V |
| | R | J26-12 | | #121 | | W/O |
| | 19 | J26-10 | | #122 | | W/Y |
| | S | J26-8 | | #123 | | W/G |
| | 20 | J26-6 | | #124 | | W/BL |
| | T | J26-4 | | #125 | | W/V |
| | 21 | J26-2 | 1 | Bit #126 Output Even | | O |
| | U | | | | | |
| | 22 | | | | | |
| | V | | | | | |
| | 23 | | | | | |
| | W | | | | | |
| | 24 | | | | | |
| | X | | | | | |
| | 25 | | | | | |
| | Y | | | | | |

NOTES:

* #22 unless otherwise specified

LIST 27

J107

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10 | | Shield | 20 | BK |

NOTES:

LIST 28

J108

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J27-20 | 1 | Bit #127 Output Even | * | O |
| | A | J27-18 | | #128 | | Y |
| | 2 | J27-16 | | #129 | | G |
| | B | J27-14 | | #130 | | BL |
| | 3 | J27-12 | | #131 | | V |
| | C | J27-10 | | #132 | | W/O |
| | 4 | J27-8 | | #133 | | W/Y |
| | D | J27-6 | | #134 | | W/G |
| | 5 | J27-4 | | #135 | | W/BL |
| | E | J27-2 | 1 | #136 | | W/V |
| | 6 | J20-20 | 2 | #137 | | O |
| | F | J20-18 | | #138 | | Y |
| | 7 | J20-16 | | #139 | | G |
| | G | J20-14 | | #140 | | BL |
| | 8 | J20-12 | | #141 | | V |
| | H | J20-10 | | #142 | | W/O |
| | 9 | J20-8 | | #143 | | W/Y |
| | I | J20-6 | | #144 | | W/G |
| | 10 | J20-4 | | #145 | | W/BL |
| | J | J20-2 | | #146 | | W/V |
| | 11 | J21-20 | | #147 | | O |
| | K | J21-18 | | #148 | | Y |
| | 12 | J21-16 | | #149 | | G |
| | L | J21-14 | | #150 | | BL |
| | 13 | J21-12 | 2 | Bit #151 Output Even | | V |

NOTES: (*) #22 unless otherwise specified.

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LIST 29

J108

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | M | J21-10 | 2 | Bit #152 Output Even | * | W/O |
| | 14 | J21-8 | | #153 | | W/Y |
| | N | J21-6 | | #154 | | W/G |
| | 15 | J21-4 | | #155 | | W/BL |
| | O | J21-2 | 2 | #156 | | W/V |
| | 16 | J22-20 | 1 | #157 | | O |
| | P | J22-18 | | #158 | | Y |
| | 17 | J22-16 | | #159 | | G |
| | Q | J22-14 | | #160 | | BL |
| | 18 | J22-12 | | #161 | | V |
| | R | J22-10 | | #162 | | W/O |
| | 19 | J22-8 | | #163 | | W/Y |
| | S | J22-6 | | #164 | | W/G |
| | 20 | J22-4 | | #165 | | W/BL |
| | T | J22-2 | | #166 | | W/V |
| | 21 | J23-20 | 1 | Bit #167 Output Even | | O |
| | U | | | | | |
| | 22 | | | | | |
| | V | | | | | |
| | 23 | | | | | |
| | W | | | | | |
| | 24 | | | | | |
| | X | | | | | |
| | 25 | | | | | |
| | Y | | | | | |

NOTES: (*) #22 unless otherwise specified.

LIST 30

J108

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10 | | Shield | 20 | BK |

NOTES:

LIST 31.

J109

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | P40-S | 5 | Bit #168 Output Even | * | O |
| | A | P40-T | | #169 | | Y |
| | 2 | P40-U | | #170 | | G |
| | B | P40-V | | #171 | | BL |
| | 3 | P40-W | | #172 | | V |
| | C | P40-X | | #173 | | W/O |
| | 4 | P40-Y | | #174 | | W/Y |
| | D | P40-Z | | #175 | | W/G |
| | 5 | P40-a | 5 | #176 | | W/BL |
| | E | J13-20 | 4 | #177 | | W/V |
| | 6 | J13-18 | | #178 | | O |
| | F | J13-16 | | #179 | | Y |
| | 7 | J13-14 | | #180 | | G |
| | G | J13-12 | | #181 | | BL |
| | 8 | J13-10 | | #182 | | V |
| | H | J13-8 | | #183 | | W/O |
| | 9 | J13-6 | | #184 | | W/Y |
| | I | J13-4 | | #185 | | W/G |
| | 10 | J13-2 | | #186 | | W/BL |
| | J | J14-20 | | #187 | | W/V |
| | 11 | J14-18 | | #188 | | O |
| | K | J14-16 | | #189 | | Y |
| | 12 | J14-14 | | #190 | | G |
| | L | J14-12 | | #191 | | BL |
| | 13 | J14-10 | 4 | Bit #192 Output Even | | V |

NOTES: * #22 unless otherwise specified

36-404P

LIST 32

J109

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | M | J14-8 | 4 | Bit #193 Output Even | * | W/O |
| | 14 | J14-6 | | #194 | | W/Y |
| | N | J14-4 | | #195 | | W/G |
| | 15 | J14-2 | 4 | #196 | | W/BL |
| | O | J15-20 | 3 | #197 | | W/V |
| | 16 | J15-18 | | #198 | | O |
| | P | J15-16 | | #199 | | Y |
| | 17 | J15-14 | | #200 | | G |
| | Q | J15-12 | | #201 | | BL |
| | 18 | J15-10 | | #202 | | V |
| | R | J15-8 | | #203 | | W/O |
| | 19 | J15-6 | | #204 | | W/Y |
| | S | J15-4 | | #205 | | W/G |
| | 20 | J15-2 | | #206 | | W/BL |
| | T | J16-20 | | #207 | | W/V |
| | 21 | J16-18 | 3 | Bit #208 Output Even | | O |
| | U | | | | | |
| | 22 | | | | | |
| | V | | | | | |
| | 23 | | | | | |
| | W | | | | | |
| | 24 | | | | | |
| | X | | | | | |
| | 25 | | | | | |
| | Y | | | | | |

NOTES: * #22 unless otherwise specified.

LIST 33

J109

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10 | | Shield | 20 | BK |

NOTES:

LIST 34

J110

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J16-16 | 3 | Bit #209 Output Even | * | O |
| | A | J16-14 | | #210 | | Y |
| | 2 | J16-12 | | #211 | | G |
| | B | J16-10 | | #212 | | BL |
| | 3 | J16-8 | | #213 | | V |
| | C | J16-6 | | #214 | | W/O |
| | 4 | J16-4 | | #215 | | W/Y |
| | D | J16-2 | 3 | #216 | | W/G |
| | 5 | J9-20 | 4 | #217 | | W/BL |
| | E | J9-18 | | #218 | | W/V |
| | 6 | J9-16 | | #219 | | O |
| | F | J9-14 | | #220 | | Y |
| | 7 | J9-12 | | #221 | | G |
| | G | J9-10 | | #222 | | BL |
| | 8 | J9-8 | | #223 | | V |
| | H | J9-6 | | #224 | | W/O |
| | 9 | J9-4 | | #225 | | W/Y |
| | I | J9-2 | | #226 | | W/G |
| | 10 | J10-20 | | #227 | | W/BL |
| | J | J10-18 | | #228 | | W/V |
| | 11 | J10-16 | | #229 | | O |
| | K | J10-14 | 4 | Bit #230 Output Even | | Y |

NOTES: J10
ALL WIRES 22 GAUGE
UNLESS OTHERWISE NOTED

36-404P

LIST 35

J110

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 12 | J10-12 | 4 | Bit #231 Output Even | * | G |
| | L | J10-10 | | #232 | | BL |
| | 13 | J10-8 | | #233 | | V |
| | M | J10-6 | | #234 | | W/V |
| | 14 | J10-4 | | #235 | | W/Y |
| | N | J10-2 | 4 | #236 | | W/G |
| | 15 | J11-20 | 3 | #237 | | W/BL |
| | 0 | J11-18 | | #238 | | W/V |
| | 16 | J11-16 | | #239 | | 0 |
| | P | J11-14 | | #240 | | Y |
| | 17 | J11-12 | | #241 | | G |
| | Q | J11-10 | | #242 | | BL |
| | 18 | J11-8 | | #243 | | V |
| | R | J11-6 | | #244 | | W/0 |
| | 19 | J11-4 | | #245 | | W/Y |
| | S | J11-2 | | #246 | | W/G |
| | 20 | J12-20 | | #247 | | W/BL |
| | T | J12-18 | | #248 | | W/V |
| | 21 | J12-16 | | #249 | | 0 |
| | U | J12-14 | | #250 | | Y |
| | 22 | J12-12 | | #251 | | G |
| | V | J12-10 | 3 | Bit #252 Output Even | | BL |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 36

J110

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | J12-8 | 3 | Bit #253 Output Even | * | V |
| | W | J12-6 | | #254 | | W/0 |
| | 24 | J12-4 | | #255 | | W/Y |
| | X | J12-2 | 3 | Bit #256 Output Even | | W/G |
| | 25 | | | | | |
| | Y | | | | | |
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10 | | Shield | 20 | BK |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 37

J111

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J5-20 | 4 | Bit #257 Output Every | * | O |
| | A | J5-19 | | #258 | | Y |
| | 2 | J5-18 | | #259 | | G |
| | B | J5-17 | | #260 | | BL |
| | 3 | J5-16 | | #261 | | V |
| | C | J5-15 | | #262 | | W/O |
| | 4 | J5-14 | | #263 | | W/Y |
| | D | J5-13 | | #264 | | W/G |
| | 5 | J5-12 | | #265 | | W/BL |
| | E | J5-11 | | #266 | | W/V |
| | 6 | J5-10 | | #267 | | O |
| | F | J5-9 | | #268 | | Y |
| | 7 | J5-8 | | #269 | | G |
| | G | J5-7 | | #270 | | BL |
| | 8 | J5-6 | | #271 | | V |
| | H | J5-5 | | #272 | | W/O |
| | 9 | J5-4 | | #273 | | W/Y |
| | I | J5-3 | | #274 | | W/G |
| | 10 | J5-2 | | #275 | | W/BL |
| | J | J5-1 | | #276 | | W/V |
| | 11 | J6-20 | | #277 | | O |
| | K | J6-19 | | #278 | | Y |
| | 12 | J6-18 | | #279 | | G |
| | L | J6-17 | | #280 | | BL |
| | 13 | J6-16 | 4 | Bit #281 Output Every | | V |

NOTES: * #22 unless otherwise specified.

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LIST 38

J111

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | M | J6-15 | 4 | Bit #282 Output Every | * | W/O |
| | 14 | J6-14 | | Bit #283 | | W/Y |
| | N | J6-13 | | #284 | | W/G |
| | 15 | J6-12 | | #285 | | W/BL |
| | O | J6-11 | | #286 | | W/V |
| | 16 | J6-10 | | #287 | | O |
| | P | J6-9 | | #288 | | Y |
| | 17 | J6-8 | | #289 | | G |
| | Q | J6-7 | | #290 | | BL |
| | 18 | J6-6 | | #291 | | V |
| | R | J6-5 | | #292 | | W/O |
| | 19 | J6-4 | | #293 | | W/Y |
| | S | J6-3 | | #294 | | W/G |
| | 20 | J6-2 | | #295 | | W/BL |
| | T | J6-1 | 4 | #296 | | W/V |
| | 21 | J7-20 | 3 | #297 | | O |
| | U | J7-19 | 3 | Bit #298 Output Every | | Y |
| | 22 | | | | | |
| | V | | | | | |
| | 23 | | | | | |
| | W | | | | | |
| | 24 | | | | | |
| | X | | | | | |
| | 25 | | | | | |
| | Y | | | | | |

NOTES: * #22 unless otherwise spec

LIST 39

J111

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10 | | Shield | 20 | BK |

NOTES:

LIST 40

J112

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J7-18 | 3 | Bit #299 Output Every | * | O |
| | A | J7-17 | | #300 | | Y |
| | 2 | J7-16 | | #301 | | G |
| | B | J7-15 | | #302 | | BL |
| | 3 | J7-14 | | #303 | | V |
| | C | J7-13 | | #304 | | W/O |
| | 4 | J7-12 | | #305 | | W/Y |
| | D | J7-11 | | #306 | | W/G |
| | 5 | J7-10 | | #307 | | W/BL |
| | E | J7-9 | | #808 | | W/V |
| | 6 | J7-8 | | #309 | | O |
| | F | J7-7 | | #310 | | Y |
| | 7 | J7-6 | | #311 | | G |
| | G | J7-5 | | #312 | | BL |
| | 8 | J7-4 | | #313 | | V |
| | H | J7-3 | | #314 | | W/O |
| | 9 | J7-2 | | #315 | | W/Y |
| | I | J7-1 | | #316 | | W/G |
| | 10 | J8-20 | | #317 | | W/BL |
| | J | J8-19 | | #318 | | W/V |
| | 11 | J8-8 | | #329 | | O |
| | K | J8-7 | | #330 | | Y |
| | 12 | J8-6 | | #331 | | G |
| | L | J8-5 | | #332 | | BL |
| | 13 | J8-4 | 3 | Bit #333 Output Every | | V |

NOTES: * #22 unless otherwise specified.

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LIST 41

J112

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | M | J8-3 | 3 | Bit #334 Output Every | * | W/O |
| | 14 | J8-2 | 3 | #335 | | W/Y |
| | N | J8-1 | 3 | #336 | | W/G |
| | 15 | J1-20 | 4 | #337 | | W/BL |
| | O | J1-19 | | #338 | | W/V |
| | 16 | J1-17 | | #340 | | O |
| | P | J1-16 | | #341 | | Y |
| | 17 | J1-15 | | #342 | | G |
| | Q | J1-14 | | #343 | | BL |
| | 18 | J1-13 | | #344 | | V |
| | R | J1-12 | | #345 | | W/O |
| | 19 | J1-11 | | #346 | | W/Y |
| | S | J1-10 | | #347 | | W/G |
| | 20 | J1-9 | | #348 | | W/BL |
| | T | J1-8 | | #349 | | W/V |
| | 21 | J1-7 | | #350 | | O |
| | U | J1-6 | | #351 | | Y |
| | 22 | J1-5 | | #352 | | G |
| | V | J1-4 | | #353 | | BL |
| | 23 | J1-3 | | #354 | | V |
| | W | J1-2 | | #355 | | W/O |
| | 24 | J1-1 | | #356 | | W/Y |
| | X | J2-20 | | #357 | | W/G |
| | 25 | J2-19 | | #358 | | W/BL |
| | Y | J2-18 | 4 | Bit #359 Output Every | | W/V |

NOTES: * #22 unless otherwise specified.

LIST 42

J112

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10 | | Shield | 20 | BK |

NOTES:

LIST 43

J113

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J8-18 | 3 | Bit #319 Output Every | * | O |
| | A | J8-17 | | #320 | | Y |
| | 2 | J8-16 | | #321 | | G |
| | B | J8-15 | | #322 | | BL |
| | 3 | J8-14 | | #323 | | V |
| | C | J8-13 | | #324 | | W/O |
| | 4 | J8-12 | | #325 | | W/Y |
| | D | J8-11 | | #326 | | W/G |
| | 5 | J8-10 | | #327 | | W/BL |
| | E | J8-9 | 3 | Bit #328 Output Every | | W/V |
| | 6 | | | | | |
| | F | | | | | |
| | 7 | | | | | |
| | G | | | | | |
| | 8 | | | | | |
| | H | | | | | |
| | 9 | | | | | |
| | I | | | | | |
| | 10 | | | | | |
| | J | | | | | |
| | 11 | J2-17 | 4 | Bit #360 Output Every | | O |
| | K | J2-16 | | #361 | | Y |
| | 12 | J2-15 | | #362 | | G |
| | L | J2-14 | | #363 | | BL |
| | 13 | J2-13 | 4 | Bit #364 Output Every | | V |

NOTES: * #22 unless otherwise specified.

36-404P

LIST 44

J113

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | M | J2-12 | 4 | Bit #365 Output Every | * | W/O |
| | 14 | J2-11 | | #366 | | W/Y |
| | N | J2-10 | | #367 | | W/G |
| | 15 | J2-9 | | #368 | | W/BL |
| | O | J2-8 | | #369 | | W/V |
| | 16 | J2-7 | | #370 | | O |
| | P | J2-6 | | #371 | | Y |
| | 17 | J2-5 | | #372 | | G |
| | Q | J2-4 | | #373 | | BL |
| | 18 | J2-3 | | #374 | | V |
| | R | J2-2 | | #375 | | W/O |
| | 19 | J2-1 | 4 | #376 | | W/Y |
| | S | J3-20 | 3 | #377 | | W/G |
| | 20 | J3-19 | 3 | #378 | | W/BL |
| | T | J3-18 | 3 | #379 | | W/V |
| | 21 | P40-d | 5 | #159 Odd | | O |
| | U | P40-e | 5 | Bit #160 Output Odd | | Y |
| | 22 | | | | | |
| | V | | | | | |
| | 23 | | | | | |
| | W | | | | | |
| | 24 | | | | | |
| | X | | | | | |
| | 25 | | | | | |
| | Y | | | | | |

NOTES: * #22 unless otherwise specified.

LIST 45

J113

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10 | | Shield | 20 | BK |

NOTES:

LIST 46

J114

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J1-18 | 4 | Bit #339 Output Every | * | O |
| | A | J3-17 | 3 | #380 | | Y |
| | 2 | J4-15 | 3 | #402 | | G |
| | B | J4-14 | | #403 | | BL |
| | 3 | J4-13 | | #404 | | V |
| | C | J4-12 | | #405 | | W/O |
| | 4 | J4-11 | | #406 | | W/Y |
| | D | J4-10 | | #407 | | W/G |
| | 5 | J4-9 | 3 | Bit #408 Output Every | | W/BL |
| | E | | | | | |
| | 6 | | | | | |
| | F | | | | | |
| | 7 | | | | | |
| | G | | | | | |
| | 8 | | | | | |
| | H | | | | | |
| | 9 | | | | | |
| | I | | | | | |
| | 10 | | | | | |
| | J | | | | | |
| | 11 | J3-16 | 3 | Bit #381 Output Every | | W/V |
| | K | J3-15 | | #382 | | O |
| | 12 | J3-14 | | #383 | | Y |
| | L | J3-13 | | #384 | | G |
| | 13 | J3-12 | 3 | Bit #385 Output Every | | BL |

NOTES: * #22 unless otherwise specified.

36-404P

LIST 47

J114

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | M | J3-11 | 3 | Bit #386 Output Every | * | V |
| | 14 | J3-10 | | #387 | | W/O |
| | N | J3-9 | | #388 | | W/Y |
| | 15 | J3-8 | | #389 | | W/G |
| | O | J3-7 | | #390 | | W/BL |
| | 16 | J3-6 | | #391 | | W/V |
| | P | J3-5 | | #392 | | O |
| | 17 | J3-4 | | #393 | | Y |
| | Q | J3-3 | | #394 | | G |
| | 18 | J3-2 | | #395 | | BL |
| | R | J3-1 | | #396 | | V |
| | 19 | J4-20 | | #397 | | W/O |
| | S | J4-19 | | #398 | | W/Y |
| | 20 | J4-18 | | #399 | | W/G |
| | T | J4-17 | | #400 | | W/BL |
| | 21 | J4-16 | 3 | Bit #401 Output Every | | W/V |
| | U | | | | | |
| | 22 | | | | | |
| | V | | | | | |
| | 23 | | | | | |
| | W | | | | | |
| | 24 | | | | | |
| | X | | | | | |
| | 25 | | | | | |
| | Y | | | | | |

NOTES: * #22 unless otherwise specified.

LIST 48

J114

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | +4.5 | See Note | | Shield | 20 | BK |
| | -4.5 | Page 10 | | Shield | 20 | BK |

NOTES:

LIST 49

J 1

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J112-24 | 4 | Output F/F #1 Bit 356 Every | * | W/Y |
| | 2 | J112-W | | Output F/F #2 355 | | W/O |
| | 3 | J112-23 | | Output F/F #3 354 | | V |
| | 4 | J112-V | | Output F/F #4 353 | | BL |
| | 5 | J112-22 | | Output F/F #5 352 | | G |
| | 6 | J112-U | | Output F/F #6 351 | | Y |
| | 7 | J112-21 | | Output F/F #7 350 | | O |
| | 8 | J112-T | | Output F/F #8 349 | | W/V |
| | 9 | J112-20 | | Output F/F #9 348 | | W/BL |
| | 10 | J112-S | | Output F/F #10 347 | | W/G |
| | 11 | J112-19 | | Output F/F #11 346 | | W/Y |
| | 12 | J112-R | | Output F/F #12 345 | | W/O |
| | 13 | J112-18 | | Output F/F #13 344 | | V |
| | 14 | J112-Q | | Output F/F #14 343 | | BL |
| | 15 | J112-17 | | Output F/F #15 342 | | G |
| | 16 | J112-P | | Output F/F #16 341 | | Y |
| | 17 | J112-16 | | Output F/F #17 340 | | O |
| | 18 | J114-1 | | Output F/F #18 339 | | O |
| | 19 | J112-O | | Output F/F #19 338 | | W/V |
| | 20 | J112-15 | 4 | Output F/F #20 Bit 337 Every | | W/BL |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES:

All wires 22 Gauge
unless otherwise noted

LIST 50

J 1

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | * | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J2-34 | | Core Shift | | V |
| | 35 | | | | | |
| | 36 | J2-36 | | F/F Reset Trigger | | Y |
| | 37 | | | | | |
| | 38 | J2-38 | | Read Gate | | W/Y |
| | 39 | | | | | |
| | 40 | J8-41 | | Core Output | | G |
| | 41 | J2-40 | | Core Input= | | W/G |
| | 42 | -17V(C)-3 | 4 | -17V | 20 | W/S |
| | 43 | -17V(C)-3 | 4 | -17V | 20 | W/S |
| | 44 | +12V-23 | 4 | +12V | 20 | R |
| | 45 | OV(C)-3 | 4 | OV | 20 | BK |
| | 46 | OV(C)-3 | 4 | OV | 20 | BK |
| | 47 | -20V(C)-3 | 4 | -20V | 20 | S |
| | 48 | -20V(C)-3 | 4 | -20V | 20 | S |
| | 49 | -85V-23 | 4 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES:

All Wires 22 Gauge
unless otherwise noted

LIST 51

J 2

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J113-19 | 4 | Output F/F #1 Bit 376 Every | * | W/Y |
| | 2 | J113-R | | Output F/F #2 375 | | W/O |
| | 3 | J113-18 | | Output F/F #3 374 | | V |
| | 4 | J113-Q | | Output F/F #4 373 | | BL |
| | 5 | J113-17 | | Output F/F #5 372 | | G |
| | 6 | J113-P | | Output F/F #6 371 | | Y |
| | 7 | J113-16 | | Output F/F #7 370 | | O |
| | 8 | J113-O | | Output F/F #8 369 | | W/V |
| | 9 | J113-15 | | Output F/F #9 368 | | W/BL |
| | 10 | J113-N | | Output F/F #10 367 | | W/G |
| | 11 | J113-14 | | Output F/F #11 366 | | W/Y |
| | 12 | J113-M | | Output F/F #12 365 | | W/O |
| | 13 | J113-13 | | Output F/F #13 364 | | V |
| | 14 | J113-L | | Output F/F #14 363 | | BL |
| | 15 | J113-12 | | Output F/F #15 362 | | G |
| | 16 | J113-K | | Output F/F #16 361 | | Y |
| | 17 | J113-11 | | Output F/F #17 360 | | O |
| | 18 | J112-Y | | Output F/F #18 359 | | W/V |
| | 19 | J112-25 | | Output F/F #19 358 | | W/BL |
| | 20 | J112-X | 4 | Output F/F #20 Bit 357 Every | | W/G |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES:

All wires 22 Gauge
unless otherwise noted

LIST 52

J 2

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | * | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J1-34 | | Core Shift | | V |
| | 34 | J3-34 | | Core Shift | | V |
| | 35 | | | | | |
| | 36 | J1-36 | | F/F Reset Trigger | | Y |
| | 36 | J3-36 | | | | Y |
| | 37 | | | | | |
| | 38 | J1-38 | | Read Gate | | W/Y |
| | 38 | J3-38 | | | | W/Y |
| | 39 | | | | | |
| | 40 | J1-41* | | Core Output | 22 | W/G |
| | 41 | J3-40 | | Core Input | 22 | G |
| | 42 | -17V(C)-4 | 4 | -17V | 20 | W/S |
| | 43 | -17V(C)-4 | 4 | -17V | 20 | W/S |
| | 44 | +12V(C)-24 | 4 | +12V | 20 | R |
| | 45 | OV(C)-4 | 4 | OV | 20 | BK |
| | 46 | OV(C)-4 | 4 | OV | 20 | BK |
| | 47 | -20V(C)-4 | 4 | -20V | 20 | S |
| | 48 | -20V(C)-4 | 4 | -20V | 20 | S |
| | 49 | -85V-24 | 4 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES:

All wires 22 Gauge
unless otherwise noted

LIST 53

J 3

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J114-R | 3 | Output F/F #1 Bit 396 Every | | V |
| | 2 | J114-18 | | Output F/F #2 395 | | BL |
| | 3 | J114-Q | | Output F/F #3 394 | | G |
| | 4 | J114-17 | | Output F/F #4 393 | | Y |
| | 5 | J114-P | | Output F/F #5 392 | | O |
| | 6 | J114-16 | | Output F/F #6 391 | | W/V |
| | 7 | J114-O | | Output F/F #7 390 | | W/BL |
| | 8 | J114-15 | | Output F/F #8 389 | | W/G |
| | 9 | J114-N | | Output F/F #9 388 | | W/Y |
| | 10 | J114-14 | | Output F/F #10 387 | | W/O |
| | 11 | J114-M | | Output F/F #11 386 | | V |
| | 12 | J114-13 | | Output F/F #12 385 | | BL |
| | 13 | J114-L | | Output F/F #13 384 | | G |
| | 14 | J114-12 | | Output F/F #14 383 | | Y |
| | 15 | J114-K | | Output F/F #15 382 | | O |
| | 16 | J114-11 | | Output F/F #16 381 | | W/V |
| | 17 | J114-A | | Output F/F #17 380 | | Y |
| | 18 | J113-T | | Output F/F #18 379 | | W/V |
| | 19 | J113-20 | | Output F/F #19 378 | | W/BL |
| | 20 | J113-S | 3 | Output F/F #20 Bit 377 Every | | W/G |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES:
All wires 22 Gauge
unless otherwise noted

LIST 54

J 3

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | * | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J2-34 | | Core Shift | | Y |
| | 34 | J4-34 | | Core Shift | | V |
| | 35 | | | | | |
| | 36 | J2-36 | | F/F Reset Trigger | | Y |
| | 36 | J4-36 | | F/F Reset Trigger | | Y |
| | 37 | | | | | |
| | 38 | J2-38 | | Read Gate | | W/Y |
| | 38 | J4-38 | | Read Gate | | W/Y |
| | 39 | | | | | |
| | 40 | J2-41 | | Core Output | 22 | G |
| | 41 | J4-40 | | Core Input | 22 | W/G |
| | 42 | -17V(C)-5 | 3 | -17V | 20 | W/S |
| | 43 | -17V(C)-5 | 3 | -17V | 20 | W/S |
| | 44 | +12V-25 | 3 | +12V | 20 | R |
| | 45 | OV(C)-5 | 3 | OV | 20 | BK |
| | 46 | OV(C)-5 | 3 | OV | 20 | BK |
| | 47 | -20V(C)-5 | 3 | -20V | 20 | S |
| | 48 | -20V(C)-5 | 3 | -20V | 20 | S |

NOTES:
All wires 22 Gauge
unless otherwise noted

LIST 55

J 3

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 49 | -85-25 | 3 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 20 | BK |

NOTES:
All wires 22 Gauge
unless otherwise noted

LIST 56

J 4

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | Output F/F #1 | * | |
| | 2 | | | Output F/F #2 | | |
| | 3 | | | Output F/F #3 | | |
| | 4 | | | Output F/F #4 | | |
| | 5 | | | Output F/F #5 | | |
| | 6 | | | Output F/F #6 | | |
| | 7 | | | Output F/F #7 | | |
| | 8 | | | Output F/F #8 | | |
| | 9 | J114-5 | 3 | Output F/F #9 Bit 408 Every | | W/BL |
| | 10 | J114-D | | Output F/F #10 407 | | W/G |
| | 11 | J114-4 | | Output F/F #11 406 | | W/Y |
| | 12 | J114-C | | Output F/F #12 405 | | W/O |
| | 13 | J114-3 | | Output F/F #13 404 | | V |
| | 14 | J114-B | | Output F/F #14 403 | | BL |
| | 15 | J114-2 | | Output F/F #15 402 | | G |
| | 16 | J114-21 | | Output F/F #16 401 | | W/V |
| | 17 | J114-T | | Output F/F #17 400 | | W/BL |
| | 18 | J114-20 | | Output F/F #18 399 | | W/G |
| | 19 | J114-S | | Output F/F #19 398 | | W/Y |
| | 20 | J114-19 | 3 | Output F/F #20 Bit 397 Every | | W/O |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES:
All Wires 22 Gauge
unless otherwise noted

LIST 57

J 4

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | * | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J3-34 | | Core Shift | | V |
| | 34 | J8-34 | | Core Shift | | V |
| | 35 | | | | | |
| | 36 | J3-36 | | F/F Reset Trigger | | Y |
| | 36 | J8-36 | | F/F Reset Trigger | | Y |
| | 37 | | | | | |
| | 38 | J3-38 | | Read Gate | | W/Y |
| | 38 | J8-38 | | Read Gate | | W/Y |
| | 39 | | | | | |
| | 40 | J3-41 | | Core Output | 22 | W/G |
| | 41 | P40-q | | Core Input | 22 | BL |
| | 42 | -17V(C)-6 | 3 | -17V | 20 | W/S |
| | 43 | -17V(C)-6 | 3 | -17V | 20 | W/S |
| | 44 | +12V-26 | 3 | +12V | 20 | R |
| | 45 | OV(C)-6 | 3 | OV | 20 | BK |
| | 46 | OV(C)-6 | 3 | OV | 20 | BK |
| | 47 | -20V(C)-6 | 3 | -20V | 20 | S |
| | 48 | -20V(C)-6 | 3 | -20V | 20 | S |

NOTES:
All wires 22 Gauge
unless otherwise noted

LIST 58

J 4

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 49 | -85V-26 | 3 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES:
All wires 22 Gauge
unless otherwise noted

LIST 59

J 5

20 BIT S.R. (76-7A

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J111-J | 4 | Output F/F #1 Bit 276 Every * | | W/V |
| | 2 | J111-10 | | Output F/F #2 275 | | W/BL |
| | 3 | J111-I | | Output F/F #3 274 | | W/G |
| | 4 | J111-9 | | Output F/F #4 273 | | W/Y |
| | 5 | J111-H | | Output F/F #5 272 | | W/O |
| | 6 | J111-8 | | Output F/F #6 271 | | V |
| | 7 | J111-G | | Output F/F #7 270 | | BL |
| | 8 | J111-7 | | Output F/F #8 269 | | G |
| | 9 | J111-F | | Output F/F #9 268 | | Y |
| | 10 | J111-6 | | Output F/F #10 267 | | O |
| | 11 | J111-E | | Output F/F #11 266 | | W/V |
| | 12 | J111-5 | | Output F/F #12 265 | | W/BL |
| | 13 | J111-D | | Output F/F #13 264 | | W/G |
| | 14 | J111-4 | | Output F/F #14 263 | | W/Y |
| | 15 | J111-C | | Output F/F #15 262 | | W/O |
| | 16 | J111-3 | | Output F/F #16 261 | | V |
| | 17 | J111-B | | Output F/F #17 260 | | BL |
| | 18 | J111-2 | | Output F/F #18 259 | | G |
| | 19 | J111-A | | Output F/F #19 258 | | Y |
| | 20 | J111-1 | 4 | Output F/F #20 Bit 257 Every | | O |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES:
All wires 22 Gauge
unless otherwise noted

LIST 60

J 5

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J6-34 | | Core Shift | | V |
| | 34 | J9-34 | | Core Shift | | V |
| | 35 | | | | | |
| | 36 | J6-36 | | F/F Reset Trigger | | Y |
| | 36 | P40-g | 3 | F/F Reset Trigger | | Y |
| | 37 | | | | | |
| | 38 | J6-38 | | Read Gate | | W/Y |
| | 38 | P40-h | 3 | Read Gate | | W/Y |
| | 39 | | | | | |
| | 40 | J12-41 | | Core Output | 22 | G |
| | 41 | J6-40 | | Core Input | 22 | W/G |
| | 42 | -17V(C)-7 | 4 | -17V | 20 | W/S |
| | 43 | -17V(C)-7 | 4 | -17V | 20 | W/S |
| | 44 | +12V-27 | 4 | +12V | 20 | R |
| | 45 | OV(C)-7 | 4 | OV | 20 | BK |
| | 46 | OV(C)-7 | 4 | OV | 20 | BK |
| | 47 | -20V(C)-7 | 4 | -20V | 20 | S |
| | 48 | -20V(C)-7 | 4 | -20V | 20 | S |

NOTES:
All wires 22 Gauge
unless otherwise noted

LIST 61

J 5

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 49 | -85V-27 | 4 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 20 | BK |

NOTES:

All wires 22 Gauge
unless otherwise noted

LIST 62

J 6

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J111-T | 4 | Output F/F #1 Bit 296 Every * | | W/V |
| | 2 | J111-20 | | Output F/F #2 295 | | W/BL |
| | 3 | J111-S | | Output F/F #3 294 | | W/G |
| | 4 | J111-19 | | Output F/F #4 293 | | W/Y |
| | 5 | J111-R | | Output F/F #5 292 | | W/O |
| | 6 | J111-18 | | Output F/F #6 291 | | V |
| | 7 | J111-Q | | Output F/F #7 290 | | BL |
| | 8 | J111-17 | | Output F/F #8 289 | | G |
| | 9 | J111-P | | Output F/F #9 288 | | Y |
| | 10 | J111-16 | | Output F/F #10 287 | | O |
| | 11 | J111-O | | Output F/F #11 286 | | W/V |
| | 12 | J111-15 | | Output F/F #12 285 | | W/BL |
| | 13 | J111-N | | Output F/F #13 284 | | W/G |
| | 14 | J111-14 | | Output F/F #14 283 | | W/Y |
| | 15 | J111-M | | Output F/F #15 282 | | W/O |
| | 16 | J111-13 | | Output F/F #16 281 | | V |
| | 17 | J111-L | | Output F/F #17 280 | | BL |
| | 18 | J111-12 | | Output F/F #18 279 | | G |
| | 19 | J111-K | | Output F/F #19 278 | | Y |
| | 20 | J111-11 | 4 | Output F/F #20 Bit 277 Every | | O |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES:

All wires 22 Gauge
unless otherwise noted

LIST 63

J 6

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J5-34 | | Core Shift | | V |
| | 34 | J7-34 | | Core Shift | | V |
| | 35 | | | | | |
| | 36 | J5-36 | | F/F Reset Trigger | | Y |
| | 36 | J7-36 | | F/F Reset Trigger | | Y |
| | 37 | | | | | |
| | 38 | J5-38 | | Read Gate | | W/Y |
| | 38 | J7-38 | | Read Gate | | W/Y |
| | 39 | | | | | |
| | 40 | J5-41 | | Core Output | 22 | W/G |
| | 41 | J7-40 | | Core Input | 22 | G |
| | 42 | -17V(C)-8 | 4 | -17V | 20 | W/S |
| | 43 | -17V(C)-8 | 4 | -17 V | 20 | W/S |
| | 44 | +12V-28 | 4 | +12V | 20 | R |
| | 45 | 0V(C)-8 | 4 | 0V | 20 | BK |
| | 46 | 0V(C)-8 | 4 | 0V | 20 | BK |
| | 47 | -20V(C)-8 | 4 | -20V | 20 | S |
| | 48 | -20V(C)-8 | 4 | -20V | 20 | S |

NOTES:

* All wires 22 Gauge unless otherwise noted

LIST 64

J 6

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 49 | -85-28 | 4 | -85V | 20 | W/BK |
| | 50 | Rack | 4 | Chassis Gnd | 22 | BK |

NOTES:

All wires 22 Gauge unless otherwise noted

LIST 65

J 7

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J112-I | 3 | Output F/F #1 Bit 316 Every * | | W/G |
| | 2 | J112-9 | | Output F/F #2 315 | | W/Y |
| | 3 | J112-H | | Output F/F #3 314 | | W/O |
| | 4 | J112-8 | | Output F/F #4 313 | | V |
| | 5 | J112-G | | Output F/F #5 312 | | BL |
| | 6 | J112-7 | | Output F/F #6 311 | | G |
| | 7 | J112-F | | Output F/F #7 310 | | Y |
| | 8 | J112-6 | | Output F/F #8 309 | | O |
| | 9 | J112-E | | Output F/F #9 308 | | W/V |
| | 10 | J112-5 | | Output F/F #10 307 | | W/BL |
| | 11 | J112-D | | Output F/F #11 306 | | W/G |
| | 12 | J112-4 | | Output F/F #12 305 | | W/Y |
| | 13 | J112-C | | Output F/F #13 304 | | W/O |
| | 14 | J112-3 | | Output F/F #14 303 | | V |
| | 15 | J112-B | | Output F/F #15 302 | | BL |
| | 16 | J112-2 | | Output F/F #16 301 | | G |
| | 17 | J112-A | | Output F/F #17 300 | | Y |
| | 18 | J112-1 | | Output F/F #18 299 | | O |
| | 19 | J111-U | | Output F/F #19 298 | | Y |
| | 20 | J111-21 | 3 | Output F/F #20 Bit 297 Every | | O |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES:

All Wires 22 Gauge
unless otherwise noted

LIST 66

J 7

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J6-34 | | Core Shift | | V |
| | 34 | J8-34 | | Core Shift | | V |
| | 35 | | | | | |
| | 36 | J6-36 | | F/F Reset Trigger | | Y |
| | 36 | J8-36 | | F/F Reset Trigger | | Y |
| | 37 | | | | | |
| | 38 | J6-38 | | Read Gate | | W/Y |
| | 38 | J8-38 | | Read Gate | | W/Y |
| | 39 | | | | | |
| | 40 | J6-41 | | Core Output | 22 | G |
| | 41 | J8-40 | | Core Input | 22 | W/G |
| | 42 | -17V(C)-9 | 3 | -17V | 20 | W/S |
| | 43 | -17V(C)-9 | 3 | -17V | 20 | W/S |
| | 44 | +12V-29 | 3 | +12V | 20 | R |
| | 45 | OV(C)-9 | 3 | OV | 20 | BK |
| | 46 | OV(C)-9 | 3 | OV | 20 | BK |
| | 47 | -20V(C)-9 | 3 | -20V | 20 | S |
| | 48 | -20V(C)-9 | 3 | -20V | 20 | S |

NOTES:

All wires 22 Gauge
unless otherwise noted

LIST 67

J 7

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 49 | -85V-29 | 3 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES:
All wires 22 Gauge
unless otherwise noted

LIST 68

J 8

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J112-N | 3 | Output F/F #1 Bit 336 every * | | W/G |
| | 2 | J112-14 | | Output F/F #2 335 | | W/Y |
| | 3 | J112-M | | Output F/F #3 334 | | W/O |
| | 4 | J112-13 | | Output F/F #4 333 | | V |
| | 5 | J112-L | | Output F/F #5 332 | | BL |
| | 6 | J112-12 | | Output F/F #6 331 | | G |
| | 7 | J112-K | | Output F/F #7 330 | | Y |
| | 8 | J112-11 | | Output F/F #8 329 | | O |
| | 9 | J113-E | | Output F/F #9 328 | | W/V |
| | 10 | J113-5 | | Output F/F #10 327 | | W/BL |
| | 11 | J113-D | | Output F/F #11 326 | | W/G |
| | 12 | J113-4 | | Output F/F #12 325 | | W/Y |
| | 13 | J113-C | | Output F/F #13 324 | | W/O |
| | 14 | J113-3 | | Output F/F #14 323 | | V |
| | 15 | J113-B | | Output F/F #15 322 | | BL |
| | 16 | J113-2 | | Output F/F #16 321 | | G |
| | 17 | J113-A | | Output F/F #17 320 | | Y |
| | 18 | J113-1 | | Output F/F #18 319 | | O |
| | 19 | J112-J | | Output F/F #19 318 | | W/V |
| | 20 | J112-10 | 3 | Output F/F #20 Bit 317 every | | W/BL |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES:
ALL WIRES 22 GAUGE
UNLESS OTHERWISE NOTED.

LIST 69

J 8

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J4-34 | | Core Shift | | V |
| | 34 | J7-34 | | Core Shift | | V |
| | 35 | | | | | |
| | 36 | J4-36 | | F/F Reset Trigger | | Y |
| | 36 | J7-36 | | F/F Reset Trigger | | Y |
| | 37 | | | | | |
| | 38 | J4-38 | | Read Gate | | W/Y |
| | 38 | J7-38 | | Read Gate | | W/Y |
| | 39 | | | | | |
| | 40 | J7-41 | | Core Output | 22 | W/G |
| | 41 | J1-40 | | Core Input | 22 | G |
| | 42 | -17V(C)-10 | 3 | -17V | 20 | W/S |
| | 43 | -17V(C)-10 | 3 | -17V | 20 | W/S |
| | 44 | +12v-30 | 3 | +12V | 20 | R |
| | 45 | OV(C)-10 | 3 | OV | 20 | BK |
| | 46 | OV(C)-10 | 3 | OV | 20 | BK |
| | 47 | -20V(C)-10 | 3 | -20V | 20 | S |
| | 48 | -20V(C)-10 | 3 | -20V | 20 | S |

NOTES:
All wires 22 Gauge
unless otherwise noted

LIST 70

J 8

20 BIT S.R. (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 49 | -85V-30 | 3 | -85V | 20 | W/BK |
| | 50 | Rack | 3 | Chassis Gnd | 22 | BK |

NOTES:
All wires 22 Gauge
unless otherwise noted

LIST 71

J9
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J106-J | 4 | Output F/F #1 Odd Bit 226 | * | W/V |
| | 2 | J110-I | | Even | | W/G |
| | 3 | J106-10 | | Output F/F #2 Odd Bit 225 | | W/BL |
| | 4 | J110-9 | | Even | | W/Y |
| | 5 | J106-I | | Output F/F #3 Odd Bit 224 | | W/G |
| | 6 | J110-H | | Even | | W/O |
| | 7 | J106-9 | | Output F/F #4 Odd Bit 223 | | W/V |
| | 8 | J110-8 | | Even | | V |
| | 9 | J106-H | | Output F/F #5 Odd Bit 222 | | W/O |
| | 10 | J110-G | | Even | | BL |
| | 11 | J106-8 | | Output F/F #6 Odd Bit 221 | | V |
| | 12 | J110-7 | | Even | | G |
| | 13 | J106-G | | Output F/F #7 Odd Bit 220 | | BL |
| | 14 | J110-F | | Even | | Y |
| | 15 | J106-7 | | Output F/F #8 Odd Bit 219 | | G |
| | 16 | J110-6 | | Even | | O |
| | 17 | J106-F | | Output F/F #9 Odd Bit 218 | | Y |
| | 18 | J110-E | | Even | | W/V |
| | 19 | J106-6 | | Output F/F #10 Odd Bit 217 | | O |
| | 20 | J110-5 | 4 | Even | | W/BL |
| | 21 | | | | | |
| | 22 | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 72

J9
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | | | | * | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J5-34 | | Core Shift | | V |
| | 34 | J10-34 | | | | V |
| | 35 | J10-35 | | Odd Reset | | O |
| | 35 | J13-35 | | | | O |
| | 36 | J10-36 | | Even Reset | | G |
| | 36 | J13-36 | | | | G |
| | 37 | J10-37 | | Odd F/F Gate | | W/O |
| | 37 | J13-37 | | | | W/O |
| | 38 | J10-38 | | Even F/F Gate | | W/G |
| | 38 | J13-38 | | | | W/G |
| | 39 | | | | | |
| | 39 | | | | | |
| | 40 | J16-41 | | Core Output | 22 | G |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 73

J9
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 41 | J10-40 | | Core Input | 22 | W/G |
| | 42 | -17V(C)-11 | 4 | -17V | 20 | W/S |
| | 43 | -17V(C)-11 | 4 | -17V | 20 | W/S |
| | 44 | +12V-31 | 4 | +12V | 20 | R |
| | 45 | OV(C)-11 | 4 | OV | 20 | BK |
| | 46 | OV(C)-11 | 4 | OV | 20 | BK |
| | 47 | -20V(C)-11 | 4 | -20V | 20 | S |
| | 48 | -20V(C)-11 | 4 | -20V | 20 | S |
| | 49 | -85V-31 | 4 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 74

J 10
10 BIT S.R. (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J106-O | 4 | Output F/F #1 Odd Bit 236 | * | W/V |
| | 2 | J110-N | | Even | | W/G |
| | 3 | J106-15 | | Output F/F #2 Odd Bit 235 | | W/BL |
| | 4 | J110-14 | | Even | | V/Y |
| | 5 | J106-N | | Output F/F #3 Odd Bit 234 | | W/G |
| | 6 | J110-M | | Even | | W/V |
| | 7 | J106-14 | | Output F/F #4 Odd Bit 233 | | W/Y |
| | 8 | J110-13 | | Even | | V |
| | 9 | J106-M | | Output F/F #5 Odd Bit 232 | | W/O |
| | 10 | J110-L | | Even | | BI |
| | 11 | J106-13 | | Output F/F #6 Odd Bit 231 | | V |
| | 12 | J110-12 | | Even | | G |
| | 13 | J106-L | | Output F/F #7 Odd Bit 230 | | BL |
| | 14 | J110-K | | Even | | Y |
| | 15 | J106-12 | | Output F/F #8 Odd Bit 229 | | G |
| | 16 | J110-11 | | Even | | O |
| | 17 | J106-K | | Output F/F #9 Odd Bit 228 | | Y |
| | 18 | J110-J | | Even | | W/V |
| | 19 | J106-11 | | Output F/F #10 Odd Bit 227 | | O |
| | 20 | J110-10 | 4 | Even | | W/BL |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES:
ALL WIRES 22 GAUGE
UNLESS OTHERWISE NOTED.

LIST 75

J10
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | * | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J9-34 | | Core Shift | | V |
| | 34 | J11-34 | | Core Shift | | V |
| | 35 | J9-35 | | Odd Reset | | O |
| | 35 | J11-35 | | Odd Reset | | O |
| | 36 | J9-36 | | Even Reset | | G |
| | 36 | J11-36 | | Even Reset | | G |
| | 37 | J9-37 | | Odd F/F Gate | | W/O |
| | 37 | J11-37 | | Odd F/F Gate | | W/O |
| | 38 | J9-38 | | Even F/F Gate | | "/G |
| | 38 | J11-38 | | Even F/F gate | | W/G |
| | 39 | | | | | |
| | 40 | J9-41 | | Core Output | | W/G |
| | 41 | J11-40 | | Core Input | | G |
| | 42 | -17V(C)-12 | 4 | -17V | 20 | W/S |
| | 43 | -17V(C)-12 | | -17V | | W/S |
| | 44 | +12V-32 | | +12V | | R |
| | 45 | 0V(C)-12 | 4 | 0V | 20 | BK |

NOTES: All wires 22 Gauge unless otherwise specified

LIST 76

J10
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 46 | 0V(C)-12 | 4 | 0V | 20 | BK |
| | 47 | -20V(C)-12 | | -20V | 20 | S |
| | 48 | -20V(C)-12 | | -20V | 20 | S |
| | 49 | -85V-32 | 4 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Ground | 22 | BK |

NOTES:

LIST 77

J 11

10 BIT S.R. (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J106-T | 3 | Output F/F #1 Odd Bit 246 | * | W/V |
| | 2 | J110-S | | Even | | W/G |
| | 3 | J106-20 | | Output F/F #2 Odd Bit 245 | | W/BL |
| | 4 | J110-19 | | Even | | W/Y |
| | 5 | J106-S | | Output F/F #3 Odd Bit 244 | | W/G |
| | 6 | J110-R | | Even | | W/O |
| | 7 | J106-19 | | Output F/F #4 Odd Bit 243 | | W/Y |
| | 8 | J110-18 | | Even | | V |
| | 9 | J106-R | | Output F/F #5 Odd Bit 242 | | W/O |
| | 10 | J110-Q | | Even | | BL |
| | 11 | J106-18 | | Output F/F #6 Odd Bit 241 | | V |
| | 12 | J110-17 | | Even | | G |
| | 13 | J106-Q | | Output F/F #7 Odd Bit 240 | | BL |
| | 14 | J110-P | | Even | | Y |
| | 15 | J106-17 | | Output F/F #8 Odd Bit 239 | | G |
| | 16 | J110-16 | | Even | | O |
| | 17 | J106-P | | Output F/F #9 Odd Bit 238 | | Y |
| | 18 | J110-O | | Even | | W/V |
| | 19 | J106-16 | | Output F/F #10 Odd Bit 237 | | O |
| | 20 | J110-15 | 3 | Even | | W/BL |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED.

LIST 78

J11

10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J10-34 | | Core Shift | | V |
| | 34 | J12-34 | | Core Shift | | V |
| | 35 | J10-35 | | Odd Reset | | O |
| | 35 | J12-35 | | Odd Reset | | O |
| | 36 | J10-36 | | Even Reset | | G |
| | 36 | J12-36 | | Even Reset | | G |
| | 37 | J10-37 | | Odd F/F Gate | | W/O |
| | 37 | J12-37 | | Odd F/F Gate | | W/O |
| | 38 | J10-38 | | Even F/F Gate | | W/G |
| | 38 | J12-38 | | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 40 | J10-41 | | Core Output | | G |
| | 41 | J12-40 | | Core Input | | W/G |
| | 42 | -17V(D)-3 | | -17V | 20 | W/S |
| | 43 | -17V(D)-3 | | -17V | | W/S |
| | 44 | +12V-33 | | +12V | | R |
| | 45 | 0V(D)-3 | | 0V | 20 | BK |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE SPECIFIED

LIST 79

J11

10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 46 | 0V(D)-3 | | 0V | 20 | BK |
| | 47 | -20V(D)-3 | | -20V | | S |
| | 48 | -20V(D)-3 | | -20V | | S |
| | 49 | -85V-33 | | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES:

LIST 80

J 12

10 BIT S.R. (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J106-Y | 3 | Output F/F #1 Odd Bit 256 | * | W/V |
| | 2 | J110-X | | " Even " | | W/G |
| | 3 | J106-25 | | Output F/F #2 Odd Bit 255 | | W/BL |
| | 4 | J110-24 | | " Even " | | W/Y |
| | 5 | J106-X | | Output F/F #3 Odd Bit 254 | | W/G |
| | 6 | J110-W | | " Even " | | W/O |
| | 7 | J106-24 | | Output F/F #4 Odd Bit 253 | | W/Y |
| | 8 | J110-23 | | " Even " | | V |
| | 9 | J106-W | | Output F/F #5 Odd Bit 252 | | W/O |
| | 10 | J110-V | | " Even " | | BL |
| | 11 | J106-23 | | Output F/F #6 Odd Bit 251 | | V |
| | 12 | J110-22 | | " Even " | | G |
| | 13 | J106-V | | Output F/F #7 Odd Bit 250 | | BL |
| | 14 | J110-U | | " Even " | | Y |
| | 15 | J106-22 | | Output F/F #8 Odd Bit 249 | | G |
| | 16 | J110-21 | | " Even " | | O |
| | 17 | J106-U | | Output F/F #9 Odd Bit 248 | | Y |
| | 18 | J110-T | | " Even " | | W/V |
| | 19 | J106-21 | | Output F/F #10 Odd Bit 247 | | O |
| | 20 | J110-20 | 3 | " Even " | | W/BL |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED.

LIST 81

J12

10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J11-34 | | Core Shift | | V |
| | 34 | J16-34 | | Core Shift | | V |
| | 35 | J11-35 | | Odd Reset | | O |
| | 36 | J11-36 | | Even Reset | | G |
| | 37 | J11-37 | | Odd F/F Gate | | W/O |
| | 38 | J11-38 | | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 40 | J11-41 | | Core Output | | W/G |
| | 41 | J5-40 | | Core Input | | G |
| | 42 | -17(D)-4 | | -17V | 20 | W/S |
| | 43 | -17V(D)-4 | | -17V | | W/S |
| | 44 | +12-34 | | +12V | | R |
| | 45 | 0V(D)-4 | | 0V | | BK |
| | 46 | 0V(D)-4 | | 0V | | BK |
| | 47 | -20V(D)-4 | | -20V | | S |
| | 48 | -20V(D)-4 | | -20V | | S |
| | 49 | -85V-34 | | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Ground | 22 | BK |

NOTES: ALL WIRES 22 UNLESS OTHERWISE SPECIFIED.

LIST 82

J13

10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J105-N | 4 | Output F/F #1 Odd Bit 186 | * | W/G |
| | 2 | J109-10 | | Even | | W/BL |
| | 3 | J105-14 | | Output F/F #2 Odd Bit 185 | | W/Y |
| | 4 | J109-I | | Even | | W/G |
| | 5 | J105-M | | Output F/F #3 Odd Bit 184 | | W/O |
| | 6 | J109-9 | | Even | | W/Y |
| | 7 | J105-13 | | Output F/F #4 Odd Bit 183 | | V |
| | 8 | J109-H | | Even | | W/O |
| | 9 | J105-12 | | Output F/F #5 Odd Bit 182 | | BL |
| | 10 | J109-8 | | Even | | V |
| | 11 | J105-J | | Output F/F #6 Odd Bit 181 | | G |
| | 12 | J109-G | | Even | | BL |
| | 13 | J105-K | | Output F/F #7 Odd Bit 180 | | Y |
| | 14 | J109-7 | | Even | | G |
| | 15 | J105-11 | | Output F/F #8 Odd Bit 179 | | O |
| | 16 | J109-F | | Even | | Y |
| | 17 | J105-I | | Output F/F #9 Odd Bit 178 | | W/V |
| | 18 | J109-6 | | Even | | O |
| | 19 | J105-10 | | Output F/F #10 Odd Bit 177 | | W/BL |
| | 20 | J109-E | 4 | Even | | W/V |
| | 21 | | | | | |
| | 22 | | | | | |

NOTES: All wires 22 gauge unless otherwise specified.

LIST 83

J13
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | P40-s | | Core Shift | | V |
| | 34 | J14-34 | | Core Shift | | V |
| | 35 | J9-35 | | Odd Reset | | O |
| | 35 | J14-35 | | Odd Reset | | O |
| | 36 | J9-36 | | Even Reset | | G |
| | 36 | J14-36 | | Even Reset | | G |
| | 37 | J9-36 | | Odd F/F Gate | | W/O |
| | 37 | J14-36 | | Odd F/F Gate | | W/O |
| | 38 | J9-36 | | Even F/F Gate | | W/G |
| | 38 | J14-36 | | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 39 | | | | | |
| | 40 | P40-r | | Core Output | | G |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 84

J13
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 41 | J14-40 | | Core Input | | W/G |
| | 42 | -17V(D)-5 | | -17V | 20 | W/S |
| | 43 | -17V(D)-5 | | -17V | 20 | W/S |
| | 44 | +12V-35 | | +12V | 20 | R |
| | 45 | OV(D)-5 | | OV | 20 | BK |
| | 46 | OV(D)-5 | | OV | 20 | BK |
| | 47 | -20V(D)-5 | | -20V | 20 | S |
| | 48 | -20V(D)-5 | | -20V | 20 | S |
| | 49 | -85V-35 | | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES: ALL WIRES: 22 GAUGE UNLESS OTHERWISE NOTED

LIST 85

J14
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J105-S | 4 | Output F/F #1 Odd Bit 196 | * | W/G |
| | 2 | J109-15 | | Even | | W/BL |
| | 3 | J105-19 | | Output F/F #2 Odd Bit 195 | | W/Y |
| | 4 | J109-N | | Even | | W/G |
| | 5 | J105-R | | Output F/F #3 Odd Bit 194 | | W/O |
| | 6 | J109-14 | | Even | | W/Y |
| | 7 | J105-18 | | Output F/F #4 Odd Bit 193 | | V |
| | 8 | J109-M | | Even | | W/O |
| | 9 | J105-Q | | Output F/F #5 Odd Bit 192 | | BL |
| | 10 | J109-13 | | Even | | V |
| | 11 | J105-17 | | Output F/F #6 Odd Bit 191 | | G |
| | 12 | J109-L | | Even | | BL |
| | 13 | J105-P | | Output F/F #7 Odd Bit 190 | | Y |
| | 14 | J109-12 | | Even | | G |
| | 15 | J105-16 | | Output F/F #8 Odd Bit 189 | | O |
| | 16 | J109-K | | Even | | Y |
| | 17 | J105-O | | Output F/F #9 Odd Bit 188 | | W/V |
| | 18 | J109-11 | | Even | | O |
| | 19 | J105-15 | | Output F/F #10 Odd Bit 187 | | W/BL |
| | 20 | J109-J | 4 | Even | | W/V |
| | 21 | | | | | |
| | 22 | | | | | |

NOTES: ALL WIRES 22 GauGE
UNLESS OTHERWISE NOTED

LIST 86

J14
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J13-34 | | Core Shift | | V |
| | 34 | J15-34 | | Core Shift | | V |
| | 35 | J13-35 | | Odd Reset | | O |
| | 35 | J15-35 | | Odd Reset | | O |
| | 36 | J13-36 | | Even Reset | | G |
| | 36 | J15-36 | | Even Reset | | G |
| | 37 | J13-37 | | Odd F/F Gate | | W/O |
| | 37 | J15-37 | | Odd F/F Gate | | W/O |
| | 38 | J13-38 | | Even F/F Gate | | W/G |
| | 38 | J15-38 | | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 39 | | | | | |
| | 40 | J13-41 | | Core Output | | W/G |

NOTES: ALL WIRES 22 GAUGE
UNLESS OTHERWISE NOTED

LIST 87

J14
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 41 | J15-40 | | Core Input | | G |
| | 42 | -17(D)-6 | | -17V | 20 | W/S |
| | 43 | -17(D)-6 | | -17V | 20 | W/S |
| | 44 | +12-36 | | +12V | 20 | R |
| | 45 | OV(D)-6 | | OV | 20 | BK |
| | 46 | OV(D)-6 | | OV | 20 | BK |
| | 47 | -20V(D)-6 | | -20V | 20 | S |
| | 48 | -20V(D)-6 | | -20V | 20 | S |
| | 49 | -85V-36 | | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 88

J15
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J105-X | 3 | Output F/F #1 Odd Bit 206 | * | W/G |
| | 2 | J109-20 | | Even | | W/BL |
| | 3 | J105-24 | | Output F/F #2 Odd Bit 205 | | W/Y |
| | 4 | J109-S | | Even | | W/G |
| | 5 | J105-W | | Output F/F #3 Odd Bit 204 | | W/O |
| | 6 | J109-19 | | Even | | W/Y |
| | 7 | J105-23 | | Output F/F #4 Odd Bit 203 | | V |
| | 8 | J109-R | | Even | | W/O |
| | 9 | J105-V | | Output F/F #5 Odd Bit 202 | | BL |
| | 10 | J109-18 | | Even | | V |
| | 11 | J105-22 | | Output F/F #6 Odd Bit 201 | | G |
| | 12 | J109-Q | | Even | | BL |
| | 13 | J105-U | | Output F/F #7 Odd Bit 200 | | Y |
| | 14 | J109-17 | | Even | | G |
| | 15 | J105-21 | | Output F/F #8 Odd Bit 199 | | O |
| | 16 | J109-P | | Even | | Y |
| | 17 | J105-T | | Output F/F #9 Odd Bit 198 | | W/V |
| | 18 | J109-16 | | Even | | O |
| | 19 | J105-20 | | Output F/F #10 Odd Bit 197 | | W/BL |
| | 20 | J109-O | 3 | Even | | W/V |
| | 21 | | | | | |
| | 22 | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 89

J15
10 BIT SR (7608A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J14-34 | | Core Shift | | V |
| | 34 | J16-34 | | Core Shift | | V |
| | 35 | J14-35 | | Odd Reset | | O |
| | 35 | J16-35 | | Odd Reset | | O |
| | 36 | J14-36 | | Even Reset | | G |
| | 36 | J16-36 | | Even Reset | | G |
| | 37 | J14-37 | | Odd F/F Gate | | W/O |
| | 37 | J16-37 | | Odd F/F Gate | | W/O |
| | 38 | J14-38 | | Even F/F Gate | | W/G |
| | 38 | J16-38 | | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 39 | | | | | |
| | 40 | J14-41 | | Core Output | | G |
| | 41 | J16-40 | | Core Input | | W/G |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 90

J15
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 42 | -17V(D)-7 | | -17V | 20 | W/S |
| | 43 | -17V(D)-7 | | -17V | 20 | W/S |
| | 44 | +12V-37 | | +12V | 20 | R |
| | 45 | OV(D)-7 | | OV | 20 | B/K |
| | 46 | OV(D)-7 | | OV | 20 | BK |
| | 47 | -20V(D)-7 | | -20V | 20 | S |
| | 48 | -20V(D)-7 | | -20V | 20 | S |
| | 49 | -85V-37 | | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 91

J16
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J106-E | 3 | Output F/F #1 Odd Bit 216 | * | W/V |
| | 2 | J110-D | | Even | | W/G |
| | 3 | J106-5 | | Output F/F #2 Odd Bit 215 | | W/BL |
| | 4 | J110-4 | | Even | | W/Y |
| | 5 | J106-D | | Output F/F #3 Odd Bit 214 | | W/G |
| | 6 | J110-C | | Even | | W/0 |
| | 7 | J106-4 | | Output F/F #4 Odd Bit 213 | | W/V |
| | 8 | J110-3 | | Even | | V |
| | 9 | J106-C | | Output F/F #5 Odd Bit 212 | | W/0 |
| | 10 | J110-B | | Even | | BL |
| | 11 | J106-3 | | Output F/F #6 Odd Bit 211 | | V |
| | 12 | J110-2 | | Even | | G |
| | 13 | J106-B | | Output F/F #7 Odd Bit 210 | | BL |
| | 14 | J110-A | | Even | | Y |
| | 15 | J106-2 | | Output F/F #8 Odd Bit 209 | | G |
| | 16 | J110-1 | | Even | | 0 |
| | 17 | J106-A | | Output F/F #9 Odd Bit 208 | | Y |
| | 18 | J109-21 | | Even | | 0 |
| | 19 | J106-1 | | Output F/F #10 Odd Bit 207 | | 0 |
| | 20 | J109-T | 3 | Even | | W/V |
| | 21 | | | | | |
| | 22 | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 92

J16
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J15-34 | | Core Shift | | V |
| | 34 | J12-34 | | Core Shift | | V |
| | 35 | J15-35 | | Odd Reset | | 0 |
| | 35 | P40-j | | Odd Reset | | 0 |
| | 36 | J15-36 | | Even Reset | | G |
| | 36 | P40-m | | Even Reset | | G |
| | 37 | J15-37 | | Odd F/F Gate | | W/0 |
| | 37 | P40-k | | Odd F/F Gate | | W/0 |
| | 38 | J15-38 | | Even F/F Gate | | W/G |
| | 38 | P40-n | | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 39 | | | | | |
| | 40 | J15-41 | | Core Output | | W/G |
| | 41 | J9-40 | | Core Input | | G |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 93

J16
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 42 | -17V(D)-8 | | -17V | 20 | W/S |
| | 43 | -17V(D)-8 | | -17V | 20 | W/S |
| | 44 | +12V-38 | | +12V | 20 | R |
| | 45 | OV(D)-8 | | OV | 20 | BK |
| | 46 | OV(D)-8 | | OV | 20 | BK |
| | 47 | -20V(D)-8 | | -20V | 20 | S |
| | 48 | -20V(D)-8 | | -20V | 20 | S |
| | 49 | -85V-38 | | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 94

J20
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J104-R | 2 | Output F/F #1 Odd Bit 146 | | W/O |
| | 2 | J108-J | | Even | | W/V |
| | 3 | J104-18 | | Output F/F #2 Odd Bit 145 | | V |
| | 4 | J108-10 | | Even | | W/BL |
| | 5 | J104-Q | | Output F/F #3 Odd Bit 144 | | BL |
| | 6 | J108-I | | Even | | W/G |
| | 7 | J104-17 | | Output F/F #4 Odd Bit 143 | | G |
| | 8 | J108-9 | | Even | | W/Y |
| | 9 | J104-P | | Output F/F #5 Odd Bit 142 | | Y |
| | 10 | J108-H | | Even | | W/O |
| | 11 | J104-16 | | Output F/F #6 Odd Bit 141 | | O |
| | 12 | J108-8 | | Even | | V |
| | 13 | J104-O | | Output F/F #7 Odd Bit 140 | | W/V |
| | 14 | J108-G | | Even | | BL |
| | 15 | J104-15 | | Output F/F #8 Odd Bit 139 | | W/BL |
| | 16 | J108-7 | | Even | | G |
| | 17 | J104-N | | Output F/F #9 Odd Bit 138 | | W/G |
| | 18 | J108-F | | Even | | Y |
| | 19 | J104-14 | | Output F/F # 10 Odd Bit 137 | | W/Y |
| | 20 | J108-6 | 2 | Even | | O |
| | 21 | | | | | |
| | 22 | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 95

J20

10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | | | | * | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J21-34 | 2 | Core Shift | | V |
| | 34 | J24-34 | | Core Shift | | V |
| | 35 | J21-35 | | Odd Reset | | O |
| | 35 | J24-35 | | Odd Reset | | O |
| | 36 | J21-36 | | Even Reset | | G |
| | 36 | J24-36 | | Even Reset | | G |
| | 37 | J21-37 | | Odd F/F Gate | | W/O |
| | 37 | J24-37 | | Odd F/F Gate | | W/O |
| | 38 | J21-38 | | Even F/F Gate | | W/G |
| | 38 | J24-38 | 2 | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 40 | J27-41 | 1 | Core Output | | G |
| | 41 | J21-40 | 2 | Core Input | | W/G |
| | 42 | -17V(B)-3 | 2 | -17V | 20 | W/S |

NOTES: * #22 unless otherwise specified.

LIST 96

J20

10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 43 | -17V(B)-3 | 2 | -17V | 20 | W/S |
| | 44 | +12V(A)-3 | | +12V | 20 | R |
| | 45 | 0V(B)-3 | | 0V | 20 | BK |
| | 46 | 0V(B)-3 | | 0V | 20 | BK |
| | 47 | -20V(B)-3 | | -20V | 20 | S |
| | 48 | -20V(B)-3 | | -20V | 20 | S |
| | 49 | -85V(A)-3 | 2 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Ground | 22 | BK |

NOTES: * #22 unless otherwise specified.

LIST 97

J21
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J104-W | 2 | Output F/F #1 Odd Bit 156 | | W/O |
| | 2 | J108-O | | Even | | W/V |
| | 3 | J104-23 | | Output F/F #2 Odd Bit 155 | | V |
| | 4 | J108-15 | | Even | | W/BL |
| | 5 | J104-V | | Output F/F #3 Odd Bit 154 | | BL |
| | 6 | J108-N | | Even | | W/G |
| | 7 | J104-22 | | Output F/F #4 Odd Bit 153 | | G |
| | 8 | J108-14 | | Even | | W/Y |
| | 9 | J104-U | | Output F/F #5 Odd Bit 152 | | Y |
| | 10 | J108-M | | Even | | W/O |
| | 11 | J104-21 | | Output F/F #6 Odd Bit 151 | | O |
| | 12 | J108-13 | | Even | | V |
| | 13 | J104-T | | Output F/F #7 Odd Bit 150 | | W/V |
| | 14 | J108-L | | Even | | BL |
| | 15 | J104-20 | | Output F/F #8 Odd Bit 149 | | W/BL |
| | 16 | J108-12 | | Even | | G |
| | 17 | J104-S | | Output F/F #9 Odd Bit 148 | | W/G |
| | 18 | J108-K | | Even | | Y |
| | 19 | J104-19 | | Output F/F #10 Odd Bit 147 | | W/Y |
| | 20 | J108-11 | 2 | Even | | O |
| | 21 | | | | | |
| | 22 | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 98

J21
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J20-34 | 2 | Core Shift | | V |
| | 34 | J22-34 | | Core Shift | | V |
| | 35 | J20-35 | | Odd Reset | | O |
| | 35 | J22-35 | | Odd Reset | | O |
| | 36 | J20-36 | | Even Reset | | G |
| | 36 | J22-36 | | Even Reset | | G |
| | 37 | J20-37 | | Odd F/F Gate | | W/O |
| | 37 | J22-37 | | Odd F/F Gate | | W/O |
| | 38 | J20-38 | | Even F/F Gate | | W/G |
| | 38 | J22-38 | 2 | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 40 | J20-41 | 2 | Core Output | | W/G |
| | 41 | J22-40 | 2 | Core Input | | G |
| | 42 | -17V(B)-4 | 2 | -17V | 20 | W/S |

NOTES: * #22 unless otherwise specified.

LIST 99

J21
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 43 | -17V(B)-4 | 2 | -17V | 20 | W/S |
| | 44 | +12V(A)-4 | | +12V | | R |
| | 45 | 0V(B)-4 | | 0V | | BK |
| | 46 | 0V(B)-4 | | 0V | | BK |
| | 47 | -20V(B)-4 | | -20V | | S |
| | 48 | -20V(B)-4 | | -20V | | S |
| | 49 | -85V(A)-4 | 2 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Ground | 22 | BK |

NOTES:

LIST 100

J22
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J40-F | 1 | Output F/F #1 Odd Bit 166 | * | W/G |
| | 2 | J108-T | | Even | | W/V |
| | 3 | J40-E | | Output F/F #2 Odd Bit 165 | | W/Y |
| | 4 | J108-20 | | Even | | W/BL |
| | 5 | J40-D | | Output F/F #3 Odd Bit 164 | | W/O |
| | 6 | J108-S | | Even | | W/G |
| | 7 | J40-C | | Output F/F #4 Odd Bit 163 | | V |
| | 8 | J108-19 | | Even | | W/Y |
| | 9 | J40-B | | Output F/F #5 Odd Bit 162 | | BL |
| | 10 | J108-R | | Even | | W/O |
| | 11 | J40-A | | Output F/F #6 Odd Bit 161 | | G |
| | 12 | J108-18 | | Even | | V |
| | 13 | J40-e | | Output F/F #7 Odd Bit 160 | | Y |
| | 14 | J108-Q | | Even | | BL |
| | 15 | J40-d | | Output F/F #8 Odd Bit 159 | | O |
| | 16 | J108-17 | | Even | | G |
| | 17 | J104-X | | Output F/F #9 Odd Bit 158 | | W/G |
| | 18 | J108-P | | Even | | Y |
| | 19 | J104-24 | | Output F/F #10 Odd Bit 157 | | W/Y |
| | 20 | J108-16 | 1 | Even | | O |
| | 21 | | | | | |
| | 22 | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 101

J22
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | | | | * | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J21-34 | 1 | Core Shift | | V |
| | 34 | J23-34 | | Core Shift | | V |
| | 35 | J21-35 | | Odd Reset | | O |
| | 35 | J23-35 | | Odd Reset | | O |
| | 36 | J21-36 | | Even Reset | | G |
| | 36 | J23-36 | | Even Reset | | G |
| | 37 | J21-37 | | Odd F/F Gate | | W/O |
| | 37 | J23-37 | | Odd F/F Gate | | W/O |
| | 38 | J21-38 | | Even F/F Gate | | W/G |
| | 38 | J23-38 | 1 | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 40 | J21-41 | | Core Output | | G |
| | 41 | J23-40 | | Core Input | | W/G |
| | 42 | -17V(B)-5 | 1 | -17V | 20 | W/S |

NOTES: * #22 unless otherwise specified.

LIST 102

J22
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 43 | -17V(B)-5 | 1 | -17V | 20 | W/S |
| | 44 | +12V(A)-5 | | +12V | | R |
| | 45 | 0V(B)-5 | | 0V | | BK |
| | 46 | 0V(B)-5 | | 0V | | BK |
| | 47 | -20V(B)-5 | | -20V | | S |
| | 48 | -20V(B)-5 | | -20V | | S |
| | 49 | -85V(A)-5 | 1 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES: * #22 unless otherwise specified.

LIST 103

J 23

10 BIT S.R. (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J40-R | 1 | Output F/F #1 Odd Bit 176 | * | W/G |
| | 2 | J40-a | | Even | | W/BL |
| | 3 | J40-Q | | Output F/F #2 Odd Bit 175 | | W/Y |
| | 4 | J40-Z | | Even | | W/G |
| | 5 | J40-P | | Output F/F #3 Odd Bit 174 | | W/O |
| | 6 | J40-Y | | Even | | W/Y |
| | 7 | J40-N | | Output F/F #4 Odd Bit 173 | | V |
| | 8 | J40-X | | Even | | W/O |
| | 9 | J40-M | | Output F/F #5 Odd Bit 172 | | BL |
| | 10 | J40-W | | Even | | V |
| | 11 | J40-L | | Output F/F #6 Odd Bit 171 | | G |
| | 12 | J40-V | | Even | | BL |
| | 13 | J40-K | | Output F/F #7 Odd Bit 170 | | Y |
| | 14 | J40-U | | Even | | G |
| | 15 | J40-J | | Output F/F #8 Odd Bit 169 | | O |
| | 16 | J40-T | | Even | | Y |
| | 17 | J40-H | | Output F/F #9 Odd Bit 168 | | W/V |
| | 18 | J40-S | | Even | | O |
| | 19 | J40-G | | Output F/F #10 Odd Bit 167 | | W/BL |
| | 20 | J108-21 | 1 | Even | | O |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED.

LIST 104

J23

10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | * | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J22-34 | 1 | Core Shift | | V |
| | 35 | J22-35 | | Odd Reset | | O |
| | 36 | J22-36 | | Even Reset | | G |
| | 37 | J22-37 | | Odd F/F Gate | | W/O |
| | 38 | J22-38 | 1 | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 40 | J22-41 | | Core Output | | W/G |
| | 41 | J40-r | 1 | Core Input | | G |
| | 42 | -17V(B)-6 | | -17V | 20 | W/S |
| | 43 | -17V(B)-6 | | -17V | | W/S |
| | 44 | -12V(A)-6 | | +12V | | R |
| | 45 | 0V(B)-6 | | 0V | | BK |
| | 46 | 0V(B)-6 | | 0V | | BK |
| | 47 | -20V(B)-6 | | -20V | | S |
| | 48 | -20V(B)-6 | | -20V | | S |
| | 49 | -85V(A)-6 | 1 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | | BK |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED.

LIST 105

J24
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J103-11 | 2 | Output F/F #1 Odd Bit 106 | * | W/O |
| | 2 | J107-11 | | Even | | O |
| | 3 | J103-J | | Output F/F #2 Odd Bit 105 | | V |
| | 4 | J107-J | | Even | | W/V |
| | 5 | J103-10 | | Output F/F #3 Odd Bit 104 | | BL |
| | 6 | J107-10 | | Even | | W/BL |
| | 7 | J103-I | | Output F/F #4 Odd Bit 103 | | G |
| | 8 | J107-I | | Even | | W/G |
| | 9 | J103-9 | | Output F/F #5 Odd Bit 102 | | Y |
| | 10 | J107-9 | | Even | | W/Y |
| | 11 | J103-H | | Output F/F #6 Odd Bit 101 | | O |
| | 12 | J107-H | | Even | | W/O |
| | 13 | J103-8 | | Output F/F #7 Odd Bit 100 | | W/V |
| | 14 | J107-8 | | Even | | V |
| | 15 | J103-G | | Output F/F #8 Odd Bit 99 | | W/BL |
| | 16 | J107-G | | Even | | BL |
| | 17 | J103-7 | | Output F/F #9 Odd Bit 98 | | W/G |
| | 18 | J107-7 | | Even | | G |
| | 19 | J103-F | | Output F/F #10 Odd Bit 97 | | W/Y |
| | 20 | J107-F | 2 | Even | | Y |
| | 21 | | | | | |
| | 22 | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 106

J 24
10 BIT S.R. (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | | | | * | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J20-34 | 2 | Core Shift | | V |
| | 34 | J25-34 | 2 | Core Shift | | V |
| | 35 | J20-35 | 2 | Odd Reset | | O |
| | 35 | J25-35 | 2 | Odd Reset | | O |
| | 36 | J20-36 | 2 | Even Reset | | G |
| | 36 | J25-36 | 2 | Even Reset | | G |
| | 37 | J20-37 | 2 | Odd F/F Gate | | W/O |
| | 37 | J25-37 | 2 | Odd F/F Gate | | W/O |
| | 38 | J20-38 | 2 | Even F/F Gate | | W/G |
| | 38 | J25-38 | 2 | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 40 | J33-41 | | Core Output | | G |
| | 41 | J25-40 | | Core Input | | W/G |
| | 42 | -17V(B)-7 | 2 | -17V | 20 | W/S |
| | 43 | -17V(B)-7 | 2 | -17V | 20 | W/S |
| | 44 | +12V(A)-7 | 2 | +12V | 20 | R |

NOTES:
All wires 22 Guage unless otherwise noted

LIST 107

J 24

10 BIT S.R. (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 45 | OV(B)-7 | 2 | OV | 20 | BK |
| | 46 | OV(B)-7 | 2 | OV | 20 | BK |
| | 47 | -20V(B)-7 | 2 | -20V | 20 | S |
| | 48 | -20V(B)-7 | 2 | -20V | 20 | S |
| | 49 | -85V(A)-7 | 2 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES:
All wires 22 Gauge
unless otherwise noted

LIST 108

J25

10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J104-C | 2 | Output F/F #1 Odd Bit 116 | * | W/O |
| | 2 | J107-16 | | Even | | O |
| | 3 | J104-3 | | Output F/F #2 Odd Bit 115 | | V |
| | 4 | J107-0 | | Even | | W/V |
| | 5 | J104-B | | Output F/F #3 Odd Bit 114 | | BL |
| | 6 | J107-15 | | Even | | W/BL |
| | 7 | J104-2 | | Output F/F #4 Odd Bit 113 | | G |
| | 8 | J107-N | | Even | | W/G |
| | 9 | J104-A | | Output F/F #5 Odd Bit 112 | | Y |
| | 10 | J107-14 | | Even | | W/Y |
| | 11 | J104-1 | | Output F/F #6 Odd Bit 111 | | O |
| | 12 | J107-M | | Even | | W/O |
| | 13 | J103-13 | | Output F/F #7 Odd Bit 110 | | W/V |
| | 14 | J107-13 | | Even | | V |
| | 15 | J103-L | | Output F/F #8 Odd Bit 109 | | W/BL |
| | 16 | J107-L | | Even | | BL |
| | 17 | J103-12 | | Output F/F #9 Odd Bit 108 | | W/G |
| | 18 | J107-12 | | Even | | G |
| | 19 | J103-K | | Output F/F #10 Odd Bit 107 | | W/Y |
| | 20 | J107-K | 2 | Even | | Y |
| | 21 | | | | | |
| | 22 | | | | | |

NOTES: ALL WIRES 22 GAUGE
UNLESS OTHERWISE NOTED

LIST 109

J25
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J24-34 | 2 | Core Shift | | V |
| | 34 | J26-34 | 2 | Core Shift | | V |
| | 35 | J24-35 | 2 | Odd Reset | | O |
| | 35 | J26-35 | 2 | Odd Reset | | O |
| | 36 | J24-36 | 2 | Even Reset | | G |
| | 36 | J26-36 | 2 | Even Reset | | G |
| | 37 | J24-37 | 2 | Odd F/F Gate | | W/O |
| | 37 | J26-37 | 2 | Odd F/F Gate | | W/O |
| | 38 | J24-38 | 2 | Even F/F Gate | | W/G |
| | 38 | J26-38 | 2 | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 39 | | | | | |
| | 40 | J24-41 | | Core Output | | W/G |
| | 41 | J26-40 | | Core Input | | G |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 110

J25
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 42 | -17V(B)-8 | 2 | -17V | 20 | W/S |
| | 43 | -17V(B)-8 | | -17V | | W/S |
| | 44 | +12V(A)-8 | | +12V | | R |
| | 45 | OV(B)-8 | | OV | | BK |
| | 46 | OV(B)-8 | | OV | | BK |
| | 47 | -20V(B)-8 | | -20V | | S |
| | 48 | -20V(B)-8 | | -20V | | S |
| | 49 | -85V(A)-8 | 2 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 111

J26
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J104-H | 1 | Output F/F #1 Odd Bit 126 | * | W/O |
| | 2 | J107-21 | | Even | | O |
| | 3 | J104-8 | | Output F/F #2 Odd Bit 125 | | W/V |
| | 4 | J107-T | | Even | | V |
| | 5 | J104-G | | Output F/F #3 Odd Bit 124 | | BL |
| | 6 | J107-20 | | Even | | W/BL |
| | 7 | J104-7 | | Output F/F #4 Odd Bit 123 | | G |
| | 8 | J107-S | | Even | | W/G |
| | 9 | J104-F | | Output F/F #5 Odd Bit 122 | | Y |
| | 10 | J107-19 | | Even | | W/Y |
| | 11 | J104-6 | | Output F/F #6 Odd Bit 121 | | O |
| | 12 | J107-R | | Even | | W/O |
| | 13 | J104-E | | Output F/F #7 Odd Bit 120 | | W/V |
| | 14 | J107-18 | | Even | | V |
| | 15 | J104-5 | | Output F/F #8 Odd Bit 119 | | W/BL |
| | 16 | J107-Q | | Even | | BL |
| | 17 | J104-D | | Output F/F #9 Odd Bit 118 | | W/G |
| | 18 | J107-17 | | Even | | G |
| | 19 | J104-4 | | Output F/F #10 Odd Bit 117 | | W/Y |
| | 20 | J107-P | 1 | Even | | Y |
| | 21 | | | | | |
| | 22 | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 112

J26
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J27-34 | 1 | Core Shift | | V |
| | 34 | J25-34 | | Core Shift | | V |
| | 35 | J27-35 | | Odd Reset | | O |
| | 35 | J25-35 | | Odd Reset | | O |
| | 36 | J27-36 | | Even Reset | | G |
| | 36 | J25-36 | | Even Reset | | G |
| | 37 | J27-37 | | Odd F/F Gate | | W/O |
| | 37 | J25-37 | | Odd F/F Gate | | W/O |
| | 38 | J27-38 | | Even F/F Gate | | W/G |
| | 38 | J25-38 | 1 | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 40 | J25-41 | | Core Output | | G |
| | 41 | J27-40 | | Core Input | | W/G |
| | 42 | -17V(B)-9 | 1 | -17V | 20 | W/S |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE SPECIFIED

LIST 113

J26

10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 43 | -17V(B)-9 | 1 | -17V | 20 | W/S |
| | 44 | +12V(A)-9 | | +12 V | | R |
| | 45 | 0V(B)-9 | | 0V | | BK |
| | 46 | 0V(B)-9 | | 0V | | BK |
| | 47 | -20V(B)-9 | | -20V | | S |
| | 48 | -20V(B)-9 | | -20V | | S |
| | 49 | -85V(A)-9 | 1 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES:

LIST 114

J27

10 BIT SR (76-8A)

| TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|
| 1 | J104-M | 1 | Output F/F #1 Odd Bit 136 | * | W/O |
| 2 | J108-E | | Even | | W/V |
| 3 | J104-13 | | Output F/F #2 Odd Bit 135 | | V |
| 4 | J108-5 | | Even | | W/BL |
| 5 | J104-L | | Output F/F #3 Odd Bit 134 | | BL |
| 6 | J108-D | | Even | | W/G |
| 7 | J104-12 | | Output F/F #4 Odd Bit 133 | | G |
| 8 | J108-4 | | Even | | W/Y |
| 9 | J104-K | | Output F/F #5 Odd Bit 132 | | Y |
| 10 | J108-C | | Even | | W/O |
| 11 | J104-11 | | Output F/F #6 Odd Bit 131 | | O |
| 12 | J108-3 | | Even | | V |
| 13 | J104-J | | Output F/F #7 Odd Bit 130 | | W/V |
| 14 | J108-B | | Even | | BL |
| 15 | J104-10 | | Output F/F #8 Odd Bit 129 | | W/BL |
| 16 | J108-2 | | Even | | G |
| 17 | J104-I | | Output F/F #9 Odd Bit 128 | | W/G |
| 18 | J108-A | | Even | | Y |
| 19 | J104-9 | | Output F/F #10 Odd Bit 127 | | W/Y |
| 20 | J108-1 | 1 | Even | | O |
| 21 | | | | | |
| 22 | | | | | |

TES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 115

J27
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J29-16 | 1 | Core Shift | | V |
| | 34 | J26-34 | | Core Shift | | V |
| | 35 | J29-18 | | Odd Reset | | O |
| | 35 | J26-35 | | Odd Reset | | O |
| | 36 | J29-20 | | Even Reset | | G |
| | 36 | J26-36 | | Even Reset | | G |
| | 37 | J29-19 | | Odd F/F Gate | | W/O |
| | 37 | J26-37 | | Odd F/F Gate | | W/O |
| | 38 | J29-21 | | Even F/F Gate | | W/G |
| | 38 | J26-38 | 1 | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 40 | J26-41 | | Core Output | | W/G |
| | 41 | J20-40 | | Core Input | | G |
| | 42 | -17V(B)-10 | 1 | -17V | 20 | W/S |
| | 43 | -17V(B)-10 | | -17V | | W/S |
| | 44 | +12V(A)-10 | | +12V | | R |
| | 45 | 0V(B)-10 | 1 | 0V | 20 | BK |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE SPECIFIED

LIST 116

J27
10 BIT SR (76-8A)

| TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|
| 46 | 0V(B)-10 | 1 | 0V | 20 | BK |
| 47 | -20V(B)-10 | | -20V | | S |
| 48 | -20V(B)-10 | | -20V | | S |
| 49 | -85V(A)-10 | 1 | -85V | 20 | W/GK |
| 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES:

LIST 117

J29
CONTROL

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J34-13 | 1 | Data #1 | 22 | V |
| | 2 | J34-14 | | #2 | | G |
| | 3 | J34-15 | | #3 | | Y |
| | 4 | J34-16 | | #4 | | O |
| | 5 | J34-17 | | Copy #1 | | V |
| | 6 | J34-18 | | #2 | | G |
| | 7 | J34-19 | | #3 | | Y |
| | 8 | J34-20 | | #4 | | O |
| | 9 | J34-21 | | EOW #1 | | V |
| | 10 | J34-22 | | #2 | | G |
| | 11 | J34-23 | | #3 | | Y |
| | 12 | J34-24 | | #4 | | O |
| | 13 | J101-24 | | D/A Hold | | BL |
| | 14 | J40-q | | Data Output | | G |
| | 15 | J33-40 | | SR Input | | W/G |
| | 16 | J27-34 | | Core Drive (Trigger | | V |
| | 16 | J33-34 | | Core Drive (Trigger) | | V |
| | 17 | | | | | |
| | 18 | J27-35 | | Odd Reset | | O |
| | 18 | J33-35 | | Odd Reset | | O |
| | 19 | J27-37 | | Odd Gate | | W/O |
| | 19 | J33-37 | | Odd Gate | | W/O |
| | 20 | J27-36 | | Even Reset | | G |
| | 20 | J33-36 | 1 | Even Reset | 22 | G |

NOTES:

LIST 118

J29
CONTROL

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 21 | J27-38 | 1 | Even Gate | * | W/G |
| | 21 | J33-38 | | Even Gate | | W/G |
| | 22 | J32-36 | | Every Reset | | Y |
| | 22 | J40-g | | Every Reset | | Y |
| | 23 | J32-38 | | Every Gate | | W/Y |
| | 23 | J40-h | | Every Gate | | W/Y |
| | 24 | J32-41 | 1 | SR Output | | G |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | J34-32 | 1 | Test Odd | | Y |
| | 33 | J34-33 | 1 | Test Even | | O |
| | 34 | J107-1 | 1 | Bit 86 Even Output | | W/O |
| | 35 | J103-1 | | Bit 86 Odd Output | | O |
| | 36 | J102-22 | | Bit 85 Even Output | | G |
| | 37 | J102-U | | Bit 84 Odd Output | | Y |
| | 38 | J102-21 | | Bit 83 Every Output | | O |
| | 39 | J102-T | | Bit 82 Every Output | | W/V |
| | 40 | J102-20 | 1 | Bit 81 Every Output | 20 | W/BL |
| | 41 | -17V(D)-32 jumper | | -17V (D) | 20 | W/S |
| | 42 | -17V(D)-32 jumper | | -17V (D) | 20 | W/S |

NOTES: * #22 unless otherwise specified.

LIST 119

## J29 CONTROL

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 43 | -20V(D)-32 | 1 | -20V (D) | 20 | S |
| | 44 | +12V (A)-2 | | +12V | 22 | R |
| | 45 | 0V(A)-10 | | 0V | 20 | BK |
| | 46 | 0V(A)-10 | | 0V | 20 | BK |
| | 47 | -20V(A)-3 | | -20V | 20 | S |
| | 48 | -20V(A)-3 | | -20V | 20 | S |
| | 49 | -85V(A)-2 | 1 | -85V | 22 | W/BK |
| | 50 | Rack | | Chassis Ground | 22 | BK |

NOTES:

LIST 120

## J30 POWER CONTROL

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | | | | | |
| | 3 | | | | | |
| | 4 | | | | | |
| | 5 | TB1-1 | 1A | AC Common | 20 | W |
| | 6 | | | | | |
| | 7 | F1-2 | 1A | AC Ø1 Fused | 20 | W/BR |
| | 8 | | | | | |
| | 9 | | | | | |
| | 10 | SW1-1 | 1A | AC Ø1 Switched | 20 | G |
| | 11 | | | | | |
| | 12 | | | | | |
| | 13 | Contactor-G | 1A | AC Ø1 From Contactor | 20 | G |
| | 14 | | | | | |
| | 15 | | | | | |
| | 16 | 0V(A)-8 | jumper | 0V | 20 | BK |
| | 17 | 0V(A)-8 | jumper | 0V | 20 | BK |
| | 18 | | | | | |
| | 19 | | | | | |
| | 20 | | | | | |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES:

LIST 121

## J30
## POWER CONTROL

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | * | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | +12V(A)-19 | 1 | +12V (A) Supply | | R |
| | 35 | | | | | |
| | 36 | -20V(A)-19 | | -20V (A) Supply | | S |
| | 37 | | | | | |
| | 38 | -85V(A)-19 | | -85V (A) Supply | | W/BK |
| | 39 | | | | | |
| | 40 | -17V(B)-12 | | -17V (B) Supply | | W/S |
| | 41 | | | | | |
| | 42 | -20V(B)-12 | | -20V (B) Supply | | S |
| | 43 | | | | | |
| | 44 | J40-BG | | -17V (C) Supply | | W/S |
| | 45 | | | | | |
| | 46 | J40-BF | | -20V (C) Supply | | S |
| | 47 | | | | | |
| | 48 | -17V(D)-38 | | -17V (D) Supply | | W/S |
| | 49 | -20V(D)-38 | | -20V (D) Supply | | S |
| | 50 | Rack | 1 | Chassis Ground | | BK |

NOTES: all wires 22 gauge unless otherwise specified.

LIST 122

## J31
## 20 BIT SR (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J102-I | 2 | Output F/F #1 - Bit 60 Every | * | W/G |
| | 2 | J102-9 | | Output F/F #2 - Bit 59 Every | | W/Y |
| | 3 | J102-H | | Output F/F #3 - Bit 58 Every | | W/O |
| | 4 | J102-8 | | Output F/F #4 - Bit 57 Every | | V/ |
| | 5 | J102-G | | Output F/F #5 - Bit 56 Every | | BL |
| | 6 | J102-7 | | Output F/F #6 - Bit 55 Every | | G |
| | 7 | J102-F | | Output F/F #7 - Bit 54 Every | | Y |
| | 8 | J102-6 | | Output F/F #8 - Bit 53 Every | | O |
| | 9 | J102-E | | Output F/F #9 - Bit 52 Every | | W/V |
| | 10 | J102-5 | | Output F/F #10 - Bit 51 Every | | W/BL |
| | 11 | J102-D | | Output F/F #11 - Bit 50 Every | | W/G |
| | 12 | J102-4 | | Output F/F #12 - Bit 49 Every | | W/Y |
| | 13 | J102-C | | Output F/F #13 - Bit 48 Every | | W/O |
| | 14 | J102-3 | | Output F/F #14 - Bit 47 Every | | V |
| | 15 | J102-B | | Output F/F #15 - Bit 46 Every | | BL |
| | 16 | J102-2 | | Output F/F #16 - Bit 45 Every | | G |
| | 17 | J102-A | 2 | Output F/F #17 - Bit 44 Every | | Y |

NOTES: (*) #22 unless otherwise specified

LIST 123

J31

20 BIT SR (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 18 | J102-1 | 2 | Output F/F # 18 - Bit 43 Every | 22 | O |
| | 19 | J101-U | 2 | Output F/F # 19 Bit 42 Every | 22 | Y |
| | 20 | J101-21 | 2 | Output F/F # 20 Bit 41 Every | 22 | O |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J32-34 | 2 | Core Shift | 22 | V |
| | 34 | J35-34 | 2 | Core Shift | 22 | V |
| | 35 | | | | | |
| | 36 | J32-36 | 2 | F/F Reset Trigger | 22 | Y |
| | 36 | J35-36 | 2 | F/F Reset Trigger | 22 | Y |

NOTES:

LIST 124

J31

20 BIT SR (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 37 | | | | | |
| | 38 | J32-38 | 2 | Read Gate | 22 | W/Y |
| | 38 | J35-38 | | Read Gate | 22 | W/Y |
| | 39 | | | | | |
| | 40 | J36-41 | | Core Output | | G |
| | 41 | J32-40 | | Core Input | 20 | W/G |
| | 42 | -17V(D)-36 | 2 | -17V | 20 | W/S |
| | 43 | -17V(D)-36 | | -17V | 20 | W/S |
| | 44 | +12V(A)-15 | | +12V | 20 | R |
| | 45 | 0V(A)-15 | | 0V | 20 | BK |
| | 46 | 0V(A)-15 | | 0V | 20 | BK |
| | 47 | -20V(D)-36 | | -20V | 20 | S |
| | 48 | -20V(D)-36 | | -20V | 20 | S |
| | 49 | -85V(A)-15 | | -85V | 20 | W/BK |
| | 50 | Rack | 2 | Chassis Ground | 22 | BK |

NOTES:

LIST 125

J32

20 BIT SR (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J102-S | 2 | Output F/F #1 - Bit 80 Every | * | W/G |
| | 2 | J102-19 | | Output F/F #2 - Bit 79 Every | | W/Y |
| | 3 | J102-R | | Output F/F #3 - Bit 78 Every | | W/O |
| | 4 | J102-18 | | Output F/F #4 - Bit 77 Every | | V |
| | 5 | J102-Q | | Output F/F #5 - Bit 76 Every | | BL |
| | 6 | J102-17 | | Output F/F #6 - Bit 75 Every | | G |
| | 7 | J102-P | | Output F/F #7 - Bit 74 Every | | Y |
| | 8 | J102-16 | | Output F/F #8 - Bit 73 Every | | O |
| | 9 | J102-O | | Output F/F #9 - Bit 72 Every | | W/V |
| | 10 | J102-15 | | Output F/F #10 - Bit 71 Every | | W/BL |
| | 11 | J102-N | | Output F/F #11 - Bit 70 Every | | W/G |
| | 12 | J102-14 | | Output F/F #12 - Bit 69 Every | | W/Y |
| | 13 | J102-M | | Output F/F #13 - Bit 68 Every | | W/O |
| | 14 | J102-13 | | Output F/F #14 - Bit 67 Every | | V |
| | 15 | J102-L | | Output F/F #15 - Bit 66 Every | | BL |
| | 16 | J102-12 | | Output F/F #16 - Bit 65 Every | | G |
| | 17 | J102-K | 2 | Output F/F #17 - Bit 64 Every | | Y |

NOTES: (*) #22 unless otherwise specified.

LIST 126

J32

20 BIT SR (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 18 | J102-11 | 2 | Output F/F #18 Bit 63 Every | 22 | O |
| | 19 | J102-J | 2 | Output F/F #19 Bit 62 Every | 22 | W/V |
| | 20 | J102-10 | 2 | Output F/F #20 Bit 61 Every | 22 | W/BL |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J33-34 | 1 | Core Shift | 22 | V |
| | 34 | J31-34 | 1 | Core Shift | 22 | V |
| | 35 | | | | | |
| | 36 | J31-36 | 2 | F/F Reset Trigger | 22 | Y |
| | 37 | J29-24 | 2 | F/F Reset Trigger | 22 | Y |

NOTES:

LIST 127

J32
20 BIT SR (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 38 | J31-38 | 2 | Read Gate | * | W/Y |
| | 38 | J29-23 | | | | W/Y |
| | 39 | | | | | |
| | 40 | J31-41 | | Core Output | | W/G |
| | 41 | J29-24 | | Core Input | | G |
| | 42 | -17V(D)-35 | 2 | -17V | 20 | W/S |
| | 43 | -17V(D)-35 | | -17V | | W/S |
| | 44 | +12V(A)-14 | | +12V | | R |
| | 45 | 0V(A)-14 | | 0V | | BK |
| | 46 | 0V(A)-14 | | 0V | | BK |
| | 47 | -20V(D)-35 | | -20V | | S |
| | 48 | -20V(D)-35 | | -20V | | S |
| | 49 | -85V(A)-14 | 2 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Ground | | BK |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE SPECIFIED.

LIST 128

J33
10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J103-6 | 1 | Output F/F #1 Odd Bit 96 | * | W/O |
| | 2 | J107-6 | | Even " | | O |
| | 3 | J103-E | | Output F/F #2 Odd Bit 95 | | V |
| | 4 | J107-E | | Even " | | W/V |
| | 5 | J103-5 | | Output F/F #3 Odd Bit 94 | | BL |
| | 6 | J107-5 | | Even | | W/BL |
| | 7 | J103-D | | Output F/F #4 Odd Bit 93 | | G |
| | 8 | J107-D | | Even | | W/G |
| | 9 | J103-4 | | Output F/F #5 Odd Bit 92 | | Y |
| | 10 | J107-4 | | Even | | W/Y |
| | 11 | J103-C | | Output F/F #6 Odd Bit 91 | | O |
| | 12 | J107-C | | Even | | W/O |
| | 13 | J103-3 | | Output F/F #7 Odd Bit 90 | | W/V |
| | 14 | J107-3 | | Even | | V |
| | 15 | J103-B | | Output F/F #8 Odd Bit 89 | | W/BL |
| | 16 | J107-B | | Even | | BL |
| | 17 | J103-2 | | Output F/F #9 Odd Bit 88 | | W/G |
| | 18 | J107-2 | | Even | | G |
| | 19 | J103-A | | Output F/F #10 Odd Bit87 | | W/Y |
| | 20 | J107-A | I | Even | | Y |
| | 21 | | | | | |
| | 22 | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 129

J33

20 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J29-16 | 1 | Core Shift | | V |
| | 34 | J32-34 | | Core Shift | | V |
| | 35 | J29-18 | | Odd Reset | | O |
| | 35 | J40-j | | Odd Reset | | O |
| | 36 | J29-20 | | Even Reset | | G |
| | 36 | J40-m | | Even Reset | | G |
| | 37 | J29-19 | | Odd F/F Gate | | W/O |
| | 37 | J40-k | | Odd F/F Gate | | W/O |
| | 38 | J29-21 | | Even F/F Gate | | W/G |
| | 38 | J40-n | 1 | Even F/F Gate | | W/G |
| | 39 | | | | | |
| | 40 | J29-15 | 1 | Core Output | | W/G |
| | 41 | J24-40 | 1 | Core Input | | G |
| | 42 | -17V(D)-34 | 1 | -17V | 20 | W/S |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE SPECIFIED

LIST 130

J33

10 BIT SR (76-8A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 43 | -17V(D)-34 | 1 | -17V | 20 | W/S |
| | 44 | +12V(A)-13 | | +12V | | R |
| | 45 | 0V(A)-13 | | 0V | | BK |
| | 46 | 0V(A)-13 | | 0V | | BK |
| | 47 | -20V(D)-34 | | -20V | | S |
| | 48 | -20V(D)-34 | | -20V | | S |
| | 49 | -85V(A)-13 | 1 | -85V | 20 | W/GK |
| | 50 | Rack | | Chassis Ground | 22 | BK |

NOTES:

LIST 131

J34

TEST

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J99-A | 1 | Data #1 Input | * | V |
| | 2 | J99-B | | Data #2 Input | | G |
| | 3 | J99-C | | Data #3 Input | | Y |
| | 4 | J99-D | | Data #4 Input | | O |
| | 5 | J99-E | | Copy #1 Input | | V |
| | 6 | J99-F | | Copy #2 Input | | G |
| | 7 | J99-G | | Copy #3 Input | | Y |
| | 8 | J99-H | | Copy #4 Input | | O |
| | 9 | J99-J | | EOW #1 Input | | V |
| | 10 | J99-K | | EOW #2 Input | | G |
| | 11 | J99-L | | EOW #3 Input | | Y |
| | 12 | J99-M | | EOW #4 Input | | O |
| | 13 | J29-1 | 1 | Data #1 To Control | | V |
| | 14 | J29-2 | | Data #2 to Control | | G |
| | 15 | J29-3 | | Data #3 To Control | | Y |
| | 16 | J29-4 | | Data #4 To Control | | O |
| | 17 | J29-5 | | Copy #1 to Control | | V |
| | 18 | J29-6 | | Copy #2 To Control | | G |
| | 19 | J29-7 | | Copy #3 to Control | | Y |
| | 20 | J29-8 | | Copy #4 to Control | | O |
| | 21 | J29-9 | | EOW #1 To Control | | V |
| | 22 | J29-10 | | EOW #2 To Control | | G |
| | 23 | J29-11 | | EOW #3 To Control | | Y |
| | 24 | J29-12 | | EOW #4 to Control | | O |
| | 25 | | | | | |

NOTES: * #22 unless otherwise specified.

LIST 132

J34

TEST

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | J29-32 | 1 | Test Odd | 22 | Y |
| | 33 | J29-33 | 1 | Test Even | 22 | O |
| | 34 | | | | | |
| | 35 | | | | | |
| | 36 | | | | | |
| | 37 | | | | | |
| | 38 | | | | | |
| | 39 | | | | | |
| | 40 | | | | | |
| | 41 | | | | | |
| | 42 | | | | | |
| | 43 | | | | | |
| | 44 | +12V(A)-12 | 1 | +12V (A) Supply | 20 | R |
| | 45 | 0V(A)-12 | | 0V (A) Supply | | BK |
| | 46 | 0V(A)-12 | | 0V (A) Supply | | BK |
| | 47 | -20V(A)-12 | | -20V (A) Supply | | S |
| | 48 | -20V(A)-12 | | -20V (A) Supply | | S |
| | 49 | -85V(A)-12 | 1 | -85V (A) Supply | 20 | W/BK |
| | 50 | Rack | | Chassis Ground | 22 | BK |

NOTES: * #22 unless otherwise specified.

LIST 133

J35

20 BIT SR (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J101-J | 2 | Output F/F #1 Bit 20 Every | * | W/V |
| | 2 | J101-10 | | Output F/F #2 Bit 19 Every | | W/BL |
| | 3 | J101-I | | Output F/F #3 Bit 18 Every | | W/G |
| | 4 | J101-9 | | Output F/F #4 Bit 17 Every | | W/Y |
| | 5 | J101-H | | Output F/F #5 Bit 16 Every | | W/O |
| | 6 | J101-8 | | Output F/F #6 Bit 15 Every | | V |
| | 7 | J101-G | | Output F/F #7 Bit 14 Every | | BL |
| | 8 | J101-7 | | Output F/F #8 Bit 13 Every | | G |
| | 9 | J101-F | | Output F/F #9 Bit 12 Every | | Y |
| | 10 | J101-6 | | Output F/F #10 Bit 11 Every | | O |
| | 11 | J101-E | | Output F/F #11 Bit 10 Every | | W/V |
| | 12 | J101-5 | | Output F/F #12 Bit 9 Every | | W/BL |
| | 13 | J101-D | | Output F/F #13 Bit 8 Every | | W/G |
| | 14 | J101-4 | | Output F/F #14 Bit 7 Every | | W/Y |
| | 15 | J101-C | | Output F/F #15 Bit 6 Every | | W/O |
| | 16 | J101-3 | | Output F/F #16 Bit 5 Every | | V |
| | 17 | J101-B | 2 | Output F/F #17 Bit 4 Every | | BL |

NOTES: * #22 unless otherwise specified.

LIST 134

J35

20 BIT SR (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 18 | J101-2 | 2 | Output F/F #18 Bit #3 Every | 22 | G |
| | 19 | J101-A | 2 | Output F/F #19 Bit #2 Every | 22 | Y |
| | 20 | J101-1 | 2 | Output F/F #20 Bit #1 Every | 22 | O |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J31-34 | 2 | Core Shift | | V |
| | 34 | J36-34 | | Core Shift | | V |
| | 35 | | | | | |
| | 36 | J31-36 | | F/F Reset Trigger | | Y |
| | 36 | J36-36 | | F/F Reset Trigger | | Y |
| | 37 | | | | | |
| | 38 | J31-38 | | Read Gate | | W/Y |
| | 38 | J36-38 | 2 | Read Gate | | W/Y |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 135

J35
20 BIT SR (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 39 | | | | | |
| | 40 | | | Core Output | | |
| | 41 | J36-40 | | Core Input | | W/G |
| | 42 | -17V(B)-11 | 2 | +17V | 20 | W/S |
| | 43 | -17V(B)-11 | | -17V | | W/S |
| | 44 | +12V(A)-11 | | +12V | | R |
| | 45 | 0V(B)-11 | | 0V | | BK |
| | 46 | 0V(B)-11 | | 0V | | BK |
| | 47 | -20V(B)-11 | | -20V | | S |
| | 48 | -20V(B)-11 | | -20V | | S |
| | 49 | -85V(A)-11 | 2 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE NOTED

LIST 136

J36
20 BIT SR (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | J101-T | 2 | Output F/F #1 Bit 40 Every | * | W/V |
| | 2 | J101-20 | | Output F/F #2 Bit 39 Every | | W/BL |
| | 3 | J101-S | | Output F/F #3 Bit 38 Every | | W/G |
| | 4 | J101-19 | | Output F/F #4 Bit 37 Every | | W/Y |
| | 5 | J101-R | | Output F/F #5 Bit 36 Every | | W/O |
| | 6 | J101-18 | | Output F/F #6 Bit 35 Every | | V |
| | 7 | J101-Q | | Output F/F #7 Bit 34 Every | | BL |
| | 8 | J101-17 | | Output F/F #8 Bit 33 Every | | G |
| | 9 | J101-P | | Output F/F #9 Bit 32 Every | | Y |
| | 10 | J101-16 | | Output F/F #10 Bit 31 Every | | O |
| | 11 | J101-0 | | Output F/F #11 Bit 30 Every | | W/V |
| | 12 | J101-15 | | Output F/F #12 Bit 29 Every | | W/BL |
| | 13 | J101-N | | Output F/F #13 Bit 28 Every | | W/G |
| | 14 | J101-14 | | Output F/F #14 Bit 27 Every | | W/Y |
| | 15 | J101-M | | Output F/F #15 Bit 26 Every | | W/O |
| | 16 | J101-13 | | Output F/F #16 Bit 25 Every | | V |
| | 17 | J101-L | 2 | Output F/F #17 Bit 24 Every | | BL |

NOTES: (*) #22 unless otherwise specified

LIST 137

J36

20 BIT SR (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 18 | J101-12 | 2 | Output F/F #18 Bit #23 Every | * | G |
| | 19 | J101-K | 2 | Output F/F #19 Bit #22 Every | | Y |
| | 20 | J101-11 | 2 | Output F/F #20 Bit #21 Every | | O |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | J40-s | 2 | Core Shift | | V |
| | 34 | J35-34 | | Core Shift | | V |
| | 35 | | | | | |
| | 36 | J35-36 | | F/F Reset Trigger | | W |
| | 37 | | | | | |
| | 38 | J35-38 | 2 | Read Gate | | W/Y |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE SPECIFIED.

LIST 138

J36

20 BIT SR (76-7A)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 39 | | | | | |
| | 40 | J35-41 | | Core Output | 22 | W/B |
| | 41 | J31-40 | | Core Input | 22 | G |
| | 42 | -17V(B)-12 | 2 | -17V | 20 | W/S |
| | 43 | -17V(B)-12 | | -17V | | W/S |
| | 44 | +12V(A)-16 | | +12V | | R |
| | 45 | 0V(B)-12 | | 0V | | BK |
| | 46 | 0V(B)-12 | | 0V | | BR |
| | 47 | -20V(B)-12 | | -20V | | S |
| | 48 | -20V(B)-12 | | -20V | | S |
| | 49 | -85V(A)-16 | 2 | -85V | 20 | W/BK |
| | 50 | Rack | | Chassis Ground | 22 | BK |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE SPECIFIED.

LIST 139

J37

Power Supply

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | T902-1 | 1A | B Supply | 20 | W |
| | 2 | T902-1 | 1A | B Supply | 20 | W |
| | 3 | | | | | |
| | 4 | T902-2 | 1A | B Supply | 20 | BR |
| | 5 | T902-2 | 1A | B Supply | 20 | BR |
| | 6 | | | | | |
| | 7 | | | | | |
| | 8 | | | | | |
| | 9 | | | | | |
| | 10 | | | | | |
| | 11 | | | | | |
| | 12 | | | | | |
| | 13 | | | | | |
| | 14 | | | | | |
| | 15 | | | | | |
| | 16 | | | | | |
| | 17 | | | | | |
| | 18 | | | | | |
| | 19 | | | | | |
| | 20 | | | | | |
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |

NOTES:

LIST 140

J37

Power Supply

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | | | | | |
| | 33 | | | | | |
| | 34 | | | | | |
| | 35 | | | | | |
| | 36 | | | | | |
| | 37 | | | | | |
| | 38 | | | | | |
| | 39 | | | | | |
| | 40 | | | | | |
| | 41 | | | | | |
| | 42 | | | | | |
| | 43 | | | | | |
| | 44 | +12(A)-18 | 1 | +12V Power Supply | 20 | R |
| | 45 | OV(A)-17 | 1 | OV Power Supply | 20 | BK |
| | 46 | OV(A)-17 | 1 | OV Power Supply | 20 | BK |
| | 47 | -20(A)-20 | 1 | -20V(A) Power Supply | 20 | S |
| | 48 | -20(A)-20 | 1 | -20V(A) Power Supply | 20 | S |
| | 49 | -85V(A)-18 | 1 | -85V Power Supply | 20 | W/BK |
| | 50 | Rack | | Chassis Gnd | 22 | BK |

NOTES:

LIST 141

J40

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | A | J22-11 | | Bit #161 Output Odd | * | G |
| | B | J22-9 | | #162 | | BL |
| | C | J22-7 | | #163 | | V |
| | D | J22-5 | | #164 | | W/O |
| | E | J22-3 | | #165 | | W/Y |
| | F | J22-1 | | #166 | | W/G |
| | G | J23-19 | | #167 | | W/BL |
| | H | J23-17 | | #168 | | W/V |
| | J | J23-15 | | #169 | | O |
| | K | J23-13 | | #170 | | Y |
| | L | J23-11 | | #171 | | G |
| | M | J23-9 | | #172 | | BL |
| | N | J23-7 | | #173 | | V |
| | P | J23-5 | | #174 | | W/O |
| | Q | J23-3 | | #175 | | W/Y |
| | R | J23-1 | | Bit #176 Output Odd | | W/G |
| | S | J23-18 | | Bit #168 Output Even | | O |
| | T | J23-16 | | #169 | | Y |
| | U | J23-14 | | #170 | | G |
| | V | J23-12 | | #171 | | BL |
| | W | J23-10 | | #172 | | V |
| | X | J23-8 | | #173 | | W/O |
| | Y | J23-6 | | #174 | | W/Y |
| | Z | J23-4 | | #175 | | W/G |
| | a | J23-2 | | Bit #176 Output Even | | W/BL |
| | b | | | | | |

NOTES: All wires 22 gauge unless otherwise specified.

LIST 142

J40

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | c | | | | * | |
| | d | J22-15 | 1 | Bit #159 Output Odd | | O |
| | e | J22-13 | 1 | " #160 " " | | Y |
| | f | | | | | |
| | g | J29-22 | 2 | Every Reset | | Y |
| | h | J29-23 | 2 | Every Gate | | W/Y |
| | j | J33-35 | 2 | Odd Reset | | O |
| | k | J33-37 | 2 | Odd Gate | | W/O |
| | m | J33-36 | 2 | Even Reset | | G |
| | n | J33-38 | 2 | Even Gate | | W/G |
| | p | | | | | |
| | q | J29-14 | | Core Input | | BL |
| | r | J23-41 | | Core Output | | G |
| | s | J36-34 | | Core Drive Trigger | | V |
| | t | | | | | |
| | u | | | | | |
| | v | | | | | |
| | w | | | | | |
| | x | | | | | |
| | y | | | | | |
| | z | | | | | |
| | AA | | | | | |
| | AB | | | | | |

NOTES: ALL WIRES 22 GAUGE UNLESS OTHERWISE SPECIFIED.

LIST 143

J40

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | AC | | | | | |
| | AD | | | | | |
| | AE | | | | | |
| | AF | | | | | |
| | AG | | | | | |
| | AH | | | | | |
| | AJ | | | | | |
| | AK | | | | | |
| | AL | | | | | |
| | AM | | | | | |
| | AN | | | | | |
| | AP | | | | | |
| | AQ | | | | | |
| | AR | | | | | |
| | AS | | | | | |
| | AT | | | | | |
| | AU | | | | | |
| | AV | | | | | |
| | AW | | | | | |
| | AX | | | | | |
| | AY | | | | | |
| | AZ | | | | | |
| | BA | | | | | |
| | BB | | | | | |
| | BC | | | | | |

NOTES:

LIST 144

J40

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | BD | | | | | |
| | BE | | | | | |
| | BF | J30-46 | 1 | -20V(C) Power Control | 22 | S |
| | BG | J30-44 | 1 | -17V(C) Power Control | 22 | W/S |
| | BH | | | | | |
| | BJ | | | | | |
| | BK | +12V(A)-20 | 2 | +12V(A)Bus Tie | 18 | R |
| | BL | -85V(A)-20 | 2 | -85V(A)Bus Tie | 18 | W/BK |
| | BM | 0V(A)-20 | 2 | 0V Bus Tie | 12 | BK |
| | BN | -20V(D)-39 | 2 | -20V(D) Bus Tie | 18 | S |
| | BP | | | | | |
| | BQ | SW1-2 | | AC Control | 20 | Y |
| | BR | Contactor-X | | AC Control | 20 | G |
| | BS | | | | | |
| | BT | | | | | |
| | BU | -17V(D)-39 | 2 | -17V(D) Bus Tie | 16 | W/S |
| | BV | -17V(D)-40 | 2 | -17V(D) Bus Tie | 16 | W/S |
| | BW | | | | | |
| | BX | I1-2 | jumper | Ø1 Lights | 22 | G |
| | BY | I2-2 | jumper | Ø2 Lights | 22 | Y |
| | BZ | I3-2 | jumper | Ø3 Lights | 22 | O |
| | CA | Contactor-E | jumper | AC Ø2 Switched | 14 | BR |
| | CB | Contactor-F | jumper | AC Ø3 Switched | 14 | BR |
| | CC | Contactor-H | jumper | AC Ø2 Switched | 14 | BR |

NOTES:

LIST 145

J40

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | CD | J98-D-E | jumper | AC Common | 12 | W |
| | CD | J98-D-E | jumper | AC Common | 12 | W |
| | CE | Contactor-I | jumper | AC Ø3 Switched | 14 | BR |

NOTES:

LIST 146

P40

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | A | J105-2 | | Bit 161 Output Odd | * | G |
| | B | J105-B | | 162 | | BL |
| | C | J105-3 | | 163 | | V |
| | D | J105-C | | 164 | | W/O |
| | E | J105-4 | | 165 | | W/Y |
| | F | J105-D | | 166 | | W/G |
| | G | J105-5 | | 167 | | W/BL |
| | H | J105-E | | 168 | | W/V |
| | J | J105-6 | | 169 | | O |
| | K | J105-F | | 170 | | Y |
| | L | J105-7 | | 171 | | G |
| | M | J105-G | | 172 | | BL |
| | N | J105-8 | | 173 | | V |
| | P | J105-H | | 174 | | W/O |
| | Q | J105-9 | | 175 | | W/Y |
| | R | J 105-I | | Bit 176 Output Odd | | W/G |
| | S | J109-1 | | Bit 168 Output Even | | O |
| | T | J109-A | | 169 Output Even | | V |
| | U | J109-2 | | 170 | | G |
| | V | J109-B | | 171 | | BL |
| | W | J109-3 | | 172 | | V |
| | X | J109-C | | 173 | | W/O |
| | Y | J109-4 | | 174 | | W/Y |
| | Z | J109-D | | 175 | | W/G |
| | a | J109-5 | | Bit 176 Output Even | | W/BL |

NOTES:
All wires #22 gauge unless otherwise noted.

LIST 147

P40

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | b | | | | * | |
| | c | | | | | |
| | d | J113-21 | 5 | Bit 159 Output Odd | | O |
| | e | J113-22 | | " 160 " " | | Y |
| | f | | | | | |
| | g | J5-36 | | Every Reset | | Y |
| | h | J5-38 | | Every Gate | | W/Y |
| | j | J16-35 | | Odd Reset | | O |
| | k | J16-37 | | Odd Gate | | W/O |
| | m | J16-36 | | Even Reset | | G |
| | n | J16-38 | | Even Gate | | W/G |
| | p | | | | | |
| | q | J4-41 | | Core Input | | BL |
| | r | J13-40 | | Core Output | | G |
| | s | J13-34 | 5 | Core Drive (Trigger) | | V |
| | t | | | | | |
| | u | | | | | |
| | v | | | | | |
| | w | | | | | |
| | x | | | | | |
| | y | | | | | |
| | z | | | | | |
| | AA | | | | | |
| | AB | | | | | |
| | AC | | | | | |

NOTES: * All wires #22 gauge unless otherwise noted.

LIST 148

P40

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | AD | | | | * | |
| | AE | | | | | |
| | AF | | | | | |
| | AG | | | | | |
| | AH | | | | | |
| | AJ | | | | | |
| | AK | | | | | |
| | AL | | | | | |
| | AM | | | | | |
| | AN | | | | | |
| | AP | | | | | |
| | AQ | | | | | |
| | AR | | | | | |
| | AS | | | | | |
| | AT | | | | | |
| | AU | | | | | |
| | AV | | | | | |
| | AW | | | | | |
| | AX | | | | | |
| | AY | | | | | |
| | AZ | | | | | |
| | BA | | | | | |
| | BB | | | | | |
| | BC | | | | | |
| | BD | | | | | |

NOTES: *All wires #22 gauge unless otherwise noted.

LIST 149

P40

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | BE | | | | * | |
| | BF | -20V(C)-2 | 5 | -20V (C) Power Control | 22 | S |
| | BG | -17V(C)-2 | 5 | -17V (C) Power Control | 22 | W/S |
| | BH | | | | | |
| | BJ | | | | | |
| | BK | +12V(A)-40 | 5 | +12V(A)Bus Tie | 18 | R |
| | BL | -85V(A)-40 | 5 | -85V(A)Bus Tie | 18 | W/BK |
| | BM | 0V(C)-2 | 5 | 0V Bus Tie | 16 | BK |
| | BM | 0V(D)-12 | 5 | 0V Bus Tie | 16 | BK |
| | BN | -20V(D)-12 | 5 | -20V(D)Bus Tie | 18 | S |
| | BP | | | | | |
| | BQ | SW2-1 | 5 | AC Control | 20 | Y |
| | BR | SW2-2 | 5 | AC Control | 20 | G |
| | BS | | | | | |
| | BT | | | | | |
| | BU | -17V(D)-11 | 5 | -17V(D) Bus Tie | #16 | W/S |
| | BV | -17V(D)-12 | 5 | -17V(D) Bus Tie | #16 | W/S |
| | BW | | | | | |
| | BX | I4-2 | 5 | AC Ø1 Lights | #22 | G |
| | BY | I5-2 | 5 | AC Ø2 Lights | 22 | Y |
| | BZ | I6-2 | 5 | AC Ø3 Lights | 22 | O |
| | CA | T902-2 (C Supply) | 5 | AC Ø2 Switched | 14 | BR |
| | CB | T902-2 (D Supply) | 5 | AC Ø3 Switched | 14 | BR |
| | CC | T902-2 (C Supply) | 5 | AC Ø2 Switched | 14 | BR |
| | CD | T902-1 (C Supply) | 5 | AC Common | 12 | W |
| | CD | T902-1 (D Supply) | 5 | AC Common | 12 | W |

NOTES: *All wires #22 gauge unless otherwise noted.

LIST 150

P40

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | CE | T902-2 (D Supply) | 5 | AC Ø3 Switched | 14 | BR |

NOTES:

LIST 151

+12V (A) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | J29-44 | 1 | +12V Control | 22 | R |
| | 3 | J20-44 | 2 | +12V 10 Bit SR | 20 | R |
| | 4 | J21-44 | 2 | +12V | 20 | R |
| | 5 | J22-44 | 1 | +12V | 20 | R |
| | 6 | J23-44 | 1 | +12V | 20 | R |
| | 7 | J24-44 | 2 | +12V | 20 | R |
| | 8 | J25-44 | 2 | +12V | 20 | R |
| | 9 | J26-44 | 1 | +12V | 20 | R |
| | 10 | J27-44 | 1 | +12V 10 Bit SR | 20 | R |
| | 11 | J35-44 | 2 | +12V 20 Bit SR | 20 | R |
| | 12 | J34-44 | 1 | +12V Test | 22 | R |
| | 13 | J33-44 | 1 | +12V 10 Bit SR | 20 | R |
| | 14 | J32-44 | 2 | +12V 20 Bit SR | 20 | R |
| | 15 | J31-44 | 2 | +12V 20 Bit SR | 20 | R |
| | 16 | J36-44 | 2 | +12V 20 Bit SR | 20 | R |
| | 17 | | | | | |
| | 18 | J37-44 | 1 | +12V Power Supply | 20 | R |
| | 19 | J30-34 | 1 | +12V Power Control | 22 | R |
| | 20 | J40-BK | 1 | +12V Bus Tie | 18 | R |

NOTES: Terminals 1 thru 20 are on one rack and 21 thru 40 are on second rack as shown in detail on drawing D76W1A.

LIST 152

+12V(A) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 21 | | | | * | |
| | 22 | | | | | |
| | 23 | J1-44 | 4 | +12V-20 Bit SR | 20 | R |
| | 24 | J2-44 | 4 | +12V " | 20 | |
| | 25 | J3-44 | 3 | +12V " | 20 | |
| | 26 | J4-44 | 3 | +12V " | 20 | |
| | 27 | J5-44 | 4 | +12V " | 20 | |
| | 28 | J6-44 | 4 | +12V " | 20 | |
| | 29 | J7-44 | 3 | +12V " | 20 | |
| | 30 | J8-44 | 3 | +12V " | 20 | |
| | 31 | J9-44 | 4 | +12-10 Bit SR | 20 | |
| | 32 | J10-44 | 4 | +12 " | 20 | |
| | 33 | J11-44 | 3 | +12 " | 20 | |
| | 34 | J12-44 | 3 | +12V " | 20 | |
| | 35 | J13-44 | 4 | +12V " | 20 | |
| | 36 | J14-44 | 4 | +12V " | 20 | |
| | 37 | J15-44 | 3 | +12V " | 20 | |
| | 38 | J16-44 | 3 | +12V " | 20 | R |
| | 39 | | | | | |
| | 40 | P40-BK | 5 | +12V Bus Tie | 18 | R |

NOTES:
Terminals 1 through 20 are on one rack, and 21 through 40 are on second or shown on dwg.D76W1A.

LIST 153

## 0V (A) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | J98-F | 2 | 0V (Signal Ground) | 18 | BK |
| | 3 | J99-Y | 2 | 0V (Signal Ground) | 20 | BK |
| | 4 | | | | | |
| | 5 | | | | | |
| | 6 | | | | | |
| | 7 | | | | | |
| | 8 | J30-16 | | 0V Power Control | 20 | BK |
| | 8 | J30-17 | | 0V Power Control | 20 | BK |
| | 9 | | | | | |
| | 10 | J29-45 | 1 | 0V Control | 20 | BK |
| | 10 | J29-46 | 1 | 0V Control | 20 | BK |
| | 11 | | | | | |
| | 12 | J34-45 | 1 | 0V Test | 20 | BK |
| | 12 | J34-46 | 1 | 0V Test | 20 | BK |
| | 13 | J33-45 | 1 | 0V 10 Bit SR | 20 | BK |
| | 13 | J33-46 | 1 | 0V 10 Bit SR | 20 | BK |
| | 14 | J32-45 | 2 | 0V 20 Bit SR | 20 | BK |
| | 14 | J32-46 | 2 | 0V 20 Bit SR | 20 | BK |
| | 15 | J31-45 | 2 | 0V 20 Bit SR | 20 | BK |
| | 15 | J31-46 | 2 | 0V 20 Bit SR | 20 | BK |
| | 16 | | | | | |
| | 17 | J37-45 | 1 | 0V Power Supply | 20 | BK |
| | 17 | J37-46 | 1 | 0V Power Supply | 20 | BK |
| | 18 | 0V(B)-2 | 2 | 0V Bus Tie | 18 | BK |
| | 18 | 0V(B)-2 | 2 | 0V Bus Tie | 18 | BK |
| | 19 | | | | | |
| | 20 | J40-BM | 2 | 0V Bus Tie | 12 | BK |

NOTES:

LIST 154

## -20V (A) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | | | | | |
| | 3 | J29-47 | 1 | -20V Control | 20 | S |
| | 3 | J29-48 | 1 | -20V Control | 20 | S |
| | 4 | | | | | |
| | 5 | | | | | |
| | 6 | | | | | |
| | 7 | | | | | |
| | 8 | | | | | |
| | 9 | | | | | |
| | 10 | | | | | |
| | 11 | | | | | |
| | 12 | J34-47 | 1 | -20V Test | 20 | S |
| | 12 | J34-48 | 1 | -20V Test | 20 | S |
| | 13 | | | | | |
| | 14 | | | | | |
| | 15 | | | | | |
| | 16 | | | | | |
| | 17 | | | | | |
| | 18 | | | | | |
| | 19 | J30-36 | 1 | -20V (A) Power Control | 22 | S |
| | 20 | J37-47 | 1 | -20V (A) Power Supply | 20 | S |
| | 20 | J37-48 | 1 | -20V (A) Power Supply | 20 | S |

NOTES:

LIST 155

-85V (A) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | J29-49 | 1 | -85V Control | 22 | W/BK |
| | 3 | J20-49 | 2 | -85V 10 Bit SR | 20 | W/BK |
| | 4 | J21-49 | 2 | -85V | 20 | W/BK |
| | 5 | J22-49 | 1 | -85V | 20 | W/BK |
| | 6 | J23-49 | 1 | -85V | 20 | W/BK |
| | 7 | J24-49 | 2 | -85V | 20 | W/BK |
| | 8 | J25-49 | 2 | -85V | 20 | W/BK |
| | 9 | J26-49 | 1 | -85V | 20 | W/BK |
| | 10 | J27-49 | 1 | -85V 10 Bit SR | 20 | W/BK |
| | 11 | J35-49 | 2 | -85V 20 Bit SR | 20 | W/BK |
| | 12 | J34-49 | 1 | -85V Test | 20 | W/BK |
| | 13 | J33-49 | 1 | -85V 10 Bit SR | 20 | W/BK |
| | 14 | J32-49 | 2 | -85V 20 Bit SR | 20 | W/BK |
| | 15 | J31-49 | 2 | -85V 20 Bit SR | 20 | W/BK |
| | 16 | J36-49 | 2 | -85V 20 Bit SR | 20 | W/BK |
| | 17 | | | | | |
| | 18 | J37-49 | 1 | -85V Power Supply | 20 | W/BK |
| | 19 | J30-38 | 1 | -85V Power Control | 22 | W/BK |
| | 20 | J40-BL | 1 | Bus Tie | 18 | W/BK |

NOTES: Terminals 1 thru 20 are on one rack and 21 thru 40 are on second rack as shown in detail on drawing D76W1A

LIST 156

-85V(A) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | J1-49 | 4 | -85V - 20 Bit SR | 20 | W/BK |
| | 24 | J2-49 | 4 | -85V " | 20 | |
| | 25 | J3-49 | 3 | -85V " | 20 | |
| | 26 | J4-49 | 3 | -85V " | 20 | |
| | 27 | J5-49 | 4 | -85V " | 20 | |
| | 28 | J6-49 | 4 | -85V " | 20 | |
| | 29 | J7-49 | 3 | -85V " | 20 | |
| | 30 | J8-49 | 3 | -85V " | 20 | |
| | 31 | J9-49 | 4 | -85V - 10 Bit SR | 20 | |
| | 32 | J10-49 | 4 | -85V " | 20 | W/BK |
| | 33 | J11-49 | 3 | -85V " | 20 | W/BK |
| | 34 | J12-49 | 3 | -85V " | 20 | W/BK |
| | 35 | J13-49 | 4 | -85V " | 20 | W/BK |
| | 36 | J14-49 | 4 | -85V " | 20 | W/BK |
| | 37 | J15-49 | 3 | -85V " | 20 | W/BK |
| | 38 | J16-49 | 3 | -85V " | 20 | W/BK |
| | 39 | | | | | |
| | 40 | P40-BL | 5 | -85V Bus Tie | 18 | W/BK |

NOTES: Terminals 1 through 20 are on one rack and 21 through 40 are on second rack or shown in detail on drawing D76W1A.

LIST 157

## -17V (B) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | | | | | |
| | 3 | J20-42 | 2 | -17V 10 Bit SR | 20 | W/S |
| | 3 | J20-43 | 2 | -17V | 20 | W/S |
| | 4 | J21-42 | 2 | -17V | 20 | W/S |
| | 4 | J21-43 | 2 | -17V | 20 | W/S |
| | 5 | J22-42 | 1 | -17V | 20 | W/S |
| | 5 | J22-43 | 1 | -17V | 20 | W/S |
| | 6 | J23-42 | 1 | -17V | 20 | W/S |
| | 6 | J23-43 | 1 | -17V | 20 | W/S |
| | 7 | J24-42 | 2 | -17V | 20 | W/S |
| | 7 | J24-43 | 2 | -17V | 20 | W/S |
| | 8 | J25-42 | 2 | -17V | 20 | W/S |
| | 8 | J25-43 | 2 | -17V | 20 | W/S |
| | 9 | J26-42 | 1 | -17V | 20 | W/S |
| | 9 | J26-43 | 1 | -17V | 20 | W/S |
| | 10 | J27-42 | 1 | -17V | 20 | W/S |
| | 10 | J27-43 | 1 | -17V 10 Bit SR | 20 | W/S |
| | 11 | J35-42 | 2 | -17V 20 Bit SR | 20 | W/S |
| | 11 | J35-43 | 2 | -17V 20 Bit SR | 20 | W/S |
| | 12 | J30-40 | 1 | -17V (B) Power Control | 22 | W/S |
| | 12 | J36-42 | 2 | -17V 20 Bit SR | 20 | W/S |
| | 12 | J36-43 | 2 | -17V 20 Bit SR | 20 | W/S |

NOTES:

LIST 158

## 0V (B) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | 0V(A)-18 | 2 | 0V Bus Tie | 18 | BK |
| | 2 | 0V(A)-18 | 2 | 0V Bus Tie | 18 | BK |
| | 3 | J20-45 | 2 | 0V 10 Bit SR | 20 | BK |
| | 3 | J20-46 | 2 | 0V | 20 | BK |
| | 4 | J21-45 | 2 | 0V | 20 | BK |
| | 4 | J21-46 | 2 | 0V | 20 | BK |
| | 5 | J22-45 | 1 | 0V | 20 | BK |
| | 5 | J22-46 | 1 | 0V | 20 | BK |
| | 6 | J23-45 | 1 | 0V | 20 | BK |
| | 6 | J23-46 | 1 | 0V | 20 | BK |
| | 7 | J24-45 | 2 | 0V | 20 | BK |
| | 7 | J24-46 | 2 | 0V | 20 | BK |
| | 8 | J25-45 | 2 | 0V | 20 | BK |
| | 8 | J25-46 | 2 | 0V | 20 | BK |
| | 9 | J26-45 | 1 | 0V | 20 | BK |
| | 9 | J26-46 | 1 | 0V | 20 | BK |
| | 10 | J27-45 | 1 | 0V | 20 | BK |
| | 10 | J27-46 | 1 | 0V 10 Bit SR | 20 | BK |
| | 11 | J35-45 | 2 | 0V 20 Bit SR | 20 | BK |
| | 11 | J35-46 | 2 | 0V 20 Bit SR | 20 | BK |
| | 12 | J36-45 | 2 | 0V 20 Bit SR | 20 | BK |
| | 12 | J36-46 | 2 | 0V 20 Bit SR | 20 | BK |

NOTES:

LIST 159

-20V (B) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | | | | | |
| | 3 | J20-47 | 2 | -20V 10 Bit SR | 20 | S |
| | 3 | J20-48 | 2 | -20V | 20 | S |
| | 4 | J21-47 | 2 | -20V | 20 | S |
| | 4 | J21-48 | 2 | -20V | 20 | S |
| | 5 | J22-47 | 1 | -20V | 20 | S |
| | 5 | J22-48 | 1 | -20V | 20 | S |
| | 6 | J23-47 | 1 | -20V | 20 | S |
| | 6 | J23-48 | 1 | -20V | 20 | S |
| | 7 | J24-47 | 2 | -20V | 20 | S |
| | 7 | J24-48 | 2 | -20V | 20 | S |
| | 8 | J25-47 | 2 | -20V | 20 | S |
| | 8 | J25-48 | 2 | -20V | 20 | S |
| | 9 | J26-47 | 1 | -20V | 20 | S |
| | 9 | J26-48 | 1 | -20V | 20 | S |
| | 10 | J27-47 | 1 | -20V | 20 | S |
| | 10 | J27-48 | 1 | -20V 10 Bit SR | 20 | S |
| | 11 | J35-47 | 2 | -20V 20 Bit SR | 20 | S |
| | 11 | J35-48 | 2 | -20V 20 Bit SR | 20 | S |
| | 12 | J30-42 | 1 | -20V (B) Power Supply | 22 | S |
| | 12 | J36-47 | 2 | -20V 20 Bit SR | 20 | S |
| | 12 | J36-48 | 2 | -20V 20 Bit SR | 20 | S |

NOTES:

LIST 160

0V (C) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | P40-BM | 5 | 0V Bus Tie | 16 | BK |
| | 3 | J1-45 | 4 | 0V 20 Bit SR | 20 | BK |
| | 3 | J1-46 | 4 | 0V | 20 | BK |
| | 4 | J2-45 | 4 | 0V | 20 | BK |
| | 4 | J2-46 | 4 | 0V | 20 | BK |
| | 5 | J3-45 | 3 | 0V | 20 | BK |
| | 5 | J3-46 | 3 | 0V | 20 | BK |
| | 6 | J4-45 | 3 | 0V | 20 | BK |
| | 6 | J4-46 | 3 | 0V | 20 | BK |
| | 7 | J5-45 | 4 | 0V | 20 | BK |
| | 7 | J5-46 | 4 | 0V | 20 | BK |
| | 8 | J6-45 | 4 | 0V | 20 | BK |
| | 8 | J6-46 | 4 | 0V | 20 | BK |
| | 9 | J7-45 | 3 | 0V | 20 | BK |
| | 9 | J7-46 | 3 | 0V | 20 | BK |
| | 10 | J8-45 | 3 | 0V | 20 | BK |
| | 10 | J8-46 | 3 | 0V 20 Bit SR | 20 | BK |
| | 11 | J9-45 | 4 | 0V 10 Bit SR | 20 | BK |
| | 11 | J9-46 | 4 | 0V 10 Bit SR | 20 | BK |
| | 12 | J10-45 | 4 | 0V 10 Bit SR | 20 | BK |
| | 12 | J10-46 | 4 | 0V 10 Bit SR | 20 | BK |

NOTES:

LIST 161

## -17V (C) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | P40-BG | 5 | -17V(C) Power Control | 22 | W/S |
| | 3 | J1-42 | 4 | -17V 20 Bit SR | 20 | W/S |
| | 3 | J1-43 | 4 | -17V | 20 | W/S |
| | 4 | J2-42 | 4 | -17V | 20 | W/S |
| | 4 | J2-43 | 4 | -17V | 20 | W/S |
| | 5 | J3-42 | 3 | -17V | 20 | W/S |
| | 5 | J3-43 | 3 | -17V | 20 | W/S |
| | 6 | J4-42 | 3 | -17V | 20 | W/S |
| | 6 | J4-43 | 3 | -17V | 20 | W/S |
| | 7 | J5-42 | 4 | -17V | 20 | W/S |
| | 7 | J5-43 | 4 | -17V | 20 | W/S |
| | 8 | J6-42 | 4 | -17V | 20 | W/S |
| | 8 | J6-43 | 4 | -17V | 20 | W/S |
| | 9 | J7-42 | 3 | -17V | 20 | W/S |
| | 9 | J7-43 | 3 | -17V | 20 | W/S |
| | 10 | J8-42 | 3 | -17V | 20 | W/S |
| | 10 | J8-43 | 3 | -17V 20 Bit SR | 20 | W/S |
| | 11 | J9-42 | 4 | -17V 10 Bit SR | 20 | W/S |
| | 11 | J9-43 | 4 | -17V 10 Bit SR | 20 | W/S |
| | 12 | J10-42 | 4 | -17V 10 Bit SR | 20 | W/S |
| | 12 | J10-43 | 4 | -17V 10 Bit SR | 20 | W/S |

NOTES:

LIST 162

## -20V (C) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | P40-BF | 5 | -20V(C) Power Control | 22 | S |
| | 3 | J1-47 | 4 | -20V 20 Bit SR | 20 | S |
| | 3 | J1-48 | 4 | -20V | 20 | S |
| | 4 | J2-47 | 4 | -20V | 20 | S |
| | 4 | J2-48 | 4 | -20V | 20 | S |
| | 5 | J3-47 | 3 | -20V | 20 | S |
| | 5 | J3-48 | 3 | -20V | 20 | S |
| | 6 | J4-47 | 3 | -20V | 20 | S |
| | 6 | J4-48 | 3 | -20V | 20 | S |
| | 7 | J4-47 | 4 | -20V | 20 | S |
| | 7 | J4-48 | 4 | -20V | 20 | S |
| | 8 | J6-47 | 4 | -20V | 20 | S |
| | 8 | J6-48 | 4 | -20V | 20 | S |
| | 9 | J7-47 | 3 | -20V | 20 | S |
| | 9 | J7-48 | 3 | -20V | 20 | S |
| | 10 | J8-47 | 3 | -20V | 20 | S |
| | 10 | J8-48 | 3 | -20V 20 Bit SR | 20 | S |
| | 11 | J9-47 | 4 | -20V 10 Bit SR | 20 | S |
| | 11 | J9-48 | 4 | -20V 10 Bit SR | 20 | S |
| | 12 | J10-47 | 4 | -20V 10 Bit SR | 20 | S |
| | 12 | J10-48 | 4 | -20V 10 Bit SR | 20 | S |

NOTES:

LIST 163

## 0V (D) Bus

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | | | | | |
| | 3 | J11-45 | 3 | 0V 10 Bit SR | 20 | BK |
| | 3 | J11-46 | 3 | 0V 10 Bit SR | 20 | BK |
| | 4 | J12-45 | 3 | 0V 10 Bit SR | 20 | BK |
| | 4 | J12-46 | 3 | 0V 10 Bit SR | 20 | BK |
| | 5 | J13-45 | 4 | 0V 10 Bit SR | 20 | BK |
| | 5 | J13-46 | 4 | 0V 10 Bit SR | 20 | BK |
| | 6 | J14-45 | 4 | 0V 10 Bit SR | 20 | BK |
| | 6 | J14-46 | 4 | 0V 10 Bit SR | 20 | BK |
| | 7 | J15-45 | 3 | 0V 10 Bit SR | 20 | BK |
| | 7 | J15-46 | 3 | 0V 10 Bit SR | 20 | BK |
| | 8 | J16-45 | 3 | 0V 10 Bit SR | 20 | BK |
| | 8 | J16-46 | 3 | 0V 10 Bit SR | 20 | BK |
| | 9 | | | | | |
| | 10 | | | | | |
| | 11 | | | | | |
| | 12 | P40-BM | 5 | 0V Bus Tie | 16 | BK |

NOTES:

LIST 164

## -17V (D) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | | | | | |
| | 3 | J11-42 | 3 | -17V 10 Bit SR | 20 | W/S |
| | 3 | J11-43 | 3 | -17V 10 Bit SR | 20 | W/S |
| | 4 | J12-42 | 3 | -17V 10 Bit SR | 20 | W/S |
| | 4 | J12-43 | 3 | -17V 10 Bit SR | 20 | W/S |
| | 5 | J13-42 | 4 | -17V 10 Bit SR | 20 | W/S |
| | 5 | J13-43 | 4 | -17V 10 Bit SR | 20 | W/S |
| | 6 | J14-42 | 4 | -17V 10 Bit SR | 20 | W/S |
| | 6 | J14-43 | 4 | -17V 10 Bit SR | 20 | W/S |
| | 7 | J15-42 | 3 | -17V 10 Bit SR | 20 | W/S |
| | 7 | J15-43 | 3 | -17V 10 Bit SR | 20 | W/S |
| | 8 | J16-42 | 3 | -17V 10 Bit SR | 20 | W/S |
| | 8 | J16-43 | 3 | -17V 10 Bit SR | 20 | W/S |
| | 9 | | | | | |
| | 10 | | | | | |
| | 11 | P40-BU | 5 | -17V Bus Tie | 16 | W/S |
| | 12 | P40-BV | 5 | -17V Bus Tie | 16 | W/S |

NOTES: TERMINALS 1 - 12 ARE ON THE POWER SUPPLY CHASSIS AND TERMINALS 21 - 40 ARE ON THE BUS BAR IN THE OTHER RACK.

LIST 165

## -17V(D) Bus

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | J29-41 | 1 | -17V(D) Control | 20 | W/S |
| | 32 | J29-41 | 1 | -17V(D) Control | 20 | W/S |
| | 33 | | | | | |
| | 34 | J33-42 | 1 | -17V 10 Bit SR | 20 | W/S |
| | 34 | J33-43 | 1 | -17V 10 Bit SR | 20 | W/S |
| | 35 | J32-42 | 2 | -17V 20 Bit SR | 20 | W/S |
| | 35 | J32-43 | 2 | -17V 20 Bit SR | 20 | W/S |
| | 36 | J31-42 | 2 | -17V 20 Bit SR | 20 | W/S |
| | 36 | J31-43 | 2 | -17V 20 Bit SR | 20 | W/S |
| | 37 | | | | | |
| | 38 | J30-48 | 1 | -17V Power Control | 22 | W/S |
| | 39 | J40-BU | 1 | -17V Bus Tie | #16 | W/S |
| | 40 | J40-BV | 1 | -17V Bus Tie | #16 | W/S |

NOTES: TERMINALS 1 - 12 ARE ON THE POWER SUPPLY CHASSIS AND TERMINALS 21 - 40 ARE ON THE BUS BAR IN THE OTHER RACK.

LIST 166

## -20V (D) BUS

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 1 | | | | | |
| | 2 | | | | | |
| | 3 | J11-47 | 3 | -20V 10 Bit SR | 20 | S |
| | 3 | J11-48 | 3 | -20V 10 Bit SR | 20 | S |
| | 4 | J12-47 | 3 | -20V 10 Bit SR | 20 | S |
| | 4 | J12-48 | 3 | -20V 10 Bit SR | 20 | S |
| | 5 | J13-47 | 4 | -20V 10 Bit SR | 20 | S |
| | 5 | J13-48 | 4 | -20V 10 Bit SR | 20 | S |
| | 6 | J14-47 | 4 | -20V 10 Bit SR | 20 | S |
| | 6 | J14-48 | 4 | -20V 10 Bit SR | 20 | S |
| | 7 | J15-47 | 3 | -20V 10 Bit SR | 20 | S |
| | 7 | J15-48 | 3 | -20V 10 Bit SR | 20 | S |
| | 8 | J16-47 | 3 | -20V 10 Bit SR | 20 | S |
| | 8 | J16-48 | 3 | -20V 10 Bit SR | 20 | S |
| | 9 | | | | | |
| | 10 | | | | | |
| | 11 | | | | | |
| | 12 | P40-BN | 5 | -20V Bus Tie | 18 | S |

NOTES: TERMINALS 1 - 12 ARE ON THE PS CHASSIS AND TERMINALS 21 - 40 ARE ON THE BUS BAR IN THE OTHER RACK

LIST 167

## -20V(D) BUS

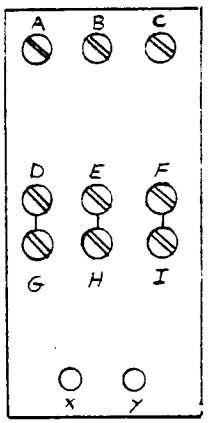
| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | 21 | | | | | |
| | 22 | | | | | |
| | 23 | | | | | |
| | 24 | | | | | |
| | 25 | | | | | |
| | 26 | | | | | |
| | 27 | | | | | |
| | 28 | | | | | |
| | 29 | | | | | |
| | 30 | | | | | |
| | 31 | | | | | |
| | 32 | J29-43 | 1 | -20V(D) Control | 20 | S |
| | 33 | | | | | |
| | 34 | J33-47 | 1 | -20V 10Bit SR | 20 | S |
| | 34 | J33-48 | 1 | -20V " | 20 | S |
| | 35 | J32-47 | 2 | -20V 20 Bit SR | 20 | S |
| | 35 | J32-48 | 2 | -20V " | 20 | S |
| | 36 | J31-47 | 2 | -20V 20 Bit SR | 20 | S |
| | 36 | J31-48 | 2 | -20V " | 20 | S |
| | 37 | | | | | |
| | 38 | J30-49 | 1 | -20V(D) Power Control | 22 | S |
| | 39 | J40-BN | 2 | -20V(D) Bus Tie | 18 | S |
| | 40 | | | | | |

NOTES: Terminals 1 through 20 are on one rack and 21 through 40 are on second rack or shown in detail on drawing D76W1A.

LIST 168

## CONTACTOR

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | A | F1-2 | Jumper | AC Ø1 Fused | 12 | W/BR |
| | B | F2-2 | | AC Ø2 Fused | 12 | W/BR |
| | C | F3-2 | | AC Ø3 Fused | 12 | W/BR |
| | D | T902-2 (B Supply) | | AC Ø1 Switched | 12 | BR |
| | E | J40-CA | | AC Ø2 Switched | 14 | BR |
| | E | TB1-2 | | AC Ø2 Switched | 16 | BR |
| | F | J40-CB | | AC Ø3 Switched | 14 | BR |
| | G | I1-2 | | AC Ø1 Switched | 22 | G |
| | G | J30-13 | | AC Ø1 "(Power Cont.) | 20 | G |
| | H | J40-CC | | AC Ø2 Switched | 14 | BR |
| | H | I2-2 | | AC Ø2 Switched | 22 | Y |
| | I | J40-CE | | AC Ø3 Switched | 14 | BR |
| | I | I3-2 | | AC Ø3 Switched | 22 | O |
| | X | J40-BR | | AC Control | 20 | G |
| | Y | TB1-1 | Jumper | AC Common | 20 | W |

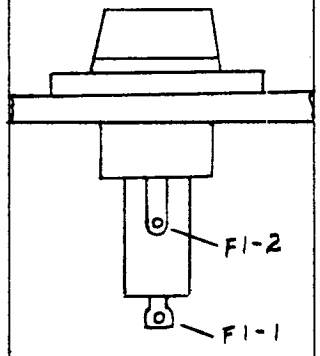



NOTES:

LIST 169

## F1, F2, F3

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | F1-1 | J98-A | | AC Ø1 | 12 | BR |
| | F1-2 | Contactor-A | | AC Ø1 Fused | 12 | W/BR |
| | F1-2 | J30-7 | | AC Ø1 Fused | 20 | W/BR |
| | F2-1 | J98-B | | ACØ2 | 12 | BR |
| | F2-2 | Contactor-B | | AC Ø2 Fused | 12 | W/BR |
| | F3-1 | J98-C | | AC Ø3 | 12 | BR |
| | F3-2 | Contactor-C | | AC Ø3 Fused | 12 | W/BR |




NOTES:

LIST 170

## I1, I2, I3

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | I1-1 | I2-1 | | AC Common | 22 | W |
| | | J98-D-E | | | 22 | W |
| | I1-2 | Contactor-G | | AC Ø1 Switched | 22 | G |
| | | J40-BX | | Ø1 Lights | 22 | G |
| | I2-1 | I1-1 | | AC Common | 22 | W |
| | | I3-1 | | | 22 | W |
| | I2-2 | Contactor-H | | AC Ø2 Switched | 22 | Y |
| | | J40-BY | | Ø2 Lights | 22 | Y |
| | I3-1 | I2-1 | | AC Common | 22 | W |
| | I3-2 | Contactor-I | | AC Ø3 Switched | 22 | O |
| | | J40-BZ | | Ø3 Lights | 22 | O |

NOTES:

LIST 171

TB1

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | TB1-1 | J30-5 | 1A | AC Common | 20 | W |
| | TB1-1 | J98-D-E | Jumper | AC Common | 16 | W |
| | TB1-1 | Contactor Y | | AC Common | 20 | W |
| | TB1-1 | Blower | | | -- | - |
| | TB1-2 | Contactor E | | AC Ø Switched | 16 | BR |
| | TB1-2 | Blower | Jumper | | -- | -- |

NOTES:

LIST 172

I4, I5, I6

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | I4-1 | I5-1 | jumper | AC Common | 22 | W |
| | I4-2 | P40-BX | 5 | AC Ø1 Lights | 22 | G |
| | I5-1 | I4-1 | jumper | AC Common | 22 | W |
| | | I6-1 | jumper | AC Common | 22 | W |
| | I5-2 | P40-BY | 5 | AC Ø2 Lights | 22 | Y |
| | I6-1 | I5-1 | jumper | AC Common | 22 | W |
| | | TB2-1 | | AC Common | 22 | W |
| | I6-2 | P40-BZ | 5 | AC Ø3 Lights | 22 | O |

NOTES:

LIST 173

TB 2

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | TB2-1 | T902-1 (D Supply) | | AC Common | 16 | W |
| | | I6-1 Blower | | AC Common | 22 | W |
| | TB2-2 | T902-2 (D Supply) | | AC Ø3 Switched | 16 | BR |
| | | Blower | | | -- | -- |

NOTES:

LIST 174

T902 (B)

(B Supply)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | T902-1 (B Supply) | J37-1 | 1A | AC Common | 20 | W |
| | | J37-2 | 1A | AC Common | 20 | W |
| | | J98-D,E | 1A | AC Common | 12 | W |
| | T902-2 (B Supply) | J37-4 | 1A | AC Ø1 Switched | 20 | BR |
| | | J37-5 | 1A | AC Ø1 Switched | 20 | BR |
| | | Contactor-D | 1A | AC Ø1 Switched | 12 | BR |

NOTES:

LIST 175

T902 (C)

(C Supply)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | T902-1 (C Supply) | P40-CD | | AC Common | 12 | W |
| | T902-2 (D Supply) | P40-CA | | AC Ø2 Switched | 14 | BR |
| | | P40-CC | | AC Ø2 Switched | 14 | BR |

NOTES:

LIST 176

T902 (D)

(D Supply)

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | T902-1 (D Supply) | P40-CD | | AC Common | 12 | W |
| | | TB2-1 | | AC Common | 16 | W |
| | T902-2 (D Supply) | P40-CB | | AC Ø3 Switched | 14 | BR |
| | (D Supply) | P40-CE | | AC Ø3 Switched | 14 | BR |
| | | TB2-2 | | AC Ø3 Switched | 16 | BR |

NOTES:

LIST 177

SW 1

| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | SW1-1 | J30-10 | | AC Control | 20 | G |
| | SW1-2 | J40-BQ | | AC Control | 20 | Y |

NOTES:

LIST 178

SW 2

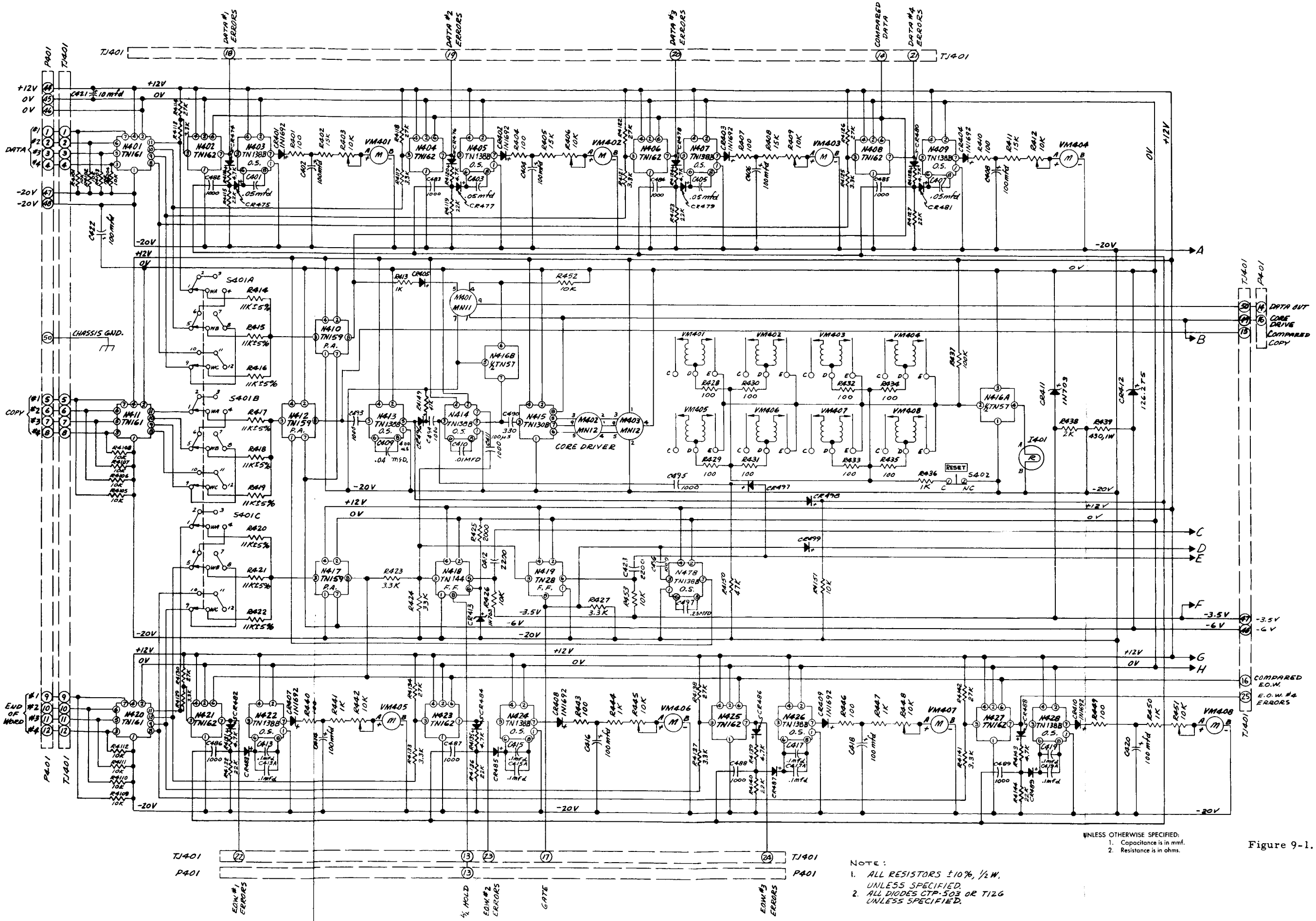
| WIRE NO. | TERMINAL | DESTINATION | CABLE | IDENTIFICATION | WIRE SIZE | COLOR |
|---|---|---|---|---|---|---|
| | SW2-1 | P40-BQ | | AC Control | | Y |
| | SW2-2 | P40-BR | | AC Control | | G |

NOTES:

LIST 179

# CHAPTER IX

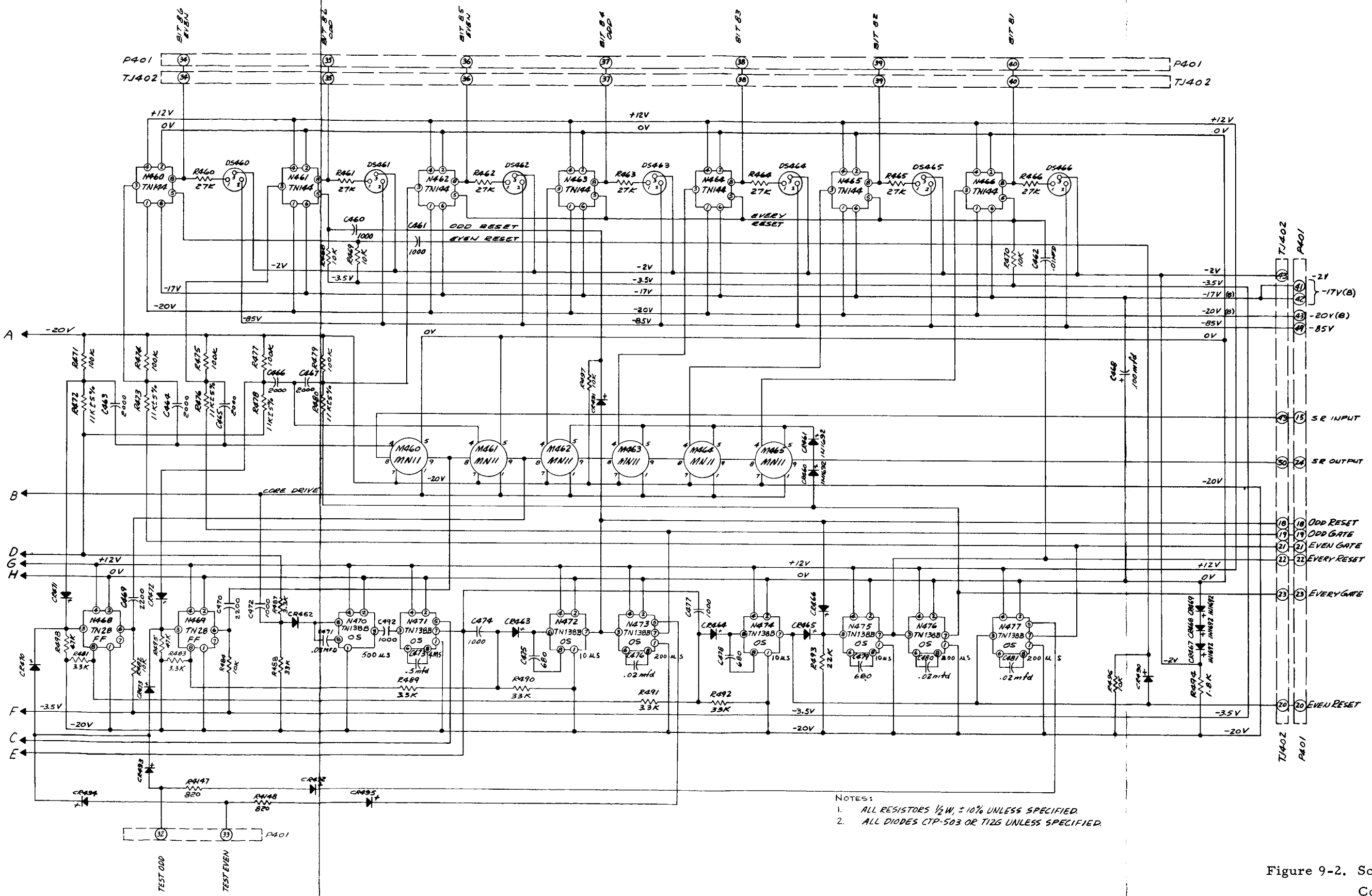
# SCHEMATICS AND DIAGRAMS




UNLESS OTHERWISE SPECIFIED:
1. Capacitance is in mmf.
2. Resistance is in ohms.

NOTE:
1. ALL RESISTORS ±10%, ½W, UNLESS SPECIFIED.
2. ALL DIODES CTP-503 OR T126 UNLESS SPECIFIED.

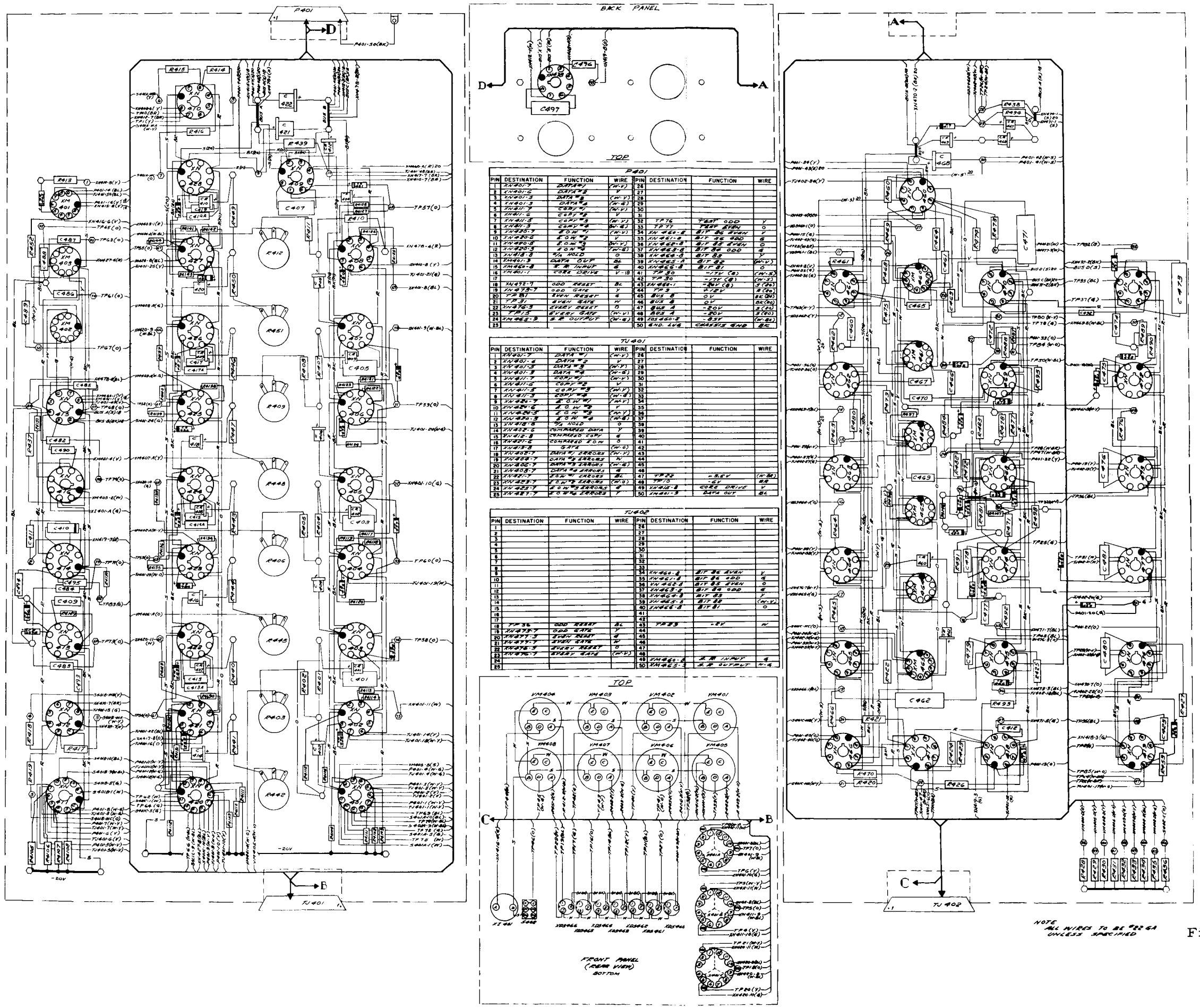
Figure 9-1. Schematic Control Chassis Dwg. #76S4A Sheet 1 of 2




NOTES:

1. ALL RESISTORS ½W, ±10% UNLESS SPECIFIED.
2. ALL DIODES CTP-503 OR T126 UNLESS SPECIFIED.

Figure 9-2. Schematic, Control Chassis, Dwg. #D76S4A Sheet 2 of 2




P401

| PIN | DESTINATION | FUNCTION | WIRE | PIN | DESTINATION | FUNCTION | WIRE |
|---|---|---|---|---|---|---|---|
| 1 | XN401-7 | DATA #1 | (W-Y) | 26 | | | |
| 2 | XN401-6 | DATA #2 | Y | 27 | | | |
| 3 | XN401-3 | DATA #3 | (W-Y) | 28 | | | |
| 4 | XN401-3 | DATA #4 | (W-G) | 29 | | | |
| 5 | XN411-7 | COMP #1 | (W-Y) | 30 | | | |
| 6 | XN411-6 | COMP #2 | Y | 31 | | | |
| 7 | XN411-3 | COMP #3 | (W-Y) | 32 | TP76 | TEST ODD | Y |
| 8 | XN411-3 | COMP #4 | (W-G) | 33 | TP77 | TEST EVEN | O |
| 9 | XN420-7 | E.O.W #1 | (W-Y) | 34 | XN462-8 | BIT B6 EVEN | Y |
| 10 | XN420-6 | E.O.W #2 | Y | 35 | XN461-8 | BIT B6 ODD | G |
| 11 | XN420-3 | E.O.W #3 | (W-Y) | 36 | XN462-8 | BIT B5 EVEN | O |
| 12 | XN420-3 | E.O.W #4 | (W-G) | 37 | XN463-8 | BIT B5 ODD | G |
| 13 | XN418-3 | S/A HOLD | O | 38 | XN464-8 | BIT B3 | Y |
| 14 | XN401-3 | DATA OUT | BL | 39 | XN463-8 | BIT B2 | (W-Y) |
| 15 | XN420-8 | X.R INPUT | G | 40 | XN465-8 | BIT B1 | O |
| 16 | XN401-1 | CORE DRIVE | Y-18 | 41 | TP30 | -17V (G) | (W-S) |
| 17 | | | | 42 | TP30 | -17V (G) | (W-S) |
| 18 | XN472-7 | ODD RESET | BL | 43 | XN464-1 | -30V (G) | S (90) |
| 19 | XN473-7 | ODD GATE | Y | 44 | TP3 | +.2V | S (20) |
| 20 | TP81 | EVEN RESET | G | 45 | B13 B | 0V | BL (90) |
| 21 | TP31 | EVEN GATE | W | 46 | B13 A | 0V | BL (90) |
| 22 | XN478-3 | EVERY RESET | O | 47 | B12 B | -20V | S (90) |
| 23 | TP15 | EVERY GATE | (W-V) | 48 | B12 A | -20V | S (90) |
| 24 | XN465-3 | X.R OUTPUT | (W-G) | 49 | 105460-2 | -83V | (W-BL) |
| 25 | | | | 50 | GND. LUG | CHASSIS GND | BL |

TU401

| PIN | DESTINATION | FUNCTION | WIRE | PIN | DESTINATION | FUNCTION | WIRE |
|---|---|---|---|---|---|---|---|
| 1 | XN401-7 | DATA #1 | (W-Y) | 26 | | | |
| 2 | XN401-6 | DATA #2 | Y | 27 | | | |
| 3 | XN401-3 | DATA #3 | (W-Y) | 28 | | | |
| 4 | XN401-3 | DATA #4 | (W-G) | 29 | | | |
| 5 | XN411-7 | COMP #1 | (W-Y) | 30 | | | |
| 6 | XN411-6 | COMP #2 | Y | 31 | | | |
| 7 | XN411-3 | COMP #3 | (W-Y) | 32 | | | |
| 8 | XN411-3 | COMP #4 | (W-G) | 33 | | | |
| 9 | XN420-7 | E.O.W #1 | (W-Y) | 34 | | | |
| 10 | XN420-6 | E.O.W #2 | Y | 35 | | | |
| 11 | XN420-3 | E.O.W #3 | (W-Y) | 36 | | | |
| 12 | XN420-3 | E.O.W #4 | (W-G) | 37 | | | |
| 13 | XN418-3 | S/A HOLD | O | 38 | | | |
| 14 | XN402-6 | COMPARED DATA | Y | 39 | | | |
| 15 | XN412-8 | COMPARED COMP | G | 40 | | | |
| 16 | XN401-2 | COMPARED E.O.W | O | 41 | | | |
| 17 | XN413-8 | GATE | (W-O) | 42 | | | |
| 18 | XN402-7 | DATA #1 ERRORS | (W-Y) | 43 | | | |
| 19 | XN403-7 | DATA #2 ERRORS | W-W | 44 | | | |
| 20 | XN402-7 | DATA #3 ERRORS | (W-G) | 45 | | | |
| 21 | XN403-7 | DATA #4 ERRORS | G | 46 | | | |
| 22 | XN402-7 | P/A #1 ERRORS | BL | 47 | TP22 | -9.5V | (W-BL) |
| 23 | XN403-7 | E.O.W #1 ERRORS | (W-O) | 48 | TP10 | -6V | BR |
| 24 | XN425-7 | E.O.W #2 ERRORS | G | 49 | XN416-8 | CORE DRIVE | V |
| 25 | XN427-7 | E.O.W #3 ERRORS | Y | 50 | XN401-3 | DATA OUT | BL |

TU402

| PIN | DESTINATION | FUNCTION | WIRE | PIN | DESTINATION | FUNCTION | WIRE |
|---|---|---|---|---|---|---|---|
| 1 | | | | 26 | | | |
| 2 | | | | 27 | | | |
| 3 | | | | 28 | | | |
| 4 | | | | 29 | | | |
| 5 | | | | 30 | | | |
| 6 | | | | 31 | | | |
| 7 | | | | 32 | | | |
| 8 | | | | 33 | | | |
| 9 | | | | 34 | XN460-8 | BIT B6 EVEN | V |
| 10 | | | | 35 | XN461-8 | BIT B6 ODD | G |
| 11 | | | | 36 | XN462-8 | BIT B5 EVEN | O |
| 12 | | | | 37 | XN463-8 | BIT B5 ODD | G |
| 13 | | | | 38 | XN464-8 | BIT B3 | Y |
| 14 | | | | 39 | XN465-8 | BIT B2 | (W-Y) |
| 15 | | | | 40 | XN466-8 | BIT B1 | O |
| 16 | | | | 41 | | | |
| 17 | | | | 42 | | | |
| 18 | TP36 | ODD RESET | BL | 43 | TP23 | -8V | W |
| 19 | XN473-7 | ODD GATE | Y | 44 | | | |
| 20 | XN477-7 | EVEN RESET | G | 45 | | | |
| 21 | XN477-7 | EVEN GATE | W | 46 | | | |
| 22 | XN476-3 | EVERY RESET | O | 47 | | | |
| 23 | XN476-7 | EVERY GATE | (W-V) | 48 | | | |
| 24 | | | | 49 | XN466-8 | X.R INPUT | G |
| 25 | | | | 50 | XN465-3 | X.R OUTPUT | W-G |

Figure 9-3. Wiring Diagram Control Chassis Dwg. #76W4A

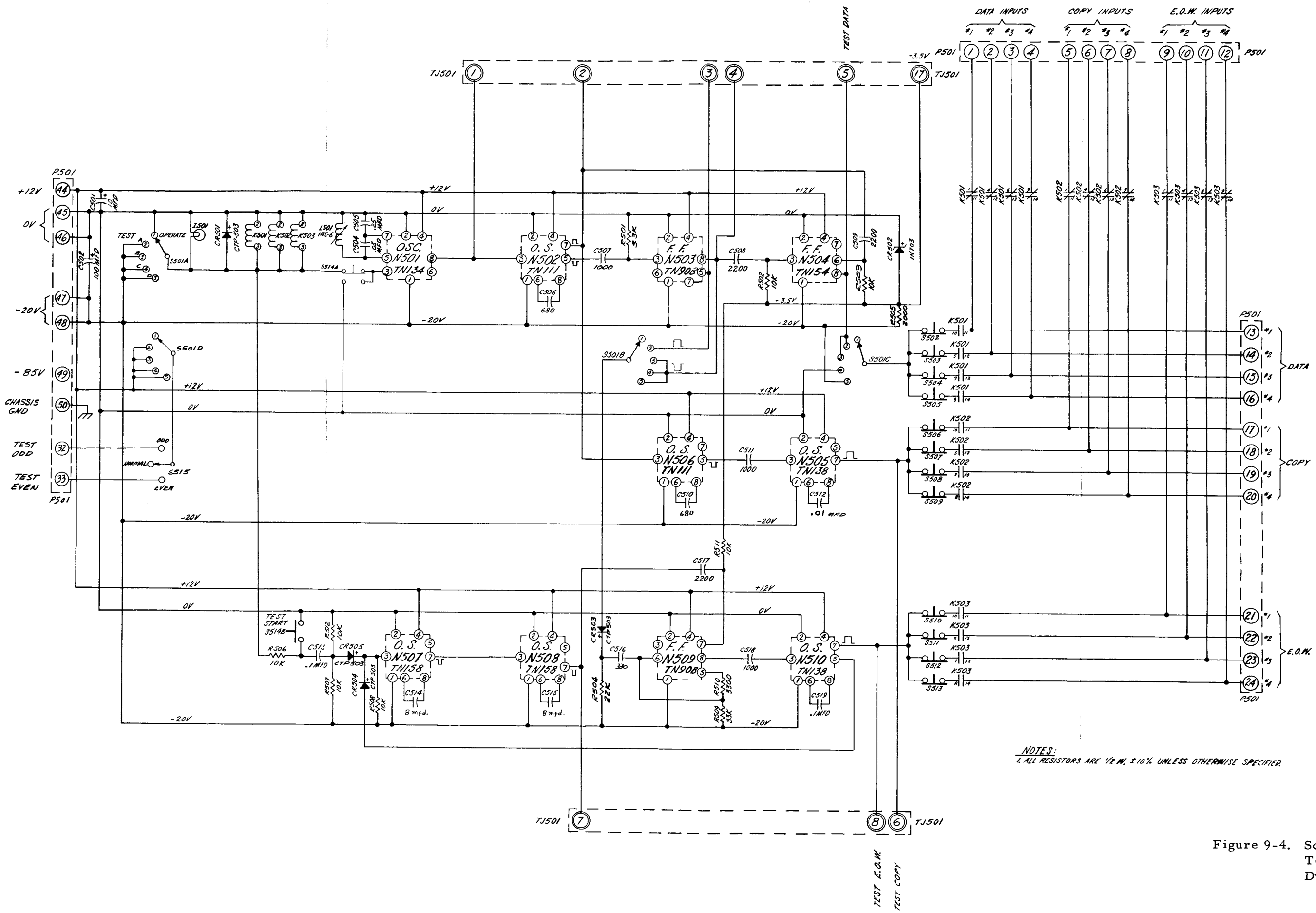
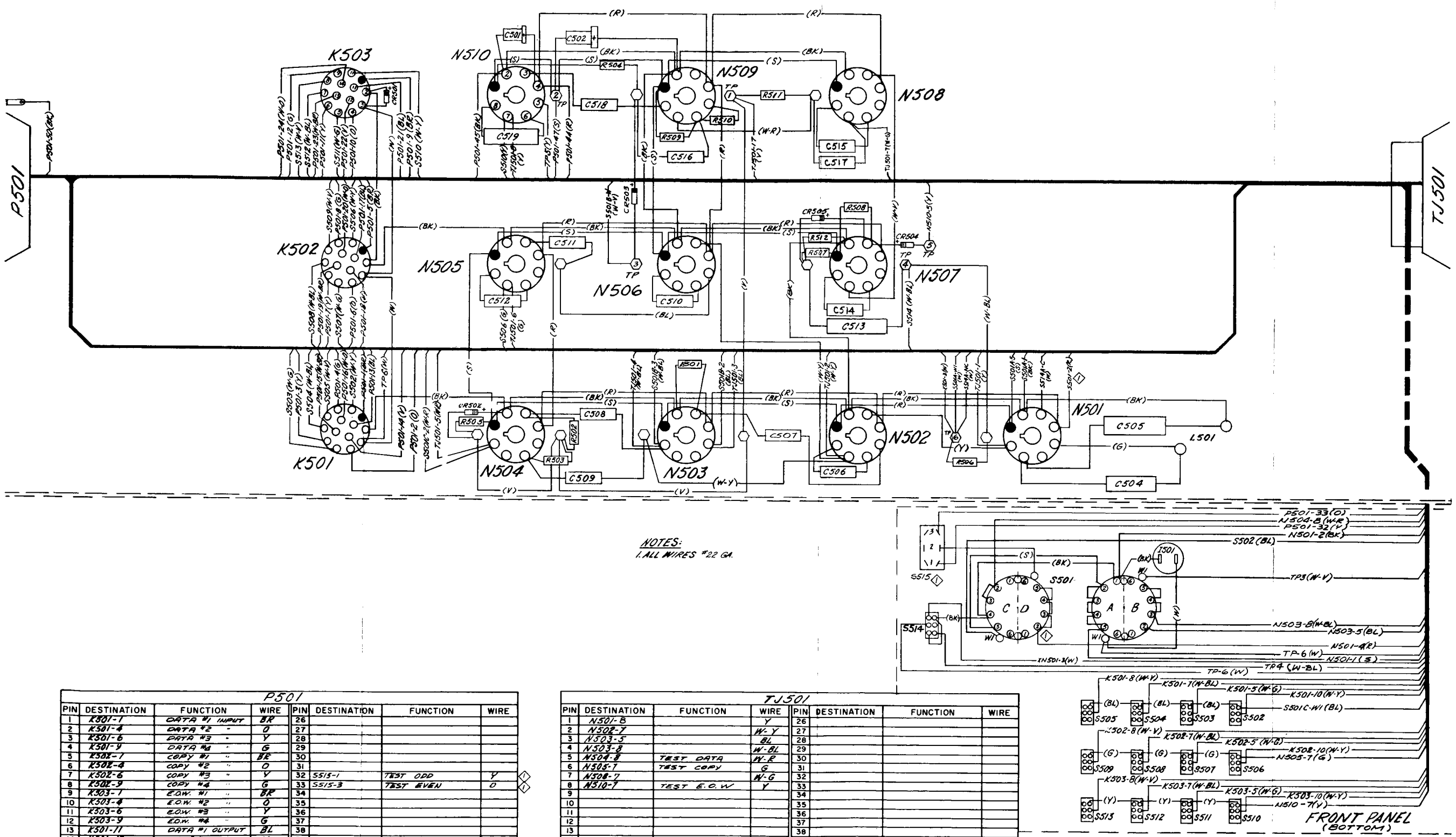
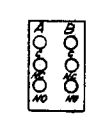



Figure 9-4. Schematic
Test Chassis
Dwg. #76S5A




NOTES:
1. ALL WIRES #22 GA.




TYPICAL ORIENTATION OF S502 THRU S514

P501

| PIN | DESTINATION | FUNCTION | WIRE | PIN | DESTINATION | FUNCTION | WIRE |
|---|---|---|---|---|---|---|---|
| 1 | K501-1 | DATA #1 INPUT | BR | 26 | | | |
| 2 | K501-4 | DATA #2 " | O | 27 | | | |
| 3 | K501-6 | DATA #3 " | Y | 28 | | | |
| 4 | K501-9 | DATA #4 " | G | 29 | | | |
| 5 | K502-1 | COPY #1 " | BR | 30 | | | |
| 6 | K502-4 | COPY #2 " | O | 31 | | | |
| 7 | K502-6 | COPY #3 " | Y | 32 | S515-1 | TEST ODD | Y |
| 8 | K502-9 | COPY #4 " | G | 33 | S515-3 | TEST EVEN | O |
| 9 | K503-1 | E.O.W. #1 " | BR | 34 | | | |
| 10 | K503-4 | E.O.W. #2 " | O | 35 | | | |
| 11 | K503-6 | E.O.W. #3 " | Y | 36 | | | |
| 12 | K503-9 | E.O.W. #4 " | G | 37 | | | |
| 13 | K501-11 | DATA #1 OUTPUT | BL | 38 | | | |
| 14 | K501-12 | DATA #2 " | V | 39 | | | |
| 15 | K501-13 | DATA #3 " | W-BR | 40 | | | |
| 16 | K501-14 | DATA #4 " | W-O | 41 | | | |
| 17 | K502-11 | COPY #1 " | BL | 42 | | | |
| 18 | K502-12 | COPY #2 " | V | 43 | | | |
| 19 | K502-13 | COPY #3 " | W-BR | 44 | N510-4 | +12V | R |
| 20 | K502-14 | COPY #4 " | W-O | 45 | N510-2 | 0V | BK |
| 21 | K503-11 | E.O.W. #1 " | BL | 46 | | | |
| 22 | K503-12 | E.O.W. #2 " | V | 47 | TP2 | -20V | S |
| 23 | K503-13 | E.O.W. #3 " | W-BR | 48 | | | |
| 24 | K503-14 | E.O.W. #4 " | W-O | 49 | | -85V | |
| 25 | | | | 50 | GND LUG | CHASSIS GND | BK |

TJ501

| PIN | DESTINATION | FUNCTION | WIRE | PIN | DESTINATION | FUNCTION | WIRE |
|---|---|---|---|---|---|---|---|
| 1 | N501-8 | | Y | 26 | | | |
| 2 | N502-7 | | W-Y | 27 | | | |
| 3 | N503-5 | | BL | 28 | | | |
| 4 | N503-8 | | W-BL | 29 | | | |
| 5 | N504-8 | TEST DATA | W-R | 30 | | | |
| 6 | N505-7 | TEST COPY | G | 31 | | | |
| 7 | N508-7 | | W-G | 32 | | | |
| 8 | N510-7 | TEST E.O.W | Y | 33 | | | |
| 9 | | | | 34 | | | |
| 10 | | | | 35 | | | |
| 11 | | | | 36 | | | |
| 12 | | | | 37 | | | |
| 13 | | | | 38 | | | |
| 14 | | | | 39 | | | |
| 15 | | | | 40 | | | |
| 16 | | | | 41 | | | |
| 17 | TP1 | -3.5V TEST | V | 42 | | | |
| 18 | | | | 43 | | | |
| 19 | | | | 44 | | | |
| 20 | | | | 45 | | | |
| 21 | | | | 46 | | | |
| 22 | | | | 47 | | | |
| 23 | | | | 48 | | | |
| 24 | | | | 49 | | | |
| 25 | | | | 50 | | | |

Figure 9-5. Wiring Diagram
Test Chassis
Dwg. #76W5A

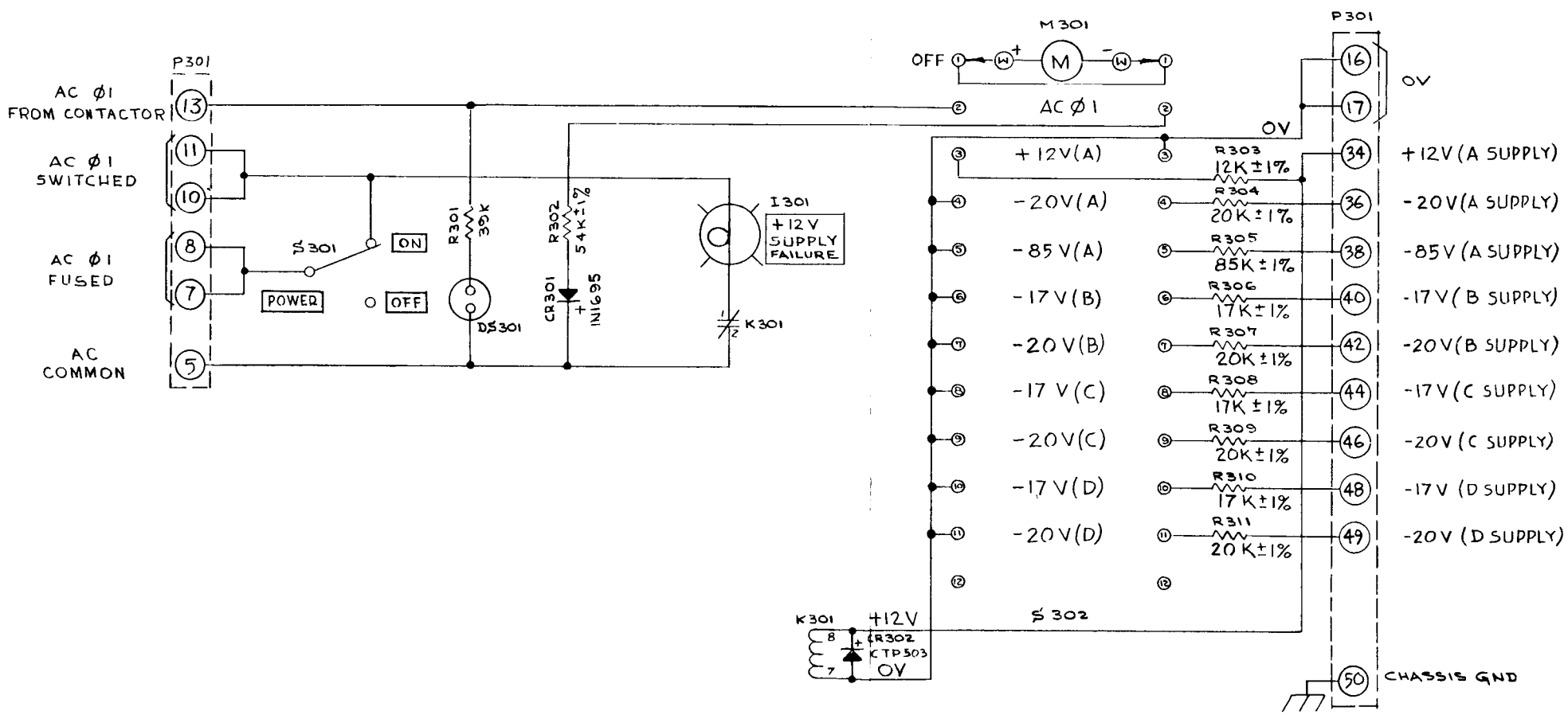
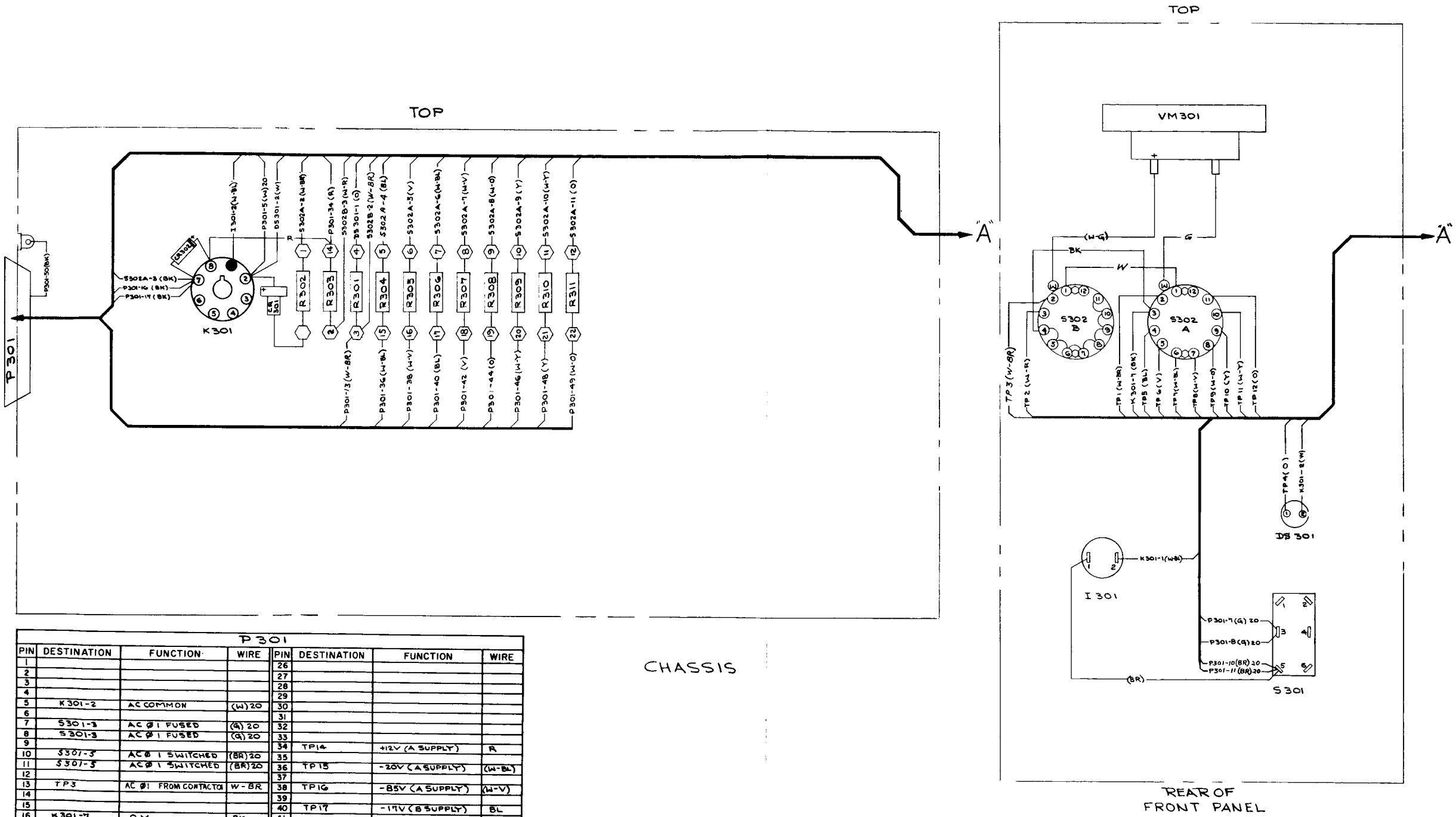



Figure 9-6. Schematic
Power Control Chassis
Dwg. #76S3A




| P301 | | | | | | | |
|---|---|---|---|---|---|---|---|
| PIN | DESTINATION | FUNCTION | WIRE | PIN | DESTINATION | FUNCTION | WIRE |
| 1 | | | | 26 | | | |
| 2 | | | | 27 | | | |
| 3 | | | | 28 | | | |
| 4 | | | | 29 | | | |
| 5 | K301-2 | AC COMMON | (W)20 | 30 | | | |
| 6 | | | | 31 | | | |
| 7 | S301-3 | AC Ø1 FUSED | (G) 20 | 32 | | | |
| 8 | S301-3 | AC Ø1 FUSED | (G) 20 | 33 | | | |
| 9 | | | | 34 | TP14 | +12V (A SUPPLY) | R |
| 10 | S301-5 | AC Ø1 SWITCHED | (BR)20 | 35 | | | |
| 11 | S301-5 | AC Ø1 SWITCHED | (BR)20 | 36 | TP15 | -20V (A SUPPLY) | (W-BL) |
| 12 | | | | 37 | | | |
| 13 | TP3 | AC Ø1 FROM CONTACTOR | W-BR | 38 | TP16 | -85V (A SUPPLY) | (W-V) |
| 14 | | | | 39 | | | |
| 15 | | | | 40 | TP17 | -17V (B SUPPLY) | BL |
| 16 | K301-7 | 0 V | BK | 41 | | | |
| 17 | K301-7 | 0 V | BK | 42 | TP18 | -20V (B SUPPLY) | V |
| 18 | | | | 43 | | | |
| 19 | | | | 44 | TP19 | -17V (C SUPPLY) | O |
| 20 | | | | 45 | | | |
| 21 | | | | 46 | TP20 | -20V (C SUPPLY) | (W-Y) |
| 22 | | | | 47 | | | |
| 23 | | | | 48 | TP21 | -17V (D SUPPLY) | Y |
| 24 | | | | 49 | TP22 | -20V (D SUPPLY) | (W-O) |
| 25 | | | | 50 | GND LUG | CHASSIS GND | BK |

CHASSIS

NOTES:
1. ALL WIRES TO BE #22 GA
UNLESS OTHERWISE SPECIFIED

Figure 9-7. Wiring Diagram
Power Control Chassis
Dwg. #76W3A

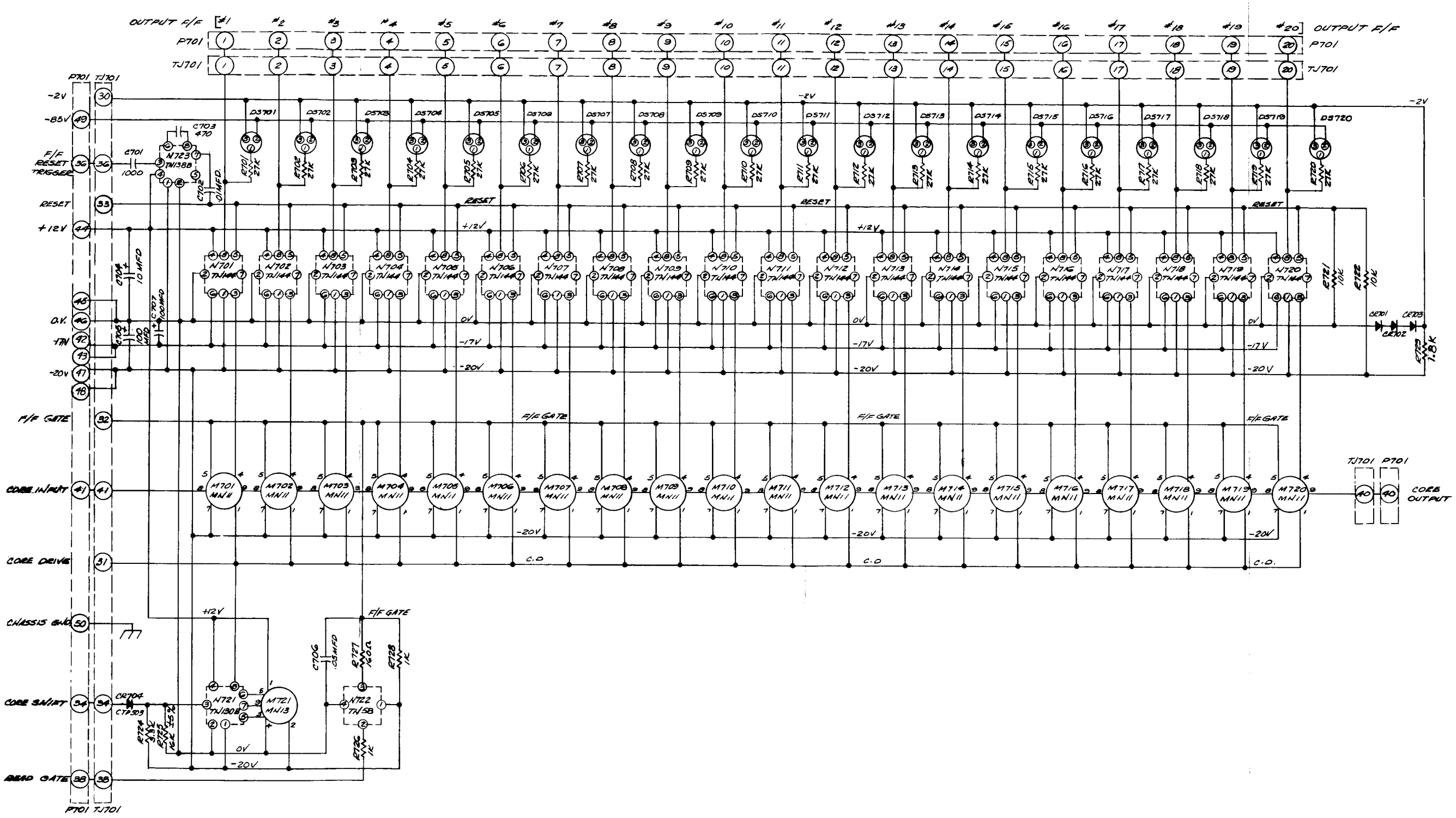
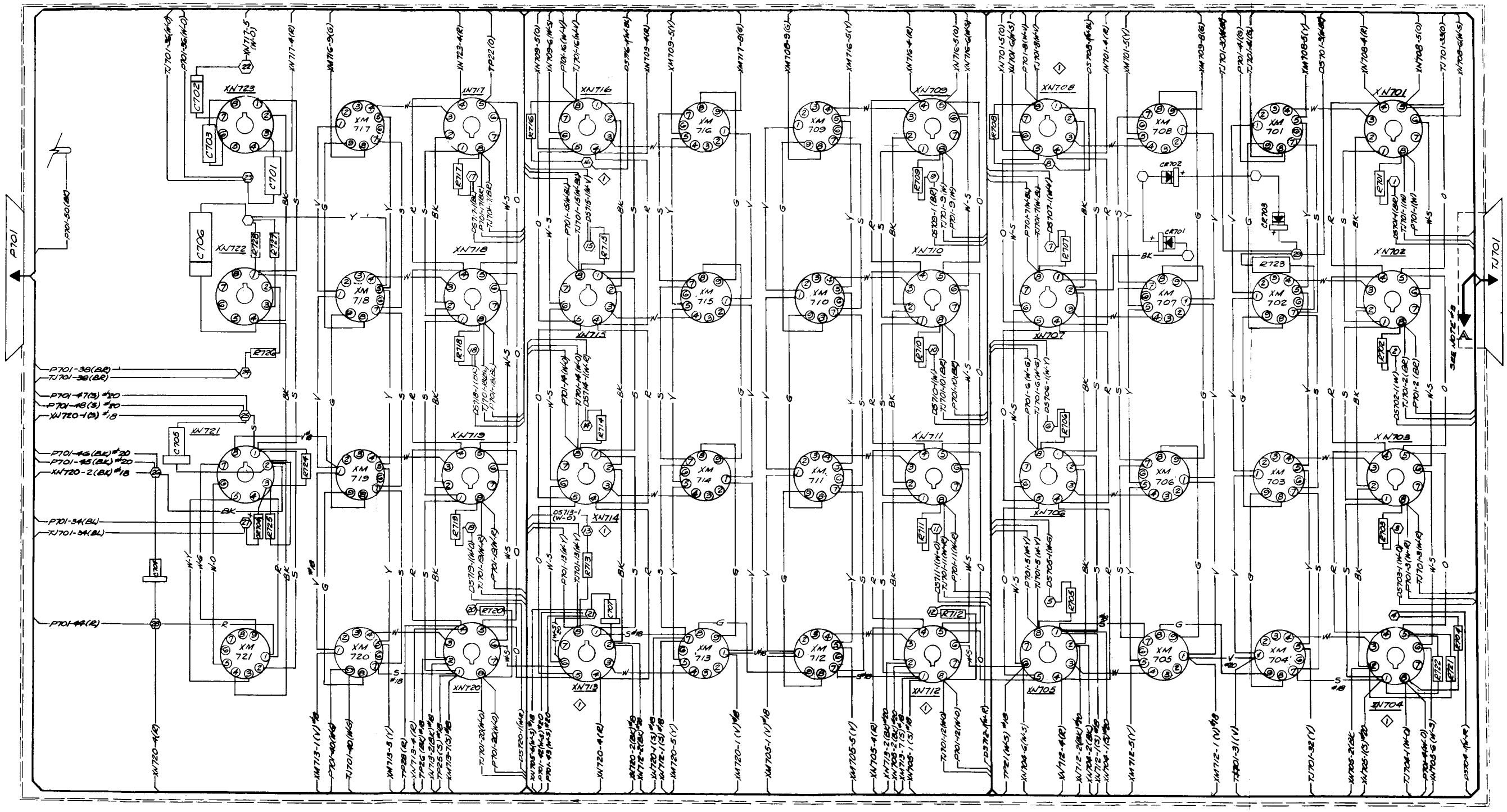



Figure 9-8. Schematic
20 Bit Shift Register Chassis
Dwg. #76S7A

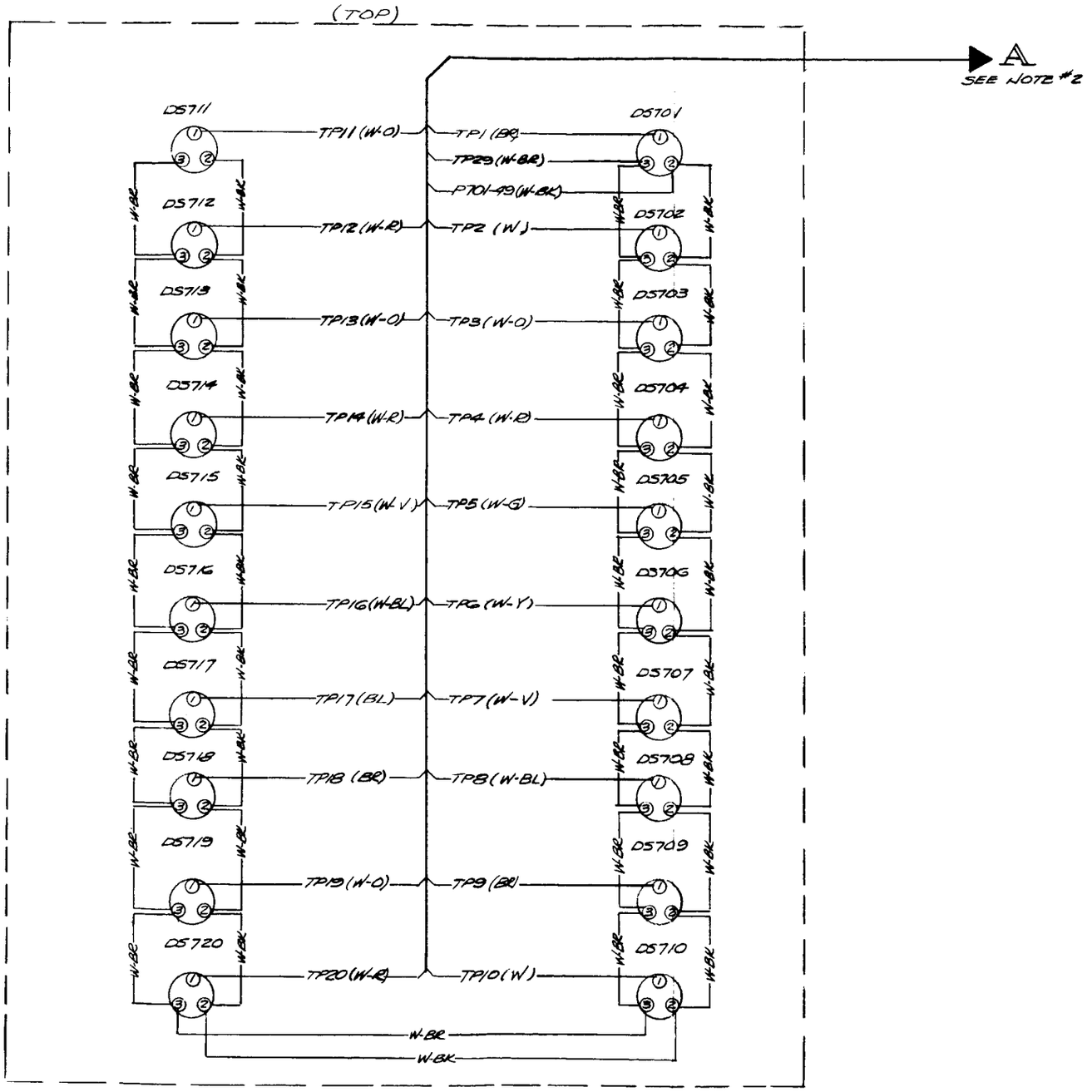



| P701 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PIN | DEST | FUNCTION | WIRE | PIN | DEST | FUNCTION | WIRE | PIN | DEST | FUNCTION | WIRE |
| 1 | XN701-8 | OUTPUT #1 | W | 18 | XN718-8 | OUTPUT #18 | BL | 34 | TP27 | CORE SHIFT | BL |
| 2 | XN702-8 | #2 | BR | 19 | XN719-8 | #19 | W-R | 35 | | | |
| 3 | XN703-8 | #3 | W-R | 20 | XN720-8 | #20 | W-O | 36 | TP23 | F/F RESET TIME | W-O |
| 4 | XN704-8 | #4 | W-O | 21 | | | | 37 | | | |
| 5 | XN705-8 | #5 | W-Y | 22 | | | | 38 | TP24 | READ GATE | BR |
| 6 | XN706-8 | #6 | W-G | 23 | | | | 39 | | | |
| 7 | XN707-8 | #7 | W-BL | 24 | | | | 40 | XM720-9 | CORE OUTPUT | W-G |
| 8 | XN708-8 | #8 | W-V | 25 | | | | 41 | XM701-8 | CORE INPUT | G |
| 9 | XN709-8 | #9 | W | 26 | | | | 42 | TP21 | -17V | W-S |
| 10 | XN710-8 | #10 | BR | 27 | | | | 43 | TP21 | -17V | W-S |
| 11 | XN711-8 | #11 | W-R | 28 | | | | 44 | TP28 | +12V | R |
| 12 | XN712-8 | #12 | W-O | 29 | | | | 45 | TP26 | 0.V | R #20 |
| 13 | XN713-8 | #13 | W-Y | 30 | | | | 46 | TP26 | 0V | BL #20 |
| 14 | XN714-8 | #14 | W-G | 31 | | | | 47 | TP25 | -20 V | S #20 |
| 15 | XN715-8 | #15 | W-BL | 32 | | | | 48 | TP25 | -20V | S #20 |
| 16 | XN716-8 | #16 | W-V | 33 | | | | 49 | DS701-2 | -8.5V | W-BK |
| 17 | XN717-8 | #17 | BR | | | | | 50 | GND LUG | CHASSIS GND | BK |

| TJ701 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PIN | DEST. | FUNCTION | WIRE | PIN | DEST | FUNCTION | WIRE | PIN | DEST | FUNCTION | WIRE |
| 1 | XN701-8 | OUTPUT #1 | W | 18 | XN718-8 | OUTPUT #18 | BL | 34 | TP27 | CORE SHIFT | BL |
| 2 | XN702-8 | #2 | BR | 19 | XN719-8 | #19 | W-R | 35 | | | |
| 3 | XN703-8 | #3 | W-R | 20 | XN720-8 | #20 | W-O | 36 | TP23 | F/F RESET TIME | W-O |
| 4 | XN704-8 | #4 | W-O | 21 | | | | 37 | | | |
| 5 | XN705-8 | #5 | W-Y | 22 | | | | 38 | TP24 | READ GATE | BR |
| 6 | XN706-8 | #6 | W-G | 23 | | | | 39 | | | |
| 7 | XN707-8 | #7 | W-BL | 24 | | | | 40 | XM720-9 | CORE OUTPUT | W-G |
| 8 | XN708-8 | #8 | W-V | 25 | | | | 41 | XM701-8 | CORE INPUT | G |
| 9 | XN709-8 | #9 | W | 26 | | | | 42 | | | |
| 10 | XN710-8 | #10 | BR | 27 | | | | 43 | | | |
| 11 | XN711-8 | #11 | W-R | 28 | | | | 44 | | | |
| 12 | XN712-8 | #12 | W-O | 29 | | | | 45 | | | |
| 13 | XN713-8 | #13 | W-Y | 30 | TP29 | -2 V | W-BR | 46 | | | |
| 14 | XN714-8 | #14 | W-O | 31 | XM704-1 | C.D | V | 47 | | | |
| 15 | XN715-8 | #15 | W-BL | 32 | XM704-5 | GATE | Y | 48 | | | |
| 16 | XN716-8 | #16 | W-V | 33 | XM701-8 | RESET | O | 49 | | | |
| 17 | XN717-8 | #17 | BR | | | | | 50 | | | |

NOTE:
1. ALL WIRES ARE TO BE #22 GA UNLESS OTHERWISE SPECIFIED.
2. ○ INDICATES TIE POINT
3. CABLE "A" CONTINUED ON SHEET 2 OF 2

Figure 9-9. Wiring Diagram
20 Bit Shift Register Chassis
Dwg. #76W7A
Sheet 1 of 2




NOTES:
1. ALL WIRES ARE TO BE #22 GA UNLESS OTHERWISE SPECIFIED.
2 CABLE "A" CONTINUED ON SHEET 1 OF 2

Figure 9-10. Wiring Diagram
20 Bit Shift Register Chassis
Dwg. #76W7A
Sheet 2 of 2

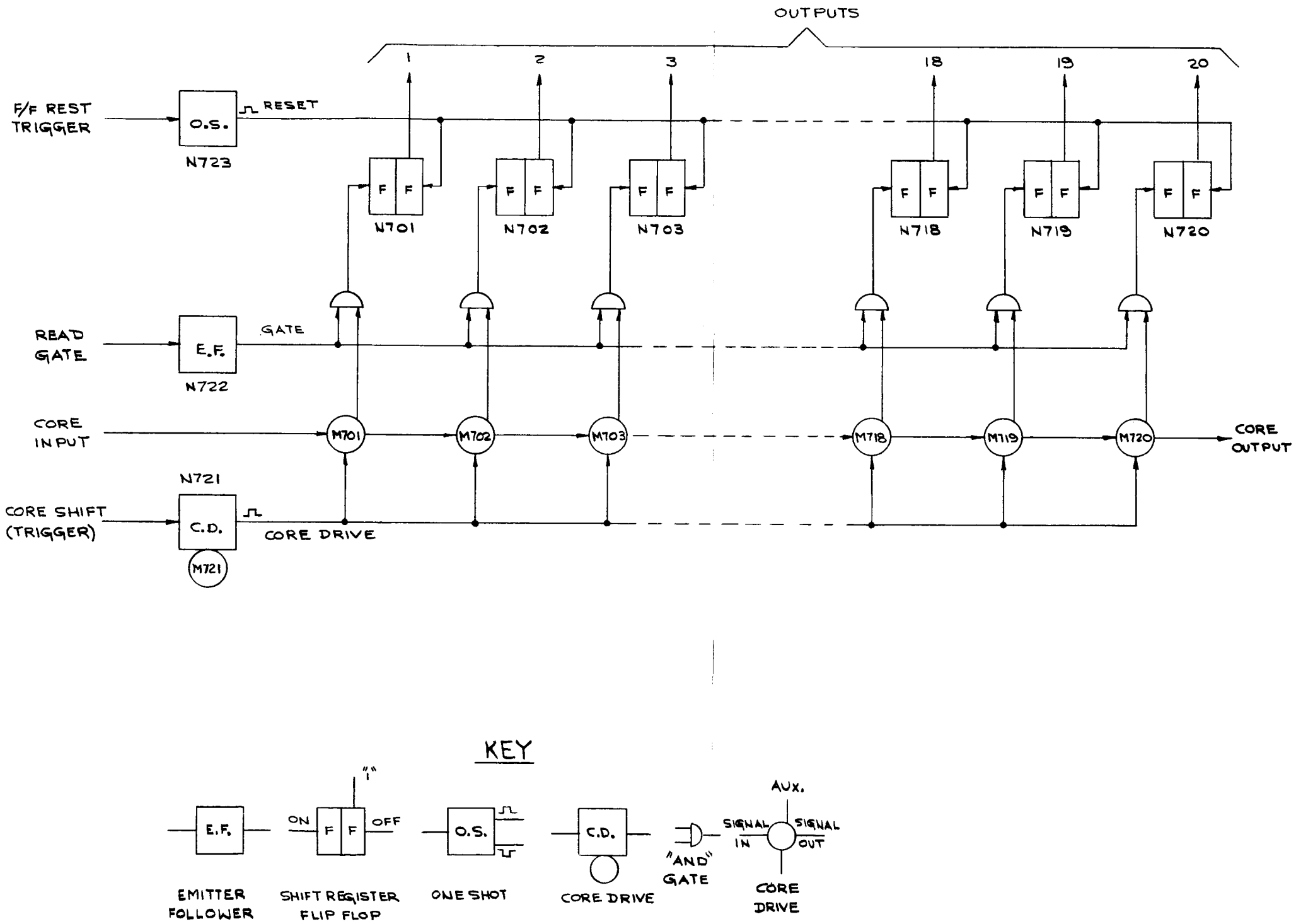



Figure 9-11. Block Diagram
20 Bit Shift Register Chassis
Dwg. #76B7A

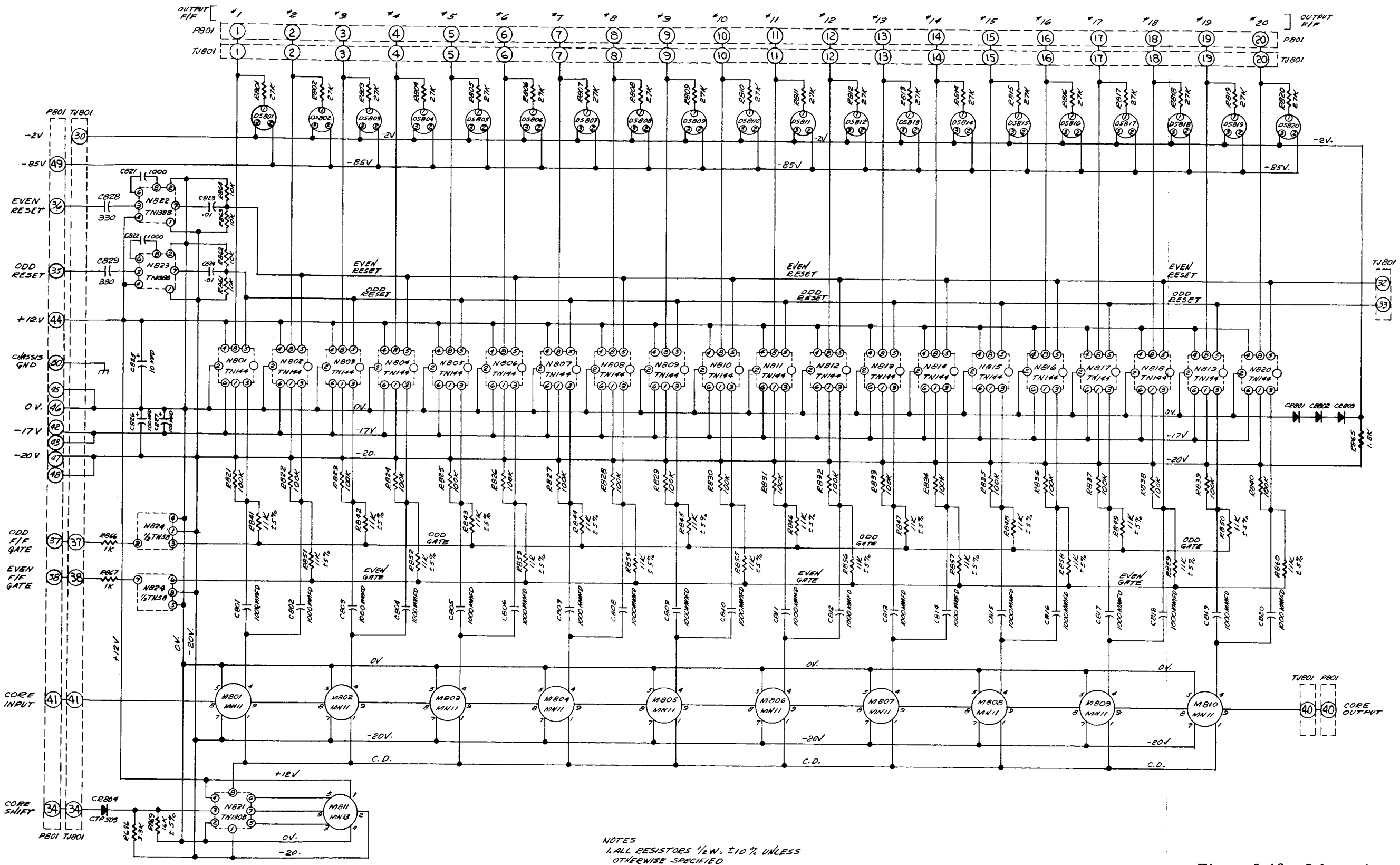
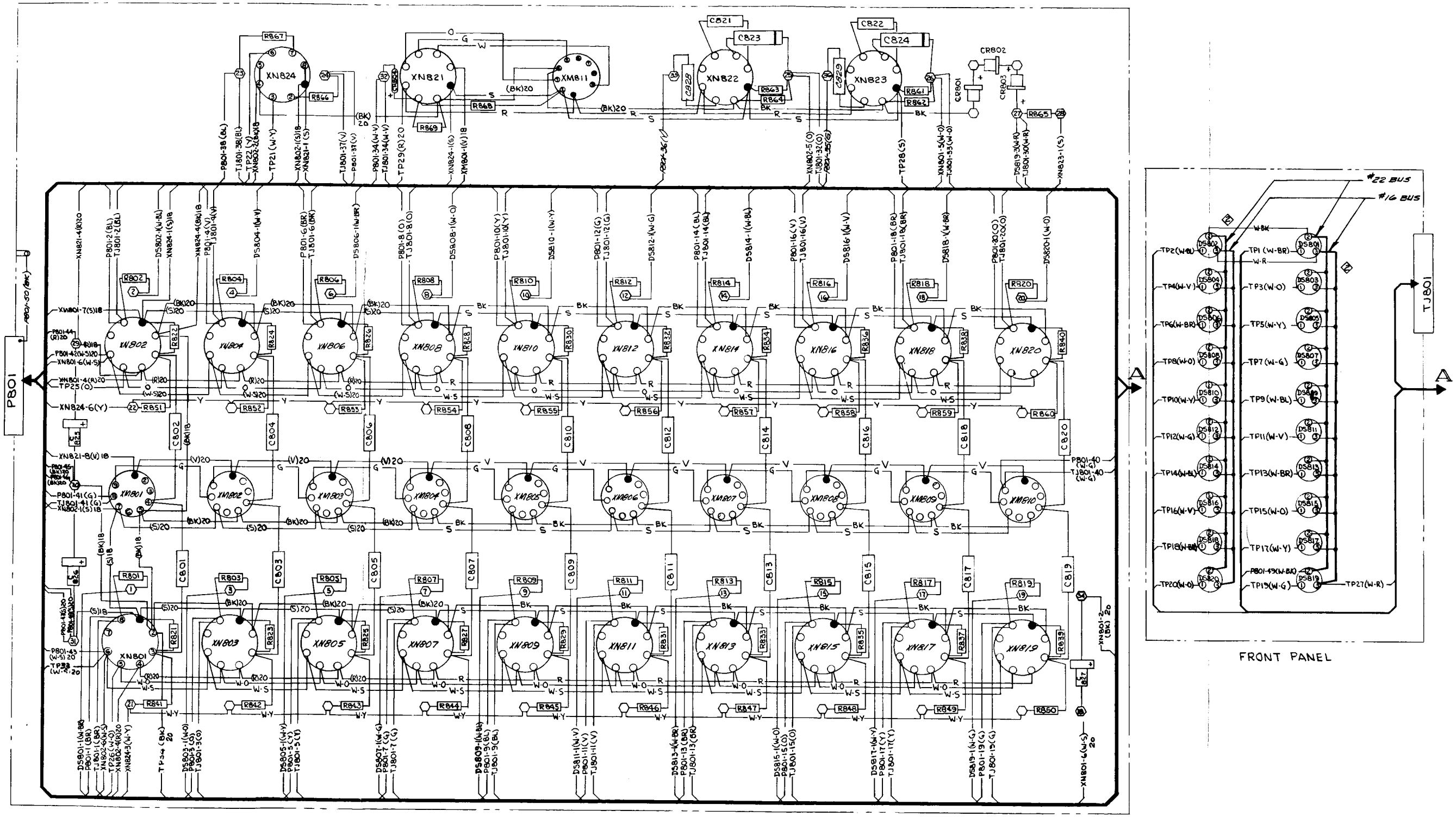



Figure 9-12. Schematic
10 Bit Shift Register Chassis
Dwg. #76S8A




| P801 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PIN | DESTINATION | FUNCTION | WIRE | PIN | DESTINATION | FUNCTION | WIRE | PIN | DESTINATION | FUNCTION | WIRE |
| 1 | XN801-8 | OUTPUT F/F | BR | 18 | XN818-8 | OUTPUT F/F | BR | 34 | TP32 | CORE SHIFT | W-V |
| 2 | XN802-8 | | BL | 19 | XN819-8 | ↓ | G | 35 | TP36 | ODD RESET | G |
| 3 | XN803-8 | | O | 20 | XN820-8 | ↓ | O | 36 | TP35 | EVEN RESET | Y |
| 4 | XN804-8 | | V | 21 | | | | 37 | TP24 | ODD GATE | V |
| 5 | XN805-8 | | Y | 22 | | | | 38 | TP23 | EVEN GATE | BL |
| 6 | XN806-8 | | BR | 23 | | | | 39 | | | |
| 7 | XN807-8 | | G | 24 | | | | 40 | XM810-9 | CORE OUTPUT | W-G |
| 8 | XN808-8 | | O | 25 | | | | 41 | XM801-8 | CORE INPUT | G |
| 9 | XN809-8 | | BL | 26 | | | | 42 | XN802-6 | -17V | *22(W-S) |
| 10 | XN810-8 | | Y | 27 | | | | 43 | XN801-6 | -17V | *22(W-S) |
| 11 | XN811-8 | | V | 28 | | | | 44 | TP29 | +12V | *20(R) |
| 12 | XN812-8 | | G | 29 | | | | 45 | TP30 | 0V | *20(BK) |
| 13 | XN813-8 | | BR | 30 | | | | 46 | TP30 | 0V | *20(BK) |
| 14 | XN814-8 | | BL | 31 | | | | 47 | TP31 | -20V | *20(S) |
| 15 | XN815-8 | | O | 32 | | | | 48 | TP31 | -20V | *20(S) |
| 16 | XN816-8 | | V | 33 | | | | 49 | DS819-2 | -85V | W-BK |
| 17 | XN817-8 | | Y | | | | | 50 | GND LUG | CHASSIS GND | BK |

| TJ801 | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| PIN | DESTINATION | FUNCTION | WIRE | PIN | DESTINATION | FUNCTION | WIRE | PIN | DESTINATION | FUNCTION | WIRE |
| 1 | XN801-8 | OUTPUT F/F | BR | 18 | XN818-8 | OUTPUT F/F | BR | 34 | TP32 | CORE SHIFT | W-V |
| 2 | XN802-8 | | BL | 19 | XN819-8 | ↓ | G | 35 | | | |
| 3 | XN803-8 | | O | 20 | XN820-8 | ↓ | O | 36 | | | |
| 4 | XN804-8 | | V | 21 | | | | 37 | TP-24 | ODD F/F GATE | V |
| 5 | XN805-8 | | Y | 22 | | | | 38 | TP-23 | EVEN F/F GATE | BL |
| 6 | XN806-8 | | BR | 23 | | | | 39 | | | |
| 7 | XN807-8 | | G | 24 | | | | 40 | XM810-9 | CORE OUTPUT | W-G |
| 8 | XN808-8 | | O | 25 | | | | 41 | XM801-8 | CORE INPUT | G |
| 9 | XN809-8 | | BL | 26 | | | | 42 | | | |
| 10 | XN810-8 | | Y | 27 | | | | 43 | | | |
| 11 | XN811-8 | | V | 28 | | | | 44 | | | |
| 12 | XN812-8 | | G | 29 | | | | 45 | | | |
| 13 | XN813-8 | | BR | 30 | TP27 | -2V | W-R | 46 | | | |
| 14 | XN814-8 | | BL | 31 | | | | 47 | | | |
| 15 | XN815-8 | | O | 32 | TP25 | EVEN RESET | O | 48 | | | |
| 16 | XN816-8 | | V | 33 | TP26 | ODD RESET | W-O | 49 | | | |
| 17 | XN817-8 | | Y | | | | | 50 | | | |

Figure 9-13. Wiring Diagram
10 Bit Shift Register Chassis
Dwg. #76W8A

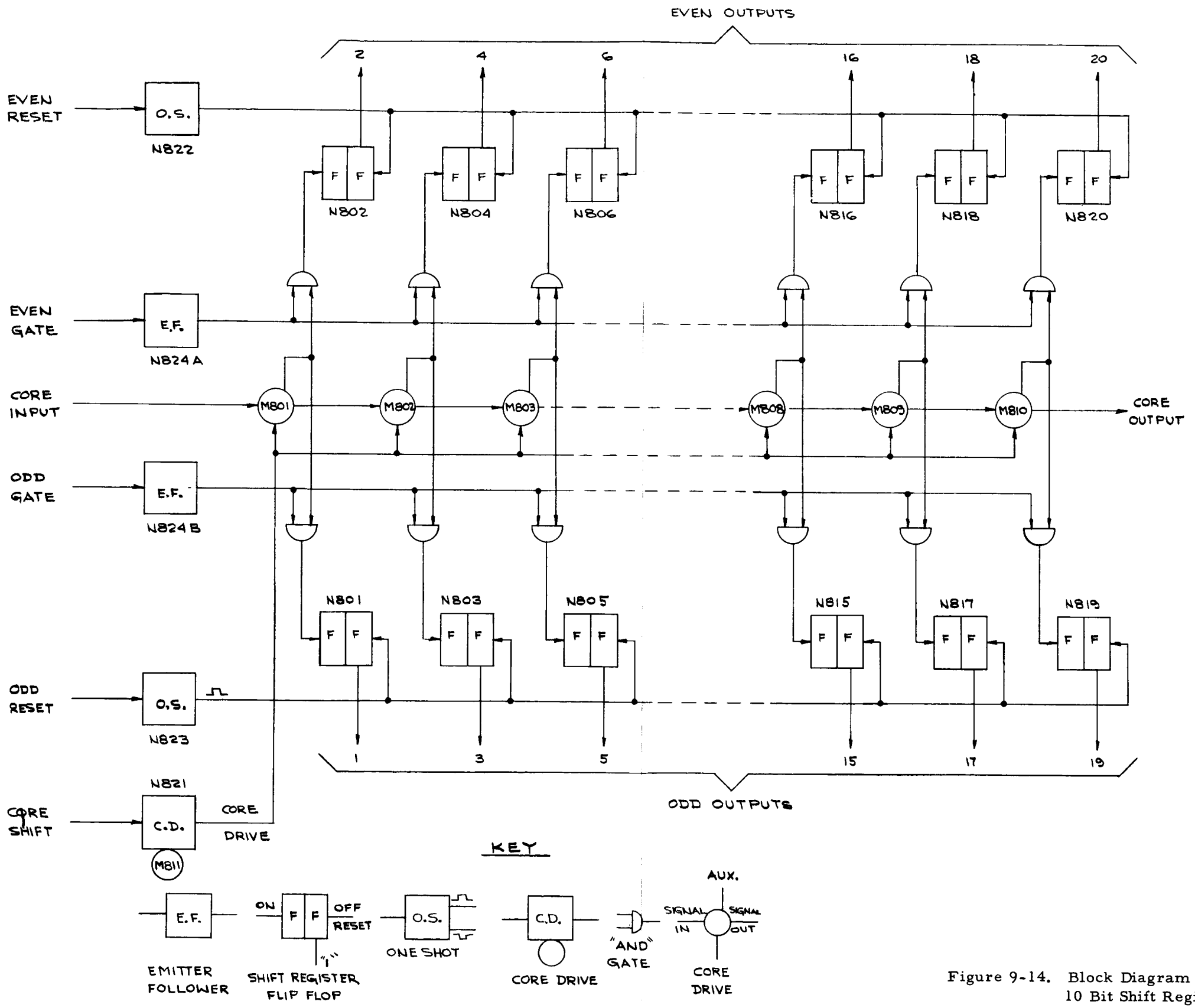
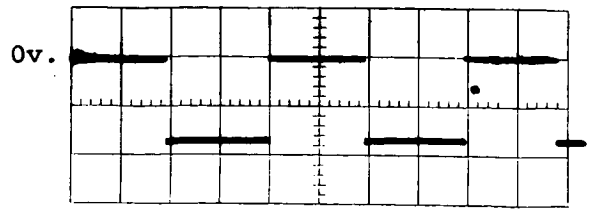
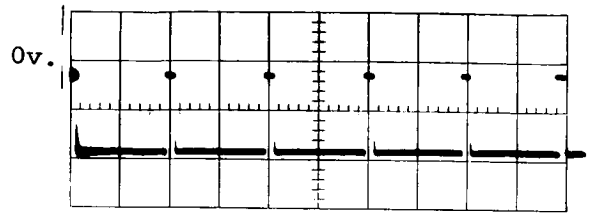


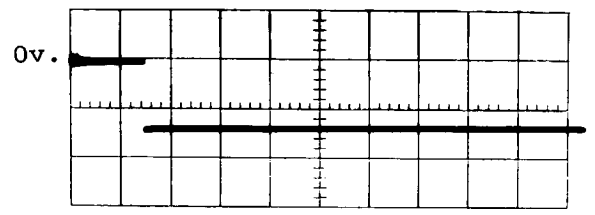

Figure 9-14. Block Diagram
10 Bit Shift Register Chassis
Dwg. #76B8A



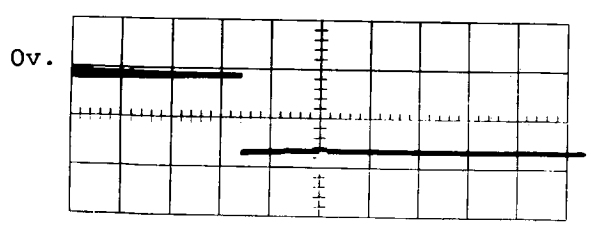

a. Control Chassis, P401, Test Jack 1
Vertical, 10v per major division
Horizontal, 500 microsec per major division
Trigger from Control, P401, Test Jack 9



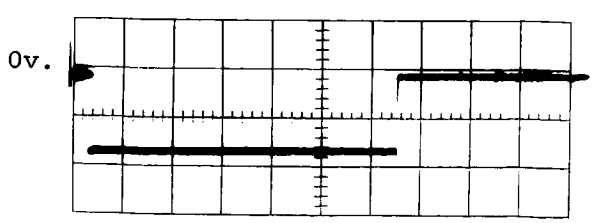

b. Control Chassis, P401, Test Jack 5
Vertical, 10v per major division
Horizontal, 500 microsec per major division
Trigger from Control, P401, Test Jack 9



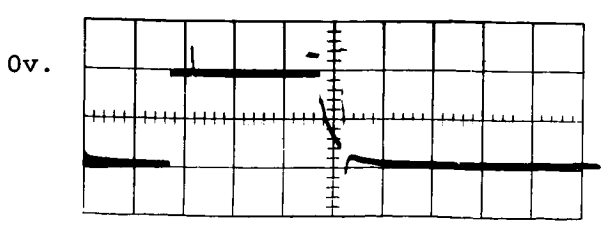

c. Control Chassis, P401, Test Jack 9
Vertical, 10v per major division
Horizontal, 500 microsec per major division
Trigger from Control, P401, Test Jack 9



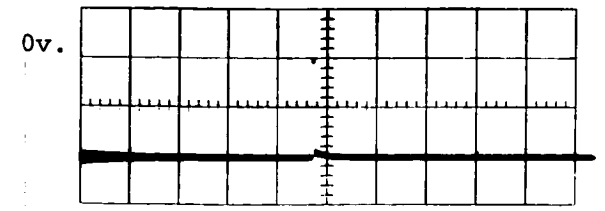

d. Control Chassis, P401, Test Jack 13
Vertical, 10v per major division
Horizontal, 100 microsec per major division
Trigger from Control, P401, Test Jack 9



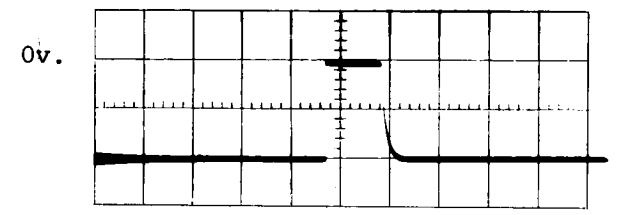

e. Control Chassis, P401, Test Jack 13
Vertical, 10v per major division
Horizontal, 1 millisecond per major division
Trigger from Control, P401, Test Jack 9



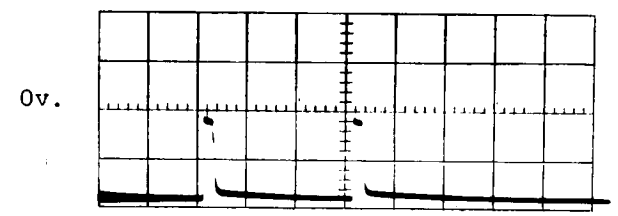

f. Control Chassis, P401, Test Jack 17
Vertical, 10v per major division
Horizontal, 200 microsec per major division
Trigger from Control, P401, Test Jack 9



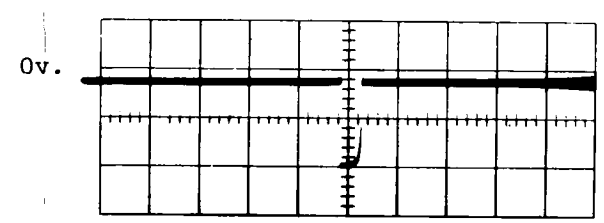

g. Control Chassis, P402, Test Jack 20
Vertical, 5v per major division
Horizontal, 200 microsec per major division
Trigger from Control, P401, Test Jack 9



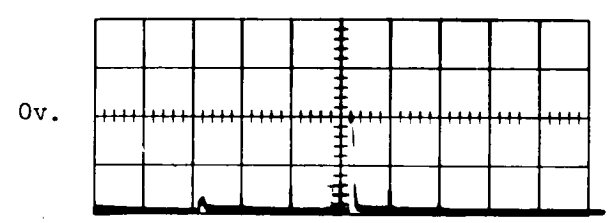

h. Control Chassis, P402, Test 23
Vertical, 5v per major division
Horizontal, 200 microsec per major division
Trigger from Control, P401, Test Jack 9




i. Control Chassis, P401, Test Jack 49
Vertical, 5v per major division
Horizontal, 200 microsec per major division
Trigger from Control, P401, Test Jack 9




j. Control Chassis, P402, Test Jack 38
Vertical, 10v per major division
Horizontal, 200 microsec per major division
Trigger from Control, P401, Test Jack 9




k. Control Chassis, P402, Test Jack 49
Vertical, 5v per major division
Horizontal, 200 microsec per major division
Trigger from Control, P401, Test Jack 9

Figure 9-15. Waveforms

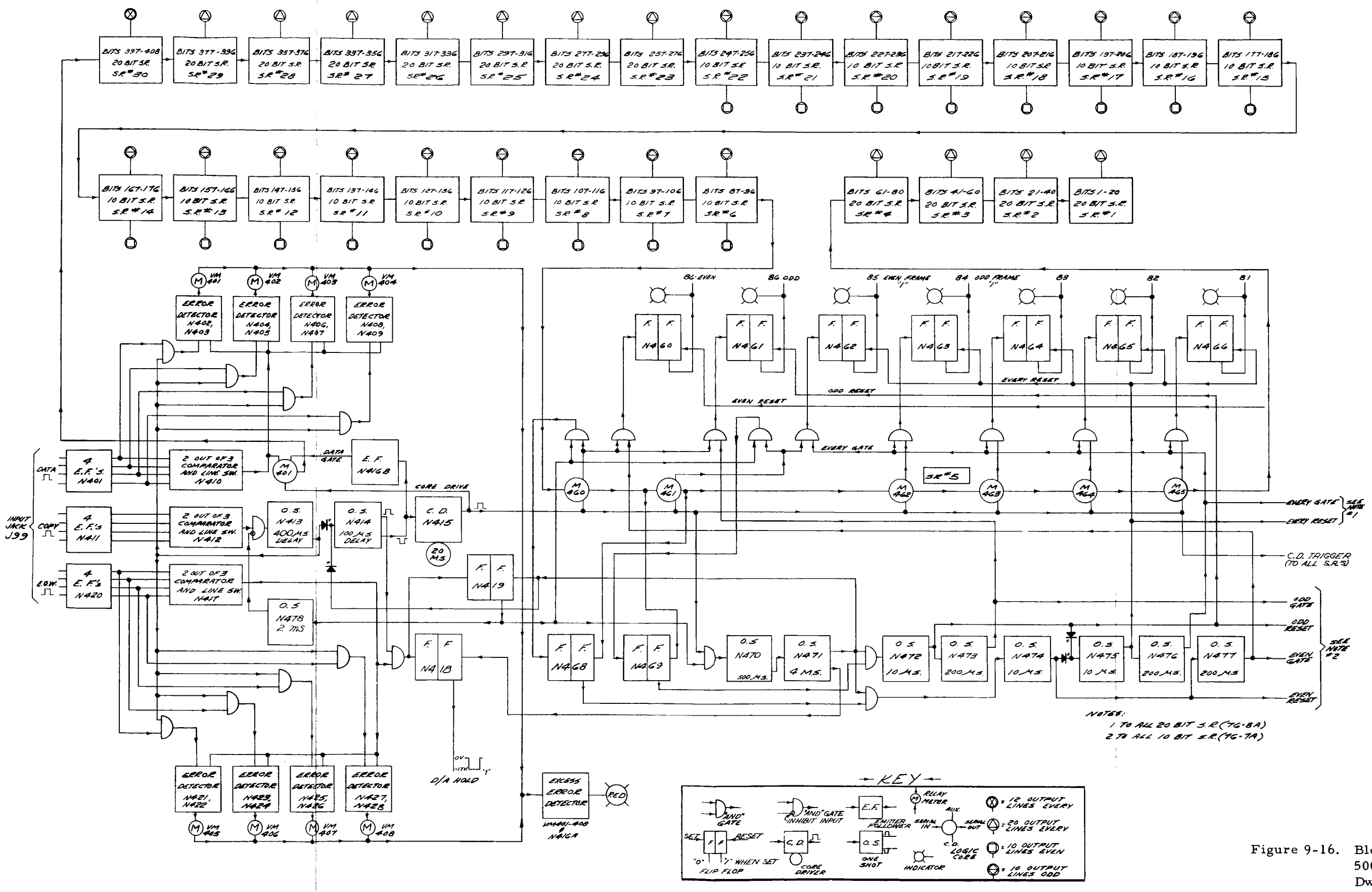



Figure 9-16. Block Diagram 500 Bit Receiver. Dwg. #76B1A

# CHAPTER X

# APPENDIX

# – 17 V AND – 20 V POWER SUPPLY

# MEC MODEL 76-9 A

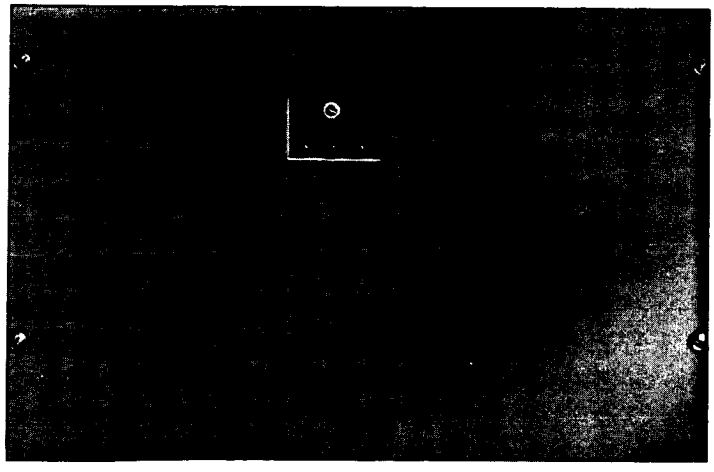
1. GENERAL

This power supply develops regulated output voltages of -17V at 40 amps and -20V at 3 amps. The -20V portion is developed by adding a -3V supply on the bottom of the -17V supply.

2. -17V SUPPLY

2-1. The 17V power supply is regulated by silicon controlled rectifiers (SCR) CR901 and CR902, by controlling the time which current can flow through their external circuit. When the external load is small, the SCRs are "on" for only a small amount of the input a-c cycle; when the external load is large, the SCRs are on for almost all of the input a-c cycle. The length of time which the SCRs are on is controlled by N901 (TN160) and its associated external circuitry.

2-2. CR901 and CR902 are SCRs which are phase-controlled elements used as a full wave rectifier element from the output of transformer T902. The two SCRs are fixed by gate signals from a common source, TN160. The operation of the circuit in TN160 is as follows: The unijunction transistor Q1 acts as a relaxation oscillator synchronized by its inter-base voltage supply. The firing circuit (TN160) is connected to the output of a single phase bridge formed by diodes CR904, CR905, CR906 and CR907, through R906. Zener diode (CR1) in the TN160 clips the rectified voltage, which charges capacitor C907 through resistor R7 in TN160. This voltage fires the unijunction transistor and whichever SCR has a positive anode voltage during that half cycle of the a-c input. Upon firing, the voltage across the SCRs decrease to the forward conduction value of less than 1 volt. This discharges capacitor C907, and keeps it discharged until the a-c input is reversed, at which time a new timing cycle starts for



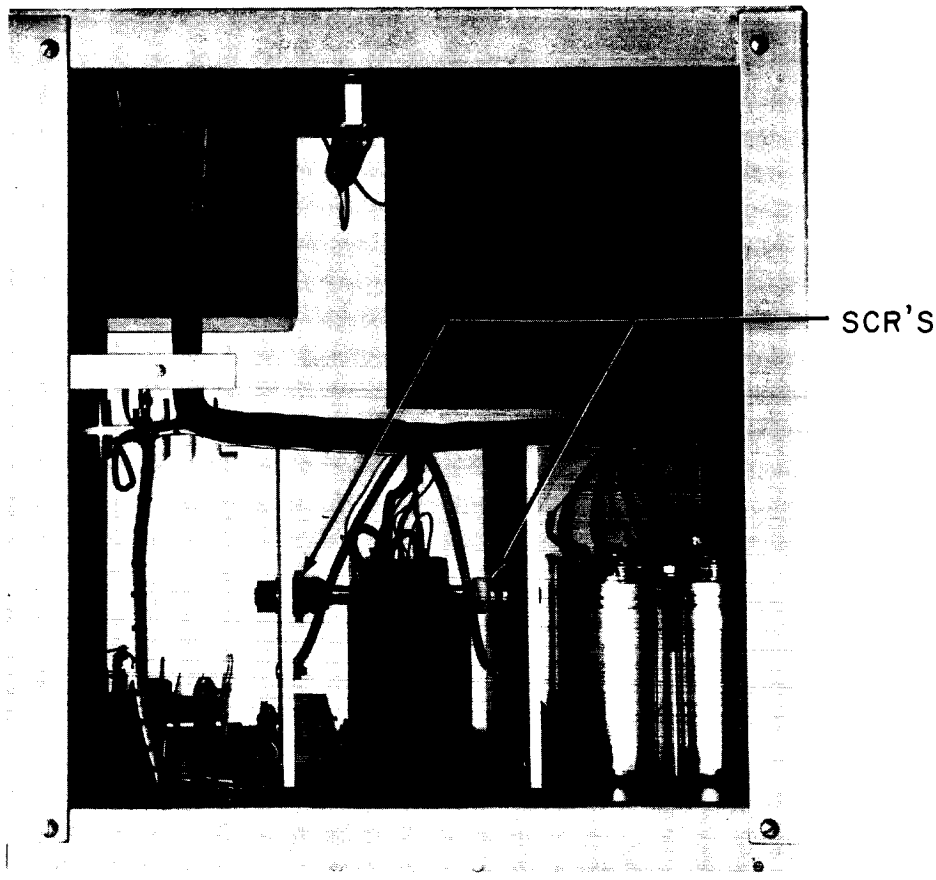
-17v and -20v Power Supply

the alternate SCR. If no current is being shunted by the voltage control circuit (Q2 and its associated circuitry) through R6, Q1 will fire within ten degrees after the beginning of each half cycle of the a-c supply voltage. At this minimum firing angle, the SCRs will deliver the maximum voltage to the load.

2-3. Q2 controls the firing angle by shunting C907. An increase of base current of Q2 will decrease the effective resistance of Q2, which will add a loading to C907, changing the charging time constant. This diversion of current will retard the firing angle so that a very small output will occur from CR901 and CR902.

2-4. DETAILED DESCRIPTION - The base current of Q2 is a feedback signal (or error voltage) developed from comparing a voltage on the base of Q2 (which is proportional to the output voltage) and a reference voltage across zener diode CR2 in the TN160. If the voltage tries to rise, more base current flows in Q2, resulting in more collector current. More collector current in Q2 will result in C907 taking longer to charge, and will therefore delay the time of the peak voltage on Q1 (the peak voltage on Q1 is the voltage necessary to fire Q1). This retards the firing angle and returns the output voltage to normal. If the output voltage drops, the reverse action takes place.

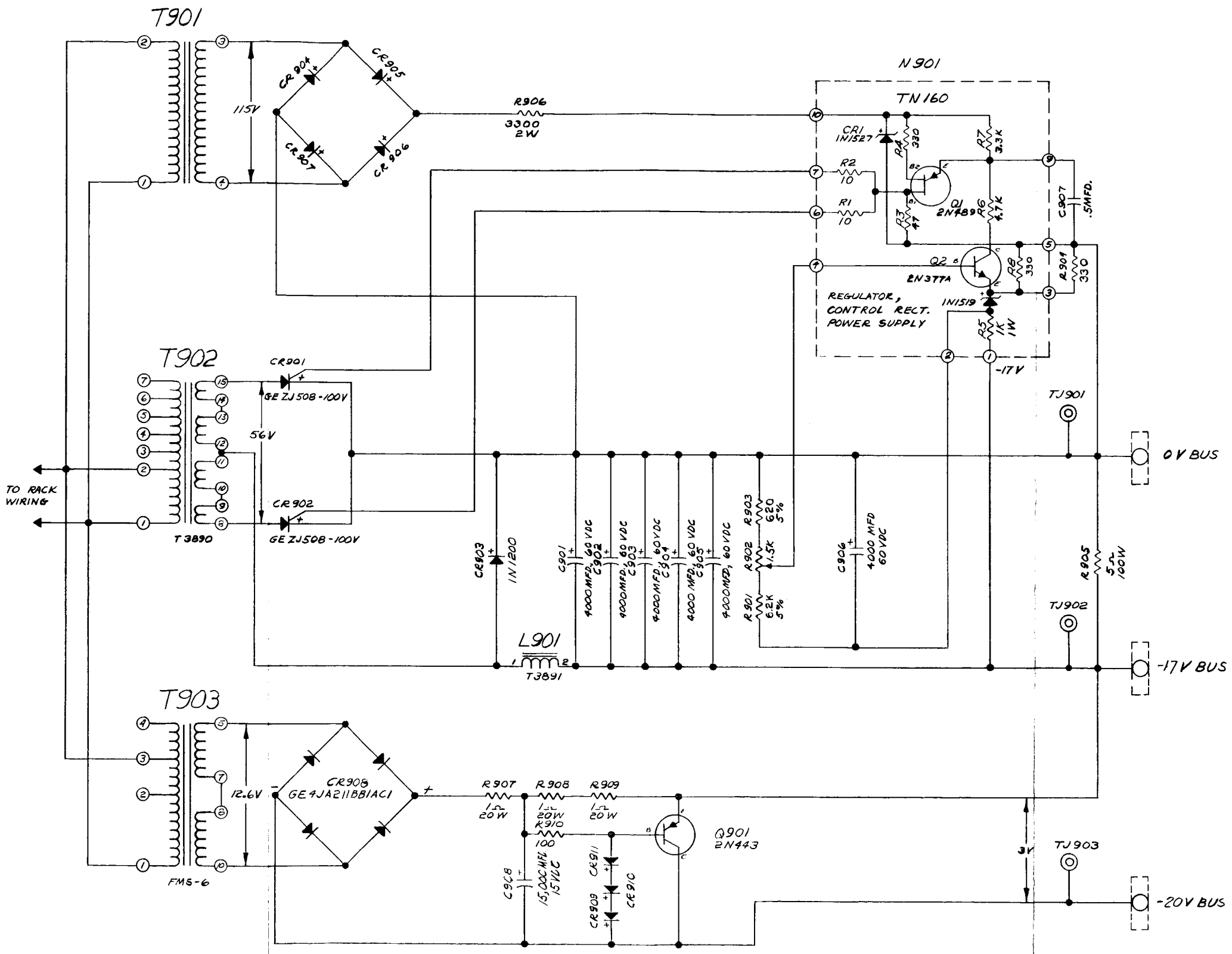
2-5. C906 and R5 are to increase stability in the feedback circuit. CR903 acts as a free wheeling diode to maintain current in the load and filter choke when the SCRs are both blocking. It contributes to over-all circuit stability. R905 is a minimum load. L901 and C901 through C905 are the filter section.




Power Supply, Bottom View, Showing Silicon-Controlled Rectifiers

## 3. -20V SUPPLY

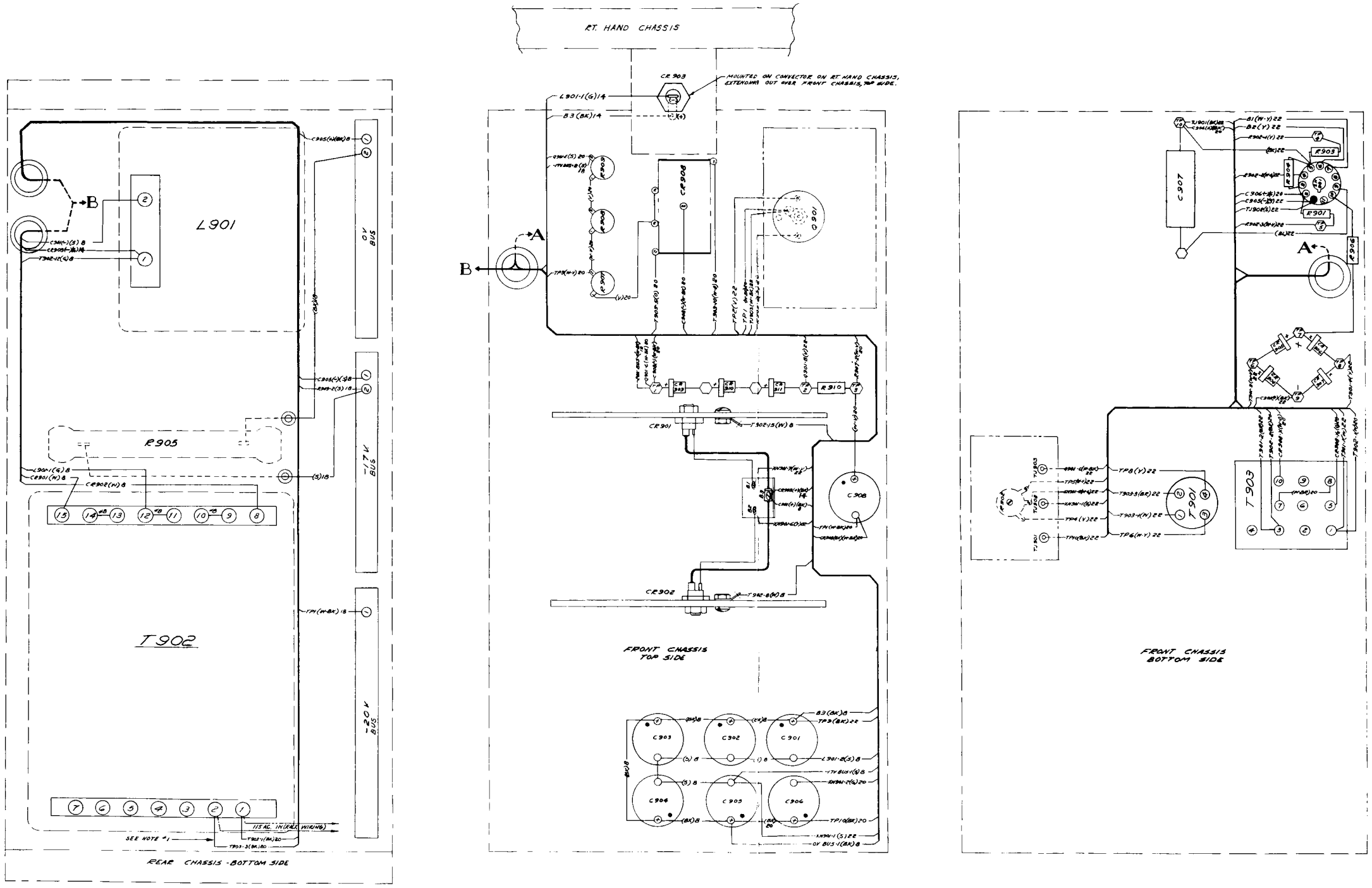
The -20V supply is only a -3V supply added on the bottom of the -17V supply. The voltage is rectified by CR908 and filtered by R907 and C908. Since the forward drop through silicon diodes are approximately constant through a large change of current, CR909, CR910 and CR911 are used as a voltage reference. Q901 acts as a shunt regulator, since its emitter voltage will be only about 0.3 volts from its base voltage, which is constant. Therefore the output voltage across Q901 is constant within the current rating of the supply. A constant current is flowing through R907, R908 and R909. When there is no external load, this current flows through Q901, but when there is an external load, current which flows through the external load is subtracted from the current flowing through Q901. R910 provides current for CR909, CR910 and CR911.




NOTES:
1. ALL RESISTORS ±10%, ½W UNLESS OTHERWISE SPECIFIED.
2. ALL DIODES #1N1692 UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED:
1. Capacitance is in mmf.
2. Resistance is in ohms.

Schematic
-20v, -17v Power Supply
Dwg. #C76S9A




NOTE:
1. LEAVE WIRES ON TERMINAL #2 LONG ENOUGH TO REACH TERMINAL #7

Wiring Diagram
-20v, -17v Power Supply
Dwg. #76W9A

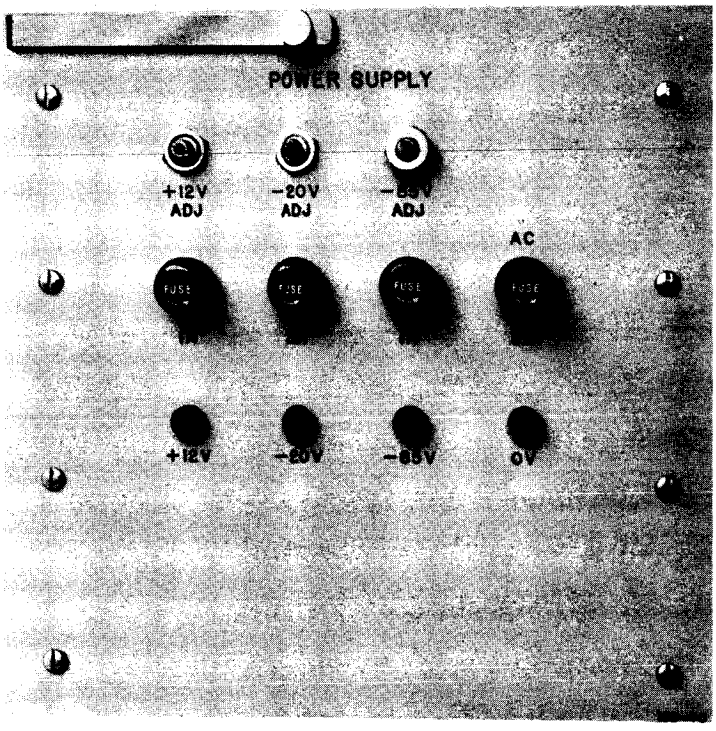
# TRANSISTOR POWER SUPPLY
# MEC MODEL 165-4 C

1. GENERAL DESCRIPTION

A Milgo type 165-4C Power Supply has three outputs: the first, a +12v, (+1v, -3v) at 1 ampere output; the second, a -20v, (+2v, -6v) at 2 amperes output; and the third, a -65v (±5v) at one ampere output. The -65v supply is stacked on the bottom of the -20v supply, thereby giving an output of -85v. The a-c input of this supply can vary from 100vac to 130vac and from 45 to 60 cycles. The unit is mounted in a standard Milgo slide-type rack and has a front panel 8-3/4 inches high by 8-7/8 inches wide. Its weight is approximately 35 pounds.

2. +12v SUPPLY

2-1. A portion of the output of transformer T401 is rectified by a bridge rectifier CR401 and filtered by resistor R401 and capacitors C401 and C402. The voltage across capacitors C401 and C402 is normally 20v (approximate). Transistor Q401 and resistors R402 and R403 act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q401 is decreased so that the IR drop across R402, R403, and Q401 will remain constant producing a constant output voltage. If the input a-c line voltage should increase, the d-c voltage across filtered capacitors C401 and C402 would increase and the effective resistance of Q401 must increase again so that the output voltage will remain constant.




Transistor Power Supply

2-2. The effective resistance of Q401 is controlled by the control section, consisting of transistors Q402, Q403, Q404, and their associated circuitry. Q404 determines whether the output voltage is too high or too low and is followed by power amplifiers Q403 and Q402, which amplify the control signal to the necessary power level for driving Q401. The base voltage of Q404 is referenced from the output of 4.7v zener diode CR402. The emitter voltage of Q404 is determined by the resistor divider network of R413, R414, and R415. The voltage from the wiper of potentiometer R414 is applied to the emitter of Q404.

2-3. As the output voltage increases, the magnitude of the voltage from the wiper of R414 will also increase proportionally. Since the output across zener diode CR402 remains constant as the output voltage increases, the emitter voltage tends to go positive with respect to the base voltage, driving Q404 toward cutoff. As Q404 goes toward cutoff, there is less collector current through R410, so there is less base current in Q403. The emitter current of Q403 decreases, reducing the current through R407 and base current of Q402. With less base current in Q402, the emitter current decreases, reducing the base current of Q401. With less base current, the effective resistance of Q401 will increase. Therefore, the output voltage decreases until Q404 senses the correct relationship between the output voltage and the zener voltage of CR402.

2-4. If the output voltage decreases below the desired value, the portion of the output voltage applied to the emitter of Q404 also decreases, tending to make the emitter more negative with respect to the base. This increases the collector current of Q404, which increases the base current of Q403, thus increasing the emitter current of Q403 and the base current of Q402. This in turn increases the emitter current of Q402 and the base current of Q401, which reduces the effective resistance of Q401, causing the output voltage to return to its regulated value. Q404 actually is matching the zener voltage to the emitter voltage.

2-5. Since a portion of the output voltage applied to the emitter of Q404 can be varied by potentiometer R414, and the emitter voltage of Q404 is to remain constant, the output voltage must be changed as the resistor R414 is changed. In this manner, the regulated output voltage can be adjusted over a range of +9v to +13v. Capacitor C403 has been added to prevent hunting. Resistors R402 and R403 are included to limit the peak current through transistor Q401 to a safe value if the output terminal is short circuited, and to provide reverse bias for Q401 and Q402. Resistor R404 provides a path for the leakage current of Q402 so that this current does not affect the base current in Q401, allowing Q401 to be more nearly cut off during a light load.

3. -20v SUPPLY

3-1. A second portion of the output of transformer T401 is rectified by bridge rectifier CR421 and filtered by parallel resistors R421A and R421B, and capacitors C421, C422, and C423. The d-c voltage across capacitors C421, C422, and C423 is 30v (approximate). Transistors Q421 and Q422 with their associated resistors R423, R424, and R422 act as a variable resistance element in series with the output load, which can be varied to maintain a constant

output voltage across a variable load. As the load current increases, the effective resistance of Q421 and Q422 is decreased so that the IR drop across R422, R423, R424, Q421, and Q422 will remain constant, producing a constant output voltage.

3-2. If the input a-c line voltage should increase, the d-c voltage across filter capacitors C421, C422, and C423 would increase, and the effective resistance of Q421 and Q422 must increase again to keep the output voltage constant. The effective resistance of Q421 and Q422 is controlled by the control section, consisting of transistors Q423, Q424, and Q425 and their associated circuitry. Transistor Q425 determines whether the output voltage is too high or too low and is followed by power amplifiers Q424 and Q423, which amplify the control signal to the necessary power level for driving Q421 and Q422. The base voltage of Q425 is referenced from the output by a 4.7v zener diode CR422. The emitter voltage of Q425 is determined by a resistor divider network R434, R435, and R436. The voltage from the wiper of potentiometer R435 is applied to the emitter of Q425.

3-3. As the output voltage increases, the magnitude of the voltage from the wiper of R435 will increase proportionally. Since the output across CR422 remains constant as the output voltage increases, the emitter voltage tends to become positive with respect to the base voltage, driving Q425, which is an NPN transistor, toward cutoff. As Q425 goes toward cutoff, there is less collector current through R431, and consequently, there is less base current in Q424. With less base current in Q424, the emitter current of Q424 decreases. With less emitter current in Q424, the current through R428 and the base current of Q423 also decrease. This reduces the emitter current in Q423 and reduces the base current in Q421 and Q422. Less base current in Q421 and Q422 increases their effective resistance, which increases the IR drop across them. Therefore, the output voltage decreases until Q425 senses the correct relationship between the output voltage and the zener voltage of CR422.

3-4. Conversely, if the output voltage decreases below the desired value, the portion of the output voltage applied to the emitter of Q425 also decreases, tending to make the emitter more negative with respect to the base. This increases the collector current of Q425, increasing the base current of Q424, which in turn increases the emitter current of Q424 and the base current of Q423. This, in turn, increases the emitter current of Q423 and the base current of Q421 and Q422, reducing the effective resistance of Q421 and Q422, and causing the output voltage to return to its regulated value. Transistor Q425 is actually matching the zener voltage to the emitter voltage.

3-5. Since a portion of the output voltage applied to the emitter of Q425 can be varied by potentiometer R435, and the emitter voltage of Q425 is to remain constant, the output voltage will have to be changed as the resistor R435 is changed. In this manner, the regulated voltage of this supply can be adjusted from -14v to -22v. Capacitors C425 and C424 provide feedback for stabilization purposes.

3-6. Resistors R423 and R424 serve two functions. First, they force the collector current of Q421 and Q422 to balance. Since the bases are tied in common, if one transistor conducts

more than the other, the higher IR drop in their associated resistor would tend to reverse bias the transistor with the most current and, in this manner, force the currents to balance. Second, if the output supply is shorted, resistors R422, R423 and R424 limit the peak current through Q421 and Q422 to a safe value while fuse F402 is melting. Resistor R425 provides a path for the leakage current of Q423 so that this leakage current does not affect the base current in Q421 and Q422. This allows Q421 and Q422 to be more nearly cut off during a light load.

4. -65v SUPPLY

4-1. A third portion of the output of transformer T401 is rectified by a bridge rectifier CR441 and filtered by resistor R441 and capacitors C441 and C442. The voltage across capacitor C441 and C442 is normally 75v (approximate). Transistor Q441, and resistors R442 and R443, act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q441 is decreased so that the IR drop across R442, R443, and Q441 will remain constant, producing a constant output voltage. If the input a-c line voltage increases, the d-c voltage across filtered capacitors C441 and C442 will increase and the effective resistance of Q441 must increase again so that the output voltage will remain constant.

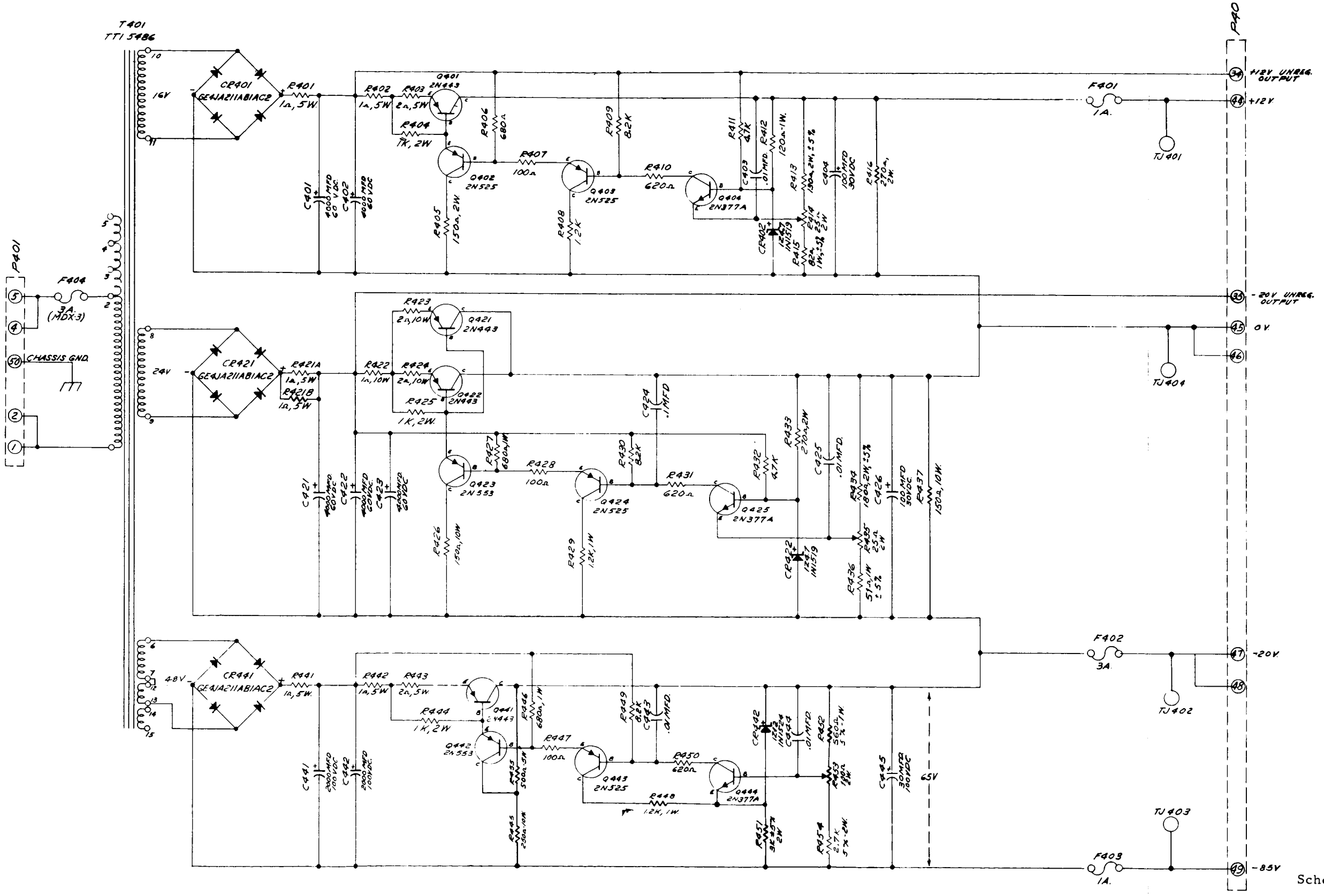
4-2. The effective resistance of Q441 is determined by the control section, consisting of transistors Q442, Q443, and Q444 and their associated circuitry. Q444 determines whether the output voltage is too high or too low and is followed by power amplifiers Q443 and Q442. These amplify the control signal to the necessary power level for driving Q441. The emitter voltage of Q444 is referenced from the output by a 12v zener diode CR442. The base voltage of Q444 is determined by the resistor divider network of R452, R453, and R454. The voltage from the wiper of potentiometer R453 is applied to the base of Q444. The zener is referenced from the positive side of this supply to reduce the emitter-to-collector voltage of Q443 and Q444 to less than 25v.

4-3. As the output voltage increases, the magnitude of the voltage from the wiper of R453 will also increase proportionally. Since the output across zener diode CR442 remains constant as the output volts increase, the base voltage tends to become negative with respect to the emitter voltage, driving Q444 toward cutoff. As Q444 goes toward cutoff, there is less collector current through R450 and less base current in Q443. The emitter current of Q443 decreases, reducing the current through R447 and the base current of Q442. With less base current, the Q442 emitter current decreases, reducing the base current of Q441. With less base current, the effective resistance of Q441 increases. Therefore, the output voltage decreases until Q444 senses the correct relationship between the output voltage and the zener voltage of CR442.

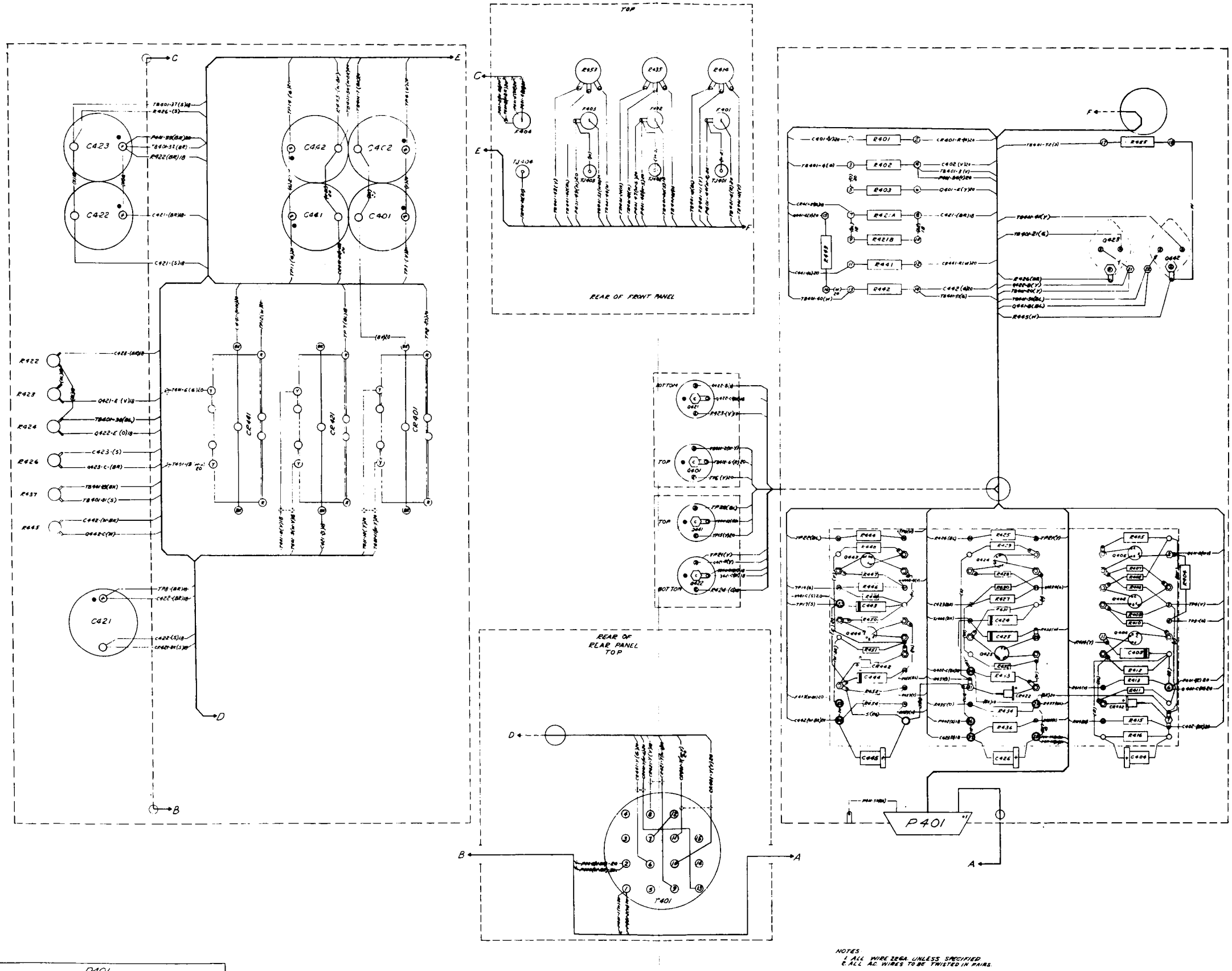
4-4. If the output voltage decreases below the desired value, the portion of the output voltage applied to the base of Q441 also decreases, tending to make the base more positive

with respect to the emitter. This increases the collector current of Q444, increasing the base current of Q443, and increasing the emitter current of Q443 and the base current of Q442. This in turn increases the emitter current of Q442 and the base current of Q441, reducing the effective resistance of Q441, and causes the output voltage to increase and to return to its regulated value. Q444 is actually matching the zener voltage to the base voltage.

4-5. Since a portion of the output voltage applied to the base of Q444 can be varied by potentiometer R453, and the base voltage of Q444 is to remain constant, the output voltage will have to be changed as the resistor R453 is changed. In this manner, the regulated output voltage can be adjusted over a range of -60v to -70v. Capacitors C443 and C444 have been added to prevent hunting. Resistors R442 and R443 are included to limit the peak current to transistor Q441 to a safe value if the output terminal is short circuited, and to provide reverse bias for Q441. Resistor R444 provides a path for the leakage current of Q442 so that this current does not affect the base current in Q441. This allows Q441 to be more nearly cut off during a light load. This -65v power supply is stacked on the bottom of the -20v supply giving a combined output of -85v.




Schematic
165-4C Power Supply
Dwg. #D165S4C




NOTES
1. ALL WIRE 22GA. UNLESS SPECIFIED
2. ALL AC WIRES TO BE TWISTED IN PAIRS.

P401

| PIN | DEST. | FUNCTION | WIRE | PIN | DEST | FUNCTION | WIRE |
|---|---|---|---|---|---|---|---|
| 1 | T401-1 | AC INPUT | (W) 20 | 41 | | | |
| 2 | T401-1 | AC INPUT | (W) 20 | 42 | | | |
| 3 | | | | 43 | | | |
| 4 | F404 | AC INPUT | (BR) 20 | 44 | F401 | +12 V | (W-R) 20 |
| 5 | F404 | AC INPUT | (BR) 20 | 45 | T401-25 | 0 V | (BK) 20 |
| 6 | | | | 46 | T401-25 | 0 V | (BK) 20 |
| 7 | | | | 47 | F402 | -20 V | (W-S) 20 |
| 8 | | | | 48 | F402 | -20 V | (W-S) 20 |
| 9 | TP-4 | [illegible] | (Y) 20 | 49 | F403 | -8.6 V | (W) 20 |
| 10 | [illegible] | [illegible] | (BR) 20 | 50 | CHASSIS | CHASSIS GND | (BK). |

Wiring Diagram
165-4C Power Supply
Dwg. #E165W46

# MAGNETIC CORES

## 1. GENERAL

A component commonly used in digital data handling equipment is a magnetic core. The term magnetic core is usually applied to a small torroid composed of magnetic material which has high permeability and also high retention. This material will have what is called a square hysteresis loop, shown in Point A, Figure MN-1. Because of this square hysteresis loop, there are two stable energy states, which make the cores adaptable to digital circuits. Magnetic cores are commonly used for shift registers, "and" gates, "or" gates, and other logic circuits, in addition to their use as blocking oscillator transformers.

## 2. THEORY OF OPERATION

### 2-1. GENERAL

a. The action of a magnetic core can best be described by referring to the drawing of the hysteresis loop (Figure MN-1). The magnetomotive force, or ampere-turns, applied to the winding of a core is measured along the X axis. Magnetic flux density (gausses), or flux lines per square centimeter, is being measured along the Y axis. Once a core has been magnetized and had this magnetization reversed several times, the relationship between flux density and magnetomotive force is described by the hysteresis loop in Figure MN-1.

b. With no current going through any of the core windings, the flux density will be either at point D or at point H, depending upon the direction in which the core has most recently been saturated. If the core is assumed to be at point D on the hysteresis loop and ampere-turns are applied in the negative direction, the relationship between the flux density and the magnetomotive force will follow the line DE. If additional ampere-turns are applied in the negative direction, the core will go on to condition F, at which point saturation has occurred and additional ampere-turns of magnetomotive force will result in only a minor increase in flux level to point G.

c. If the current through the windings is now removed, the core will return to point H on they hysteresis loop. Even though there are no ampere-turns, there is still a flux density proportional to OH in the core. The characteristics of the core material are such that this

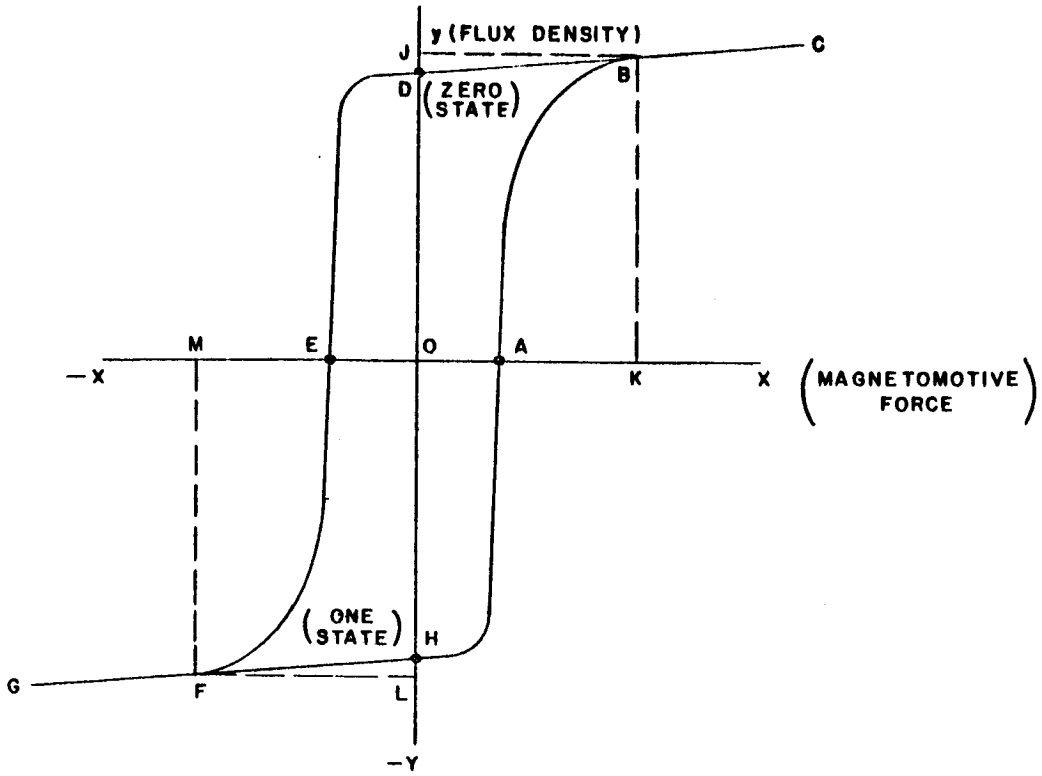



Figure MN-1. Square Hysteresis Loop

flux density will remain indefinitely as though it were a permanent magnetic. If the direction of current in the winding is reversed, positive ampere-turns are applied. This will move the condition of the core from H to A and on to B, at which point the core is now saturated in the positive direction and additional ampere-turns of magnetomotive force will cause very little change in flux density to point C. When the current in the coil is removed, the core will now go from C to D, where it will remain indefinitely until driven again.

d. The net change in flux, when going from a negative quiescent state to plus saturation, is proportional to HJ. It should be noted that other windings on the magnetic core will sense this change in flux and will generate a voltage proportional to the number of turns and the rate of change of flux. Figure MN-2 shows a simple magnetic core with three windings on it. If positive ampere-turns are then applied to winding No. 1, the core condition effectively goes from D to B. Since the hysteresis loop is very square, the change in flux during this time (proportional to DJ) is very small when compared to HJ. As a result, the voltage generated in coil No. 2 will be very small at this time.

e. If negative ampere-turns are again applied so that the core goes from D to E to F, the

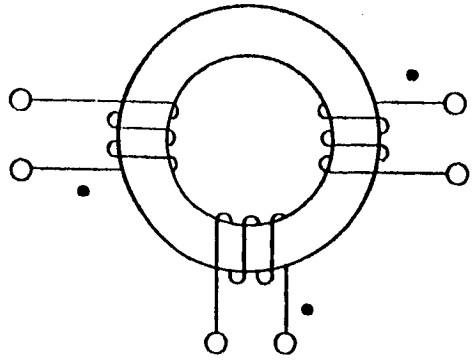


Figure MN-2. Simple Magnetic Core

change in flux will be proportional to DL. The voltage generated in winding No. 2 will now be equal in magnitude, but opposite in polarity, to the voltage generated in that winding when the core went from H to B. These pulses can be separated with diodes and used for different purposes in logic circuits. The two stable states, D and H, are referred to as the "0" state and the "1" state respectively.

## 2-2. MN11 MAGNETIC CORE

a. A Milgo MN11 magnetic core has four windings and associated components designed specifically for shift register application (Figure MN-3). Pin 7 is connected to a -25v supply. The core drive pulse, applied to pin 1, travels from -25v to approximately zero volts and return, with a rise time no greater than 5 microseconds and a fall time no greater than 10 microseconds. The pulse width must be at least 10 microseconds at 50 percent of measured points, but is normally approximately 40 microseconds wide.

b. This positive going pulse applied to pin 1 results in ampere-turns driving the core beyond positive saturation (Point C in Figure MN-1). When the core drive pulse has passed, the core is left in state D, which is defined as "O" state. The voltage at pin 8 is normally maintained at -25v but is raised to approximately -16v to insert a "1" into the core. It can be seen that the current in the input winding, as a result of a positive going pulse applied to pin 8, will magnetize the core in an opposite direction to that of the drive pulse. The state of the core will go from D to G on the hysteresis loop (Figure MN-1), and when the input pulse is passed, the core remains at H, which is defined as a "1" state.

c. When the next drive pulse occurs, the flux will travel from point H to Point C, and

transformer action of the core and windings will result in a positive pulse being generated at the dot end of all four windings. This positive pulse will be approximately 9v in magnitude with a rise time of approximately 6 microseconds. Once the core has gone from negative saturation to positive saturation, there will be no more flux change even though the drive pulse is still present, and no additional voltage is generated in the windings. This switching time, which takes place in approximately 6 microseconds, determines the width of the pulse generated by the windings.

d. The 9v pulse generated in the advance winding causes diode CR3 to conduct, and will charge capacitor C3 to approximately -16v. After the core has switched to positive saturation, the voltage at pin 6 will revert to -25v. Diode CR3, however, prevents capacitor C3 from discharging through the advance winding, so the charge is held on C3 until it discharges through an external load.

e. During a core drive pulse, the voltage at pin 2 jumps from -25v to approximately zero volts because of the IR drop in R1 caused by the shift current. With pin 2 at approximately zero volts, diode CR2 will be reverse biased and no current can flow from pin 8 through CR2 and the input winding. After the core drive pulse has passed, the -16v charge on one CR3 can now discharge through CR2 and the input windings of the next core, driving it to the "1" state. A "1" can be inserted by raising pin 8 to -21v, or more positive. It should be pointed out that a "1" can also be inserted through pin 3, or by applying a pulse to pin 5, which becomes approximately 8v positive with respect to pin 4. If there is no "1" inserted between core drive pulses, the next core drive pulse will drive the core from point D to point C on the hysteresis loop, resulting in a very small change in flux density. This will result in a very small voltage being generated in the windings (approximately 0.5v), giving a signal-to-noise ratio of approximately 18 to 1.

f. It should be noted that energy transferred to a load while shifting out a "1" comes from the core driver and not from the core. The energy in the core merely allows energy to be transferred to the output winding while the core is acting as a transformer. The Milgo MN11 operates equally well on a power supply voltage of -20v instead of -25v as described.

## 2-3. SHIFT REGISTERS

a. When connected to form a shift register, MN11 cores are connected as shown in Figure MN-3. If a positive going pulse is applied to pin 8 of the first core, a "1" will be inserted into that core. During the next core drive pulse, all of the cores will be pulsed simultaneously, since they are connected in parallel. The resultant 9v pulse from the advance winding

of the first core will charge the capacitor in the first core to approximately -16v. When the first core has switched from minus saturation to plus saturation, there will no longer be any voltage generated in the advance winding. CR3 of the first core will prevent the capacitor from discharging through the advance winding, however, and CR2 in the second core prevents this capacitor from discharging through the input winding of the second core. CR2 is reverse biased because of the IR drop in the resistor of the second core caused by the shift current.

g. When the shift pulse has passed, the pin 2 voltage of the second core will go back to -25v and the capacitor in the first core may now discharge through the input winding of the second core. The resultant current through the input winding is sufficient to drive the second core from point D to point G on the saturation curve, so that when C3 is completely discharged, the second core will be in a "1" state. While this second core was being switched from plus saturation to minus saturation, flux linkages were changing in all of the windings of this core, with the result that a voltage was generated in all of these coils with the dot end of the winding negative. Diode CR1 will prevent any current flow in the drive winding as a result of the generated voltage, and the diode CR3 will prevent any current flow in the advance winding as a result of this generated voltage.

h. During the next core drive pulse, core 2 is switched from minus saturation to plus saturation, resulting in the output capacitor of the second core being charged. After the second core drive pulse, the discharge current from this capacitor will insert a "1" into the third core and so on to the last one. Since both ends of the auxiliary winding are brought out, the auxiliary winding may be used to generate either a positive going or negative going 9v pulse. This auxiliary pulse will be approximately 9v in magnitude, with a rise time of six microseconds and a fall time of approximately one half microsecond. In addition, the auxiliary winding can be used to insert "1's" into the core by applying a suitable positive pulse to pin 5 or a suitable negative pulse to pin 4. Pins 2, 3, and 6 are brought out for additional flexibility in adapting the MN11 core to logic circuits.

## 2-4. BLOCKING OSCILLATORS

a. The use of transformers for blocking oscillators is common and widely understood. It is also possible to use a square loop magnetic core as a blocking oscillator transformer with some desirable results in control of pulse width. Figure MN-4 shows the connections of either an MN12 or an MN13 as used in a blocking oscillator.

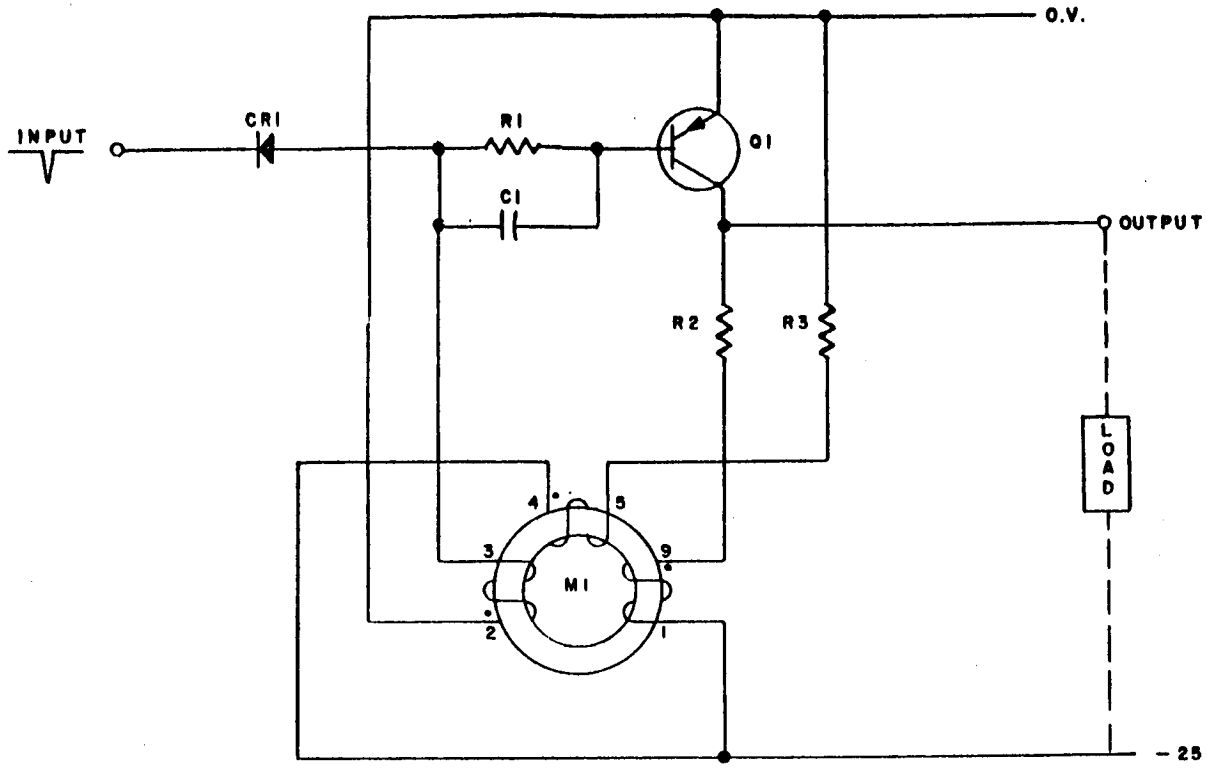



Figure MN-4. Blocking Oscillator (MN12 or MN13)

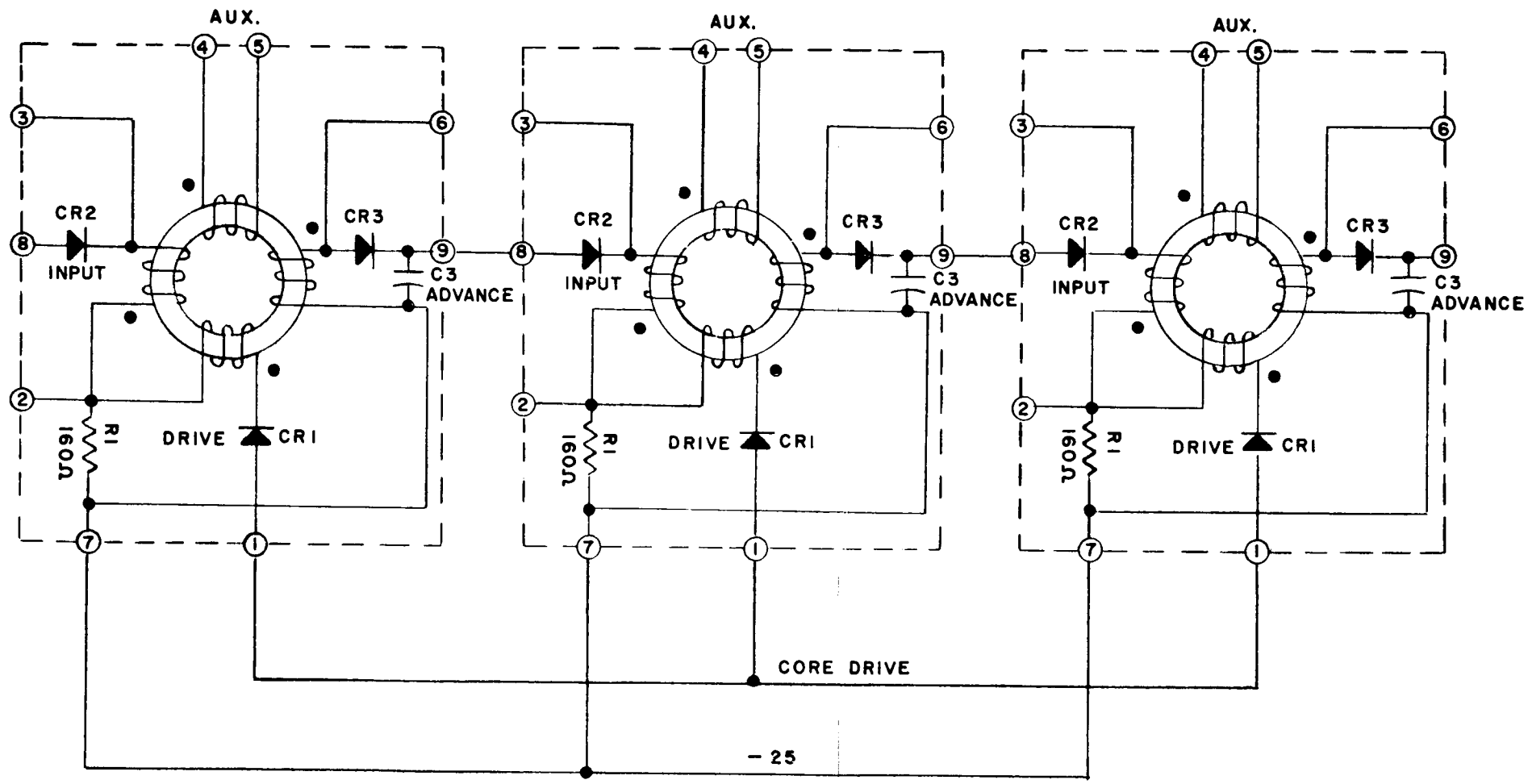
b. The 9-1 winding is the collector winding and could be compared to the primary winding of a transformer. The 2-3 winding is the feedback winding and could be compared to the secondary winding of a transformer. The 4-5 winding is the reset winding and has no counterpart in a conventional transformer. The reset winding is so connected that the current through the reset winding will drive the core into negative saturation. The transistor will normally be cut off, but when triggered by a negative pulse at the input, will go into conduction. The resulting collector current applies positive ampere-turns to the core and the flux moves from H toward A and B. The resulting flux change in the core is sensed by the feedback winding and a voltage is generated, making pin 3 negative. This negative going voltage is applied to the base of the transistor and drives the transistor into heavier conduction.

c. As the transistor conducts more heavily, the rate of change of flux increases, resulting in an even more negative voltage being applied to the base of the transistor. This feedback very quickly saturates the transistor (approximately one microsecond), but the collector current is limited by resistor R2 and the voltage generated in the collector winding of the core. As long as the core is still in the process of switching from minus saturation to plus

saturation, the core and its windings act as a transformer and the feedback winding continues to drive the transistor into saturation. When the core has finally reached saturation (B on hysteresis curve, Figure MN-1), additional ampere-turns from the collector winding will no longer result in a change of flux and no additional voltage will be generated in the feedback winding. This removes the drive to the transistor, which immediately cuts off, removing the ampere-turns from the collector winding.

d. Current through resistor R3 and the reset winding now starts to apply ampere-turns in the negative direction again and drives the core from position D to F. This results in a reversal of flux in the core, which reverses the voltage generated in the feedback winding. Pin 3 now becomes slightly positive, insuring a rapid cutoff of the transistor. Since the duration of the output pulse depends on the time it takes to switch the magnetic core, the pulse width depends on the core used and is relatively independent of the load on the blocking oscillator.

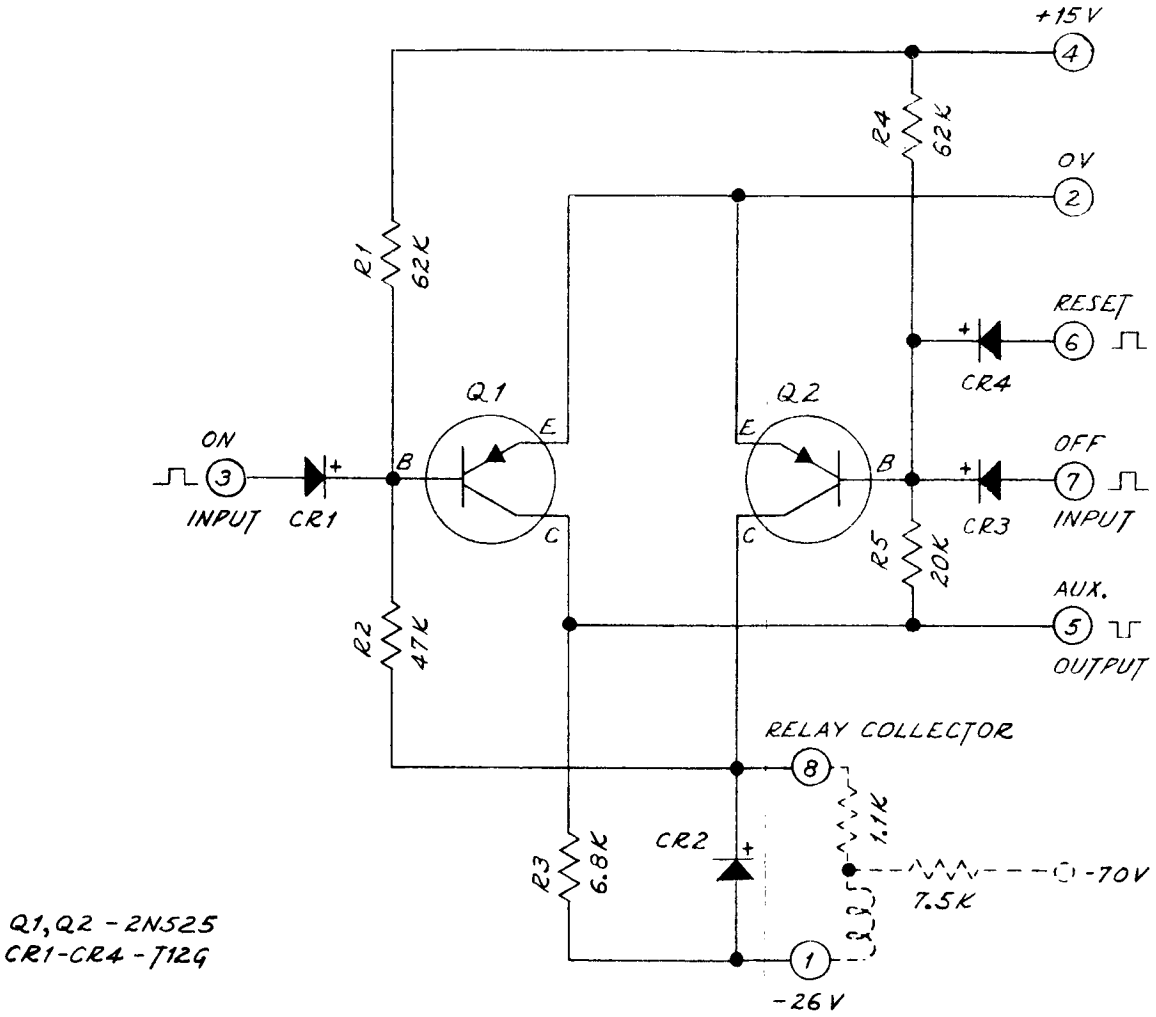
e. Two blocking oscillator cores are used in Milgo equipment: an MN12 and an MN13. The MN12 will cause a pulse approximately 10 microseconds wide to be generated by the blocking oscillator, while the MN13 will cause a pulse approximately 40 microseconds wide to be generated. It takes approximately 30 microseconds to reset an MN12 core and approximately 80 microseconds to reset an MN13 core.


AUX.
AUX.
AUX.
CR2
INPUT
CR3
C3
ADVANCE
CR2
INPUT
CR3
C3
ADVANCE
CR2
INPUT
CR3
C3
ADVANCE
160Ω
R1
DRIVE
CR1
160Ω
R1
DRIVE
CR1
160Ω
R1
DRIVE
CR1
CORE DRIVE
- 25

# TN 28
# RELAY DRIVING FLIP-FLOP

A TN28 is a bistable flip-flop which can be used for driving a relay coil or other loads of 500 ohms or more. The external load (shown on the schematic diagram in phantom between pins 8 and 1) is a special network used in conjunction with a 350 ohm relay coil which has permanent magnet bias and requires plus and minus currents for optimum operation. The network is normally defined as being in the "off" or "0" condition when transistor Q1 is saturated and Q2 is cut off, leaving the relay de-energized. The "on" or "1" condition is the opposite, with Q1 cut off and Q2 saturated, causing the relay to energize. Assuming that Q1 is saturated, then its collector is approximately -0.25 volts. Resistors R4 and R5 are then connected from +15 volts to 0 volts and by divider action hold the base of Q2 at approximately +3.5 volts. Since the emitter at Q2 is at 0 volts, this reverse bias keeps Q2 cut off. With Q1 saturated, its base is at approximately -.05 volts; so the current through resistor R1 is approximately 0.25 milliamps. The current through the series combination of R2 and the external load resistor, which may very from 500 ohms to 5K, varies from 0.53 to 0.48 milliamps. The difference between the currents in R1 and R2 is the base current of Q1, which is sufficient to drive Q1 to saturation. This satisfies the original condition, so this condition is a stable one. The input voltages at pins 3, 6 and 7 must be somewhat negative during quiescent conditions. The flip-flop may be turned "on" by raising the voltage at pin 3 to a positive value so that diode CR1 conducts, raising the base voltage of Q1 to a positive value. Note that the input pulse will be loaded somewhat, so it cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cut off. With Q1 cut off, R4 and R5 are no longer connected between 0 and +15 volts, and Q2 is no longer clamped off. Instead, Q2 base current may now flow through resistors R5 and R3, causing Q2 to saturate. Now resistors R1 and R2 are connected from +15 to 0 volts and hold the base of Q1 at approximately +6 volts, keeping Q1 in a cut off condition after the input pulse passes. This, then, is the other stable condition which will be maintained until Q2 is cut off by a positive pulse at either pin 6 or pin 7. A positive pulse at either of these pins turns Q2 off, allowing base current from Q1 to be conducted through R2 and the external load, driving Q1 back into saturation and restoring the initial condition. Diode CR2 is included to suppress the voltage of an external relay coil connected across pins 8 and 1. As Q2 goes from saturation to cutoff, the relay coil is de-energized. However, the inductance of the relay coil attempts to maintain the current through the relay coil by driving the voltage at pin 8 much more negative than the -26 volt supply. If this were allowed to happen, Q2 could be damaged by excessive emitter-collector voltage. To prevent this from happening, diode CR2 is added. During most phases of the cycle, CR2 is reverse biased and so does not enter into the operation of the circuit. When the relay is de-energized and pin 8 is driven negative by the relay inductance, CR2 is forward biased and conducts, providing a path for current through the relay coil

and eliminating the voltage spike. Although the description of operation of this network has been based on voltages of +15 volts and -25 volts, this network will operate equally on voltages of +12 volts and -20 volts or +10 volts and -15 volts.




Schematic,

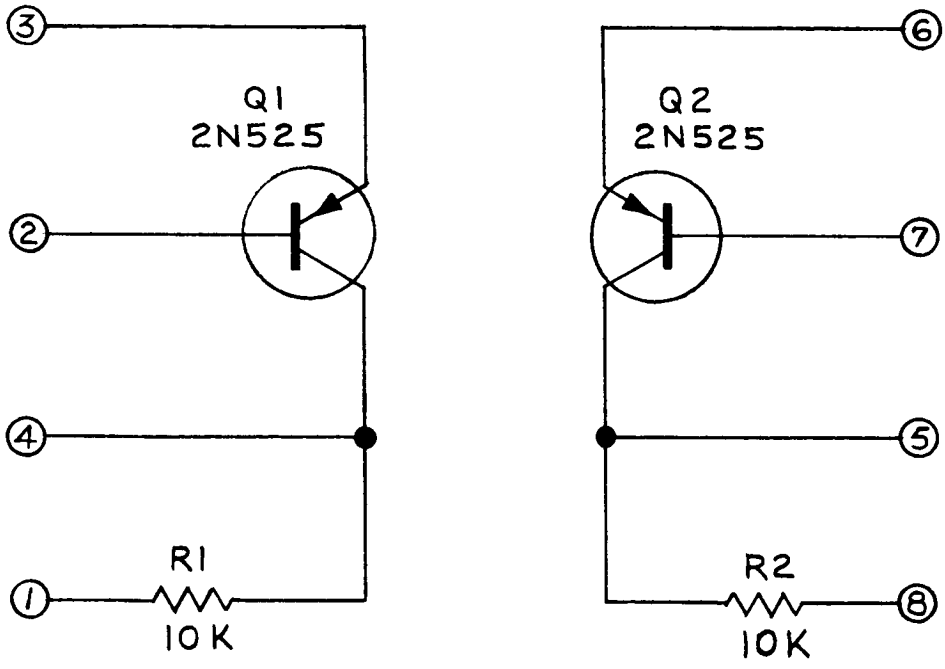
TN28 Relay Driving Flip-Flop

Dwg. #A103S28A

# TN 57
# DUAL PULSE AMPLIFIER

The TN57 contains two PNP transistors connected as two independent conventional amplifiers. Only one of these will be discussed since the other is identical to it. As normally used, a supply voltage is connected to pins 3 and 1 with the plus side on pin 3. Pin 2 will be the input and pin 4 the output. As long as pin 2 is more positive than pin 3 the transistor is cut off and the voltage at pin 4 will be the same as the voltage at pin 1. When pin 2 is approximately 0.5 volts negative with respect to pin 3 the transistor will saturate and the voltage at pin 4 will go positive until it saturates, approximately 0.25 volts more negative than the emitter. Caution must be used to connect an external base resistor in series with pin 3 to prevent damage to the transistor. The value of the external base resistor is dependent upon how negative the driving voltage goes and upon the external load that is connected to pin 4. To insure saturation the base current should be at least 1/20th of the collector current.

The TN57 may also be used in a variety of applications by the addition of external components.

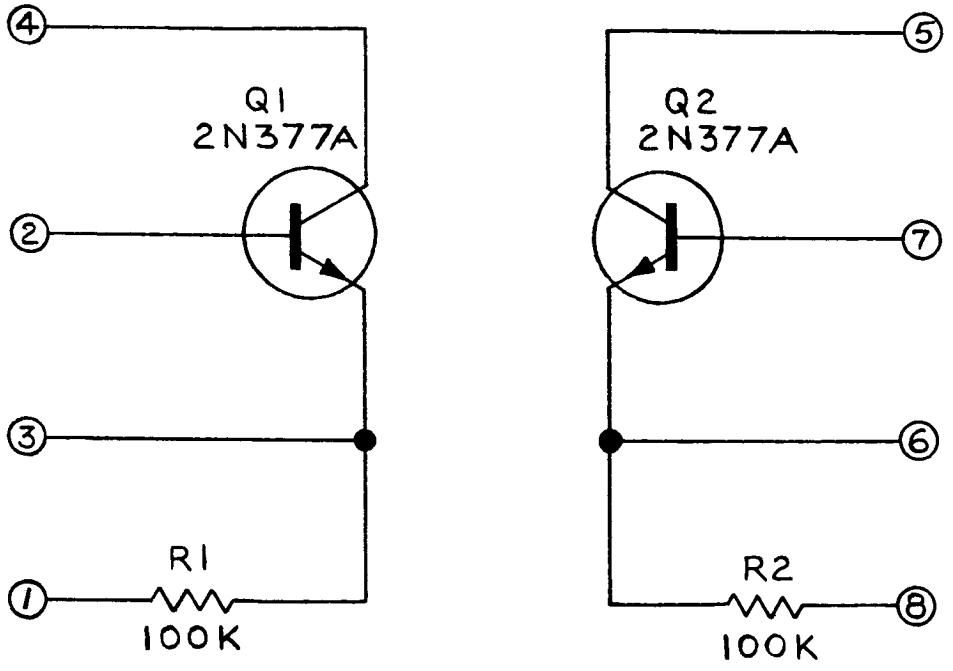



Schematic
TN57 Dual Pulse Amplifier
Dwg. #A103S57A

# TN 58
# DUAL EMITTER FOLLOWER

A TN58 consists of two NPN transistors connected as independent emitter followers. As normally used, a supply voltage is connected to pins 4 and 1 with the plus side on pin 4. As the voltage at pin 2 is varied, between the voltages at pins 4 and 1, the transistor will conduct and the voltage at the emitter, pin 3, will be approximately 0.4 volts more negative than the voltage at pin 2. Because of the power gain of the transistor a lower impedance load can be driven from pin 3 than could have been driven from the signal applied to pin 2.

The TN58 may also be used in a variety of applications by the addition of external components.




Schematic

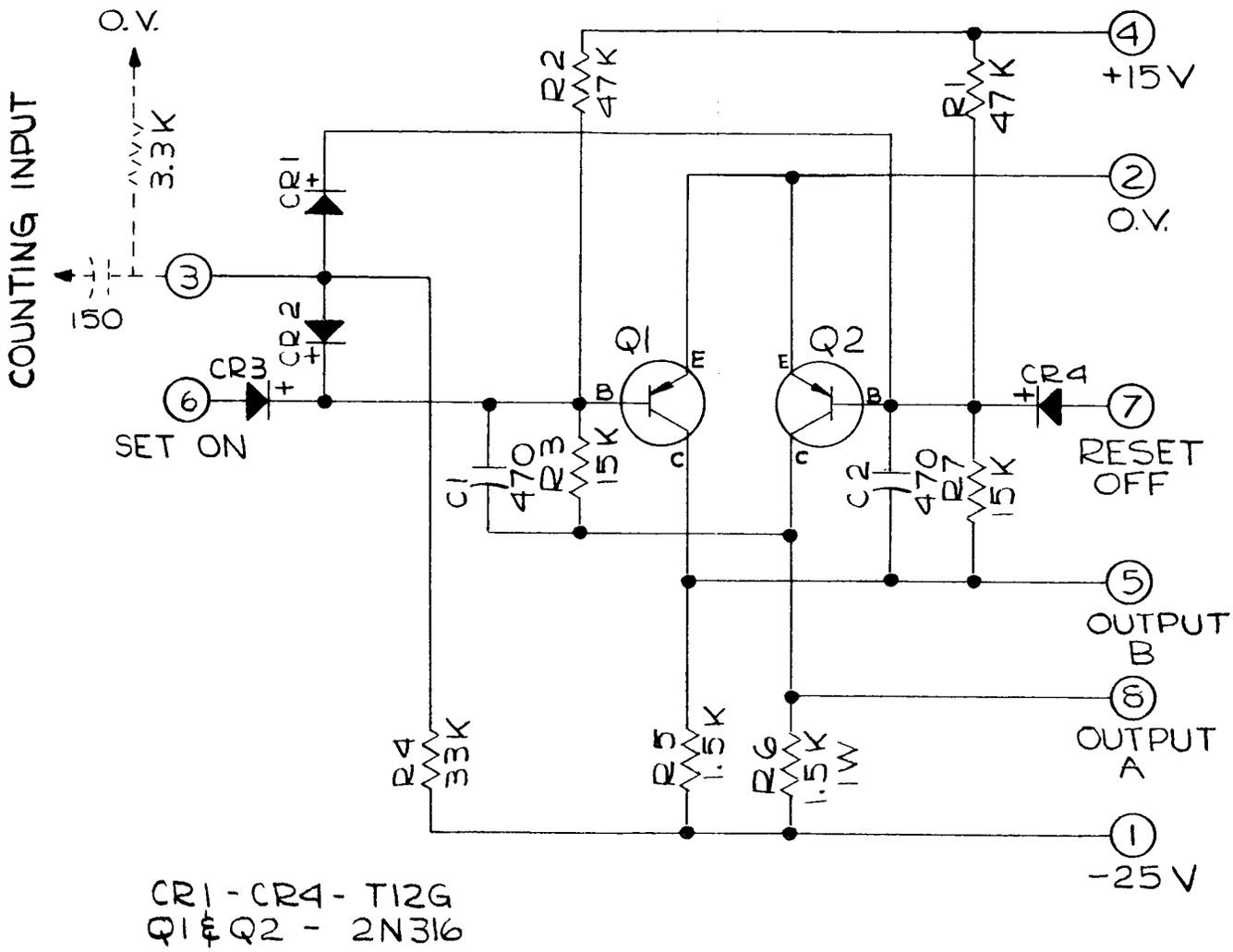
TN58 Dual Emitter Follower

Dwg. #A103S58A

# TN 90B
# BALANCED FLIP-FLOP AND DIVIDER

The TN90B is a bistable balanced flip-flop. An auxiliary input (pin 3) allows the network to be used as a divider in a counter.

The network is defined as being in the "0" state when Q1 is saturated and Q2 is off and in the "1" state when the reverse is true. Assume that Q1 is saturated ("0" state) then the collector voltage of Q1 will be approximately 0 volts and resistor divider, R1 and R7, will maintain approximately +3.5 volts of reverse bias on the base of Q2, keeping it cut off. With Q2 cut off, resistors R3 and R6 will provide a path for Q1 base current, clamping Q1 in saturation. This condition is stable and will not be changed until an input is received on pin 3 or pin 6. Pin 6 is in "1" input, in that a positive pulse above 0 volts at pin 6 will cause CR3 to conduct, thus driving the base of Q1 positive above 0 volts, reverse biasing Q1, subsequently cutting Q1 off. As Q1 is cut off its collector will go negative and due to the resistor divider, R1 and R7, the base of Q2 will go negative. As the base of Q2 goes negative, Q2 will go into saturation. As Q2 saturates, its collector will go positive and due to the resistor divider of R2 and R3 the base of Q1 will be reverse biased at approximately +3.5 volts, keeping Q1 cut off, after the input pulse has passed. The network will remain in the "1" state until reset by a positive pulse on pin 7 or triggered from a pulse on pin 3, the counting input. If a positive pulse is applied on pin 3 through an external capacitor for differentiation, both Q1 and Q2 will be cut off. Capacitors C1 and C2 retain charges which are dependent upon which one of the transistors was saturated before the input pulse occurred. Since the input pulse is differentiated by a small input capacitor, it will last a very short time, less than one microsecond. At this point, the internal capacitors C1 and C2 take over, turning on the transistor that had previously been off. For example; assume the network is the "1" state, therefore Q1 is cut off and Q2 is saturated. The voltage across C1 will be approximately 3.5 volts and across C2 will be approximately 26 volts. When pin 3 goes positive above 0 volts, both bases will be driven positive, cutting the transistors off. The collector of Q2 starts to go negative from 0 volts to -23 volts. Since this occurs almost instantaneously and C1 has been charged only 3.5 volts the base of Q1 will go negative, turning Q1 on. As Q1 is turned on, Q2 is held cut off and we are now in the "0" state as explained previously. Note, since the collector of Q1 was at -23 volts before the pulse occurred on pin 3 and there wasn't any change of collector voltage when the pulse did occur. The base of Q2 would not experience any change through C2. The output pins of the network are 5 and 8. When the network is in the "0" state pin 5 will be at 0 volts and pin 8 will be approximately -23 volts and the reverse is true when the network is in the "1" state. Although the description of operation has been based on voltages of +15 volts and -25 volts this network will operate equally on voltages of +12 volts and -20 volts or +10 volts and -15 volts.




Schematic,

TN90B Balanced Flip-Flop and Divider

Dwg. #A 103S90B

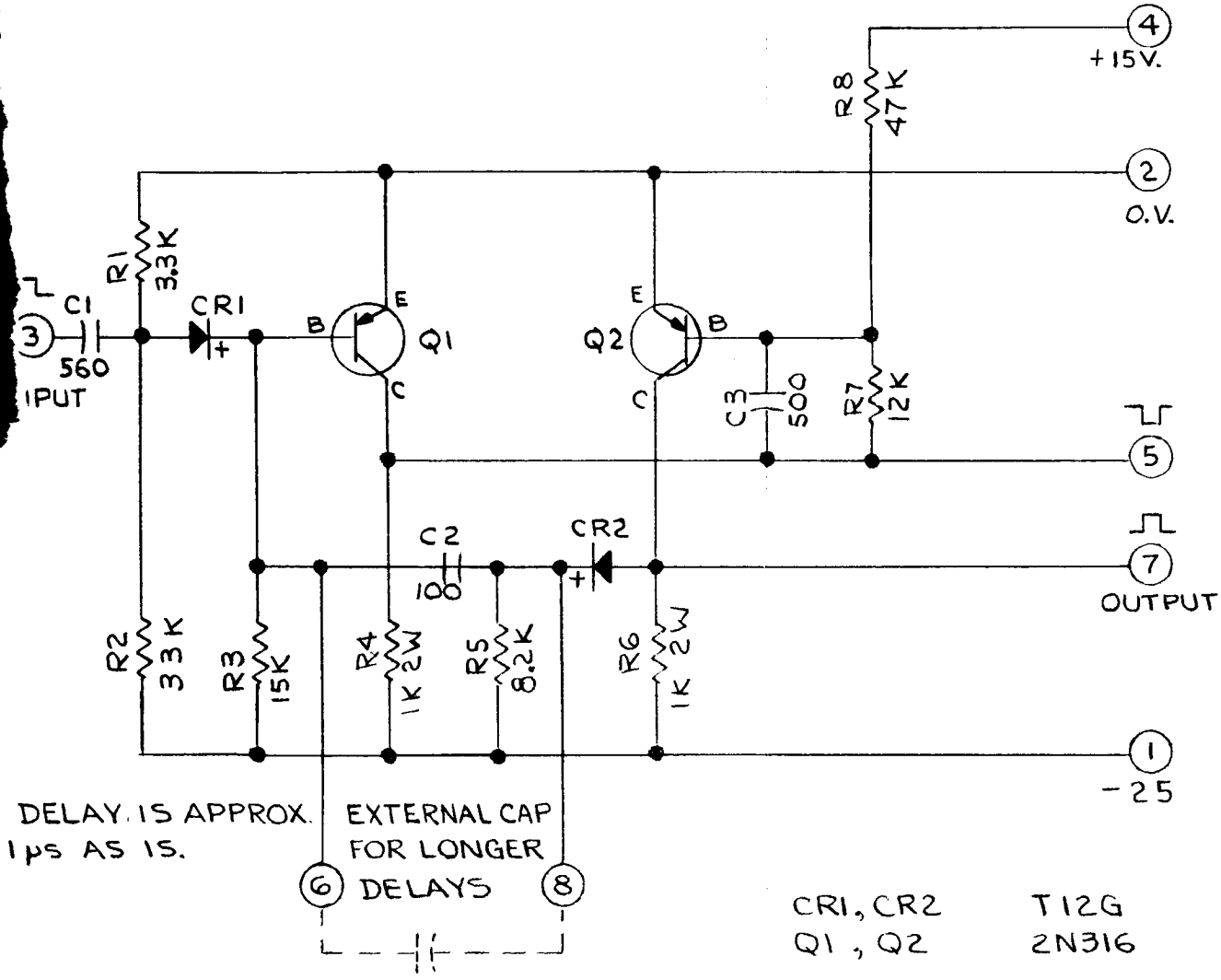
# TN 111
# ONE-SHOT (MONOSTABLE MULTIVIBRATOR)

The TN111 is a one-shot (monostable multivibrator) used for generating a pulse which can be varied from a minimum of one microsecond to well over 200 microseconds. In the quiescent condition, transistor Q1 is saturated by the base current through resistor R3. Since transistor Q1 is saturated, voltage divider R7 and R8 is connected between +15 volts and zero volts, establishing a reverse bias voltage on the Q2 base and keeping Q2 cut off.

Resistors R1 and R2 form a voltage divider, establishing a noise bias of approximately -2.5 volts, so that normal input noise will not trigger the network. A positive pulse of not less than 10 volts, with a rise time not greater than 0.5 microseconds, will trigger the network by cutting off transistor Q1. Transistor Q1 is cut off when the input pulse raises the base voltage of transistor Q1 above zero volts. Capacitor C1 is used to differentiate the input pulse so that a long duration input pulse will not affect the length of the output pulse.

With Q1 cut off, resistors R4 and R7 provide a path for the base current of transistor Q2, and Q2 saturates. The collector voltage of transistor Q2 will rise from -25 volts to almost zero volts. This rise in voltage is coupled to the base of transistor Q1 through capacitor C2, keeping transistor Q1 at cutoff until the R-C time of capacitor C2 and resistor R3 allows the base voltage of transistor Q1 to return to less than zero volts. Q1 saturates again and cuts off Q2.

This time can be lengthened by adding capacitance in parallel with capacitor C2. The terminals of C2 are brought out on pins 6 and 8 of the network. CR2 is used to decrease the fall time of the output pulse by preventing C2 from discharging through R6. Resistor R5 provides a dc path for the current of C2. This network will operate on lower power supply voltages, such as +12 and -20 volts, or +10 and -15 volts.




Schematic,

TN111 One-Shot Monostable Multivibrator

Dwg. #A103S111A

# TN 130 B
# CORE DRIVER

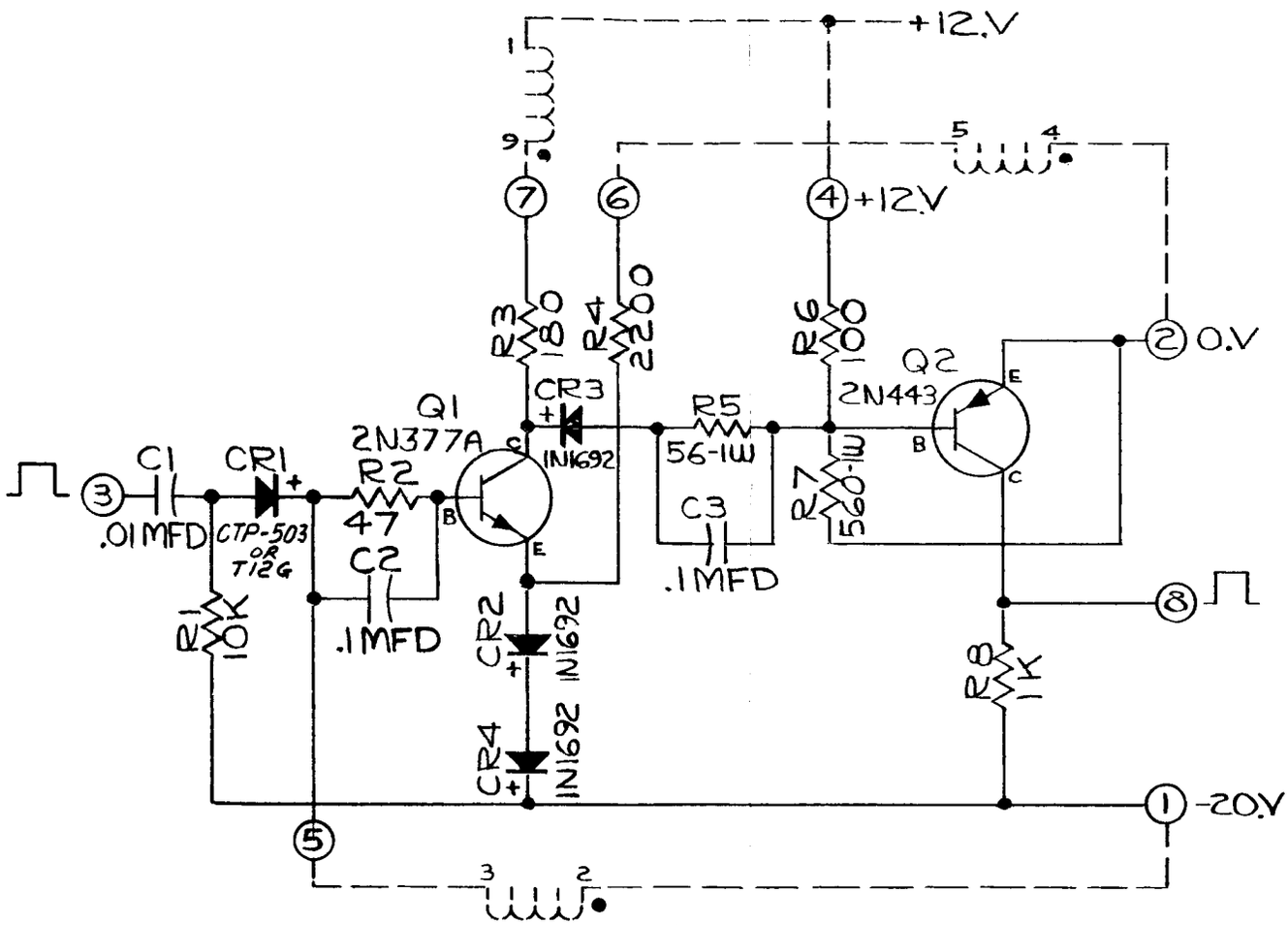
The TN130B is a blocking oscillator with amplifier which generates a positive going pulse from -20 volts to 0 volts, with a time duration determined by the core with which it is used. The TN130B is normally used with a MEC Model MN13 core, which gives it a pulse width of approximately 40 microseconds.

In the quiescent condition, transistor Q1 is maintained in cut off. The emitter voltage of Q1 is determined by the forward voltage drop of diodes CR2 and CR4 (1.5 volts) and is at approximately -18.5 volts. The base of Q1 is returned to -20 volts through R2 and the feedback winding of the core, connected from pin 5 to -20 volts. The d-c impedance of the feedback winding is approximately 5 ohms; thus the base of Q1 is nearly -20 volts, keeping Q1 reverse biased approximately 0.7 volts and properly cut off. Since there is no Q1 collector current, the collector voltage is +12 volts.

A positive going input pulse at pin 3 is coupled by capacitor C1, diode CR1, and capacitor C2, paralleled with R2 to the base of Q1. This pulse starts Q1 conducting. The resulting Q1 collector current passes through the collector winding of the external core. This generates a voltage across the collector winding coupled through the core to the feedback winding. By noting the phasing of the windings on the core, it can be seen that, as the collector voltage becomes negative, the voltage at pin 5 is becoming positive. This in turn drives Q1 further into conduction, even after the input pulse has been differentiated by C1. Q1 saturates in approximately one microsecond with an emitter-collector voltage of approximately 0.25 volts. Q1 will remain saturated as long as transformer action in the core continues to drive pin 5 of the TN network sufficiently positive to cause Q1 base current to flow. The pulse width (approximately 40 microseconds for an MN13 core) is determined by the characteristics of the core.

When the core material finally reaches saturation, transformer action in the core will cease, the feedback winding will no longer drive pin 5 positive, and Q1 base current will stop. This cuts off Q1. With no current in the collector winding of the core, the current in the reset winding resets the core. This reset current is furnished to the reset winding (pins 4 and 5 of the core) through resistor R4 and diodes CR2 and CR4. This involves going from the plus saturation condition attained during the output pulse to a minus saturation condition (reset). During this time, the voltages at the feedback winding and the collector winding are reversed. The reversal of a voltage at the feedback winding increases the reverse bias on Q1. The reversal of voltage in the collector winding tends to drive the output voltage somewhat more positive than the +12 volts on pin 7. It takes approximately 30 microseconds for the reset action to be accomplished.

The amplifier section Q2 is normally biased to cutoff by voltage divider R7 and R6. With no collector current flowing, the quiescent collector voltage of Q2 is -20 volts. The negative going pulse generated by the blocking oscillator section is coupled to the amplifier base through CR3, R5, and C3. The diode provides for rapid cut off of the amplifier, thereby minimizing the fall time. R5 and C3 serve as base current limiting and rise time determinants. The load is connected between -20 volts and 0 volts and should be limited to no less than 8 ohms (20 to 24 MN11 cores).




NOTE:
ALL RESISTORS ½ WATT ±10%
UNLESS OTHERWISE NOTED.

Schematic,

TN130B Core Driver

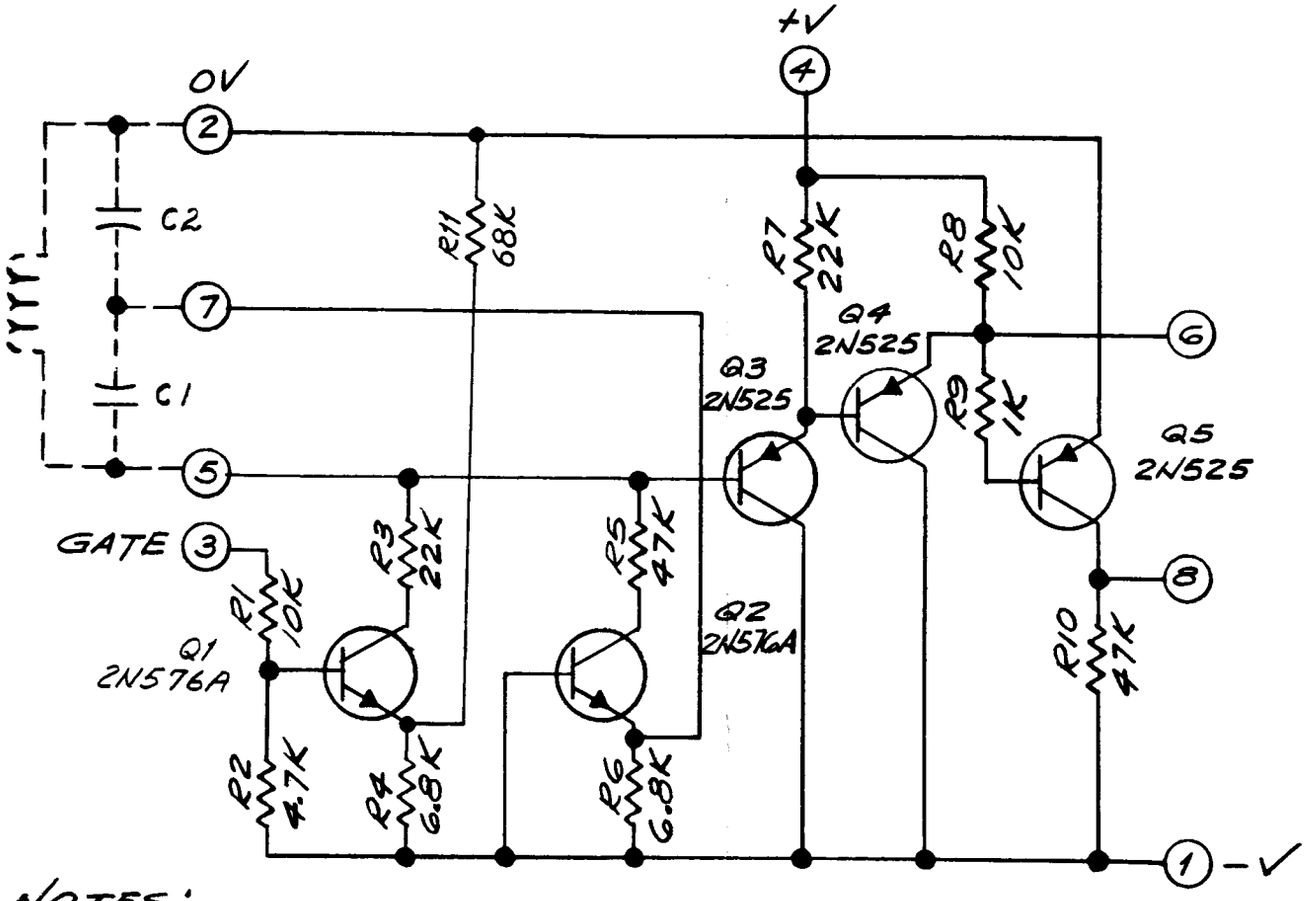
Dwg. #A103S130B

# TN 134
# GATED OSCILLATOR AND SQUARING CIRCUIT

The TN134 is a gated oscillator (80 cycles to 5 kilocycles per second), which can be turned on or off by an external switching circuit. The oscillator section (Q2) is followed by two emitter-followers (Q3 and Q4) and one squaring amplifier (Q5), which amplify and clip the signal so the output is a square wave. The oscillator tank circuit consists of an external inductor, connected between pins 2 and 5, and external capacitors C1 and C2. The oscillator is turned on by clamping pin 3 to the minus supply voltage, and is turned off by clamping pin 3 between -1 volts and 0 volts.

When the voltage at pin 3 equals the minus supply voltage, the input transistor Q1 will be at cutoff and will have little or no effect on the oscillator transistor Q2. The base of Q2 is returned to a minus voltage, cutting off Q2 and sending the tank circuit into oscillation. The first half cycle of the tank curcuit applies a positive voltage to the junction of C1 and C2, keeping Q2 cut off. C1 and C2 will be partially charged during this positive going portion of the cycle by current through R6. As the oscillation in the tank circuit reverses, the junction of C1 and C2 tends to become negative, driving Q1 toward saturation, and pulling the tank circuit negative through pin 5. When Q1 saturates the junction of C1 and C2 is no longer driven negative and Q2 cuts off, starting the cycle over again.

The phasing of the drive into Q1 is such that the tank circuit is pulsed at the proper portion of its cycle to maintain oscillation. The voltage across the tank circuit, pin 5, is coupled to the base of emitter-follower Q3. Q3 drives another emitter-follower Q4. Q4, in turn, drives amplifier Q5 from cut off to saturation. The resultant waveform at the collector of Q5 is a square wave which goes from the minus supply voltage to approximately 0 volts at the same frequency as the oscillator. When the oscillator is switched off again by the pin 3 voltage approaching 0 volts, Q5 will saturate and the output will remain at 0 volts. The supply voltages may be -25 and +15 volts, -20 volts and +12 volts, or -15 and +10 volts.




NOTES:

VOLTAGES +V +10 +12 +15
-V -15 -20 -25

C1:C2 = 1:10

ALL RESISTORS ARE 1/2 WATT UNLESS OTHERWISE SPECIFIED.

Schematic
TN134 Gated Oscillator and Squaring Circuit
Dwg.# A103S134A

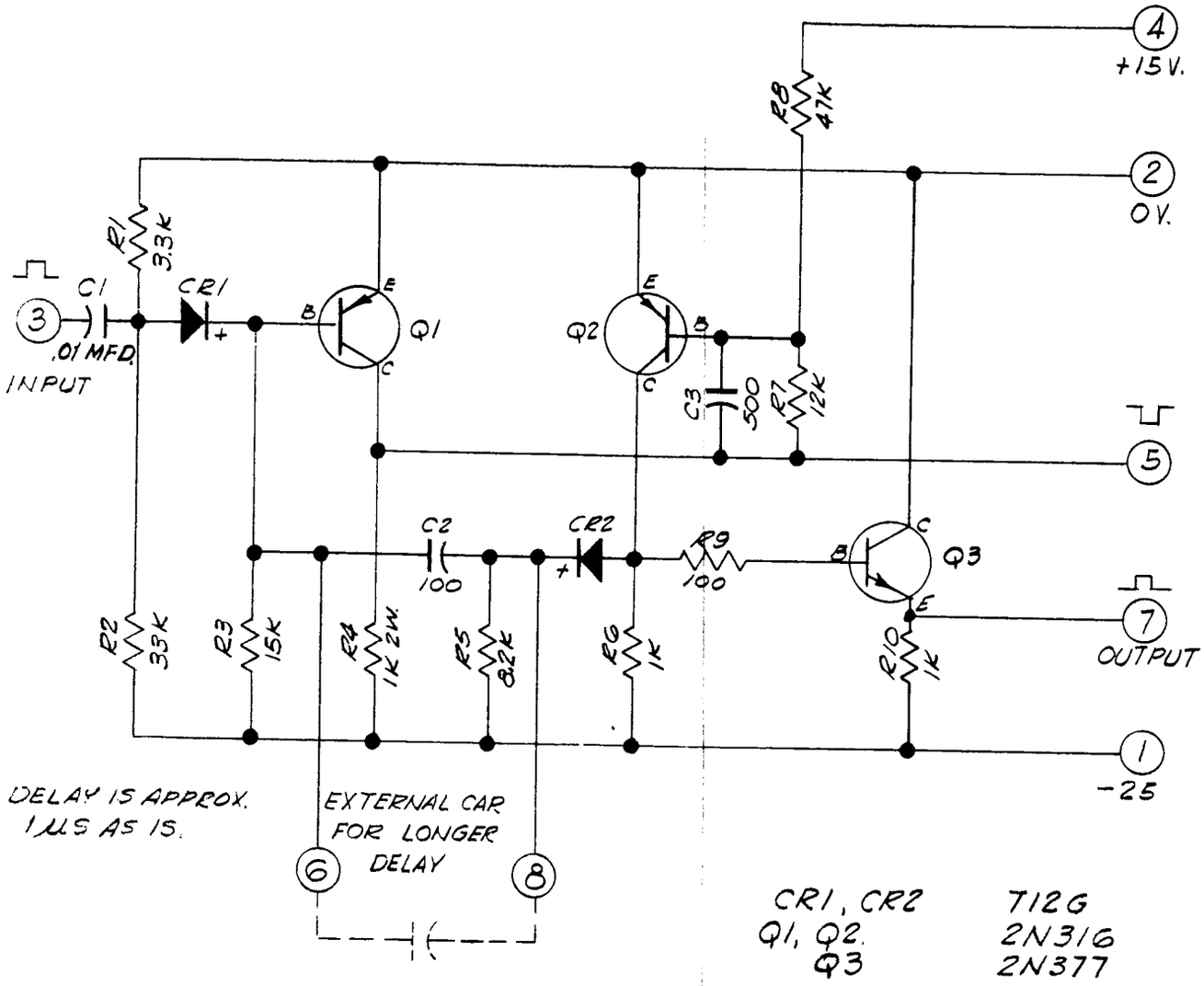
# TN 138
# ONE-SHOT WITH EMITTER FOLLOWER OUTPUT

The TN138 is a monostable flip-flop used for generating a pulse which can be varied in width from a minimum of about 2 microseconds to over 200 microseconds. In quiescent condition, transistor Q1 is saturated by the base current through resistor R3. Since transistor Q1 is saturated, voltage dividers R7 and R8 are connected between +15 volts and 0 volts, establishing a positive bias voltage on the Q2 base, and keeping Q2 cut off. Resistors R1 and R2 form a voltage divider, establishing a noise bias of approximately -2.5 volts, so that normal input noise does not trigger the network.

A positive pulse of not less than 10 volts, with a rise time not greater than 1 microsecond, will trigger the network by cutting off transistor Q1. Q1 is cut off when the input pulse raises the base voltage above 0 volts. Capacitor C1 is used to differentiate the input pulse so that a long duration pulse will not affect the length of the output pulse.

With Q1 cut off, resistors R4 and R7 provide a path for the base current of transistor Q2, and Q2 saturates. The collector voltage of transistor Q2 will rise from -25 volts to nearly 0 volts. This rise of voltage is coupled to the base of transistor Q1 through capacitor C2, keeping transistor Q1 at cutoff until the R-C time of capacitor C2 and resistor R3 allows the base voltage of transistor Q1 to return to less than 0 volts. Q1 now saturates again and cuts off Q2. This time can be lengthened by adding capacitance in parallel with capacitor C2.

The terminals of C2 are brought out on pins 6 and 8 of the network. CR2 is used to decrease the fall time of the output pulse by preventing C2 from discharging through R6. Resistor R5 provides a d-c path for current of C2. Q3 is the emitter-follower which will drive a load of 200 ohms.




| | |
|---|---|
| CR1, CR2 | T12G |
| Q1, Q2 | 2N316 |
| Q3 | 2N377 |

Schematic
TN138
Dwg. #A103S138

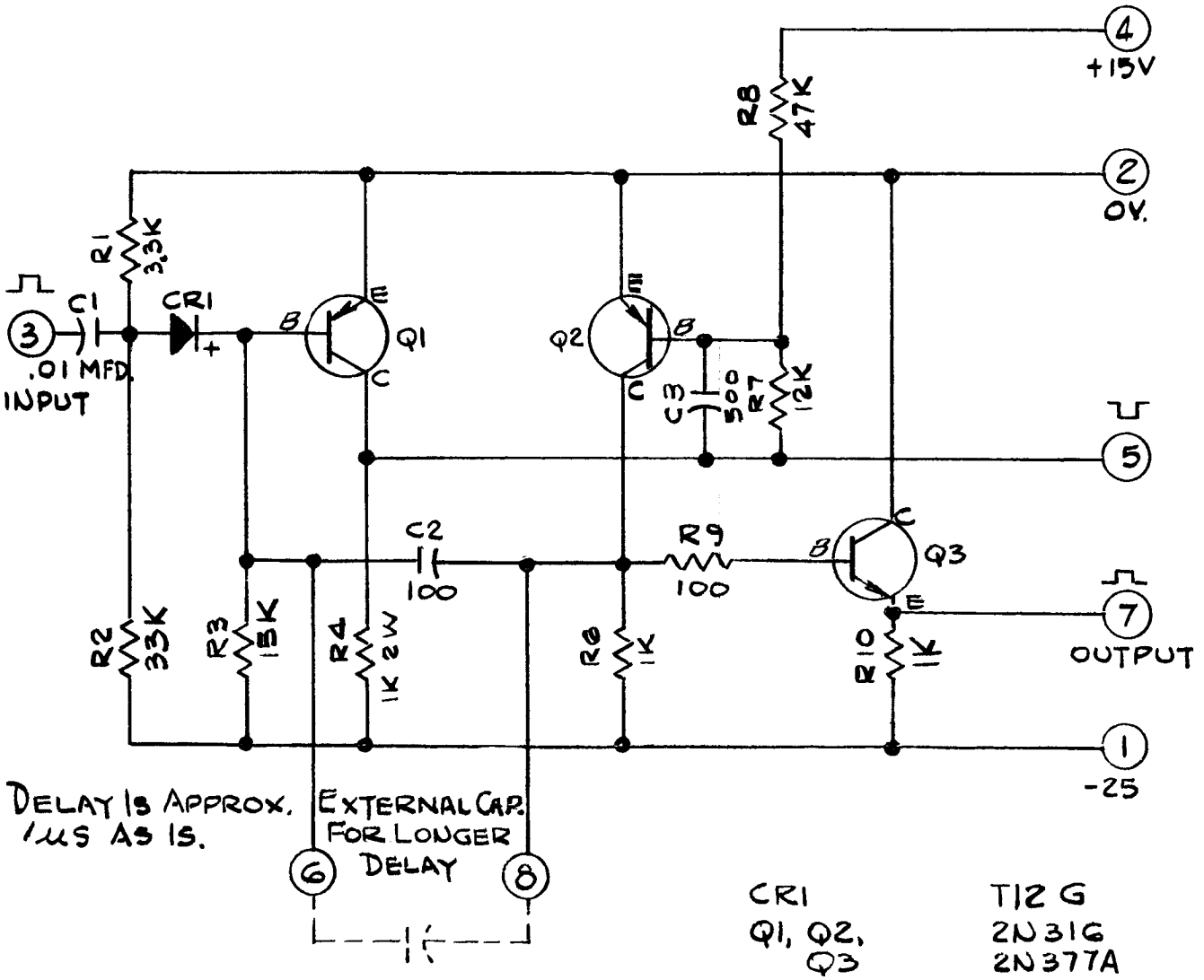
# TN 138 B
# ONE-SHOT WITH EMITTER FOLLOWER OUTPUT

The TN138B is a one-shot (monostable multivibrator) with an emitter follower output. This network can drive low impedance loads because of the emitter follower output.

The network's quiescent state is with Q1 saturated and with Q2 cut off. The base of Q1 is forward biased by R3 which is connected to -25 volts, thus saturating Q1. Since Q1 is saturated, the base of Q2 is reverse biased by the voltage divider R7 and R8 between +15 volts and the collector of Q1 (0 volts). With Q2 cut off, its collector is at approximately -25 volts; therefore the base of Q3 is at the same voltage as the emitter of Q3, keeping Q3 near cut off. Pin 7 will be at -25 volts and pin 5 will be at 0 volts. The resistor divider of R1 and R2 will maintain a reverse bias on diode CR1 of approximately 2.2 volts for protection against noise impulses. When a positive pulse of sufficient amplitude is applied to pin 3 to cause conduction of CR1, transistor Q1 will be cut off. The collector of Q1 will therefore go negative toward -25 volts. This negative going voltage potential is coupled to the base of Q2 through C3 and R7. This will cause the base of Q2 to go negative with respect to the emitter. Q2 will now conduct, and starts to saturate rapidly. The collector of Q2 will now go positive from -25 volts to 0 volts. This voltage change, being coupled through C2 to the base of Q1, will keep Q1 cut off after the input pulse has passed. C2 has now been charged, and will start to discharge through R3. When C2 has discharged sufficiently to allow the base of Q1 to return to its quiescent negative potential, Q1 will saturate. As Q1 saturates, its collector will go positive. Due to the resistor divider of R7 and R8, the base of Q2 will also go positive, reverse biasing Q2 and cutting it off. The one-shot has now returned to its quiescent condition.

The time constant of R3 and C2 determines the pulse width, which is about 1 microsecond. By adding external capacity across pins 6 and 8, the RC time constant is increased and thus the pulse width is increased. When Q2 is saturated, the base of Q3 will be positive in respect to the emitter, and this will cause Q3 to go into saturation. Pin 7, the output of the emitter follower, will go to 0 volts. Q3 will be in saturation as long as Q2 is in saturation. When Q2 is cut off, Q3 will be near cut off, and pin 7 will return to -25 volts.

Although the description of operation has been based on voltages of +15 volts and -25 volts, this network will operate equally on voltages of +10 volts and -15 volts.




Schematic,

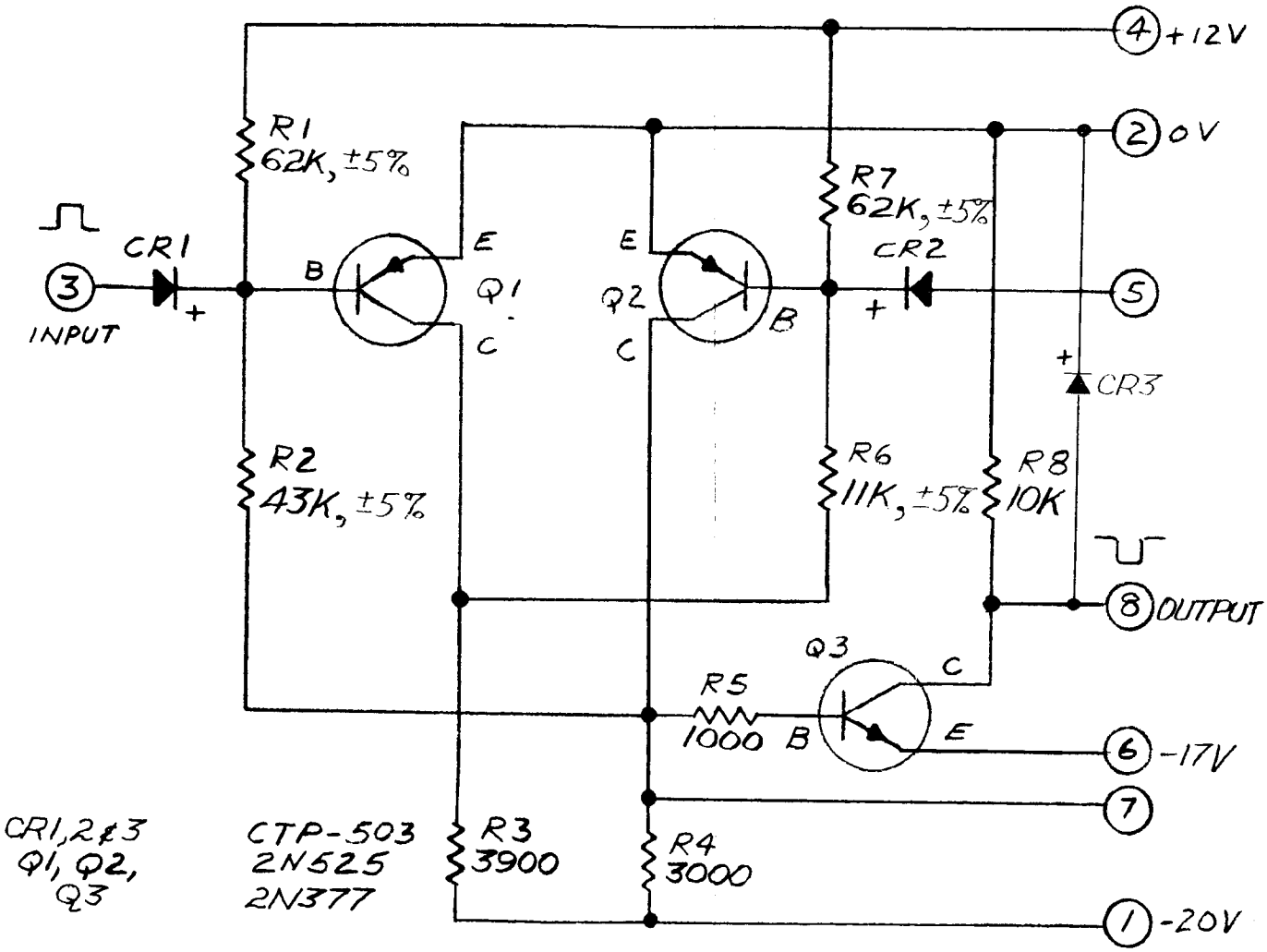
TN138B One-Shot with Emitter Follower Output

Dwg. #A103S138B

# TN 144
# FLIP-FLOP WITH PULSE AMPLIFIER OUTPUT

A TN144 is a bistable flip-flop with a pulse amplifier output which can be used to drive a load of 85 ohms or more. Since most flip-flops are limited to the amount of loading, which affects the switching of the flip-flop, a pulse amplifier has been added to permit greater loads. A transistorized neon indicator may be connected in parallel with the load to indicate the states of the flip-flop. The network is normally defined as being in the "0" state when transistor Q1 is saturated and Q2 and Q3 are cut off. The "1" state is the condition when Q1 is cut off and Q2 and Q3 are saturated. Assuming that Q1 is saturated ("0" state), then its collector is at approximately -0.25 volt. Resistors R7 and R6 are then connected from +12 volts to 0 volts, and by divider action hold the base of Q2 at approximately +1.8 volts. Since the emitter of Q2 is at 0 volts, this reverse bias keeps Q2 cut off. With Q1 saturated, its base is at approximately -0.5 volt, so the current through resistor R1 is approximately 0.2 milliamps. Since Q2 is cut off, its collector is at approximately -19 volts, and the current through R2 and R4 is therefore 0.4 milliamps. The difference between the currents in R1 and R2 is the base current of Q1, which is sufficient to clamp Q1 in saturation. This mode of operation is therefore stable. Q3 is cut off when Q2 is cut off, since the base of Q3 is at -19 volts, reverse biasing the emitter. Since Q3 is cut off, there is no collector current (except for leakage) and pin 8 is at approximately 0 volts. The input voltages at pins 3 and 5 must be somewhat negative during quiescent conditions. The flip-flop may be triggered to the "1" state by raising the voltage at pin 3 to a positive value so that diode CR1 conducts, thus raising the base voltage of Q1 to a positive value. Note that the input pulse will be loaded somewhat, so it cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cuts off. With Q1 cut off, R7 and R6 are no longer connected between the +12 volts and 0 volts, and Q2 is no longer clamped off. Instead, base current of Q2 may now flow through resistors R6 and R3, cuasing Q2 to saturate. Now resistors R1 and R2 are connected from +12 volts to 0 volts, and clamp the base of Q1 at approximately +5 volts, holding Q1 in a cut off condition after the input pulse passes. As Q2 is saturated and its collector goes positive, the base of Q3 goes positive enough to allow Q3 to saturate. R5 limits the base current of Q3. As Q3 saturates, pin 8 (the output pin) goes negative to approximately -17 volts. R8 is the collector load resistor of Q3, to furnish a minimum collector current when there is no external load from pin 8 of the network to 0 volts. This is the other stable condition which will be maintained until Q2 is cut off by a positive pulse on pin 5. A positive pulse (normally called reset) on pin 5 will allow base current from Q1 to be conducted through R2 and R4, driving Q1 back into saturation and restoring the initial condition. Diode CR3 is included to suppress the inductive effects of an external relay coil (if used) connected across pins 8 and 2. As Q3 goes from saturation to cut off, the relay coil is de-energized. However, the inductance of the relay coil attempts to

maintain the current through it by driving the voltage at pin 8 much more positive than 0 volts. If this were allowed to happen, Q2 could be damaged by the excessive collector-emitter voltage. During most phases of the cycle, CR3 is reverse biased; consequently, it does not enter into the operation of the circuit. When the relay is de-energized and pin 8 is driven positive by the relay inductance, CR3 is forward biased and conducts, providing a path for the current through the relay coil and eliminating the excessive transient voltage to appear on the collector of Q3.




Schematic,

TN144 Flip-Flop with Pulse Amplifier Output

Dwg. #A103S144A

# TN 154
# SHIFT REGISTER FLIP-FLOP
# WITH EMITTER FOLLOWER OUTPUT

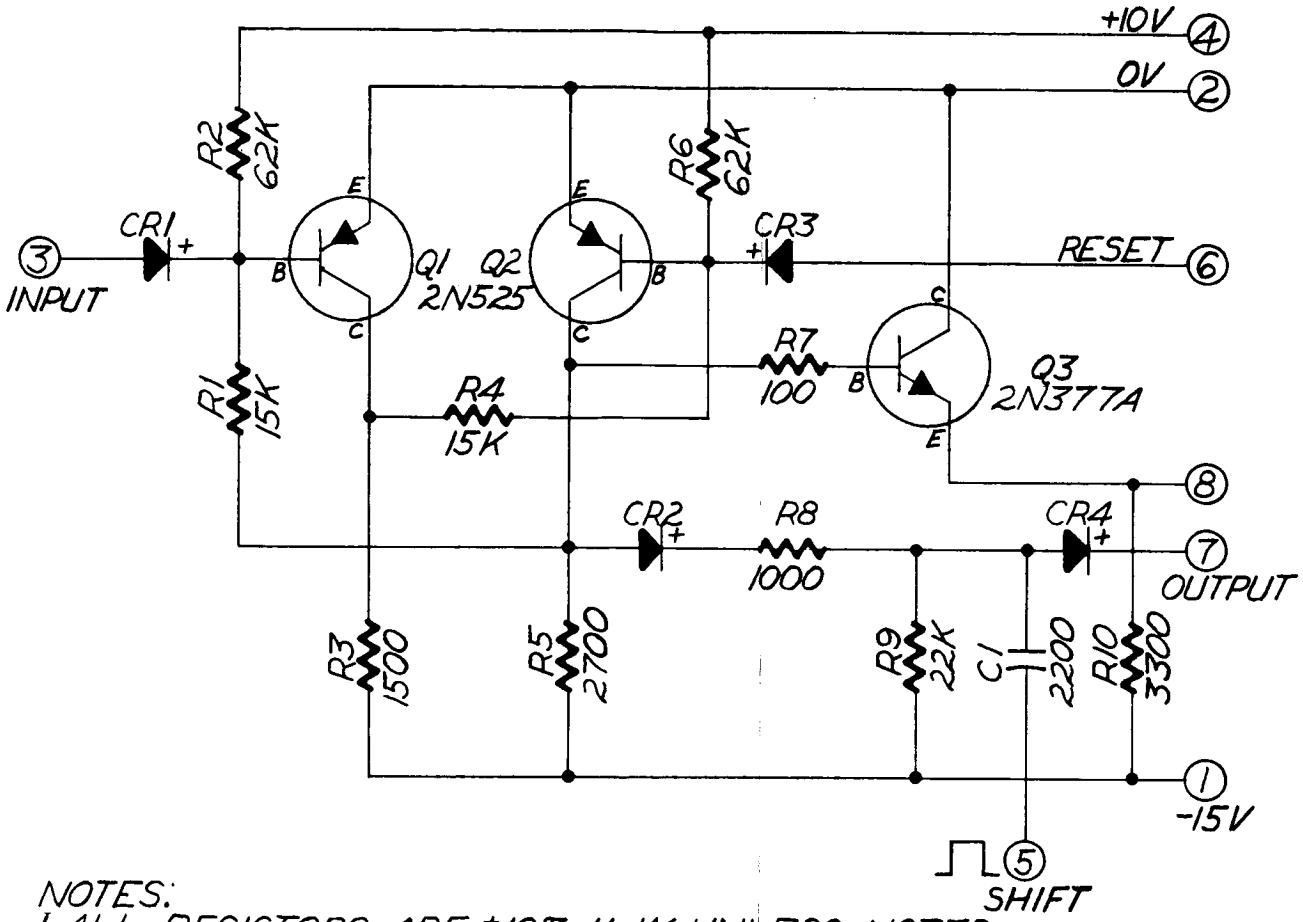
The TN154 is a bi-stable flip-flop normally used in a shift register which has an internal shift network and an emitter follower as an output. The internal shift network is used as the shift register serial output; that is, pin 7 of one TN154 is directly coupled to pin 3 of the next TN154. The emitter follower output, pin 8, is used to read out data in parallel from the shift registers. A transistorized neon light is normally connected, in parallel with the load, to pin 8, to indicate the states of the flip-flops. The light is lit when the network is in the "1" state, and off when the network is in the "0" state.

The "0" state is defined as the condition when Q1 is saturated and Q2 and Q3 are cut off. The "1" state is the condition in which the reverse is true. Assume Q1 is saturated ("0" state); then the collector voltage of Q1 will be approximately 0 volts, and the resistor divider of R4 and R6 will maintain +2 volts on the base of Q2. This will constitute a reverse bias on Q2, keeping it cut off. With Q2 cut off, resistors R1 and R5 will provide a path for Q1 base current, clamping Q1 in saturation. Since Q2 is cut off, its collector will be at approximately -13 volts; therefore the base of Q3 will be at -13 volts. This will keep Q3 near cut off, and the data output, (pin 8), will be at -13 volts. This condition is stable and will not be changed until a positive pulse above 0 volts on pin 3 causes CR1 to conduct. When CR1 conducts, the base of Q1 is driven positive above 0 volts, reverse biasing Q1, and subsequently cutting H off. As Q1 is cut off, its collector will go negative; due to the resistor divider, R4 and R6, the base of Q2 will also go negative. As the base of Q2 goes negative, Q2 will go into saturation. As Q2 saturates, its collector will go positive and, due to the resistor dividers R1 and R2, the base of Q1 will be clamped at approximately +2 volts. This keeps Q1 cut off after the input pulse has passed. Also at this time the base of Q3 will go positive, like the collector of Q2, and Q3 will saturate. Therefore the emitter of Q3 and pin 8 will go to 0 volts. The network is now in the "1" state and will remain there until reset by a positive pulse above 0 volts on pin 6. When this does occur, the network will go to the "0" state as described previously and pin 8 will go to -13 volts.

When Q2 is conducting, (a pulse has occurred on pin 3), capacitor C1 charges through CR2 and R8. CR2 is used to prevent the shift pulse from back triggering the flip-flop and to keep the charge on C1 from leaking off rapidly through R5. When shifting information through the register, the shift input, (pin 5) goes from -10 volts to approximately 0 volts for 5 microseconds. If the TN is in the "0" state, the junction of C1 and CR4 will go from -14 volts to -4 volts and back to -14 volts. If the TN is in the "1" state, this junction will move from -2 volts to +8 volts and back to -2 volts. In a shift register, pin 7 of one TN154 is connected to pin 3 of the next TN154. The pulse at the junction of C1 and CR4 will have no effect on the next flip-flop unless it goes above 0 volts. This will occur only if a "1" (Q2 saturated) is present in the first network. The reset pulse is necessary in order to reset all the TN's to a "0" state before the shift pulse, since transmitting a "1" or "0" to the next stage does not automatically remove a "1" from the preceding stage. In shifting, the 5 microsecond reset pulse first triggers all the TN's to the "0" state, and then the 5 microsecond shift pulse advances the "1" that has been temporarily stored in the capacitor. Capacitor C1 starts to discharge when the reset pulse cuts off Q2, but the RC time constant

of C2 and R9 is long enough so that it will not discharge significantly before the shift pulse occurs. CR2 will be charged 10 volts by the shift pulse. If the junction was at -2 volts ("1" state) before reset, the shift pulse will cause the junction to rise from -2 volts to +8 volts. CR6 will conduct, causing pin 5 of the next network to go positive, thus inserting a "1". If the junction was at -14 volts ("0" state) before reset, then this junction will rise to -4 volts when the shift pulse occurs, and CR6 will not conduct, because it is reverse biased. Therefore the next network will remain in the "0" state, and a "0" has been shifted.

Q3 is an emitter follower to isolate the flip-flop so that a lower impedence load can be driven from the parallel output of a shift register.




NOTES:
1. ALL RESISTORS ARE ±10%, 1/2 W UNLESS NOTED.
2. ALL DIODES ARE CTP-503 UNLESS NOTED.

Schematic
TN154
Dwg. # 103S154A

# TN 158
# CONTROLLED ONE-SHOT

The TN-158 is a controlled one-shot (mono-stable multivibrator) with an emitter follower output. It is controlled, because the unstable state may be terminated at any time by an input pulse on pin 5. This network can drive low impedance loads because of the emitter follower output.

The network's quiescent state is with Q1 saturated, and with Q2 cut off. The base of Q1 is forward biased by R3, which is connected to -20 volts, saturating Q1. Since Q1 is saturated, the base of Q2 is reverse-biased by voltage divider R6 and R7 between +12 volts and the collector of Q1 (0 volts). With Q1 saturated, its collector is at approximately 0 volts; therefore, the base of Q3 is at the same voltage, forward biasing Q3 and keeping it saturated. Therefore, pin 7 will be at approximately 0 volts. The resistor divider of R1 and R2 will maintain a reverse bias on diode CR1 of approximately 2 volts.

Now, when a positive pulse of sufficient amplitude is applied to pin 3 to cause conduction of CR1, transistor Q1 will be cut off. The collector of Q1 will therefore go negative toward -20 volts. This negative going potential is coupled to the base of Q2 through C3 and R7. This will cause the base of Q2 to go negative with respect to the emitter. Q2 will conduct, and starts to saturate rapidly. The collector of Q2 will now go positive (from -20 volts to 0 volts), and this voltage change, coupled through C2 to the base of Q1, will keep Q1 cut off after the input pulse has passed. When Q1 is cut off, Q3 will also be cut off, and pin 7 will go to -20 volts. C2 has now been charged, and will start to discharge through R3. When C2 has discharged sufficiently to allow the base of Q1 to return to its quiescent negative potential, Q1 will saturate. As Q1 saturates, its collector will go positive, and, due to the resistor divider R6 and R7, the base of Q2 will go positive. This reverse biases Q2, cutting it off. When Q1 is saturated, the base of Q3 will be positive with respect to the emitter, and this will cause Q3 to go into saturation. Pin 7, the output of the emitter follower, will return to 0 volts. The one-shot has now returned to its quiescent condition.

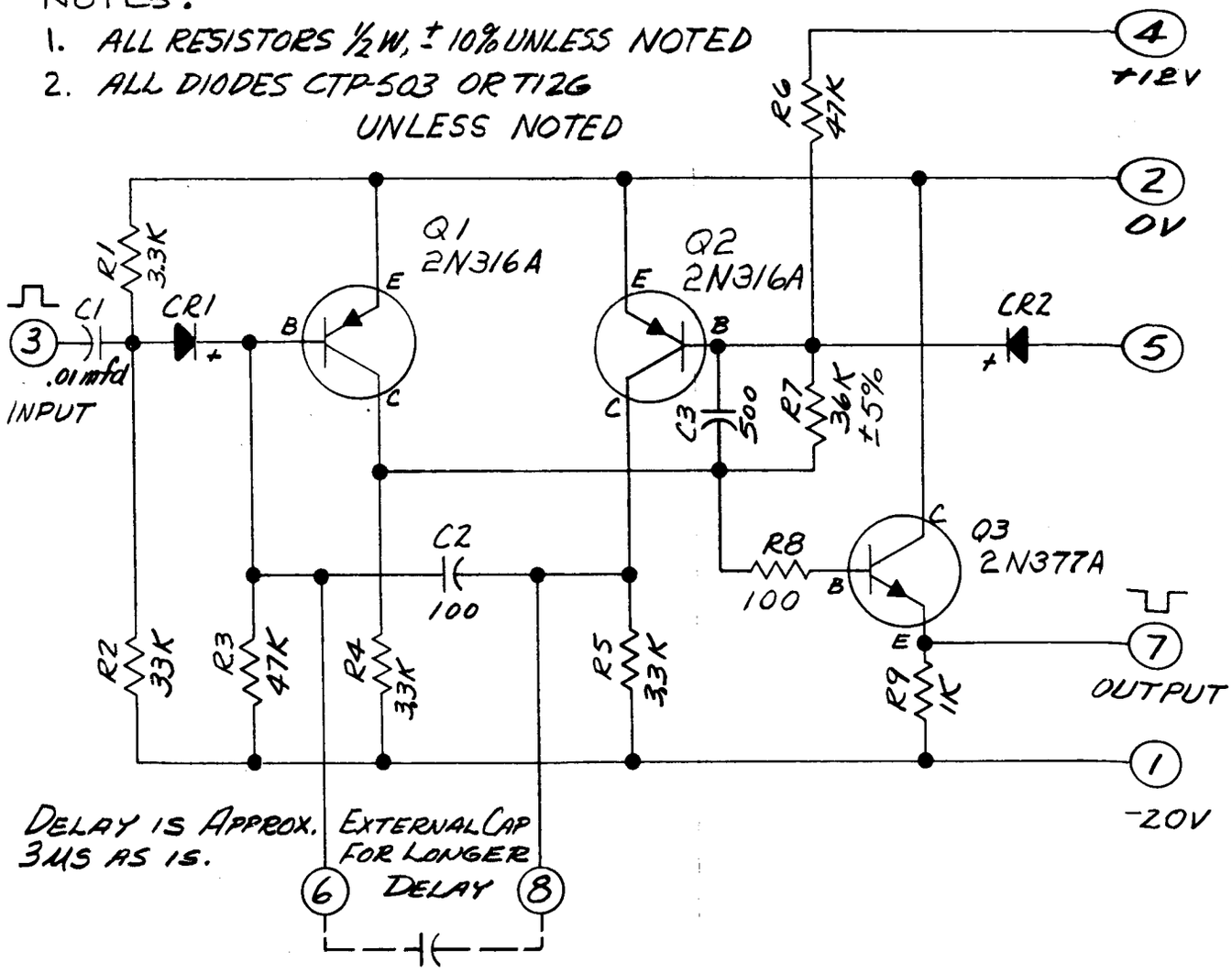
The time constant for R3 and C2 determines the pulse width, or the time duration of the unstable state, which is about 3 microseconds. By adding external capacity across pins 6 and 8, the RC time constant is increased, and thus the pulse width is increased. Pin 5 is an auxiliary input, and is used to shorten the existing time duration of the unstable state. That is, a positive pulse on pin 5 will cause Q2 to be cut off before the normal RC time of the circuit.

Assuming that the network is in the unstable state: Q1 is cut off and Q2 is saturated, while C2 is starting to discharge. A positive pulse, above 0 volts occurs on pin 5, causing CR2 to conduct. The base of Q2 will be reverse-biased, therefore Q2 will be cut off. As Q2 is cut off, its collector will go negative toward -20 volts. This negative going potential is coupled to the base of Q1 through C2. This will cause Q1 to be forward-biased, and it will start to saturate. Q2 will be held cut off by the same divider as explained previously. By cutting off Q2 from a pulse on pin 5, we have caused C2 to discharge rapidly; therefore, the one-shot is returned to its stable or quiescent state immediately.

Although the description of operation has been based on voltages of +12 volts and -20 volts, this network will operate equally as well on voltages of +10v and -15v.

NOTES:

1. ALL RESISTORS ½W, ± 10% UNLESS NOTED
2. ALL DIODES CTP-503 OR T12G UNLESS NOTED

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Dwg. #103S158A
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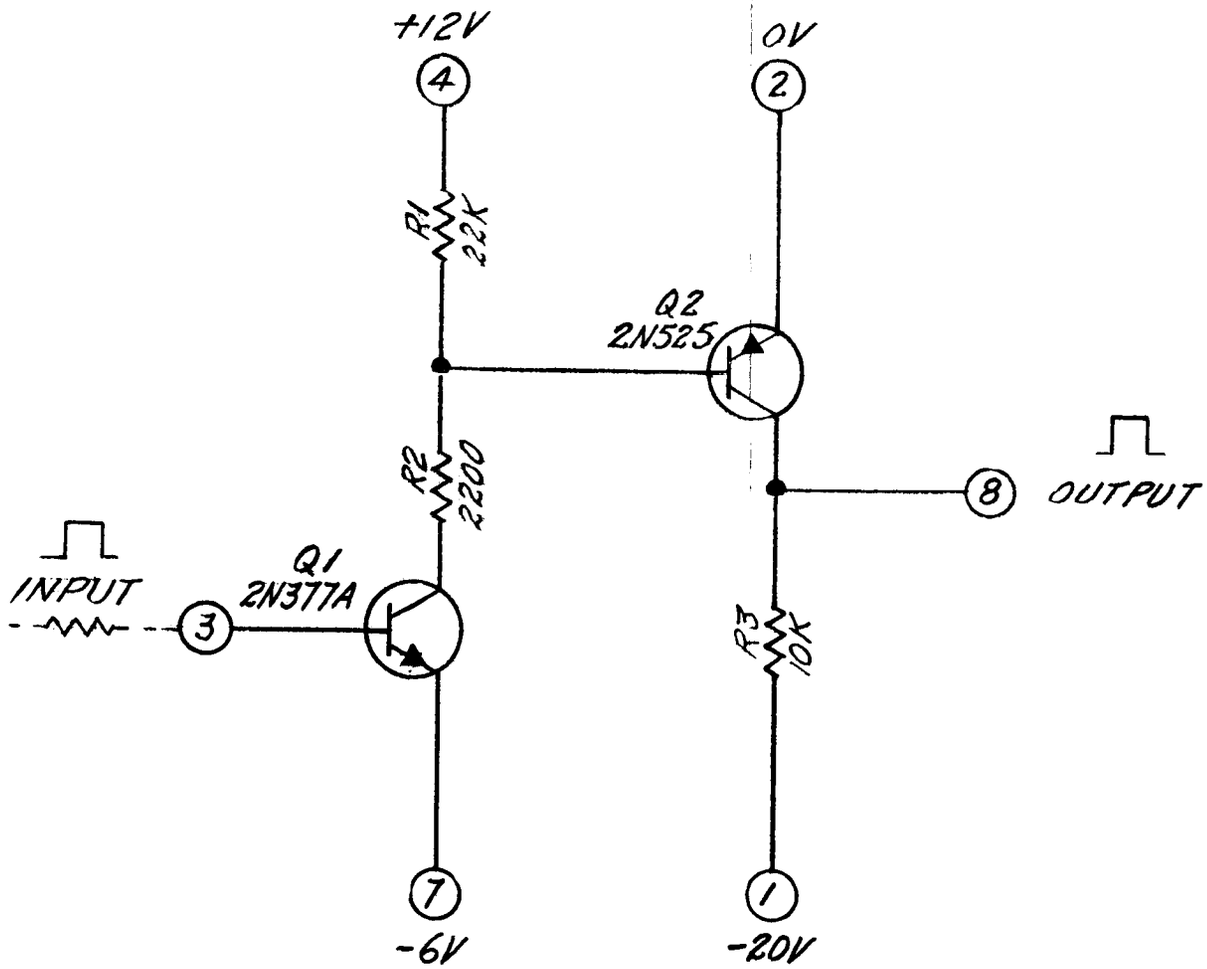
# TN 159
# PULSE AMPLIFIER

A TN159 is a two stage pulse amplifier. If this TN is connected to the power supply voltages as shown on the schematics, it may be operated as follows. With the emitter of Q1 at -6 volts, and the input to the base of Q1 through a series input resistor at a more negative voltage than -6 volts, then Q1 is cut off and the collector of Q1 is at +12 volts. With the collector of Q1 at +12 volts, then the base of Q2 is reversed bias and Q2 is also cut off. With Q2 cut off, the collector voltage of Q2 on pin 8 is at -20 volts. When the input to pin 3 is raised to a more positive voltage than -6 volts, then Q1 is forward bias and saturates. When Q1 is saturated, its collector voltage is -6 volts. R1 and R2 form a voltage divider between +12 volts and the collector of Q1 which is at -6 volts. The junction of R1 and R2 is connected to the base of Q2, therefore forward biasing Q2 and causing it to saturate. With Q2 saturated, the collector output (pin 8) is at 0 volts. Therefore, a small voltage change on either side of -6 volts on the input of pin 3 will cause a 20 volt change on the pin 8 output.

This network will operate on lower power supply voltages provided the -20 volts and +12 volts are decreased in proportion and that the pin 7 voltage is between -3 volts and -10 volts.

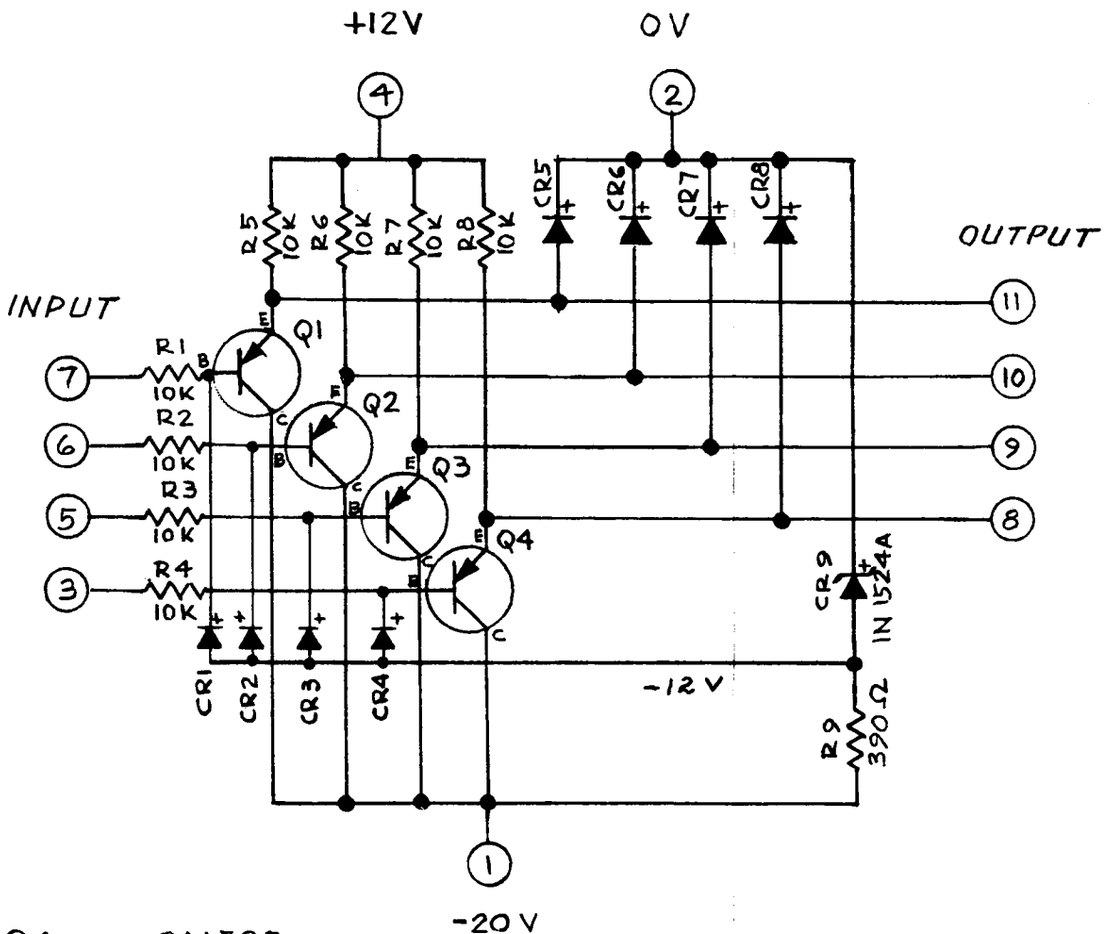



Schematic
TN159
Dwg. #103S159A

# TN 161
# FOUR EMITTER FOLLOWERS WITH DIODE CLAMPS

The TN161 is a network consisting of four independent emitter followers. The description of operation that follows will be for one emitter follower since all four circuits are identical.

The typical inputs are d-c levels, -20 volts (a "0") and 0 volts (a "1"). When the input, pin 7, is at -20 volts, CR1 will be forward biased and will conduct, causing the base to stay at -12 volts. The -12 volts is derived from a zener diode CR9 and resistor R9, connected between 0 volts and -20 volts. Q1 is now forward biased and its emitter will follow the base; i. e., the emitter is at -12 volts. Since the emitter of Q1 is a -12 volts, pin 11 is at -12 volts. The output will not change until the input voltage goes above -12 volts. As the input voltage on pin 7 goes positive, from -20 volts to -12 volts, the voltage at the base of Q1 does not change; but as the input goes more positive (from -12 volts to 0 volts), CR1 will now be reverse biased, and the base will rise to 0 volts, like the input. As the base goes positive, the emitter will follow, and also will pin 11. Any further increase of the input above 0 volts will not change voltage of the output since the output is damped at 0 volts with CR5.




Q1-Q4 2N525
CR1-CR8 CTP 503

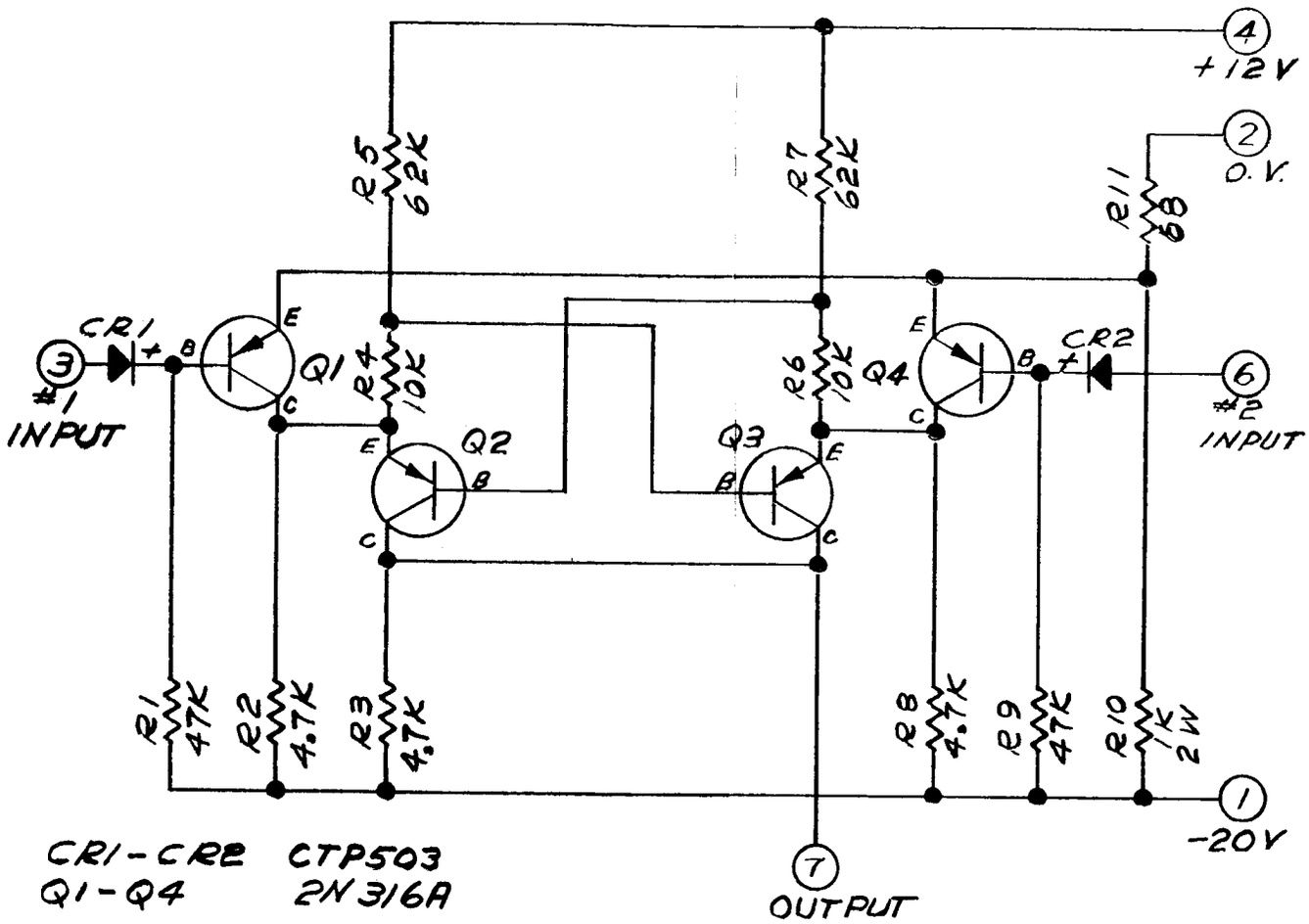
Schematic
TN161
Dwg. #103S161A

# TN 162
# PULSE COMPARATOR

The TN162 is a pulse comparator which compares the input pulses on pins 3 and 6 of the network. Basically the operation of the network is that if there is no inputs on pin 3 or pin 6 there will be no output on pin 7, i. e., it will be at -20 volts. If pin 3 or pin 6 has an input which is a pulse from -20 volts to 0 volts, there will be an output pulse on pin 7 which will be from -20 volts approximately to -3 volts. If both pin 3 and pin 6 has an input, then there will be no output from pin 7. The two inputs pin 3 and pin 6 are symmetrical inputs, in fact the complete network is a symmetrical network. Transistors Q1 and Q4 control the action of Q2 and Q3. Whenever Q1 and Q4 are in the same state, both Q1 and Q2 are cut off and there is no outputs on pin 7. Whenever Q1 and Q4 are in a different state, the symmetrical network is unbalanced and either Q2 or Q3 will conduct and pin 7 will go to -3 volts. If pin 3 has a "1" (0 volts) input, then Q1 is reversed biased and is cut off because the emitter of Q1 is maintained at approximately a -2 volts by the voltage divider R11 and R10. If the other input pin 6 is a "0" or -20 volts, then Q4 is saturated by the base current through R9 and the emitter and collector voltages are almost identical, which is at approximately -2 volts.

Divider network R6 and R7 then hold the base of Q2 at approximately +1 volt while divider network R2, R4 and R5 hold the emitter of Q2 negative, hence Q2 is cut off. Q3, however, is saturated because base current of Q3 can flow through R2 and R4 while the emitter is at -2 volts. The collector current of Q3 (flowing through R3) forms a voltage output on pin 7 which is at approximately -3 volts. If both pin 6 and pin 3 inputs are a "0" or -20 volts, then Q1 and Q4 are both saturated and Q2 and Q3 are both cut off and there is no current flowing through R3; hence pin 7 is at -20 volts. If both inputs are "1"s, then Q1 and Q4 are both cut off so Q2 and Q3 are cut off since their bases are still more positive than their emitters. This action allows this network to compare the two inputs to see if the inputs are alike. It can be briefly stated: unlike inputs give an output but like inputs give no output.

This network may be operated on lower power supplies voltages such as -15 volts and +10 volts.




Schematic
TN162
Dwg. #103S162A