A STUDY OF HIGH-SPEED AD AND DA CONVERTERS USING REDUNDANCY TECHNIQUES

By

DR. HAROLD MOTT
Associate Professor of Electrical Engineering
Project Director

and

CHESTER C. CARROLL
Instructor in Electrical Engineering
Associate Project Director

June, 1964

INTERIM REPORT

Prepared for
National Aeronautics and Space Administration
Marshall Space Flight Center
Huntsville, Alabama

Under

CONTRACT NUMBER NAS8-5341

Bureau of Engineering Research
University of Alabama

N66 27750

ABSTRACT

The results of a literature survey are presented with circuit diagrams and block diagrams of the most desirable methods of analog-to-digital conversion. There is discussion of each technique which explains the theory of operation and some of the problems encountered in the designs.

A versatile voltage amplitude comparator is reported with suggestions for its use in all basic encoder types and with design procedures which will provide increased voltage sensitivity. To indicate further the use of the comparator, a three (3) bit encoder design is presented.

The results of a reliability analysis performed on a twelve (12) bit decoder prototype designed and constructed by Ford Instrument Company are reported.

Author

ACKNOWLEDGEMENT

This report has been prepared for the Navigation Branch, Astrionics Division, George C. Marshall Space Flight Center, Huntsville, Alabama under Contract NAS8-5341.

The authors wish to acknowledge the assistance of Professor Longino A. Woodman, Director, Bureau of Engineering Research, in handling administrative details of the work. The valuable work of Mr. Tommy D. Steele and Mr. Hubert T. Nagle, student assistants, in drawing the figures and performing the reliability analysis calculations herein is gratefully acknowledged. Also, the authors are particularly grateful to Mr. Hugh Taylor and Mr. George Kirby of the Astrionics Division for their excellent counsel during the work period.

TABLE OF CONTENTS

ABSTRACT ---------- i
ACKNOWLEDGEMENT ---------- ii
TABLE OF CONTENTS ---------- iii
LIST OF ILLUSTRATIONS ---------- iv
LIST OF TABLES ---------- v
I. INTRODUCTION ---------- 1
II. ELECTRONIC AD CONVERSION METHODS ---------- 3
A. Coding Tubes ---------- 4
1. Point Beam Coding Tube ---------- 5
2. Sheet Beam Coding Tube ---------- 7
3. Cylindrical Beam Coding Tube ---------- 11
4. Segmented Sheet Beam Coding Tube ---------- 13
B. One Bit Encoding Stages ---------- 13
C. Two Bit Encoding Stages Using Delay Channels ---------- 21
D. Time Base Encoders ---------- 23
E. Peripheral Components ---------- 24
1. Diode Bridge Sampler ---------- 25
2. Tunnel Diode Sampler ---------- 28
References ---------- 31
III. A VERSATILE COMPARATOR FOR ENCODING DEVICES ---------- 33
A. Introduction ---------- 33
B. A Versatile Comparator ---------- 34
C. An Encoder Using Nth Stage Comparators ---------- 48
References ---------- 56
IV. RELIABILITY ANALYSIS OF FORD INSTRUMENT DECODER ---------- 57
References ---------- 66
BIBLIOGRAPHY ---------- 67

LIST OF ILLUSTRATIONS

Fig.	Title	Page
1.	Electron Beam Deflection Tube for Coding	6
2.	Sheet Beam Coding Tube	8
3.	Coding Tube with Quantizing Grid and Circuit Schematic	10
4.	Schematic Sectional View of Cylindrical Coding Tube	12
5.	Block Diagram of Cascade of One-Bit Encoding Stages	14
6.	Circuit Diagram of One-Bit Encoding Stage	14
7.	Block Diagram of High Speed Encoding System	17
8.	Logic Diagram for High Speed Encoding System	18
9A.	Logical Representation and Schematics of Logic Gates	19
9B.	Logical Representation and Schematics of Logic Gates	20
10.	Block Diagram of Delay Channel Encoder	22
11.	Diode Bridge Sampler	26
12.	Diode Pulse Generator	26
13.	Tunnel Diode Sampler	29
14.	Interrogation and Reset Pulse Generator	29
15.	The Compare Circuit	35
16.	Tunnel Diode Characteristics and Switching Load Line	37
17.	Reduced Equivalent Circuit	40
18.	Highly Sensitive Comparator	45
19.	Transfer Characteristic for Saturating Difference Amplifier	47
20.	An Nth Stage Encoder	49
21.	Ford Instrument Decoder	58
22.	Application Factors, K_A - Transistors, Silicon	60

LIST OF TABLES

Table	Title	Page
1.	Component Values for Versatile Comparator	43
2.	Voltage Levels and Binary Code for the Nth Stage Encoder	54
3.	Experimental Data	63
4.	Operating Power	64
5.	Mean-Time-To/Between Failures	65

I. INTRODUCTION

There has been considerable effort expended in the study of electronic analog-to-digital converters by several investigators who have had different objectives in mind. Section II of this report is a summary of the more attractive techniques which vary in classification from low precision - high speed to high precision - low speed. Some of these techniques require very sophisticated and unique design procedures while others are conventional and thereby versatile to some extent.

In surveying the literature concerned with analog-to-digital converters there seemed to be a need for accurate voltage amplitude comparison in most all techniques. The types of comparison required vary with each method of conversion which indicates the need of versatility in a single comparator or the use of a specialized design in each converter. Section III presents a method of comparison which is versatile with respect to voltage encoding range, encoding speed, and which may be utilized in all encoders requiring comparators. The versatility of this comparator is discussed extensively and the necessary modifications which would specialize this comparator for several applications are presented. Also, a unique encoder design is included which illustrates the use of the basic comparator. This particular encoder is suitable for high speed operation with relatively low precision and it does not require sample and hold circuitry which is a considerable advantage over some encoders. The use of the basic compare circuit to perform each stage of comparison suggests that it may be prepared in module form which would increase its value as a versatile comparator.

The results obtained from testing the Ford Instrument digital-to-analog converter are tabulated in Section IV to illustrate the stress levels of all components and the difference in stress levels experienced by using several types of transistors. Since the converter is only a workable prototype the reliability figures obtained will not be accurate for an integrated circuit design using this same scheme, but the procedure followed in the reliability analysis and the relative amounts that each stage is stressed should be useful in calculating a theoretical reliability figure and in the determination of the operating reliability of an integrated circuit design.

II. ELECTRONIC AD CONVERSION METHODS

In the past few years, high-speed analog-to-digital conversion techniques have enjoyed a rapidly increasing demand. When the speed of conversion is increased, the precision and the reliability of the device suffers to the extent that in some designs obtaining the required precision and the desired reliability is impossible and in other designs impractical. This suggests the decision of whether or not to sacrifice precision and reliability for speed and alludes to the desirability of optimum conversion with respect to high precision and reliability with a substantial increase in speed.

Considerable effort has been expended in the literature survey to uncover and summarize the techniques of AD conversion which will allow practical devices to be constructed so that they will demonstrate sufficient reliability and speed for specified precision. This has focused the design procedure in a manner such that the desired precision may be specified and the reliability of the device may be calculated and improved to lie above a specific value. This procedure is very desirable in that once the amount of desired precision is established, the above mentioned considerations can be used in producing a highly reliable device which will operate at the given precision.

There are several terms used in the literature and in this report which are defined below:

> DIGITIZING TIME is the time required to convert a particular value of an analog signal to a digital word. This includes pulse sampling time. Terms which are used synonymously with digitizing time are BIT RATE and CONVERSION RATE.
>
> PRECISION refers to the number of binary bits being used in representing a pulse.
>
> CONVERSION ACCURACY is the accuracy with which the converter measures the height of each input pulse.

QUANTIZATION is the process of dividing the total input amplitude range into finite steps and arranging that input voltages falling within each step produce one and only one output pulse group.

QUANTIZATION ERROR is the difference between the analog signal being encoded and the decoded value of the digit produced by that stage.[1]

CONVERTER RELIABILITY is a measure which indicates how long a converter will produce rated precision accurately.

Electronic analog-to-digital conversion techniques include coding tubes, feedback encoders, parallel encoders, time-base encoders, and solid-state encoders. All of these techniques will be discussed in the following sections and systems using them will be illustrated.

A. Coding Tubes

The idea and practice of utilizing beam coding tubes to encode an analog signal has been in existence for some time, but the use of them has been very limited. The reason for their limited use is inexplicable in view of the low cost involved, the high speeds that can be attained, and the simplicity of encoders which use coding tubes. It is understood that the use of these tubes in airborne equipment is prohibited by certain problems which arise; however, their use in ground equipment seems desirable.

There are four basic types of coding tubes, (1) those using a point electron beam, (2) those using a sheet electron beam, (3) those using a cylindrical sheet electron beam, and (4) those using a segmented sheet electron beam. All of these are cathode

---

1: Superscripts refer to references at the end of each chapter.

ray tubes in which the electron collecting screen is replaced by a binary coded mask and a segmented collecting screen.

1. Point Beam Coding Tube

A point beam coding tube consists of an electron gun, horizontal deflection plates, vertical deflection plates, coding mask, and a segmented collecting plate as indicated in Fig. 1.[2] The coding mask is aligned with the horizontal and vertical deflection plates so that the existence of particular voltage values on the plates will focus the electron beam to a particular point on the coding mask. If this particular point lies in an aperture the electron beam passes through the coding mask and is collected by the segmented collecting plate. The output current taken from the appropriate segment of the plate may be used to indicate a "1". However, if the beam strikes a point on the coding mask that is not an aperture, no electrons will be collected by the corresponding segment of the collecting plate so that this output may be used to represent a "0".

The vertical deflection plate voltage is a pulse representing the magnitude of the analog voltage to be digitized by the tube. A linear sweep voltage is used as the horizontal deflecting voltage so that the beam sweeps across the coding mask periodically. It is necessary that the pulse applied to the vertical plates remain at a constant height during the horizontal sweep across the coding mask. If the pulse remains at a constant value during the sweep across the coding mask, the segmented collecting plate will collect the electron beam in a manner so that the output currents will represent the pulse height in digital form. These output currents will occur in a sequence corresponding to the sweep time across each segment

of the collecting plate. Referring to Fig. 1, the electron beam is deflected to point "a" when the pulse is applied to the vertical deflection plates and sweeps across the mask along line a-b corresponding to one complete cycle of the linear sweep voltage applied to the horizontal deflection plates.

It has been mentioned that the voltage applied to the vertical deflection plates must be constant during the encoding of its analog value. This certainly must be true if the sweep across the apertures will produce the sequence of pulses which represents the height of the voltage applied to the vertical deflection plates. Actually, the voltage applied to the vertical plates is a pulse obtained by sampling the analog voltage which is to be encoded. The pulse time width must be at least the length of time required for the electron beam to traverse the entire height and width of the coding mask. The time between the application of the sample pulses must be at least as long as the pulse width, because the same amount of time is required to relax the electron beam.

The apertures in the coding mask form the sixteen levels which the tube is capable of encoding. These levels are represented in Fig. 1 on the coding mask by an aperture arrangement which is based on an 8-4-2-1 binary code. If the coding mask is designed for more than four bit encoding it becomes necessary to use a Gray code so that a slight misalignment of the horizontal deflection plates will not cause an error in the encoding process. A Gray code has only a single bit change from one level to another.

2. Sheet Beam Coding Tube

It has been mentioned that the encoding time resulting from the use of a point beam coding tube is approximately the time required

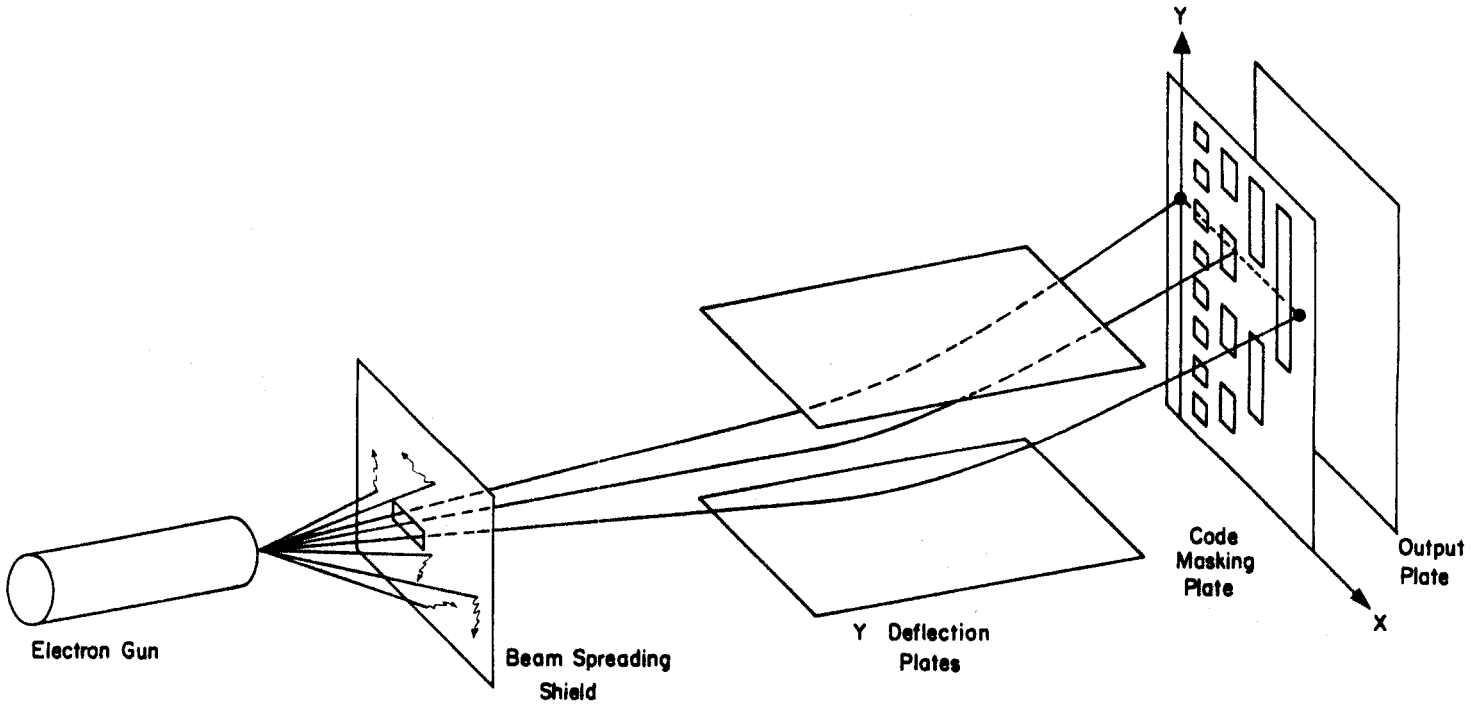


FIG. 2 - SHEET BEAM CODING TUBE

for the beam to sweep upward to the appropriate level and to sweep across the coding mask. If the electron beam is focused and screened as shown in Fig. 2 the time required to sweep across the coding mask is eliminated so that the encoding time is approximately the time required to raise the sheet electron beam to the appropriate level. Therefore, the encoding time is reduced and there is no need for sweep circuitry. Additional elements are needed to produce the sheet beam, however. Also, the individual outputs obtained from the collecting plate occur simultaneously so that a sheet beam coding tube is a parallel encoder and a point beam coding tube is a serial encoder. Theoretically any desired precision may be obtained simply by increasing the number of levels on the encoding mask. However, for practical use only eight to ten bit precision is obtainable because of the physical size of the tube needed to produce this precision. This is reasonable since the number of levels required varies as 2^n where n is the desired precision, and when n is large the voltage required to move the sheet beam from one level to another becomes very small so that the tube is unable to distinguish between voltages with very small differences.

There is a common problem to both point beam and sheet beam coding tubes which is caused by the beam striking the coding mask at a level exactly half-way between two adjacent levels so that the output results in two "pulse groups." This problem has been solved effectively by inserting a horizontal array of grid wires in front of the coding mask which separates the levels represented by the apertures in the coding mask as illustrated in Fig. 3.[3] The grid, usually called a quantizing grid, divides the input signal range into a number of equal steps and positions the electron beam to the proper level for the code corresponding to the voltage step within which the signal amplitude sample falls. This is accomplished by an electrical feedback path to the vertical deflection plates.

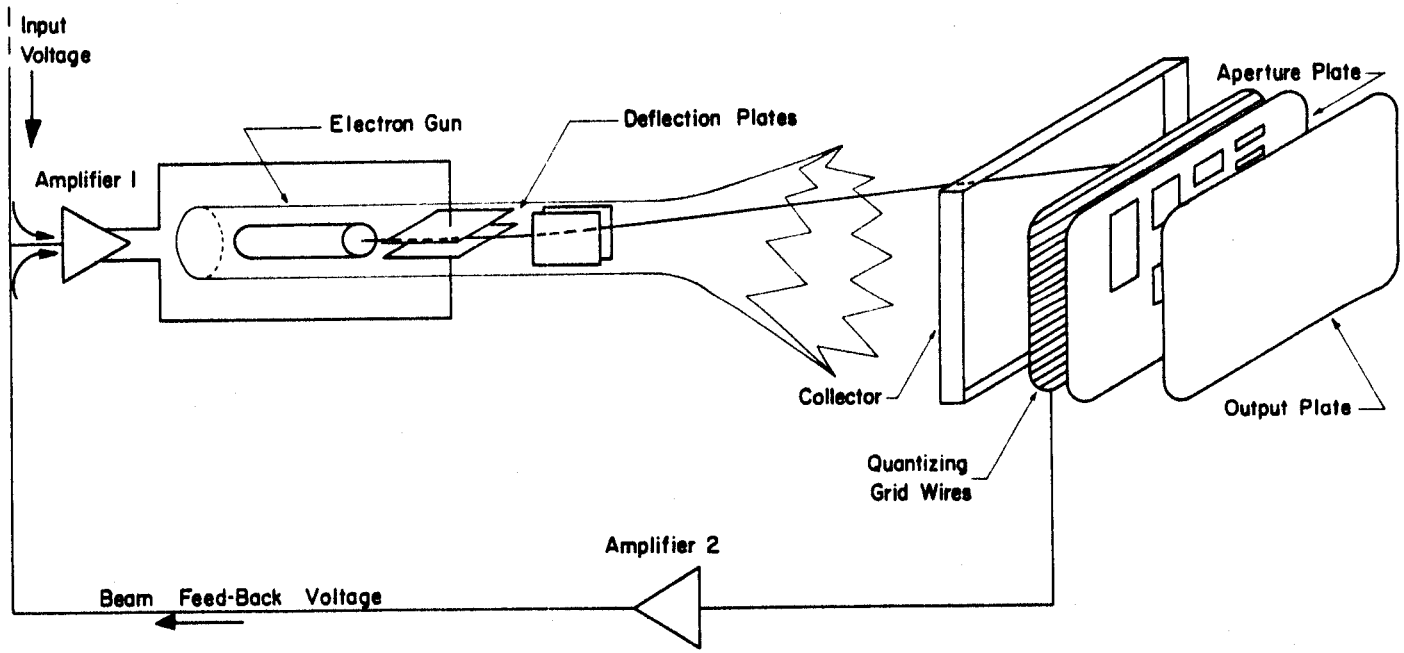


FIG. 3 - CODING TUBE WITH QUANTIZING GRID AND CIRCUIT SCHEMATIC

Although initial coding tube designs involved vacuum tube circuitry, more recent designs are compatible with transistor circuitry. The deflector voltages range from 10 to 20 volts and the output currents from 5 to 100 microamperes. Previous designs have demonstrated that the coding tube can be used in a simple and economical way to produce a technique for encoding an analog signal which is very fast, reliable, accurate, and capable of reasonably high precision.

3. Cylindrical Beam Coding Tube

A cylindrical coding tube is shown in Fig. 4. This type of coding tybe represents the most recent development in coding tubes and provides a method of encoding which is practical for high precision. It has been used to encode samples of an analog signal at sampling frequencies up to 10 Mc and higher with 8 bit precision. This particular tube is 2.6 inches in diameter, 10 inches long, and has a weight of 0.67 pounds.[4]

The electrons emitted from the cathode as shown in Fig. 4 emerge from an aperture in the inner cylinder with an initial velocity that is determined by the voltage V_0 which is the analog pulse to be digitized. A constant retarding potential exists between the inner and outer cylinders so that the electron beam is focused on the coding mask. The coding mask is part of the inner cylinder and the segmented collector plate is formed in the shape of a cylinder just inside the coding mask. The electron beam traces out a deformed spherical shape as it travels from the cathode to the collector plate. This type has increased accuracy and is capable of higher precision than the other type tubes. Also, its relative size and weight make it much more desirable than any electronic analog-to-digital converter of the same precision.

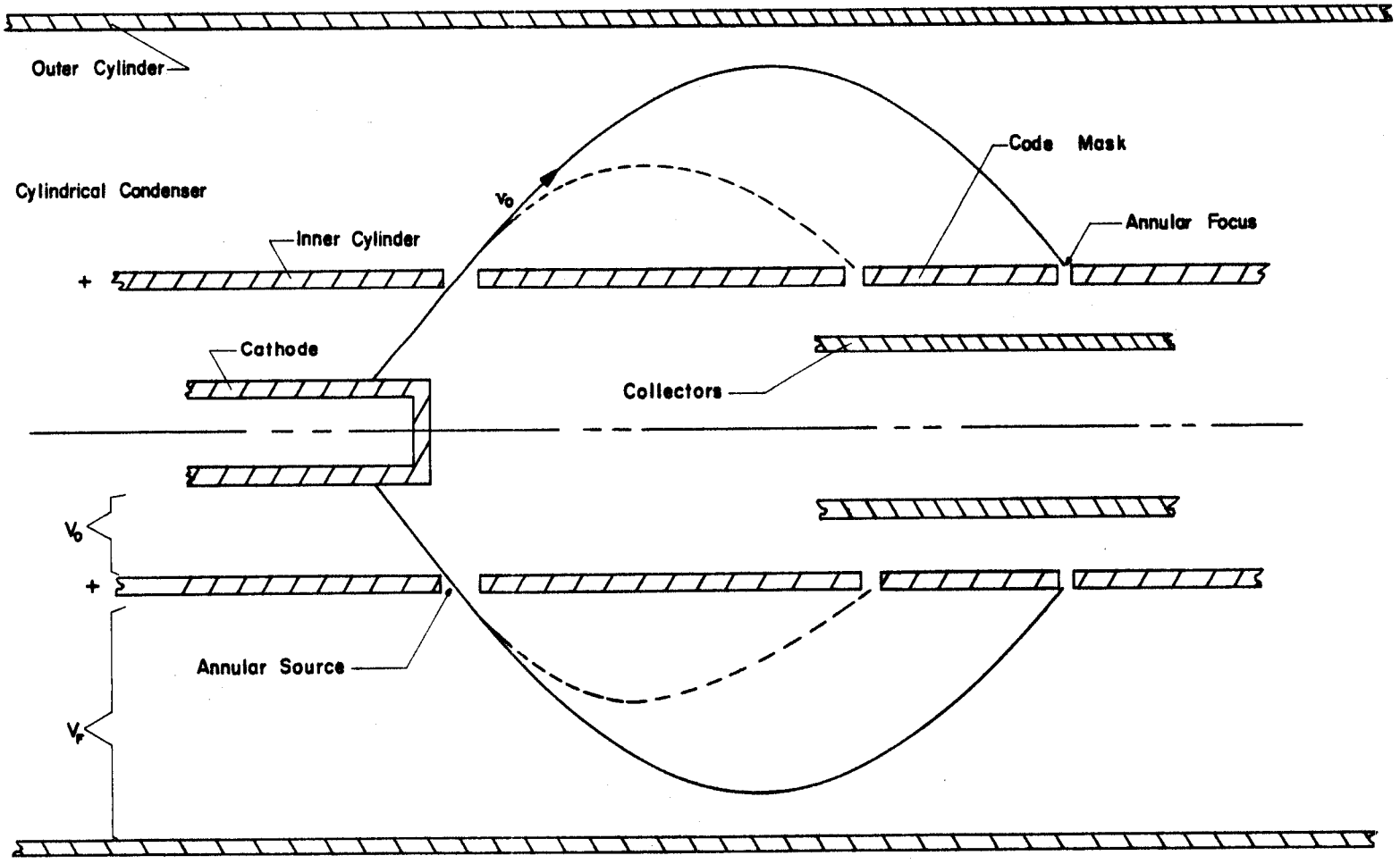


FIG. 4 - SCHEMATIC SECTIONAL VIEW OF CYLINDRICAL CODING TUBE

4. Segmented Sheet Beam Coding Tube

It is conceivable that a segmented sheet beam coding tube could be constructed so that the number of beam segments represents the precision of the encoding tube. Using this segmented beam there would be no need for the coding mask to represent all possible levels. In fact, each beam segment would only have to represent one or two levels so that a plate with an aperture at the level representing the "1" level would suffice as a coding mask for each segment. It seems desirable to consider the segmented sheet beam coding tube for use as a high precision encoding device because of its simplicity, speed, reliability, and accuracy.

B. One Bit Encoding Stages

A popular method of converting a decimal number into a binary number involves comparing the decimal number with successive values of 2 raised to a power. When the largest power of 2 that can be subtracted from the decimal number with a positive remainder is determined, the subtraction is carried out and the process is continued until the desired precision of binary representation has been attained, or until the remainder has been reduced to a desired level. This procedure can be performed by electrical networks as will be explained in the following paragraphs.

The block diagram of Fig. 5 indicates the components needed to perform the digitizing of a pulse representing an analog value.[5] This is analog-to-digital conversion with three bit precision. The explanation of the AD converter can be accomplished by assuming that a pulse of magnitude V_s is compared with a reference voltage which is the mid-value of the encoding range and is represented

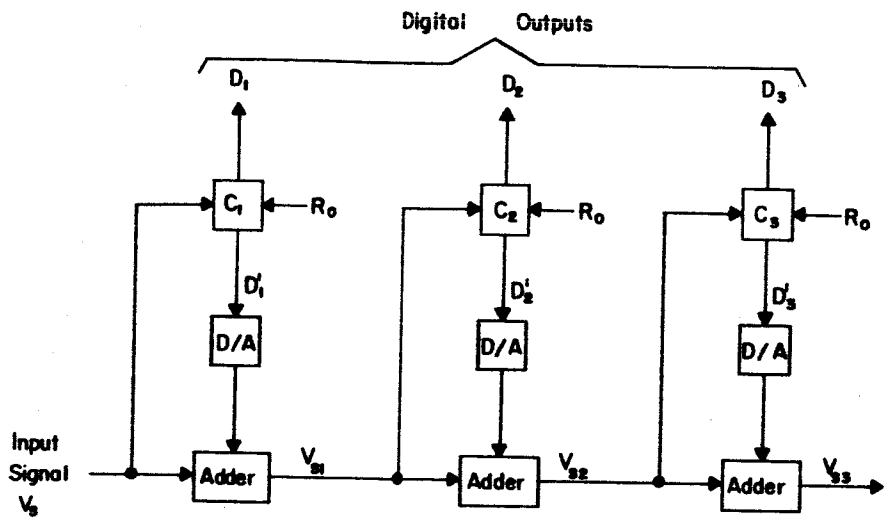


FIG. 5 - BLOCK DIAGRAM OF CASCADE OF ONE-BIT ENCODING STAGES

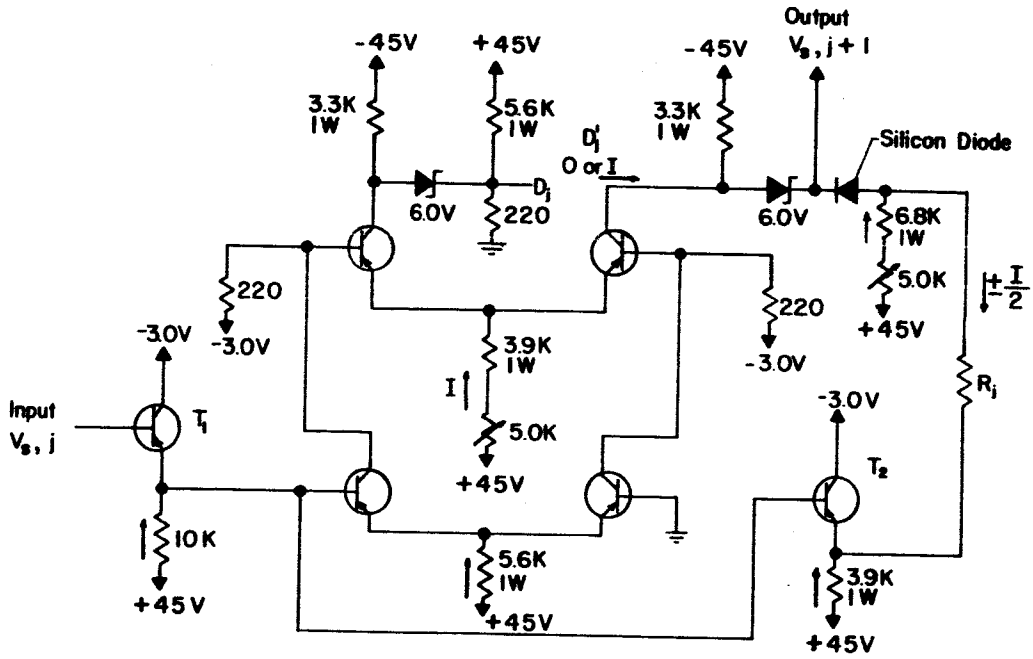


FIG. 6 - CIRCUIT DIAGRAM OF ONE-BIT ENCODING STAGE

by R_0 in the diagram. If V_S is greater than R_0, $D_1 = 1$ and $D_1' = 0$. D_1' is decoded in the digital-to-analog network in such a way that when the result is added to V_S, it corresponds to the subtraction of the binary weighted voltage of D_1 from V_S. The difference in these two voltages is then applied to the comparator in the second stage which operates in the same manner as the first stage except that the binary weight of D_2 is smaller by a factor of 2. However, if V_S is less than R_0, $D_1 = 0$ and $D_1' = 1$. In this case, D_1' is decoded in such a way that zero is subtracted from V_S in the addition process. The three stages are identical except for the DA converter which decodes according to the binary weight of each bit. Theoretically, any number of these stages may be connected in parallel to produce a very high precision converter, but later discussion will indicate that the number of stages which may be used is limited.

Fig. 6 shows the circuit diagram for a one bit encoding stage.[6] The sampled analog voltage is applied to the base of transistor T_1, which has a fan out of two; one branch of the signal dirves the comparator, the other is transmitted to a pulse summing circuit. The comparison is accomplished by cascading two current switches whose digital output provides current 0 or I to the summing circuit. The current is 0 or I, depending upon the state of the comparator. These currents are shifted to $\pm$ 1/2 by the zener diode translation network. The product of the output current of this network and the resistor R provides one of the input voltages to the summing circuit. The summing circuit produces an output voltage by adding the voltage from the digital-to-analog network to the input voltage of that stage. This output voltage provides the input to the next decoding stage. The combined function of the

digital-to-analog network and the summing circuit is to produce the difference, $V_{sn} - D_n \cdot 2^n$, where V_{sn} is the input to the nth stage, D_n is the digital output of the nth stage, and 2^n is the binary weight of the nth stage.

The emitter-follower circuit transistor, T_1, provides the high input impedance necessary for the interconnection of the one-bit stages and its low output impedance minimizes the effect of undesirable switching transients.[7] There is a small voltage drop between the base and the emitter which does not effect the accuracy of the encoding unless there is a sufficient number of stages cascaded. Partial compensation for this voltage drop is provided by taking the output signal from the negative side of a silicon diode biased in the forward direction. There is also a small voltage drop between the base and the emitter of T_2. Both of these voltage drops contribute to error in the representation of V_S so that for accurate high precision this technique is not suitable. Actually, only 5 or 6 bit precision is possible without error. If transistors with smaller voltage drops between base and emitter are used, higher precision would be possible. The encoding time is approximately 12 nanoseconds per bit.

There are other types of feedback encoders, such as programmed feedback encoders, nonprogrammed feedback encoders, and self balancing encoders. These types require more components and circuitry than is necessary with an encoder constructed of one bit encoding stages. The cascading of one bit encoding stages is an excellent technique of digitizing an analog signal.

The block diagram of a system of three bit precision is shown in Fig. 7. The three bit precision is obtained using three one-bit encoding stages. The sampler and sample pulse generator

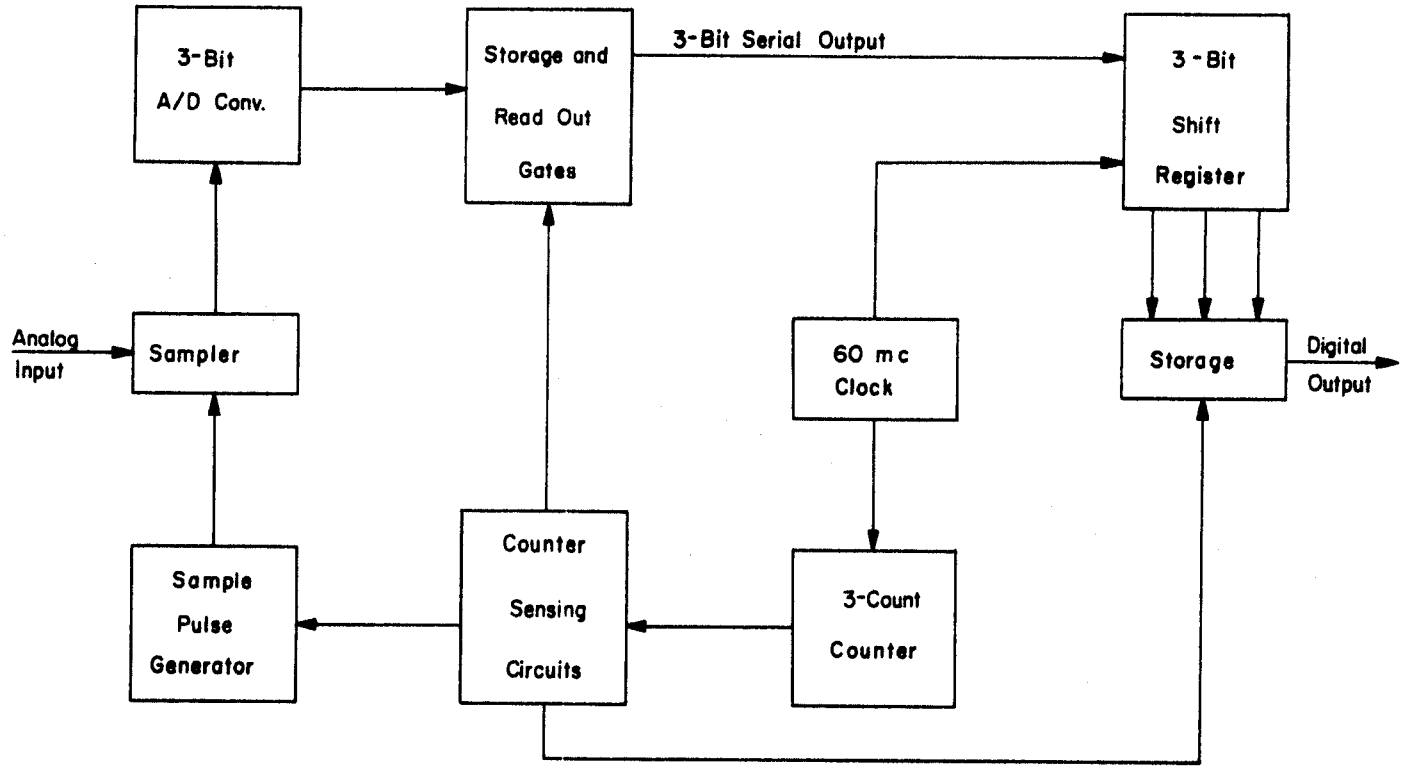


FIG. 7 - BLOCK DIAGRAM OF HIGH SPEED ENCODING SYSTEM

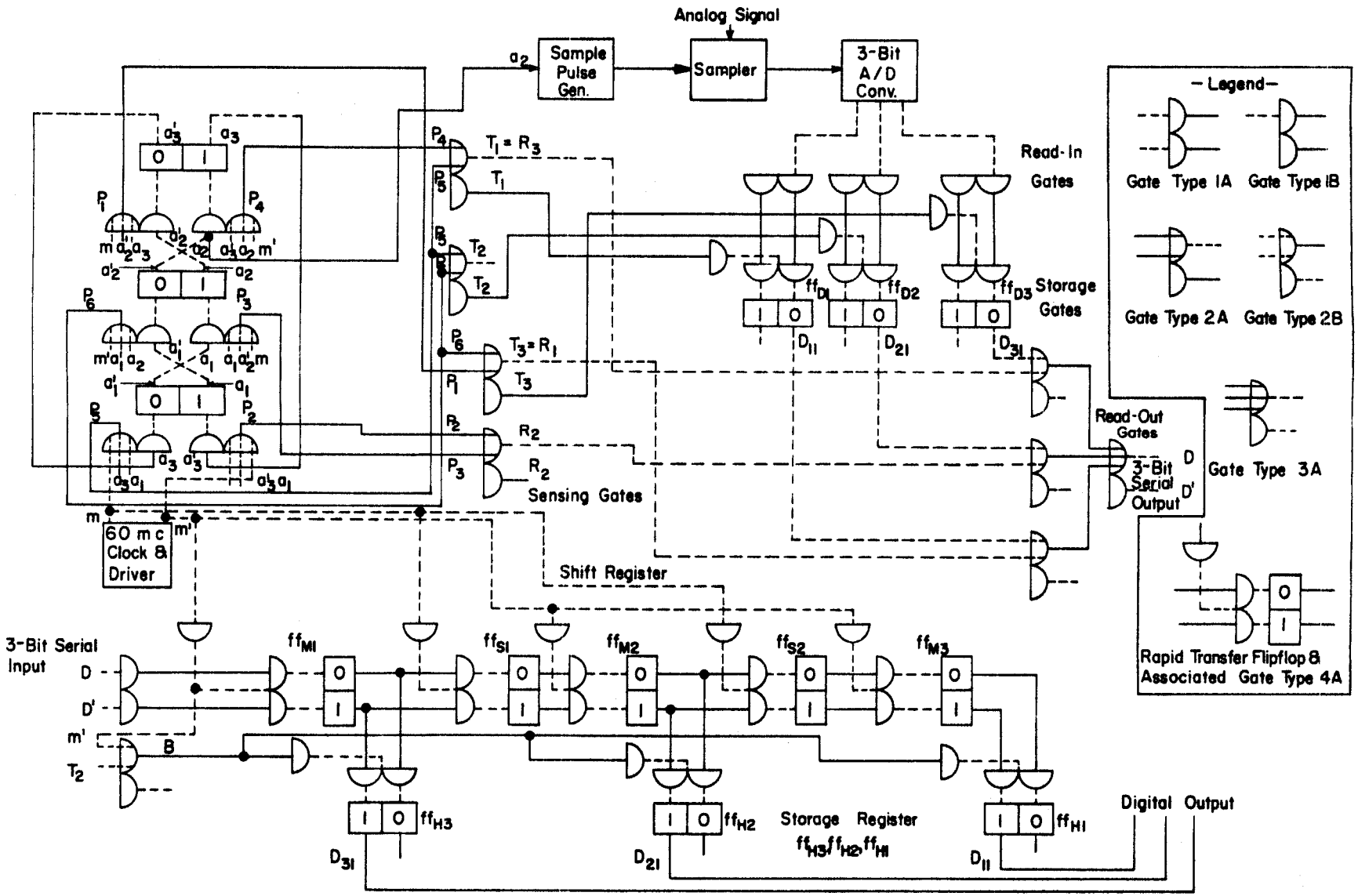


FIG. 8 - LOGIC DIAGRAM FOR HIGH SPEED ENCODING SYSTEM

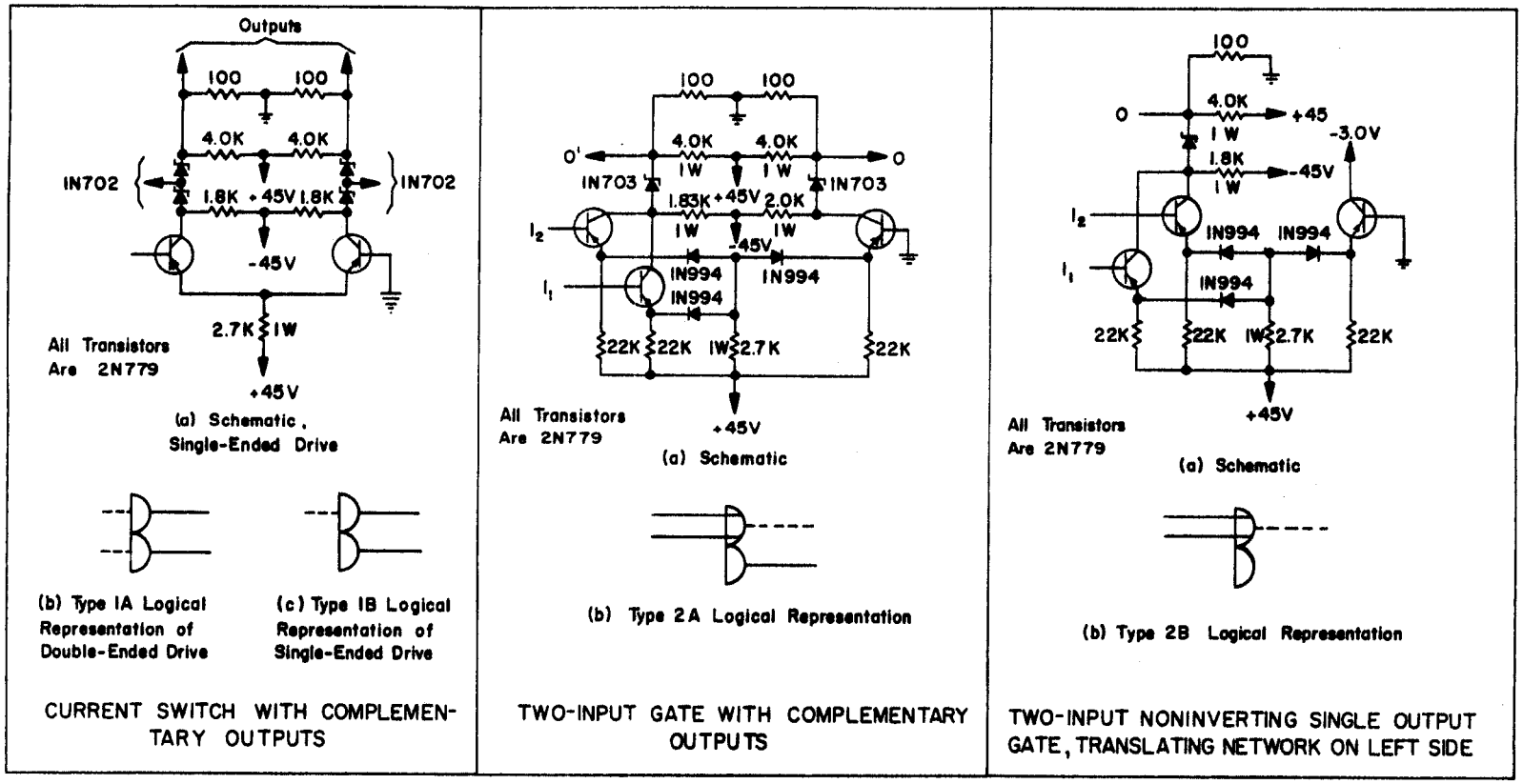
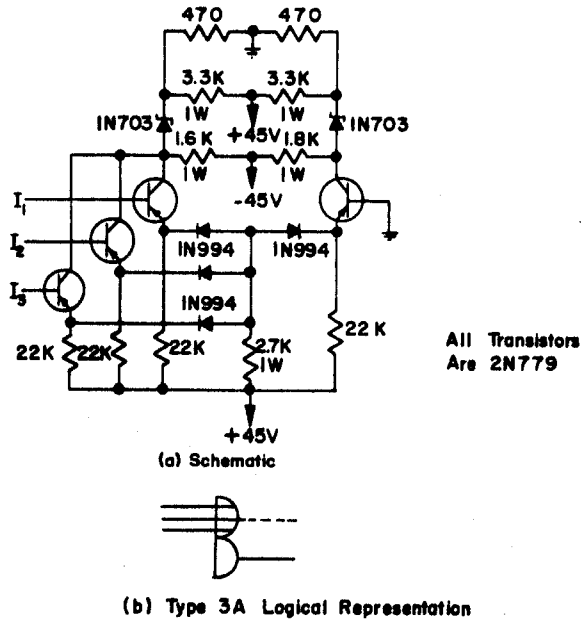


FIG. 9A - LOGICAL REPRESENTATION AND SCHEMATICS OF LOGIC GATES

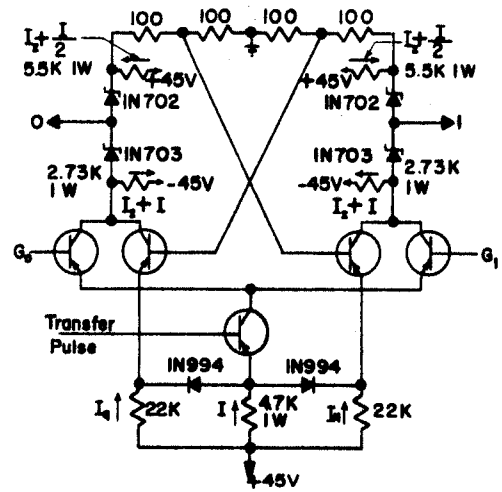


(a) Schematic

All Transistors Are 2N779

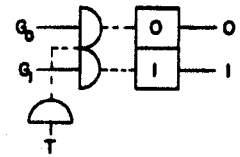
(b) Type 3A Logical Representation

THREE-INPUT GATE WITH COMPLEMENTARY OUTPUTS



(a) Schematic

All Transistors Are 2N779



(b) Type 4A Logical Representation

RAPID TRANSFER FLIPFLOP

FIG. 9B - LOGICAL REPRESENTATION AND SCHEMATICS OF LOGIC GATES

are described in a later section on peripheral components. The logic diagram is shown in Fig. 8 and the types of logic circuitry used are illustrated in Fig. 9A and 9B. This particular system was designed by Robert V. Cotton, Eugene Goldberg, and Albert F. Tillman.[8]

C. Two Bit Encoding Stages Using Delay Channels

The block diagram of an experimental encoder is shown in Fig. 10.[9] This encoder is capable of high precision with reliable, accurate, and high speed operation. For the theory of operation consider an analog current signal of arbitrary value, but within the encoding range, applied to the input. This current splits into the three main channels each having a different time delay which is proportional to the amount of time allowed for each signal to propagate through each main channel. Each main channel has isolation circuitry to prevent transmission back through the signal source. This, of course, is not necessary for the first main channel since the outputs of the other channels are not applied to its input and each sub-channel has isolation circuitry. Also, each sub-channel has isolation circuitry. The three sub-channels of the first main channel are used to determine in which quarter of the maximum encoding range the analog input lies. These quarters are represented by 00, 01, 10, and 11 in binary form but at the output of the sampling and threshold circuitry they will appear as the appropriate currents representing the binary values. If "0" is the current representing zero and "I" is the current representing one, the four quarters of the encoding range would appear as 000, I00, II0, and III at the output of the sampling and threshold circuitry. The logic circuitry as shown in the block diagram is used to convert these possibilities to 00, 0I, I0, and II which are the first two

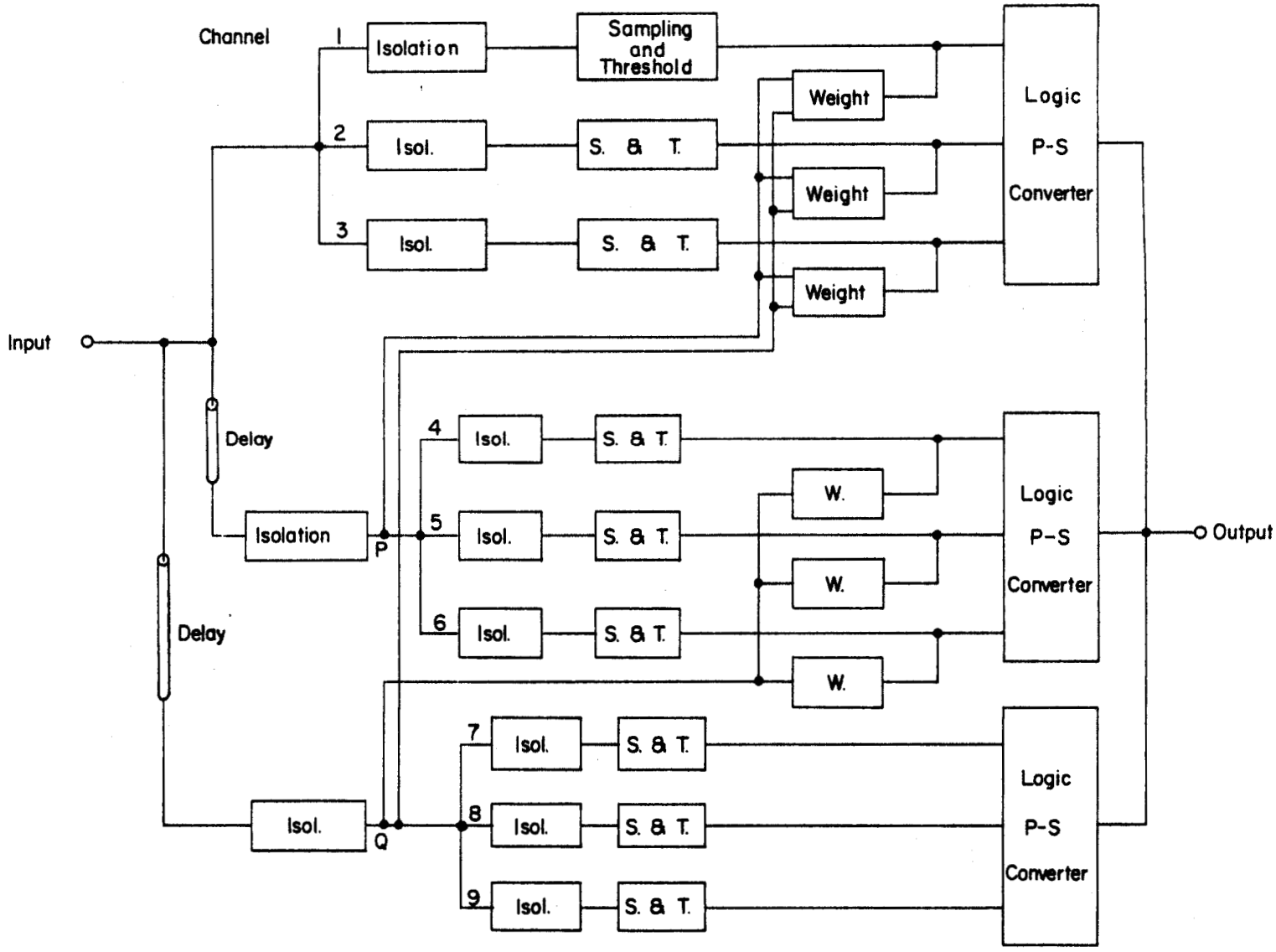


FIG.10-BLOCK DIAGRAM OF DELAY CHANNEL ENCODER

digits of the binary number representing the analog value. The outputs of the sampling and threshold circuitry are also routed through appropriate weighting circuitry to the inputs of the subsequent delay channels. When these weighted currents are combined with the delayed analog input the input to the subsequent delay channels will have the form of the original analog signal minus the analog value of the first two digits determined in the first main channel. The outputs of the three main channels are digits one and two, digits three and four, and digits five and six, respectively so that this converter has six bit precision. Theoretically any desired precision may be obtained using additional delay channels. However, these additional channels would place very strict requirements on the delay lines and the threshold circuitry.

D. Time-Base Encoders

In the past time-base encoding has been the most widely used of the analog-to-digital encoding techniques. This type of encoder uses a linear sweep voltage which has a maximum value that is greater than the maximum value of the analog voltage that is to be encoded. As the linear sweep voltage begins its positive increase from zero, a binary counter begins counting in a manner that is proportional to the time-base of the linear sweep voltage. The calibration of this counter is such that its digital output represents the magnitude of the sweep voltage at any given time. When the sweep voltage becomes equal to the analog voltage gating circuitry is used to stop the counter, trigger the digital output reading circuitry, and to trigger the storage circuitry so that the magnitude of the analog voltage is recorded in digital form. The counter is then reset to zero so that when the linear sweep voltage begins its next cycle the counter can begin counting for the representation of the next analog value.

The basic problems of this type of encoding are the readings at irregular intervals caused by sweep nonlinearities and reference level inaccuracy. Also, ambiguous readings are obtained from the counter caused by the counters changing during the readout pulse time.[10] One of the key problems is the generation of the sweep. An exponential sweep is normally used but this produces particular problems when high accuracy is aimed at the linearity of this sweep.[11]

The desirable features of this type of encoding are represented by the simplicity of the circuitry, ease of construction, and the requirement of only a few basic circuits. However, a large number of these basic circuits are needed.

E. Peripheral Components

There are several components that are needed as peripheral equipment in the design of analog-to-digital converters which are not directly related to the conversion techniques but are necessary in the construction of an analog input-digital output device. If it is desired to construct an analog-to-digital converter which has an analog signal as the input, some conversion techniques require the analog signal in pulse form so that the converter must contain a sampling device capable of sampling at a particular rate. The rate of sampling must be compatible with the conversion technique being employed. There are two types of sampling devices that exhibit desirable characteristics for use in relatively high speed converters.

A pulse representing an analog value must, necessarily, have a rise time, a pulse time-width, a pulse height, and a relaxation time. The conversion of the pulse height must take place during the time-width which is the time that the pulse height

is maintained. The rise time is the time allowed for sampling the analog signal which is the time required to raise the output voltage of the sampler from zero to a value representing the analog signal at a particular time. In high speed systems, it is desirable to keep the pulse rise time to a minimum so that maximum time will be allowed for digitizing in a given cycle. This makes higher precision and higher accuracy possible with the conversion method being used.

1. Diode Bridge Sampler

A sampling technique which performs favorably to the above conditions involves the use of a diode bridge network as shown in Fig. 11. The diodes used in the bridge network must have a low forward resistance so that a short charging time is achieved and they must also have a high back resistance so that the discharging circuit will have a large time constant. The charging time determines the rise time of the pulse and the discharging time determines the decrease in pulse height during a certain pulse width time. The capacitor connected to the output of the diode bridge should have a value which results from a compromise between a small value for fast charging and a large value for slow discharging. If the AD conversion technique being used is fast, a small value of C may be used without appreciable error because it is not necessary to maintain the pulse height for a long length of time. Conversely, a large value of C is necessary if the AD conversion method is slow.

The analog driver for the bridge is a double emitter follower consisting of T_4, T_5, and T_6, which provide the necessary low impedance driving source. This low impedance is necessary

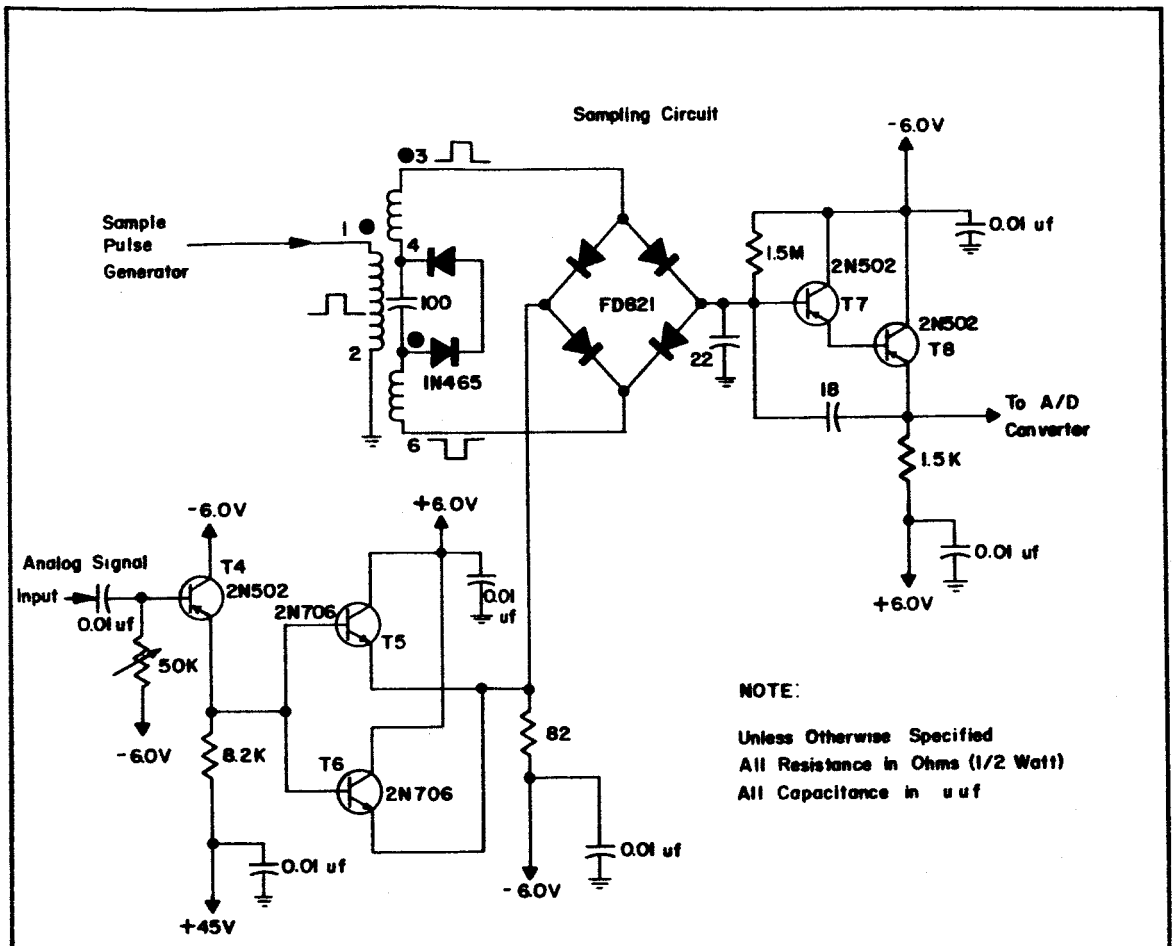


FIG.11-DIODE BRIDGE SAMPLER

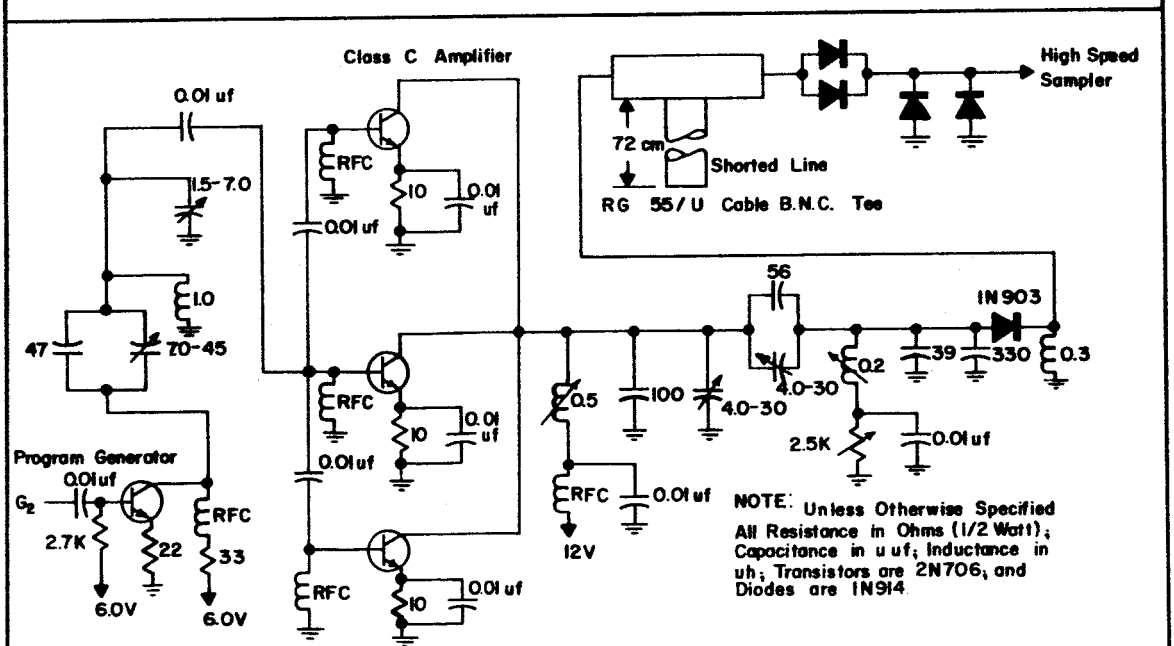


FIG.12-DIODE PULSE GENERATOR

to minimize the voltage drop so that the output pulse will be an accurate representation of the analog value. The output impedance of the driver has been measured at less than 10 ohms and is capable of delivering a 3 volt peak-to-peak signal into 20 ohms. The measured frequency response is 200 MC to the 3 db point. The sampler output emitter follower consists of transistors T_7 and T_8 which has an input impedance in excess of 1 megohm."[12]

A pulse generator that is compatible with the above sampler is shown in Fig. 12. The input for this pulse generator is the output from the program generator which indicates when the analog voltage is to be sampled by producing a pulse at the input of the pulse generator. This input pulse is used to produce the desired output pulse. It is amplified by the common emitter transistor at the input and shaped with respect to rise time, pulse width, and relaxation time by the diode pulse generator using the 1N903 diode. The power to this diode pulse generator is supplied by the parallel connection of three common emitter transistor configurations which are operated in parallel as a class C amplifier. The diode pulse generator was first reported by Boff, Moll, and Shen.[13] The pulse characteristic is the result of a discontinuity exhibited by certain solid-state diodes which may be used to generate nanosecond pulses. The low frequency components of the output pulse containing the discontinuity are cancelled by the return of the reflected wave which is a result of the application of the pulse to a shorted transmission line whose length determines the pulse width. This type of pulse generator has exhibited rise and fall times as short as one nanosecond measured at the half-amplitude points, repetition rates from 10 MC to at least 50 MC, and relatively high output power into low impedances.[14]

2. Tunnel Diode Sampler

A circuit which can be used in the sampling process and which is capable of relatively high speed operation is shown in Fig. 13. The common-base connected high frequency transistor (such as 2N917 or 2N2218) acts as an isolator and terminates the signal line properly.[15] The collector of this transistor is connected through a resistor to the threshold tunnel diode. It is called a threshold tunnel diode because it determines the level of the incoming singal and transforms it into digital information. This tunnel diode is connected through a resistor to the memory tunnel diode. The memory diode stores the value of the output from the threshold tunnel diode. The interrogation pulses and the reset pulses are applied through resistors to the threshold diode and the memory diode respectively. The signal pulse which is supplied by the collector of the common-base transistor can never fire the tunnel diode because it is biased beyond the tunneling region. However, if the signal range is from 0 to 10 ma the negative interrogation pulse, which has an amplitude of 20 ma and a pulse width of one nanosecond, will switch the threshold tunnel diode on and off in less than one nanosecond. The tunnel diode will not fire at all if the signal value is between 10 and 20 ma. The memory tunnel diode is reset by a positive, one nanosecond wide, current pulse of about 15 ma in amplitude. The reset pulse occurs a few nanoseconds before the interrogation pulse so that it is prepared for the next output of the threshold diode. This circuit is capable of operating at a 200 Mc sampling rate.[16]

"A pulse generator which can be used to generate the interrogation and reset pulses is shown in Fig. 14. The input

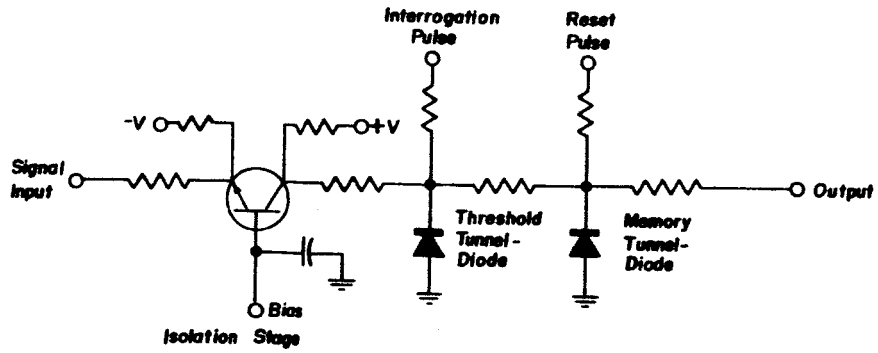


FIG.13-TUNNEL DIODE SAMPLER

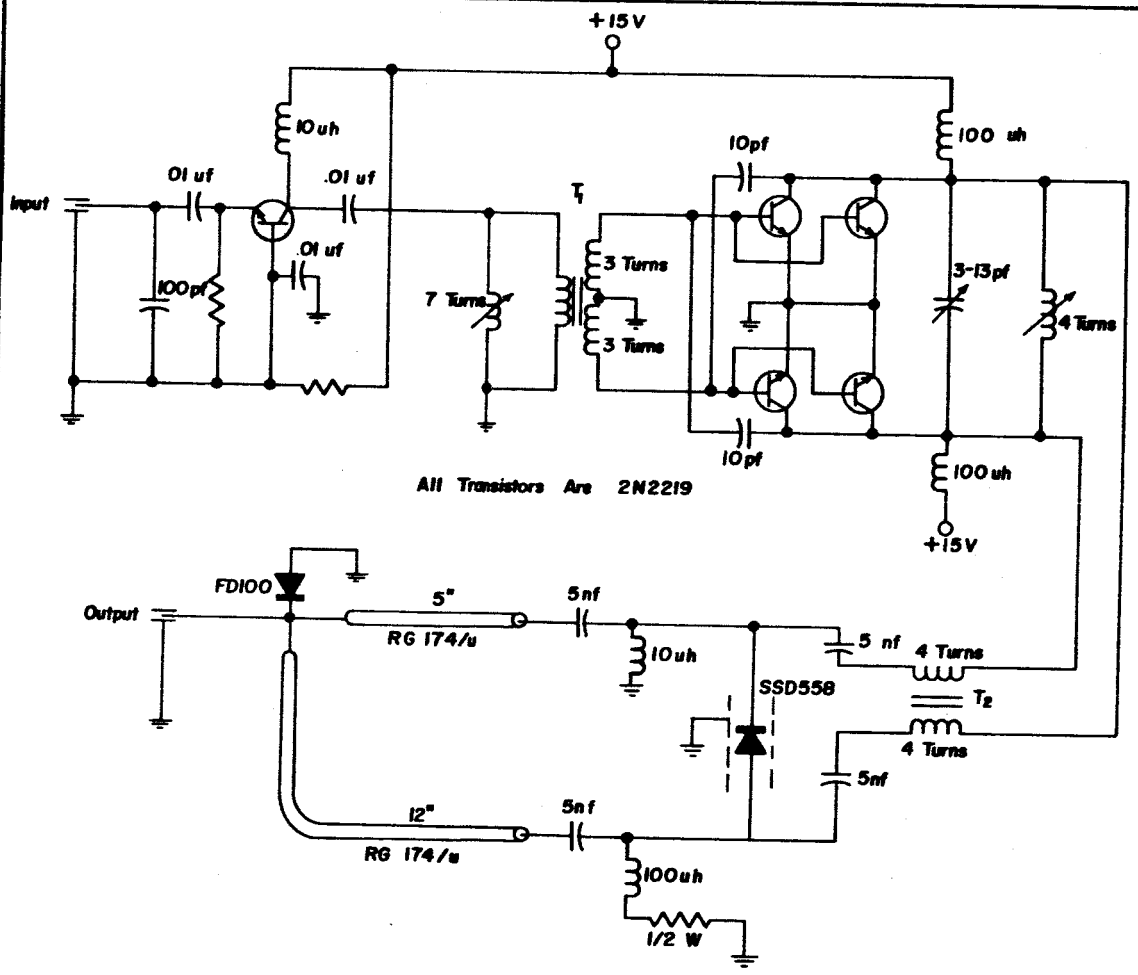


FIG.14-INTERROGATION AND RESET PULSE GENERATOR

pulse from the program generator is preamplified by the common-base connected transistor (2N2219) and is further amplified by the four high-frequency medium-power transistors in a push-pull arrangement. They work into a tuned circuit and into a symmetrizing transformer which is connected to a charge-storage diode (Type SSD 558). At both ends of the diode symmetrical voltage ramps (12 V, 0.4 nanosecond rise time) are generated. These waveforms run through two delay lines of different length and add up to a pulse (10 V, 1.0 nanosecond wide) at the output of the generator. The diode across the output reduces the baseline noise."[17]

REFERENCES

1. Savitt, Donald, "A high-speed analog-to-digital converter," IRE Transactions on Electronic Computers, vol. EC-8, No. 1, p. 31; March, 1959.

2. Sears, R. W., "Electron beam deflection tube for pulse code modulation," BSTJ, p. 45; January, 1948.

3. Reference No. 2, p. 46.

4. Herjnisch, H., "A cylindrical coding tube for 8-digit code," Proceedings of IEEE, vol. 51, No. 11, p. 1540; November, 1963.

5. Cotton, Robert V., Eugene Goldberg, and Albert F. Tillman, "Design and development of analog-to-digital converters," Final Report, Contract No. AF 33 (616)-6693 (Philco No. 2237-F), Philco Corporation, ASTIA No. AD-266731, p. 8; September, 1961.

6. Reference No. 5, p. 44.

7. Reference No. 5, p. 44.

8. Reference No. 5, pp. 29-35.

9. General Electric Company, Electromagnetic Warfare and Communications Laboratory, Aeronautical Systems Divisions, R. Remm, Project Engineer, "Insertion of wide bandwidth video data for communications from reconnaissance satellites," Contract No. AF 33 (616)-9148, ASTIA No. AD190518, p. 15; November, 1962.

10. Rehwoldt, T. V., "Analog voltage-to-digital converters," Technical Memorandum, Analytical Design Department, Chrysler Corporation, ASTIA No. AD-289595, p. 8; December, 1956.

11. Cronhjort, B. T., "A time coding analog-to-digital converter, Proceedings of the IEEE, vol. 51, No. 11, p. 1546; November, 1963.

12. Reference No. 5, p. 39.

13. Boff, A. F., J. Moll, and R. Shen, "A new high speed effect in solid-state diodes," Digest of Technical Papers, International Solid-State Circuits Conference Philadelphia, Pa., pp. 50-51; February, 1960.

14. Reference No. 5, p. 37.

15. Reference No. 9, p. 3.

16. Reference No. 9, p. 8.

17. Reference No. 9, p. 11.

III. A VERSATILE COMPARATOR FOR ENCODING DEVICES

A. INTRODUCTION

In the design of electronic alalog-to-digital converters and certain encoding devices there is a need for voltage amplitude comparators that are simple, reasonably fast, and in most applications highly sensitive to small differences in voltage amplitudes. The need of simplicity and speed is apparent when consideration is given to nonprogrammed feedback encoders, parallel encoders, and some programmed feedback encoders when they are designed for high precision operation.[1] These applications do not necessarily require a high degree of sensitivity because of the type comparisons that are performed. Each compare circuit needs only to be capable of indicating whether or not the analog voltage is greater than a particular reference voltage. For example, when the analog signal value is so near, but greater than, the reference value that a certain compare circuit errors in a less-than reference value indication, the resulting analog signal value is at least twice the value of any succeeding compare circuit reference voltage so that all the remaining compare circuits yield a greater-than reference value indication and the error is not greater than the least significant bit. The speed of the compare circuits used in these same types of encoders must necessarily be fast in view of the number of comparisons that are required to encode a single analog value.

Other encoding techniques, such as successive approximation and time base encoding, use only a single compare circuit.[2,3] The compare circuit used in an encoder which is designed to encode an analog value by making successive approximations

to it will be required to perform as many comparisons as there are bits of precision so that the speed of comparison must be relatively fast to maintain a reasonable conversion word time. Also, the compare circuit must be extremely sensitive to small voltage differences if high precision is to be obtained utilizing this technique.[4] Comparators used in time base encoders are required to constantly monitor the difference between the analog signal voltage and the reference voltage and to produce a desired switching pulse when this difference is within a certain tolerance range. This tolerance range determines the required sensitivity of the comparator and is the minimum error of the encoding device.[5]

The optimum comparator would have diversity with regard to performing all of the above mentioned comparisons to the desired specifications in each technique of analog-to-digital conversion. Excellent methods of voltage comparison for specific functions are presented in the literature.[6, 7, 8, 9, 10]

B. A VERSATILE COMPARATOR

A compare circuit which utilizes the switching characteristic of a single tunnel diode and which has demonstrated sufficient versatility for use in several of the above mentioned encoding techniques is shown in Fig. 15.

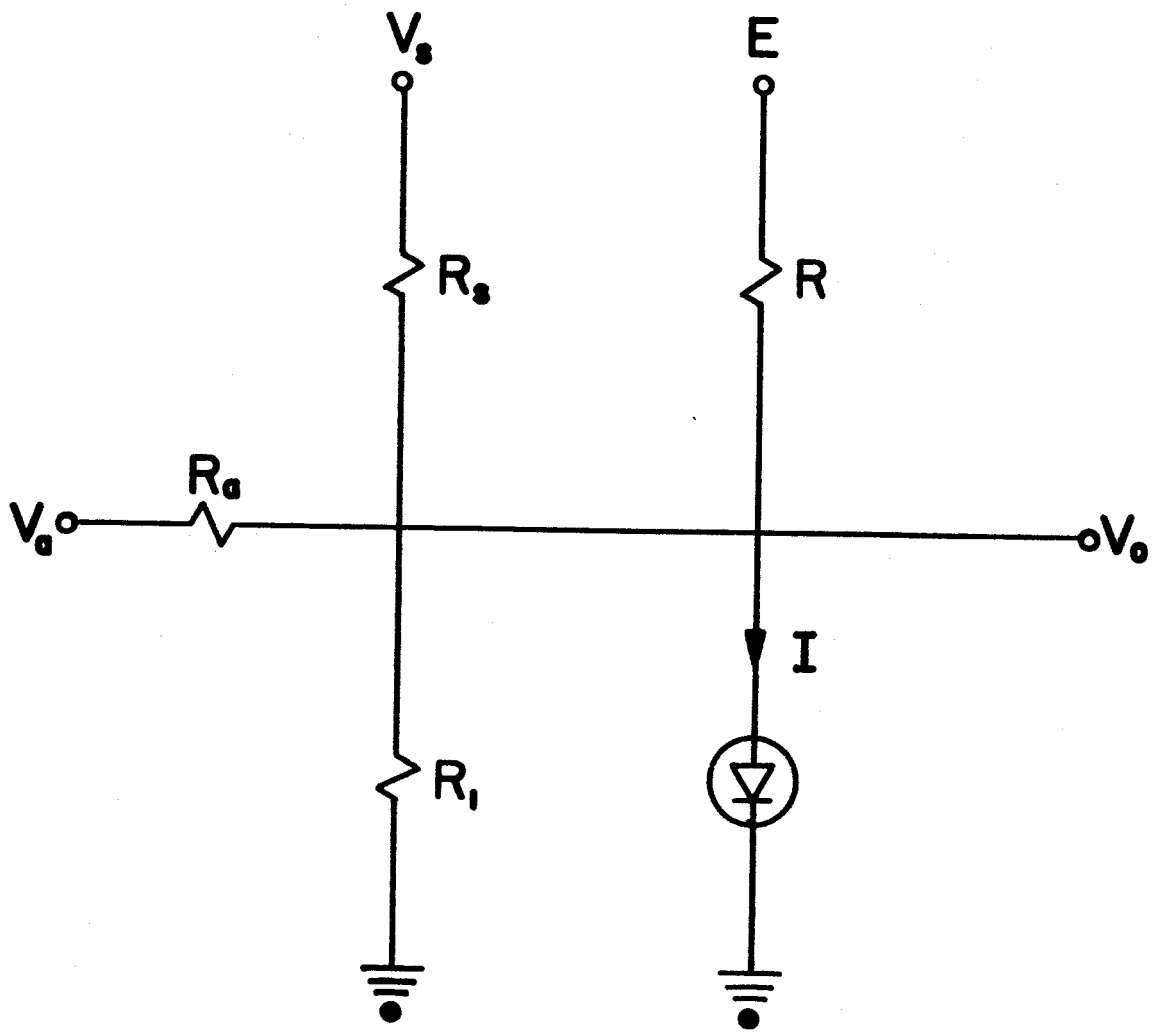


FIG. 15 – THE COMPARE CIRCUIT

The reduced equivalent circuit can be obtained using Thevenin's Theorem. The equivalent Thevenin voltage and resistance are, respectively,

$$E_T = \frac{+\frac{V_a}{R_a} + \frac{V_s}{R_s} + \frac{E}{R}}{\frac{1}{R_a} + \frac{1}{R_s} + \frac{1}{R_1} + \frac{1}{R}} \tag{1}$$

and

$$R_T = \frac{1}{\frac{1}{R_a} + \frac{1}{R_s} + \frac{1}{R_1} + \frac{1}{R}} \tag{2}$$

Then, the current through the tunnel diode is

$$I = \frac{E_T}{R_T} - \frac{V_0}{R_T}$$

$$= \frac{V_a}{R_a} + \frac{V_s}{R_s} + \frac{E}{R} - \left[\frac{1}{R_a} + \frac{1}{R_s} + \frac{1}{R_1} + \frac{1}{R}\right] \cdot V_0 \tag{3}$$

From equation (3) and by consideration of the characteristic curve of Fig. 16, it is apparent that if $V_0 = V_p$, the values of E, R_a, R_s, and R_1 can be adjusted so that the current that will switch the tunnel diode to its high voltage state is

$$I_p = \frac{E}{R} - \left[\frac{1}{R_a} + \frac{1}{R_s} + \frac{1}{R_1} + \frac{1}{R}\right] V_p \tag{4}$$

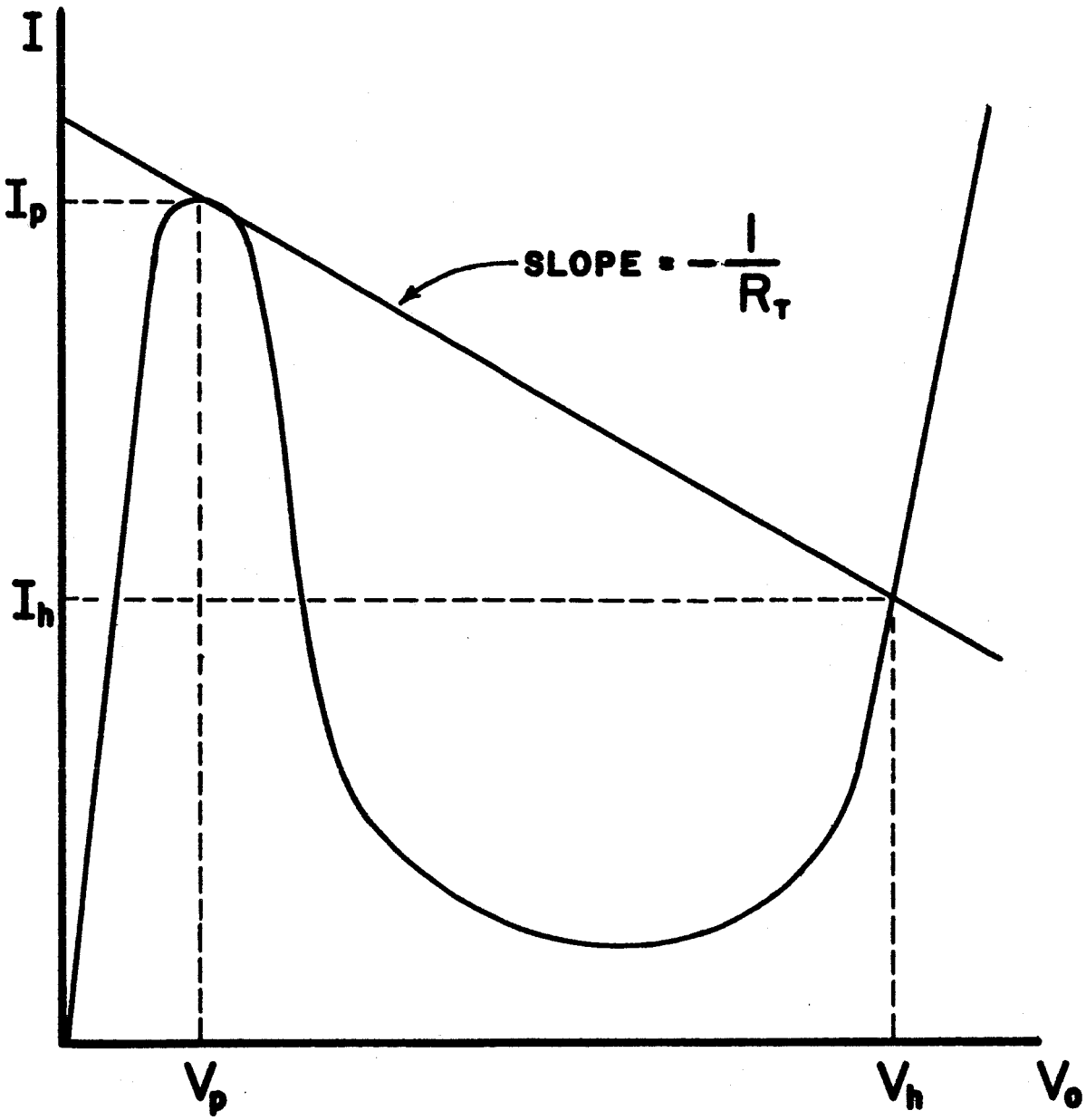


FIG. 16- TUNNEL DIODE CHARACTERISTICS AND SWITCHING LOAD TIME

It is desirable that the coefficient of V_p remain constant through particular variations in R_a. This can be accomplished by adjusting R_1 so that compensation for the variations in R_a is attained. This corresponds to maintaining a constant Thevenin resistance with respect to the tunnel diode. To illustrate this, let $R_a = 2^n R$, $R_s = R$, and $R_1 = \frac{R}{2-2^{-n}}$ for $n \geq 0$, an integer, so that

$$R_T = \frac{R}{4} \tag{5}$$

and

$$E_T = \frac{+2^{-n}V_a + V_s + E}{4} \tag{6}$$

Also from Eqs. (2), (4), and (5)

$$I_p = \frac{E - 4V_p}{R} \tag{7}$$

For a particular tunnel diode I_p and V_p are known so that a suitable choice of the bias voltage, E, will uniquely define the normalizing resistance, R, in equation (7). A proper selection of the bias voltage will force the comparator to reset after it has been switched to the high voltage state and the analog voltage is reduced to zero. This is convenient for comparison of sampled pulse amplitudes which are normally used in nth stage encoders.

The current through the tunnel diode is now

$$I = \frac{2^{-n}V_a + V_s + E - 4V_0}{R} \tag{8}$$

which indicates that a reference value of $V_s \geq -2^{-n}V_a$ will yield $I \geq I_p$ and the diode will be switched to its high voltage state. If it is desired to use p of these compare circuits in an encoding device to encode an analog voltage using p binary bits, a comparator circuit design with $n = 0$ will correspond to the least significant bit comparator and one designed with $n = p$ will be the most significant bit comparator. This allows, by the 2^{-n} factor, all comparisons to be performed at the same reference voltage and the pulse representing a certain analog signal amplitude can be reduced by a factor of 2^{-n} to allow a wide range of comparisons to be performed at a constant voltage sensitivity.

A negative direct voltage may be used for comparisons of pulse amplitudes so that E and V_s may be appropriately combined to provide considerable simplification of each stage. An appropriate combination voltage, V_1, would produce an equivalent current through a resistor $\frac{R}{2}$. If these voltages are combined into a single source, the combination of R and R_s may be replaced with $\frac{R}{2}$ yielding further circuit reduction. This reduced form for an nth stage comparator is shown in Fig. 17.

As previously mentioned, some encoding techniques require a single compare circuit which constantly monitors the difference between the reference voltage and the analog pulse amplitude. In some time base encoders a sawtooth voltage is used as a reference and in successive approximation encoders a stairstep reference corresponding to the addition of binary

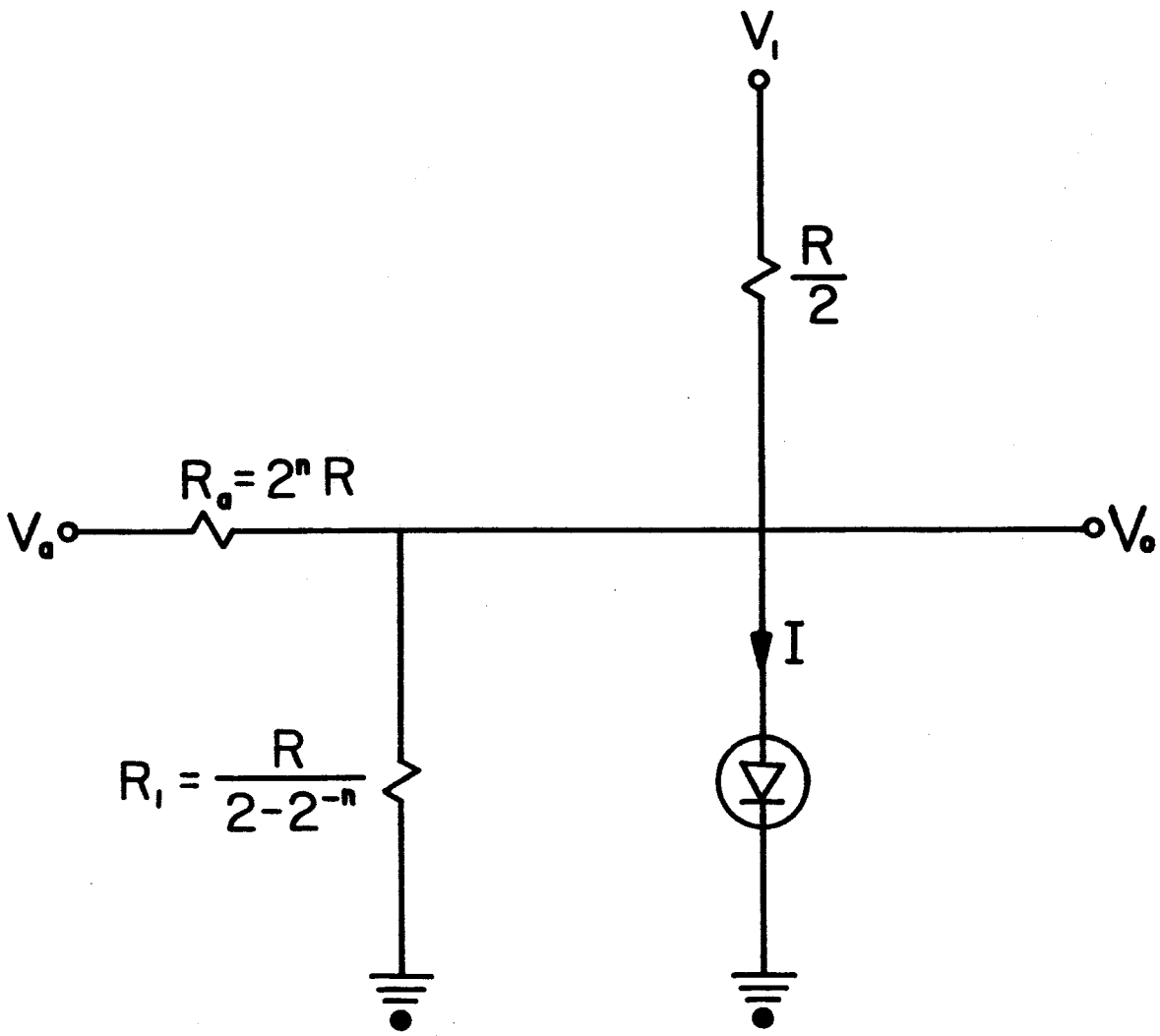


FIG. 17– REDUCED EQUIVALENT CIRCUIT

weighted voltages is used. A suitable comparator for either of these encoders can be constructed by letting $R_1 = R$, $R_a = R_s$, and using the appropriate reference voltage, V_s. The value of R_a and R_s can be varied for different analog voltage ranges to produce a reasonable sensitivity in each case. For example, $\frac{(V_s)\text{ peak}}{KR} = \frac{E}{R}$, which yields $R_a = R_s = KR = R\frac{(V_s)\text{ peak}}{E}$.

The peak value of V_s is the maximum analog voltage value that the encoder will be required to encode. The corresponding Thevenin voltage and resistance are

$$E_T = \frac{1}{2} \frac{V_a + V_s + KE}{K + 1} \tag{9}$$

and

$$R_T = \frac{1}{2} \frac{KR}{K + 1} \tag{10}$$

where $K = \frac{(V_s)\text{ peak}}{E}$, an application factor. The corresponding current through the tunnel diode is

$$I = \frac{V_a + V_s}{KR} + \frac{1}{R}\left[E - \frac{2(K+1)}{K} V_0\right] \tag{11}$$

so that $V_a + V_s = 0$ must yield the necessary switching current.

$$I_p = \frac{1}{R}\left[E - \frac{2(K+1)}{K} V_p\right] \tag{12}$$

Since I_p and V_p are known for a given tunnel diode and the application factor is known, a suitable choice of the bias voltage again uniquely defines the necessary value of normalizing resistance. The reference voltage, V_s, would be a negative sawtooth voltage if the comparator is to be used in a time base encoder and it would be a negative stair-step voltage for use in a successive approximation encoder. The proper selection of the bias voltages in these comparators would provide the necessary periodic resetting of the comparator.

Table 1 shows the reference voltage types, the resistor values, and the Thevenin voltage and resistance for each of the applications mentioned above.

TABLE 1

COMPONENT VALUES FOR VERSATILE COMPARATOR

Type of Comparison			
Component	nth Stage Comparator	Successive Approximation	Time Base
R_a	$2^n R$	KR	KR
R_s	R	KR	KR
R_1	$\frac{R}{2-2^n}$	R	R
V_s	Negative dc	Negative stairstep	Negative sawtooth
E_T	$\frac{2^{-n}V_a + V_s + E}{4}$	$\frac{1}{2}\,\frac{V_a + V_s + KE}{K+1}$	$\frac{1}{2}\,\frac{V_a + V_s + KE}{K+1}$
R_T	$\frac{R}{4}$	$\frac{1}{2}\,\frac{KR}{K+1}$	$\frac{1}{2}\,\frac{KR}{K+1}$
R	$\frac{E - 4V_p}{I_p}$	$\frac{1}{I_p}\left[E - \frac{2(K+1)}{K}V_p\right]$	$\frac{1}{I_p}\left[E - \frac{2(K+1)}{K}V_p\right]$

It has been mentioned in the above discussion that when the basic compare circuit is used to perform p comparisons that all of them will be performed with the same sensitivity. To illustrate this consider the change in V_a needed to produce a current, I_1 in each of the p stages which is equal to $2^p(I_1R)$. This shows that the voltage change in V_a is binary weighted in the same manner as the p stages are binary weighted so that the percent change in V_a required to produce an identical change in the tunnel diode current is the same for all stages and the voltage sensitivity throughout the p stages is, therefore, the same.

With regard to sensitivity, consideration should be given to how accurately the tunnel diode can be used to indicate the condition $2^{-n}V_a + V_s = 0$ when V_a or V_s, or both, are other than steady direct current voltage levels. Certainly the tunnel diode will yield the correct switching action for switching currents considerably greater or less than I_p[11, 12], but in this application there is need for an accurate indication of the condition $I = I_p$ if a high degree of accuracy is desired. For nth stage comparison the error in the output will be no greater than the least significant bit in view of previous discussion. The value of the normalizing resistance, R, can be used to adjust the voltage sensitivity to some extent by varying the ratio, $\frac{1}{R}(2^{-n}V_a + V_s)$, which is the difference in I_p and the operating current of the diode. This adjustment may not always yield tolerable results for wide voltage ranges which are to be encoded.

The sensitivity of the basic compare circuit can be increased by using a saturating difference amplifier as shown in Fig. 18. This will provide the amplification of $\frac{1}{R}(2^{-n}V_a + V_s)$ so that conditions very

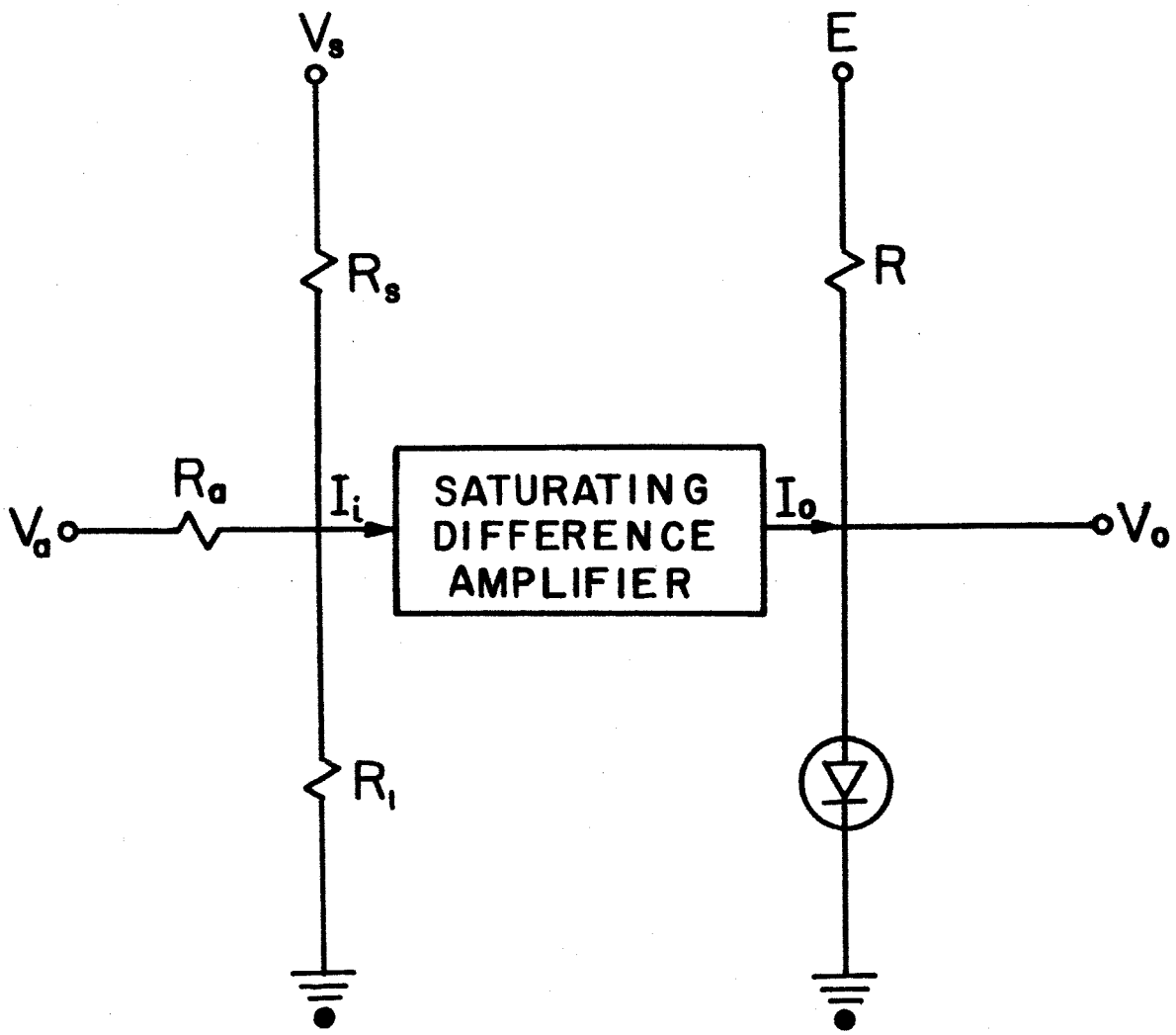


FIG. 18 - HIGHLY SENSITIVE COMPARATOR

near $2^{-n}V_a + V_s = 0$ are more distinguishable and it will provide the necessary limitations in tunnel diode current for large values of $2^{-n}V_a + V_s$. It may be more desirable to accept the tolerance of the original compare circuit for nth stage comparison because of the increased complexity in the encoder. However, for succesive approximation and time base encoders the addition of the saturating difference amplifier seems very desirable in view of the dependence of the encoding accuracy on the accuracy of a single comparator. The desired transfer characteristic of the amplifier is shown in Fig.19 with I_m less than the maximum forward current of the tunnel diode.

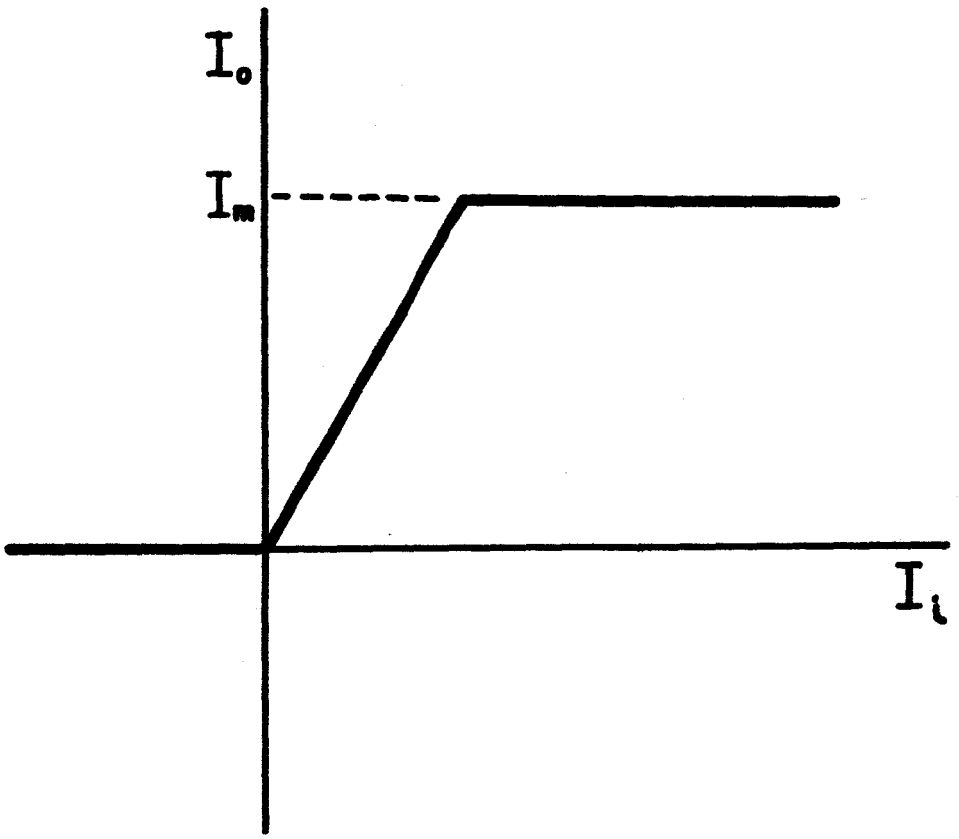


FIG. 19—TRANSFER CHARACTERISTIC FOR SATURATING DIFFERENCE AMPLIFIER

C. AN ENCODER USING Nth STAGE COMPARATORS

The circuit of Fig. 20 illustrates the use of the basic comparator in performing the encoding of an analog voltage with three bit precision. Normally the comparators of an nth stage encoder provide only the necessary comparisons and the encoder contains other components to prepare the analog value for each stage of comparison. The output of each compare stage in Fig. 19 indicates the appropriate binary digit and it also provides the necessary adjustment of the reference voltage in each of the following stages which corresponds to a reduction of the analog value by weighted binary values.

The reduction in analog value is made possible by an appropriate adjustment of the weighting resistor, R_{wn}, which will adjust the short circuit tunnel diode current by $\frac{V_n}{R_{wn}}$ in each of the successive stages. Accurate reduction is achieved by restricting the Thevenin resistance to the same value for each comparator. This value of Thevenin resistance may be represented as $\frac{R}{C}$ where $C \geq 4$. The minimum value of C is dependent on the reference voltage chosen as will be shown in the following discussion.

In the present encoder it seems desirable to vary the amount of current produced by the reference voltage in each stage rather than vary the amount produced by the analog signal in view of the manner in which the outputs are used to adjust the tunnel diode currents in successive stages. If $R_a = R$, $R_{so} = R$, $R_{s1} = \frac{2R}{3}$, $R_{s2} = \frac{4R}{7}$, and $C_1 = \frac{V_s}{V_{nh}}$ = a constant since a constant Thevenin resistance

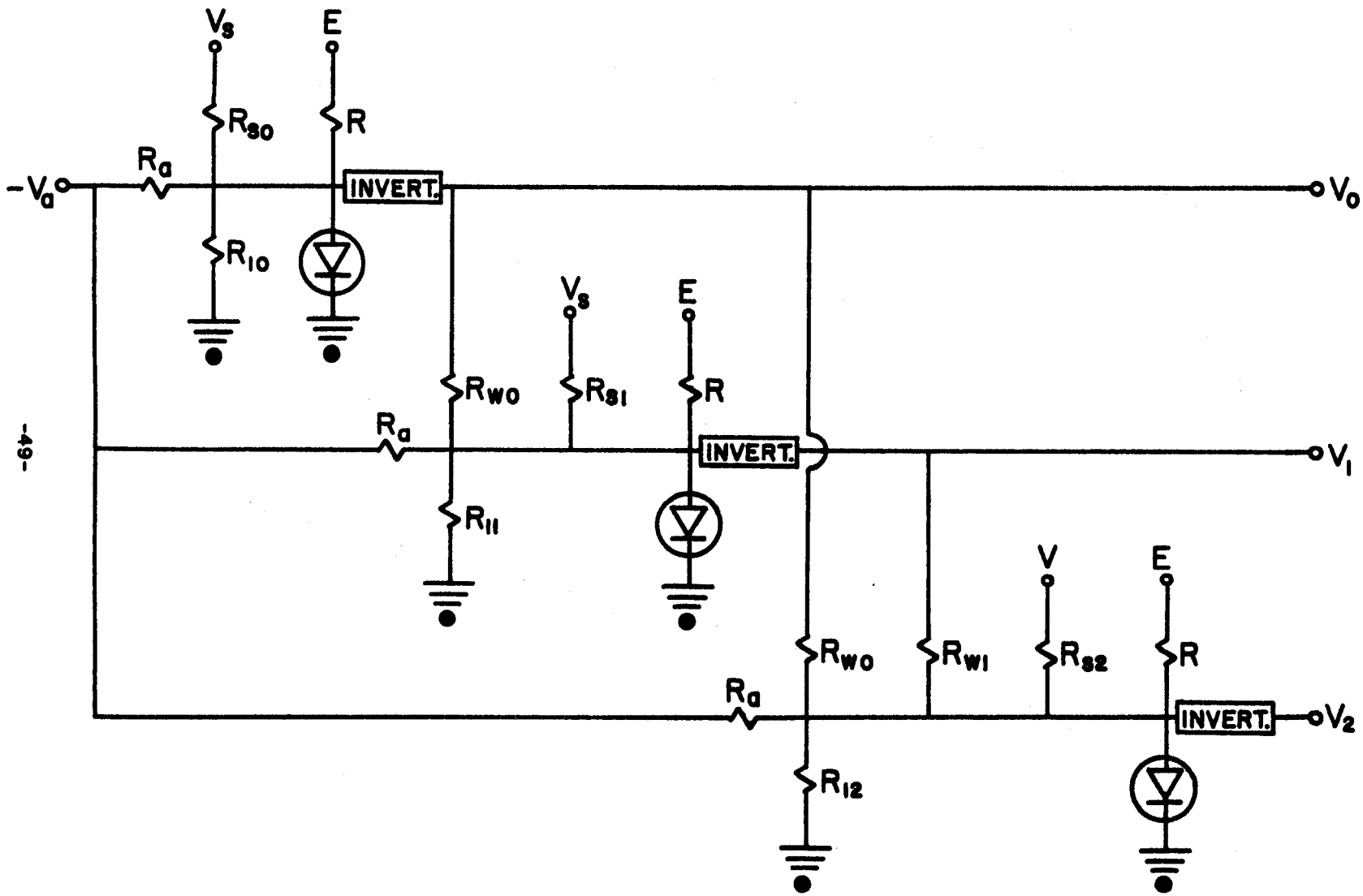


FIG. 20 – AN Nth STAGE ENCODER

produces the same tunnel diode high voltage state, V_{nh} in each stage, then, the required weighting resistances is $R_{wn} = \frac{R}{C_1} 2^n$ as determined from the requirement

$$\frac{V_{nh}}{R_{wn}} = \frac{V_s}{2^n R} \tag{13}$$

Calculation of the Thevenin resistance for each stage using the above resistor values and equating the result to $\frac{R}{C}$ will yield the following compensation resistor values:

$$R_{10} = \frac{R}{C - 3} \tag{14}$$

$$R_{11} = \frac{R}{C - 7/2 - C_1} \tag{15}$$

$$R_{12} = \frac{R}{C - 15/4 - 3/2\, C_1} \tag{16}$$

The resulting tunnel diode currents for the three stages are

$$I_0 = \frac{1}{R} V_s - V_a + E - CV_0 \tag{17}$$

$$I_1 = \frac{1}{R} \frac{3V_s}{2} - V_a + C_1V_0 + E - CV_1 \tag{18}$$

$$I_2 = \frac{1}{R} \frac{7V_s}{4} - V_a + C_1V_0 + \frac{C_1V_1}{2} + E - CV_2 \tag{19}$$

where $V_{0h} = V_{1h} = V_{2h} = -\frac{V_s}{C_1}$ and V_0, V_1, and V_2 have low voltage state values less than V_p. The minimum currents which will switch the diodes are

$$I_{0p} = \frac{1}{R} \; (E - CV_{0p}) \tag{20}$$

$$I_{1p} = \frac{1}{R} \; (E - CV_{1p}) \tag{21}$$

$$I_{2p} = \frac{1}{R} \; (E - CV_{2p}) \tag{22}$$

These switching conditions indicate the values of V_a that will prevent each comparator stage from switching to the high voltage state when a positive pulse of magnitude V_s occurs. The values are

$$V_a > V_s \tag{23}$$

$$V_a > \frac{3V_s}{2} + C_1V_0 \tag{24}$$

$$V_a > \frac{7V_s}{4} + C_1V_0 + \frac{C_1V_1}{2} \tag{25}$$

The analog voltage would always be compared to the reference voltage in the n = 0 stage. However, in the n = 1 stage, it is compared with either $\frac{1V_s}{2}$ or $\frac{3V_s}{2} + C_1V_{0L}$ depending on whether or not the n = 0 stage is in the high or low voltage state. The comparison performed by the n = 2 stage depends on the state of both previous comparators and the possible comparisons are with

$$\frac{IV_s}{4}, \; \frac{3V_s}{4} + \frac{C_1V_{12}}{2}, \; \frac{5V_s}{4} + C_1V_{0L}, \; \frac{7V_s}{4} + C_1V_{0L} + \frac{C_1V_{1L}}{2} .$$

If a particular comparator output is in the low voltage state it will produce a small error current in all successive stages which will not exceed 7.5% of $\frac{V_s}{R}$ in either of the n=1 or n = 2 stages. This maximum error occurs only for particular analog voltage values, but for any analog value the error is less than the least significant bit value of $\frac{V_s}{4R}$. Additional stages would increase the percent error until further addition would not be practical. The inverting transistor stage at the output of each comparator which is necessary to vary the comparison voltage level can be used to eliminate this error if it is properly biased to clip the low voltage state. This inverter can also be used to compensate for the fan out error of each comparator with a suitable gain adjustment. In the previous manipulations resulting in values of compensation resistance required, it was assummed that the inverter exhibits high input resistance with respect to the Thevenin resistance and low output resistance with respect to the weighting resistance.

The encoder will encode analog signals from zero to minus $2V_S$ which indicates that positive signals must be inverted and a sign bit used or that the analog signal be decreased by V_S direct current volts before it is encoded. If the signal is decreased by V_S before it is encoded the encoding would be shifted to include the range $-V_S$ to $+V_S$ which would appear as zero volts for $+V_S$ and $-2V_S$ for $-V_S$. The output corresponding to the low voltage state of the tunnel diode in each compare stage represents a binary zero and the output corresponding to the high voltage state represents a binary one. Resetting of

the tunnel diodes can be accomplished by providing a sufficiently negative direct current in the absence of the positive switching pulse, which is provided in this encoder by the always negative input voltage. Table 2 indicated the encoding ranges, the shifted voltage ranges, the output voltage levels, and the binary code. The addition of the sign bit as mentioned above would provide an additional bit of precision and eliminate the necessity of shifting the voltage range.

TABLE 2

VOLTAGE LEVELS AND BINARY CODE FOR THE NTH STAGE ENCODER

Analog Voltage	Shifted Range Applied to Encoder	Output Voltage Levels			Binary Code
		V_0	V_1	V_2	
$-V_s$ to $-\frac{3V_s}{4}$	$-2V_s$ to $-\frac{7V_s}{4}$	V_L	V_L	V_L	000
$-\frac{3V_s}{4}$ to $-\frac{V_s}{2}$	$\frac{7V_s}{4}$ to $-\frac{3V_s}{2}$	V_L	V_L	V_h	001
$-\frac{V_s}{2}$ to $-\frac{V_s}{4}$	$-\frac{3V_s}{2}$ to $-\frac{5V_s}{4}$	V_L	V_h	V_L	010
$-\frac{V_s}{4}$ to 0	$-\frac{5V_s}{4}$ to $-V_s$	V_L	V_h	V_h	011
0 to $\frac{V_s}{4}$	$-V_s$ to $-\frac{3V_s}{4}$	V_h	V_L	V_L	100
$\frac{V_s}{4}$ to $\frac{V_s}{2}$	$-\frac{3V_s}{4}$ to $-\frac{V_s}{2}$	V_h	V_L	V_h	101
$\frac{V_s}{2}$ to $\frac{3V_s}{4}$	$-\frac{V_s}{2}$ to $-\frac{V_s}{4}$	V_h	V_h	V_L	110
$\frac{3V_s}{4}$ to V_s	$-\frac{V_s}{4}$ to 0	V_h	V_h	V_h	111

The reference voltage for this encoder is a periodic positive pulse of amplitude V_S and of sufficient pulse width to allow signal transmission through the three compare stages. If the frequency of the reference voltage is sufficiently high with regard to the highest frequency component of the analog signal, there is no need in sampling and holding the analog signal before it is encoded in view of the speed of the encoder which is primarily dependent on the switching speed of the tunnel diodes. An accurate account of the digital word periods can be accomplished by monitoring the output of the center stage. For higher precision encoding it may be necessary to provide sample and hold circuitry.

REFERENCES

1. Robert V. Cotton, Eugene Golberg, and Albert F. Tillman, "Design and development of analog-to-digital converters," Final Report Contract No. AF 33 (616)-6693 (Philco No. 2237-F), Philco Corporation, ASTIA No. AD-266731, pp. 4-15; September, 1961.

2. D. W. Allen and L. Smith, "High accuracy, airborne, voltage-to-digital converters, Part 1," Royal Aircraft Establishment, ASTIA No. AD-277088, p. 34; March, 1962.

3. B. T. Cronhjort, "A time coding analog-to-digital converter," Proceedings of the IEEE vol. 51, No. 11, p. 1542; November, 1963.

4. Reference No. 2, p. 22.

5. Reference No. 3, p. 1545.

6. Reference No. 2, p. 21.

7. Reference No. 1, p. 80.

8. H. Weinstein, "A high speed compare circuit," IEEE Trans. on Electronic Computers, vol. EC-12, No. 4, pp. 410-411; August, 1963.

9. R. A. Kaenel, "Hysteresis-Free-Diode Amplitude comparator," IRE Trans. on Electronic Computers, vol. EC-11, No. 2, pp. 286-287; April, 1962.

10. General Electric Company, Electromagnetic Warfare and Communications Laboratory, Aeronautical Systems Division, R. Remm, Project Engineer, "Insertion of wide band-width data for communications from reconnaisance satellites," Contract AF 33(657) 9148, ASTIA No. 290518, p. 4; November 25, 1962.

11. R. H. Bergman, "Tunnel diode logic circuits," IRE Trans. on Electronic Computers, Vol. EC-9, pp. 430-438; December, 1960.

12. G. W. Neff, S. A. Butler, and D. L. Critchlow, "Esaki diode logic circuits," IRE Trans. on Electronic Computers, Vol. EC-9, pp. 423-429; December, 1960.

IV. RELIABILITY ANALYSIS OF FORD INSTRUMENT DECODER

An experimental reliability analysis was performed on the Ford Instrument Decoder shown in Fig. 21.[1] The results of this analysis illustrate the stress levels of all components and the difference in stress levels experienced by using several types of transistors. Since the converter is only a workable prototype the reliability figures obtained will not be accurate for an integrated circuit design using this same scheme, but the procedure followed in the reliability analysis and the relative amounts that each stage is stressed should be useful in calculating a theoretical reliability figure and in the determination of the operating reliability of an integrated circuit design.

The first step in the experimental analysis was to determine a useful reliability equation for time sensitive items. The following equation was found to be adequate:

$$R\ (0, t) = e^{-t/\bar{t}} \tag{26}$$

The probability of survival (R) from time zero to time (t) equals the negative exponential of the ratio of the operating time (t) to the mean-time-between failure $(\bar{t})$.

The mean-time-to/between-failures for a system $(\bar{t})$ equals the sum of the products of the component adjusted failure rates (F_r) divided into one million. This adjusted failure rate (F_r) is the product of the generic failure rate (GF_r), the number of identical components used (N), the operating mode factor (K_{op}), and the application factor (K_A). If the redundancy is present, the failure rate of the redundant components equals the generic failure rate

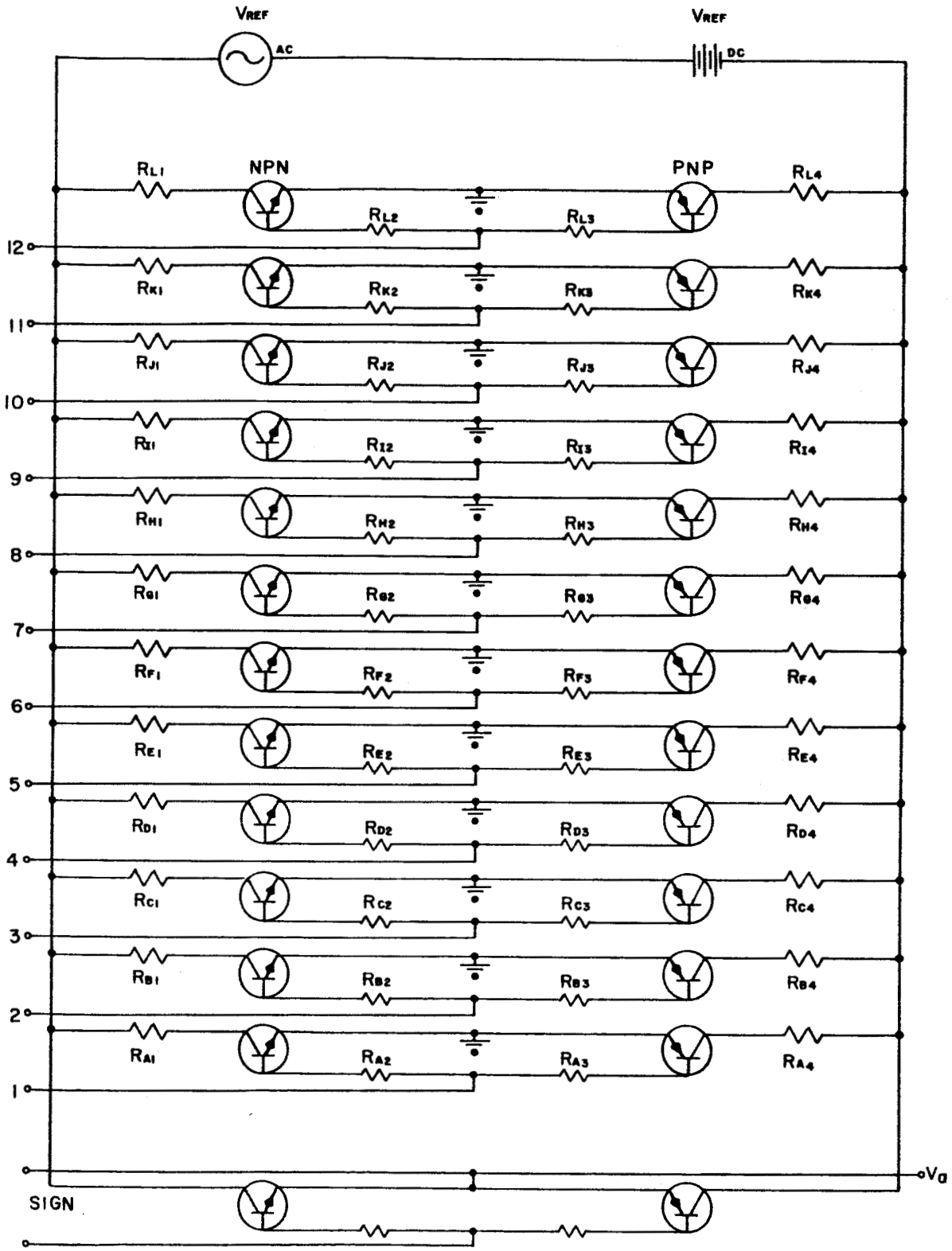


FIG. 21– FORD INSTRUMENT DECODER

of one of the components times the redundancy factor (K_r).[2] The final equation is shown below:

$$\bar{t} = \frac{10^6}{\Sigma GF_r (N) K_{op} K_r K_A} \tag{27}$$

The first quantity to be determined was the application factor (K_A). In finding (K_A), the graph shown in Fig. 22[3] was used for the silicon transistors. Similar charts were used for the collector and base resistors and the germanium transistors. The ambient temperature (T_a) was assumed to be 25°C.

The next step was to determine the ratio of operating power to rated power. Rated power for the collector resistors was determined to be 500 milliwatts; for the base resistors, 250 milliwatts. The rated power for the transistors is described by the following equation:

$$P = \frac{T_j - T_a}{K} \tag{28}$$

The junction temperature (T_j) and the constant (K) were given on the transistor characteristics.[4] The rated power for the 2N619 transistors was calculated to be 386 milliwatts; for the 2N1034 transistors, 250 milliwatts; for the 2N428 transistors, 150 milliwatts. The operating power was determined from actual measurements made with the decoder in operation. The measurements are presented in Table 3, while the results

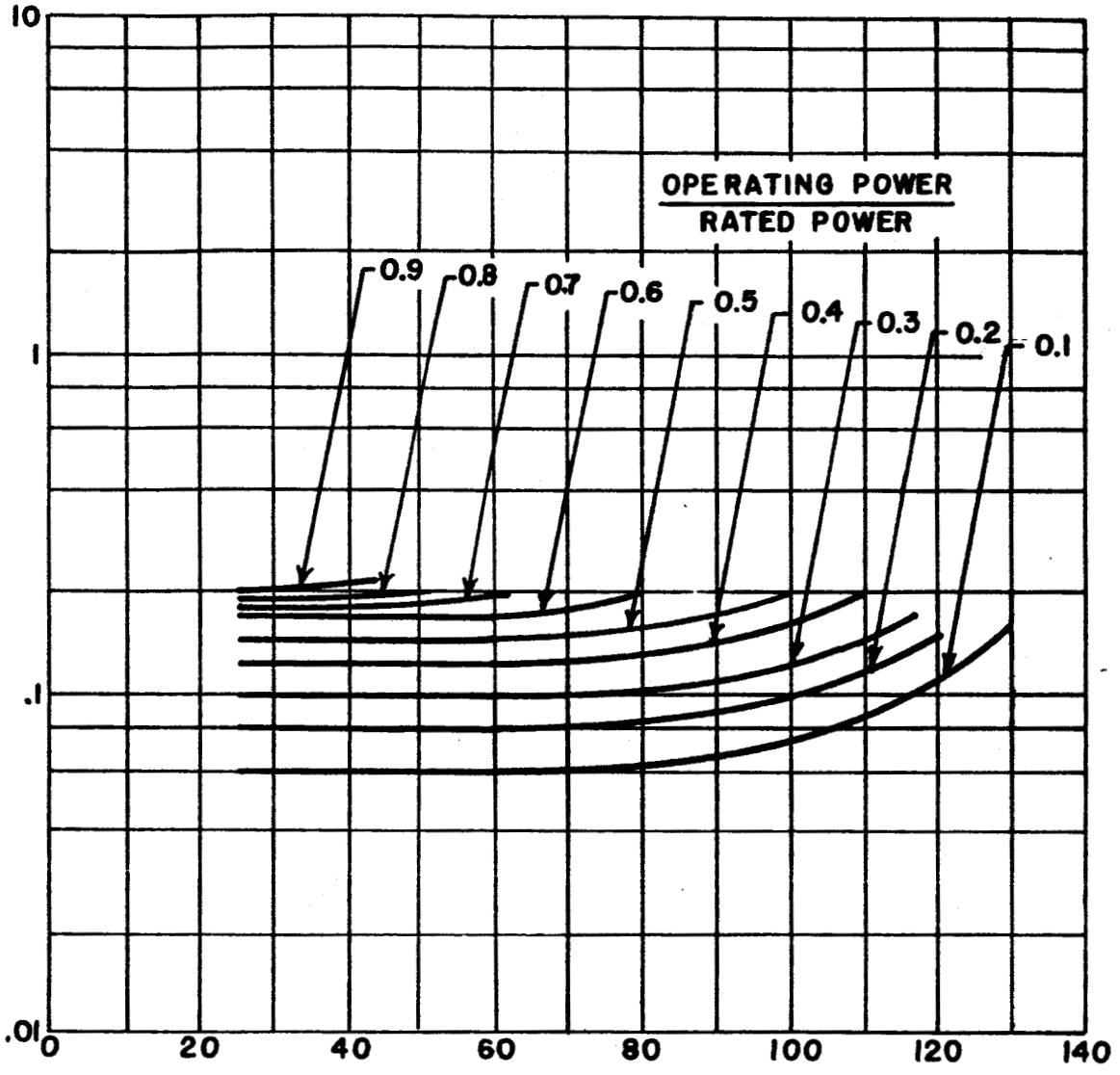


FIG. 22- APPLICATION FACTORS,[3] K_A- TRANSISTORS, SILICON

obtained from this data are shown in Table 4. Thus, with the ambient temperature and the ratio of operating power to rated power, the application factor (K_A) was read directly from the curves of Fig. 22.

The second quantity to be sought was the generic failure rate (GF_r).[5] The generic failure rates were found from tabular data to be, for the resistors, 0.57; for the transistors, 0.86; and for solder joints, 0.005. The operating mode factor (K_{Op}) was determined to be one, assuming the decoder is to be used in a laboratory computer. No components are redundant; therefore, the redundancy factor (K_r) equals one. Thus, with these quantities determined, the mean-time-to/between-failure was calculated using equation (27). These calculations are summarized in Table 5.

The last step was to substitute the mean-time-to/between-failure ($\bar{t}$) into equation (26), thus fixing the reliability as follows:

$$R(0, t) = e^{-t/1.48 \ (10^5)} \tag{29}$$

Though this reliability analysis is only an approximation, there are several assumptions that were made which should be mentioned when considering the dependability of the foregoing analysis. They are listed below:

1. The condition of digital inputs representing 2048, or 2047, was considered the most critical state for the decoder.

2. The operating power for the transistors was approximated by the product of collector current and collector-to-emitter voltage.

3. All application factors were read from the ratio of operating power to rated power equal to 0.1 curves, though the actual ratios were substantially smaller.

4. The application factor (K_A) for solder joints was assumed to be one.

5. All joints were assumed to be soldered and the total number of such joints was approximated at 108.

6. The decoder was assumed to be operating at room temperature 25°C.

TABLE 3

EXPERIMENTAL DATA

Transistor	Collector Resistor Voltage		Base Resistor Voltage		Collector Voltage		Collector Resistors	Base Resistors	
	NPN (Volts)	PNP (MV)	NPN (Volts)	PNP (MV)	NPN (MV)	PNP (Volts)		NPN (K)	PNP (K)
A	0	9800	0	5200	9900	0.011	6.25K	1.8	.62
B	9.8	39	5.2	76	86	9.8	12.5 K	30	20
C	9.8	64	4.6	77	60	9.8	25K	3	24
D	9.8	1	4.0	0.3	49	9.8	50K	2.4	7.5
E	9.8	270	4.5	26	10	9.5	100K	10	8.2
F	9.8	560	5.0	93	26	9.2	200K	12	30
G	9.8	1450	4.5	79	32	8.3	400K	3.9	16
H	9.8	2	5.0	0	22	9.7	800K	12	8.5
I	9.8	39	5.0	0.2	24	9.6	1.6M	15	4.3
J	9.8	33	5.2	0.6	15	9.4	3.2M	100	25
K	9.8	99	4.9	1.8	29	9.0	6.4M	6.2	68
L	9.8	19	5.0	0.2	18	8.6	12.8M	13	12

TABLE 4

OPERATING POWER

Transistor	Collector Resistor Power		Base Resistor Power		Transistor Power	
	NPN (MW)	PNP (MW)	NPN (MW)	PNP (MW)	NPN (μ W)	PNP (μ W)
A	0	15.4	0	43.5	0	17.3
B	7.7	$1.2(10^{-4})$	.9	$2.9(10^{-4})$	67.4	30.4
C	3.8	$1.6(10^{-4})$	7.1	$2.5(10^{-4})$	23.5	25.5
D	1.9	$1.3(10^{-8})$	6.7	$1.2(10^{-8})$	9.6	0.16
E	1.0	$7.3(10^{-4})$	2.0	$8(10^{-5})$	0.9	25.6
F	0.5	$1.6(10^{-4})$	2.1	$2.9(10^{-4})$	1.3	24
G	0.2	$5.25(10^{-8})$	5.2	$3.9(10^{-4})$	0.8	38
H	0.1	$6.6(10^{-9})$	2.1	0	0.3	0.28
I	0.1	$9.5(10^{-7})$	1.7	$1\ (10^{-8})$	0.15	0.23
J	0.03	$3.7(10^{-12})$	0.3	$1.4(10^{-8})$	0.05	0.09
K	0.02	$1.53(10^{-6})$	3.9	$4.8(10^{-8})$	0.05	0.13
L	0.01	$2.8(10^{-8})$	1.9	$3.3(10^{-9})$	0.01	0.01

TABLE 5

MEAN-TIME-TO/BETWEEN FAILURES

Part Description	Generic Failure Rate	K_A	K_{op}	Total Adjusted Fr/Part	K_r	No. of Items	Total Adjusted Failure Rate
Collector Resistors:	0.57	0.175	1	0.100	1	24	2.400
Base Resistors:							
R_{A3}	0.57	0.190	1	0.108	1	1	0.108
All Others	0.57	0.175	1	0.10	1	23	2.300
Transistors:							
2N428	1.91	.032	1	.059	1	7	0.413
2N1034	0.86	.060	1	.052	1	6	0.312
2N619	0.86	.060	1	.052	1	13	0.676
Solder Joints	0.005	1	1	0.005	1	108	0.540
Analysis by T. Nagle Approved by C. Carroll	Sum of Total Adjusted Failure Rates = 6.749						
	$\bar{t} = \frac{10^6}{\Sigma F_r} = \frac{10^6}{6.749} = 1.48\ (10^5)$						

BIBLIOGRAPHY

1. D. W. Allen and L. Smith, "High accuracy, airborne, voltage-to-digital converters, Part 1," Royal Aircraft Establishment, March, 1962. ASTIA No. AD 277088.

2. N. Aron and C. Granger, "Analog to digital converter uses transfluxors," Electronics 621.3805, Vol. 35, page 62-66.

3. M. S. Axelrod, A. S. Farber and D. E. Rosenheim, "Some new high speed tunnel diode logic circuits," IBM Journal of Research and Development Vol. 6, pp. 158-169; April, 1962.

4. C. W. Barbour, "Capcode analog to digital converter," Instruments and Control Systems, Vol. 35, No. 8, pp. 104-105; August, 1962.

5. Igor Batovsky, "Reliability Theory and Practice," Englewood Cliffs, New Jersey: Prentice-Hall, Inc. 1961.

6. J.R.A. Beale, W.L. Stephenson, E. Wolfendale, "A study of high-speed avalanche transistors," The Proceedings of the Institution of Electrical Engineers, Part B, Vol. 104, pp. 394-402; 1957.

7. R.H. Bergman, "Tunnel diode logic circuits," IRE Trans. on Electronic Computers, Vol. EC-9, pp. 430-438; December, 1960.

8. A. Blaustein, "Analog to pulse converter," Instruments and Control Systems, Vol. 35; p. 107, August, 1962.

9. A. F. Boff, J. Moll, and R. Shen, "A new high speed effect in solid-state diodes," Digest of Technical Papers, International Solid-State Circuits Conference, Philadelphia, Pa., pp. 50-51, February, 1960.

10. T.A. Brubaker and G. A. Korn, "Accurate amplitude distribution analyzer combining analog and digital logic," Scientific Instruments, Vol. 32, pp. 317-322; March, 1961.

11. R.L. Chase, "A servo-stabilized analog to digital converter for high resolution pulse-height analysis," IRE Trans. on Nuclear Science, Vol. NS-9, pp. 119-122, Jan. 1962.

REFERENCES

1. A. Romeo and R. Biarchini, "Design and development of a 12 bit digital-to-analog converter," Final Report No. FD-1022, Contract No. DA-30-069-1135, Ford Instrument Company, p. 16; February, 1960.

2. D. R. Earles, "Reliability Application and Analysis Guide," The Martin Company, pp. 6-7; July, 1961.

3. Reference No. 2, p. 86.

4. Technical Information, "Transistor Characteristics," Raytheon Manufacturing Company.

5. Reference No. 2, p. 87.

12. "Comparing pulse amplitudes," ENGINEERING; Jan. 19, 1962.

13. Robert V. Cotton, Eugene Goldberg, and Albert F. Tillman, "Design and development of analog-to-digital converters," FINAL REPORT, Contract No. AF 33 (616)-6693 (Philco No. 2237-F), Philco Corporation, Sept. 1961. ASTIA Technical Document No. AD-266731.

14. Robert V. Cotton, Interim Technical Report, "Investigation and study of a simplified conversion," Contract No. AF 33 (616)-6693 (Philco No. 2237-I), Philco Corporation, April 20, 1960.

15. R. M. Crayford, "Analog to pulse duration coding and logic," Instruments and Control Systems, Vol. 35, pp. 97-100; Jan. 1962.

16. B. T. Cronhjort, "A time coding analog-to-digital converter," Proceedings of the IEEE, Vol. 51, No. 11, pp. 1541-1549; November, 1963.

17. W. M. Dematteis, "A linear 4-bit current ladder for digital to analog conversion," Application Lab Report 752, Philco Corporation, Lansdale Division; Dec. 6, 1961.

18. W. M. Dematteis, "A 4-bit digital-to-analog converter," Application Lab Report 743, Philco Corporation, Lansdale Division; Oct. 25, 1961.

19. P. P. Fisher, "Analog to digital converters," ELECTRO-TECHNOLOGY, Vol. 69, No. 3, pp. 165-168, March, 1962.

20. A. A. Fleischer and E. Johnson, "An analog to digital converter capable of nanosecond resolution," IEEE TRANS. ON NUCLEAR SCIENCE, Vol. NS-10, pp. 31-35; Jan. 1963.

21. H. L. Funk, T. J. Harrision, and J. Jursik, "Converter that digitizes low level signals for control computers" AUTOMATIC CONTROL, Vol. 18, pp. 21-23; March, 1963.

22. W. M. Gaines and P. P. Fischer, "Tentative recommendation for the definition and testing of the dynamic performance of analog-to-digital converters," COMMUNICATION AND ELECTRONICS, pp. 387-394; Sept. 1961.

23. W.M. Gaines and P.P. Fisher, "Terminology for functional characteristics of analog-to-digital converters, CONTROL ENGINEERING, Vol. 8, pp. 97-98; February, 1961.

24. General Electric Company, Electromagnetic Warfare and Communications Laboratory, Aeronautical Systems Division, R. Remm, Project Engineer, "Insertion of wide bandwidth video data for communications from reconnaissance satellites," Contract No. AF 33 (657) 9148, General Electric Company, Nov. 25, 1962. ASTIA No. AD 290518.

25. W.M. Goodall, "Television by pulse code modulation," THE BELL SYSTEM TECHNICAL JOURNAL, pp. 44-57, Jan. 1948.

26. F.H. Goodenough, "High speed sampling and digitizing equipment for P.C.M. telemetry," IRE 1962.

27. B.M. Gordon and W.H. Seauer, "Designing Sampled data systems," CONTROL ENGINEERING, Vol. 8, pp. 127-132, April, 1961.

28. I. Hashi and M. Otsuka, "Multichannel pulse height analyzer using parametron logic," JAPANESE JOURNAL OF APPLIED PHYSICS, Vol. 1, No. 2, pp. 125-129; August, 1962.

29. G.C. Henderson, "Special purpose analogue-digital converter," ELECTRONIC ENGINEER, Vol. 32, pp. 602-608; October, 1960.

30. H. Heynisch, "A cylindrical coding tube for 8-digit code," Proceedings of the IEEE, Vol. 51, No. 11, pp. 1536-1541; November, 1963.

31. M. Y. Hsiao, "A decoder scheme using magnetic-core matrices for systematic codes," IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, Vol. EC-11, No. 4, pp. 575-576; August, 1962.

32. R.A. Kaenel, "High speed analog-to-digital converters utilizing tunnel diodes," IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, Vol. EC-10, No. 3, pp. 273-284; June, 1961.

33. R.A. Kaenel, "Hysteresis-free tunnel-diode amplitude comparator," IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, Vol. EC-11 No. 2, pp. 286-287; April, 1962.

34. T. Kiyono, K. Ikeda, and H. Ichiki, "Analog-to-digital converter utilizing an Esaki-diode stack," IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, Vol. EC-11, No. 6, pp. 789-791; Dec., 1962.

35. W.H.P. Leslie and D. Nairn, "Fast counter for adding or subtracting randomly related pulse trains," ELECTRONIC ENGINEER, Vol. 34, pp. 227-233; April, 1962.

36. O. B. Laug, "Pulse voltage comparator measures height of positive or negative pulses," ELECTRONICS, Vol. 34, pp. 70-71; Sept. 8, 1961.

37. R.S. Mackay, "Multichannel a/d converter links computer to the process," CONTROL ENGINEERING, Vol. 8, p. 149; June, 1961.

38. John S. Mayo, "Pulse-code modulation," ELECTRO-TECHNOLOGY, SCIENCE and ENGINEERING SERIES, Vol. 70, pp. 87-98; Nov., 1962.

39. Micro SADIC System, "High speed analog-to-digital converter," ELECTRO-TECHNOLOGY, Vol. 68, p. 142; Sept. 1961.

40. G.W. Neff, S. A. Butler, and D. L. Critchlow, "Esaki diode logic circuits," IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, Vol. EC-9, No. 6, pp. 423-429; December, 1960.

41. Peter G. Neumann, "Encoding and decoding for cyclic permutation codes," IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, Vol. EC-11, No. 4, pp. 507-511; August, 1962.

42. Robert E. Onley and Paul G. Sedlewiez, "Solid State analog-to-digital converter," Contract No. W62-0749-d, Aerial Measurements Laboratory, Northwestern University, May-June-July, 1962, ASTIA No. AD283377.

43. R. I. Ostler, "Practical methods of analog-to-digital conversion," INST. OF PRACTICE, December, 1960.

44. J. Pawlat and J. Wolloch, "A static ac to dc comparator with wide frequency range," COMMUNICATIONS AND ELECTRONICS, pp. 73-80; March, 1962.

45. R. J. Plummer, Final Report, Signal Corps Contract No. DA-36-039-sc-15475. Federal Telecommunications Laboratories; October, 1954. ASTIA Technical Document No. AD-61, 027.

46. "Pulse-amplitude comparator," RADIO-ELECTRONICS; August, 1962.

47. T.V. Rehwoldt, "Analog voltage-to-digital converters," Technical Memorandum, Analytical Design Department, Chrysler Corporation, Dec. 6, 1956. ASTIA No. AD-289595.

48. O.A. Reichardt, "Analog function generation by a general purpose digital computer," INSTRUMENTS AND CONTROL SYSTEMS, Vol. 35, p. 125, Jan., 1962.

49. R.K. Richards, "Digital Computer Components and Circuits," New York; D. Van Nostrand, Inc., Jan., 1959.

50. Donald Savitt, "A high-speed analog to digital converter," IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, Vol. EC-8, No. 1, pp. 31-35; March, 1959.

51. R.W. Sears, "Electron beam deflection tube for pulse code modulation," THE BELL SYSTEM TECHNICAL JOURNAL, pp. 44-57; Jan. 1948.

52. B. D. Smith, "An unusual analog-digital conversion method," IRE TRANSACTIONS ON INSTRUMENTATION, p. 155; June, 1956.

53. B.D. Smith, "Coding by feedback methods," PROCEEDINGS OF THE IRE, Vol. 47, No. 8, pp. 1053-1058; August, 1953.

54. P. R. Thomas, "Analyzer counts and times amplitude excursions," CONTROL ENGINEERING, Vol. 8, p. 163; April, 1961.

55. Vasil Uzunoglu, "A bistable flip-flop circuit using tunnel diode," PROCEEDINGS OF THE IRE, Vol. 49, No. 9, p. 1440; Sept. 1961.

56. Vasil Uzunoglu, "Circuits using tunnel diode flip-flops and PNPN diodes," IRE TRANSACTIONS ON ELECTRONIC COMPUTERS, Vol. EC-11, No. 6, p. 793-797; Dec., 1962.

57. V.A. VanProag and others, "Magnetic core converts voltage to pulse duration," CONTROL ENGINEERING, Vol. 8, pp. 87-88; August, 1961.

58. H. Weinstein, "A high-speed compare circuit," IEEE Transactions on Electronic Computers, Vol. EC-12, No. 4, pp. 410-411; August, 1963.

59. F. H. Wells, and J.C. Page, "Pulse counting and fast scaling transistor circuits," British Institution of Radio Engineers Journal, Vol. 23, pp. 231-235; March, 1962.

60. N. Winterbottom and J.S.B. Walters, "High-speed analogue to digital converter," Electronic Engineer, Vol. 33, pp. 144-149; March, 1961.

61. F.C. Yao, "Analysis of signal transmission in ultra high speed transistorized digital computers," IEEE Transactions on Electronic Computer, Vol. EC-12, No. 4, pp. 372-383; August, 1963.