Final Report

on

STUDY IN OPTIMIZATION OF MICROCIRCUIT DESIGN

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STUDY IN OPTIMIZATION OF MICROCIRCUIT DESIGN

1. INTRODUCTION

The last three years has seen an extremely rapid growth in the technology and application of microcircuits. Much of this growth is the direct result of a heavy investment on the part of both military and civilian agencies in this area. While initial efforts were based on the hope of obtaining reduced weight and power requirements, much of the present emphasis on microcircuits is based on the desire to provide electrical functions more reliably than are obtained by their hand-wired macroscale counterparts. As such, many studies have already been made in the area of system design and organization with a view towards achieving this goal. Simultaneously, considerable work has been undertaken to study the basic physics of failure, and to obtain an understanding of the fundamental mechanisms that affect reliability.

In addition to the above studies, the development of microcircuits has taken place in a rapidly changing technological environment. Most of these technological developments have greatly increased the performance of microcircuits, while simultaneously reducing their cost.

This program is aimed at investigating problems pertaining to aspects of device technology, circuit design, and logical design which directly influence the reliable operation of a microcircuit subsystem. A program of this sort is, of necessity, interdisciplinary in nature. In contrast to the use of personnel whose specialty interests are in these areas, we have attempted to pull together at Rensselaer an organization in which each member has a broad range of interest in <u>all</u> these areas.

Three tasks have been selected for this effort. The specific aims of these tasks are as follows.

a) To investigate the use of Nickel as a substitute for Gold in the fabrication of high speed microcircuits.

b) To investigate the noise immunity of high speed saturated logic microcircuits.

c) To investigate oscillation hazards in asynchronous sequential circuits.

These problems cover, respectively, important aspects of device technology, circuit design, and logical design which bear directly on the reliable operation of high speed microcircuit subsystems.

In this report, a brief outline of each program is first presented, with a summary of the work accomplished. Details of this work are referred to a series of Appendixes which follow. Suggestions for further work along these lines are also made.

2. SUITABLE ALTERNATIVES TO GOLD IN SILICON

2.1 The Problem

At the present time, gold is used extensively in the fabrication of silicon devices requiring low minority carrier lifetime. Usually, gold diffusion is the final process in fabrication, prior to metallization and encapsulation. The introduction of gold results in a number of problems:

a) Gold has an extremely high diffusion constant, about five to six orders of magnitude greater than that of the usual semiconductor dopants (Boron and Phosphorus). Thus, the gold atoms cannot be considered immobile in devices which must be stored at 300° C or higher.

b) Gold is a noble metal. Diffusion can only occur out of the elemental metal, since all presently known gold salts dissociate at typical diffusion temperatures (1100° C - 1200° C).

c) Gold forms a eutectic with silicon at 375° C. Thus, the diffusion proceeds from a gold-silicon alloy, resulting in damage of the surface to a depth of many microns. This is of no consequence when the entire microcircuit must be gold doped. In this case, gold is applied to the side of the wafer that constitutes the substrate, and the damaged layer is mechanically removed prior to encapsulation. In some important microcircuit applications, selective lifetime reduction is necessary for optimum performance (an example of a circuit of this type is the diode-transistor logic gate.) Here, it is necessary to use the actual side of the wafer on which the microcircuit is fabricated. Since modern microcircuit devices are fabricated within the first few microns of semiconductor material, the use of gold is not feasible in this instance.

d) Gold is metallurgically incompatible with aluminum, which is ordinarily used for making contacts to the devices in the microcircuit. At elevated temperature, gold in the presence of aluminum and silicon gives rise to the well-known "purple plague", which is a serious mechanism for semiconductor failure.

2.2 The Approach

There are a number of materials that are potentially useful for reducing lifetime in silicon. Thus, almost all of the transition elements (iron, nickel, cobalt, and copper) are suitable candidates for this application. In general, all these elements exhibit one or more deep lying impurity levels in silicon, and provide recombination centers for minority carriers. These elements provide the starting point for a search for a substitute for gold. Ideally, such a substitute

would have a lower diffusion constant than that for gold in silicon, the ability to be diffused from a glass-like source which does not damage the surface of the silicon, a suitable capture cross-section so as to provide sufficient reduction in the lifetime of minority carriers, and metallurgical compatibility with the material used for making electrical contacts.

For the purpose of this program, nickel was selected as a candidate for study. The choice of this material was based on the fact that there is already in existence a body of knowledge concerning some of its properties in silicon. In addition, we have considerable past experience at Rensselaer on the utilization of nickel in microwave devices*.

2.3 Program Effort

2.3.1 Literature Study

The program was initiated with a short survey of the existing literature on nickel in silicon. The findings of this survey are as follows:

a) Using radioactive tracer analysis, the solid solubility of nickel in silicon is seen** to be retrograde in character, peaking at 5×10^{17} atoms per cc. at 1260° C. Figure 1 shows this solid solubility characteristic. It should be emphasized that this curve indicates the total nickel content that can be present in silicon. In addition to electronically active nickel, this includes inactive nickel in its various forms (oxides, silicides, precipitates and interstitials).

b) Figure 2 shows the phase diagram for the nickel-silicon system. The phase indicating solid solution of nickel in silicon is not shown in this diagram. The formation of $NiSi_2$ by a peritectic reaction is of importance, and is seen to take place at temperatures above 993° C. This compound (48.90 wt % of Si)

* Ghandhi, S. K. et al, "Impact Ionization Devices", Trans. IEEE Group on Electron Devices, ED-13, no. 6, p. 515-519, 1966.

** Yoshida, M. and Furusho, K., "Behavior of Nickel as an Impurity in Silicon", Japan J. Appl. Phys., v. 3, no. 9, p. 521-529 (1964).

is formed on the surface of the wafers during our experiments, and it is expected that it is also present within the wafer to some extent.

c) Nickel diffuses interstitially into the silicon lattice, and freezes into both substitutional and interstitial sites. In addition, compound formation is present in increasingly large amounts at diffusion temperatures above 1000° C.

Consequently, we may expect only a fraction of the nickel to be electronically active in silicon. Over the range 1100° to 1200° C, the diffusion constant has been estimated* to be on the order of 10^{-4} to 10^{-5} cm^2/sec.

d) Nickel is weakly p-type in silicon. Hall measurements and concentration temperature dependence measurements have established two acceptor states, at 0.35 ± 0.03 eV. below conduction band and 0.23 ± 0.03 eV. above the valence band. These are both deep lying states, and can serve as centers about which the recombination of minority carriers can take place. In contrast, gold is amphoteric in nature, and provides one donor and one acceptor state in silicon.

2.3.2 Compensation Effects

A study has been made of the compensation effects of nickel in silicon. The aim of this study (theoretical as well as experimental) was to determine the percentage of electronically active nickel in silicon. In this manner, it is possible to predict such device properties as parasitic series resistence when nickel is used for lifetime degredation in semiconductor devices.

A theoretical analysis was made of the compensation effects of nickel in n-type silicon. This analysis considered the statistics of multiple-charge states,

* Alberts, J. H., and Verheyhe, M. L., Appl. Phys. Letters, v. 1, p. 19-20 (1962).

and resulted in the development of a design curve relating the majority carrier concentration both before and after nickel doping, as a function of nickel concentration. Details of this analysis are outlined in Appendix A. With the aid of this curve, it is possible to determine the shift in the Fermi level, and also the degree of resistivity change when nickel is added to n-type silicon. By correlating with actual resistivity changes determined by experiment, it is possible to use this analysis to determine the amount of nickel that is electronically active at various diffusion temperatures.

Experiments were conducted to determine the compensation effects of nickel in silicon. A number of slices of n-silicon, ranging in resistivity from 0.1 ohm-cm to 2.5 ohm-cm were used in the experimental study. This is generally considered to be the useful range of resistivities for the fabrication of semiconductor diodes and transistors. Resistivities as high as 6.0 ohm-cm were used in a few of the experiments.

These slices were first lapped to 1000 grit and etched, and specific resistivity measurements made with a four-point probe. Next, the wafers were coated with nickel. Many experiments in the gold doping of silicon have stressed the necessity of complete removal of SiO_2 prior to the coating step, if uniform diffusion is desired. To this end, Wilcox* and co-workers have noted (with gold) that electroless plating methods are superior to vacuum deposition, if the electroless deposition step is carried out in a oxide-dissolving solution. Consequently, a highly basic electroless nickel bath was used in our experiments.

It is worth noting at this point that the use of a plated diffusion source often leads to many contaminants entering the host lattice. These contaminants

*Wilcox, W. R., et al, Jour. Electrochem. Soc., v. 111, no. 12, p. 1377-1380, 1964.

fall into two classes -- the highly soluble shallow impurities (such as phosphorous and aluminum) and the relatively insoluble deep lying impurities (such as cobalt, manganese, iron, and copper). A comparison of the widely differing diffusion constants of nickel and the shallow lying impurities shows that a lapping step, after diffusion, is effective in eliminating any trace of the latter slow diffusion impurities. In addition, a comparison of the solid solubility of nickel with that of other deep lying impurities shows that, even in the presence of the latter, the former is predominant. A final check on the freedom from detectable amounts of unwanted contaminants was seen in infrared transmission runs (performed on another program at Rensselaer) of samples doped in this manner, which were singularly free from spurious absorptions.

Diffusion runs were made at temperatures ranging from 900° C to 1250° C. In each case, the diffusion time for nickel was computed on the basis of the known diffusion constant for gold (a good guess, at best!) and a generous safety factor used to ensure uniform doping. Since infinite source diffusion was used, the doping level of the samples was considered to be that set by the solid solubility limit for that temperature.

After diffusion, the samples were rapidly quenched in air, and cleaned and etched to remove all surface contamination. At this point, the specific resistivity was again measured by the four-point probe.

Since the four-point probe technique leaves considerable margin for error, additional measurements were taken by an alternate technique, as follows:

Individual wafers of differing resistivity were selected. These wafers were quartered. The first quarter from each wafer was plated with N+ contacts, sintered, and diced. Measurements were made of the physical dimensions and resistance of individual dice after ensuring that the contacts were "ohmic". From this data,

resistivity values were obtained, and an average taken. In each case, a correction was made for the fact that the effective thickness of the wafer was reduced because of the lapped nature of its surface (prior to the application of N+ contacts).

The experiment was repeated on the other quarters, after nickel diffusion at temperatures ranging from 900° C to 1150° C. The curves for resistivity before and after nickel diffusion are shown in Figure 3. Data on the 900° and 950° C nickel diffusions showed essentially no detectable increase in resistivity. Using the data from the 1000° C diffusion curve, it is seen that the resistivity is increased from 6.75 ohm-cm to 10 ohm-cm due to nickel diffusion at 1000° C. With the aid of Appendix A, we calculate an active nickel concentration of 1.035×10^{14} atoms/cc for this case, of which 7% is singly ionized and 93% doubly ionized. With the aid of the solid solubility curve, this would indicate that about 0.10% of the nickel is in active sites for this diffusion temperature.

The fraction of active nickel in silicon is seen to fall off at higher temperatures. This would appear reasonable, because of the increased formation of compounds at higher temperatures. By 1150° C, highly variable results were noted from sample to sample. In fact, at 1250° C, the resistivity of the material after diffusion was actually found to be less than that before diffusion! No attempts were made to explain these diffusion anomalies. It was decided that further experiments would be confined to the temperature range of 1150° C and lower.

2.3.3 Minority Carrier Lifetime

Experiments were conducted to determine the effect of nickel doping on the minority carrier lifetime. Initially it was planned to conduct these experiments with wafers of 0.25, 0.5, 1.0 and 2.5 ohm-cm resistivities. However, time did not permit such a complete study to be undertaken, and the lifetime experiments were confined to the use of 0.5 ohm-cm wafers. It was felt that this was not an undue restriction, since there is no reason to believe that effects will be significantly different for other resistivities.

Minority carrier lifetime was measured by the recovery time method. In this method, p-n diodes are fabricated and their recovery time correlated to the minority carrier lifetime by the technique outlined in Appendix B. This approach was used because (for our range of lifetime values) it is easier to instrument than the photo-conductive decay method. In addition, the method has self-checking features on its accuracy, as described in Appendix B.

Devices were fabricated in the following manner:

a) Wafers of 0.5 Ω cm resistivity were cleaned and lapped with 1000 grit. One side of the wafers was wax masked and the wafers etched to remove surface damage. A relatively slow etch (HF-HNO_3-CH_3COOH system) with an etch rate of about 10 μ per minute was used.

b) The wafers were now pre-deposited with B_2O_3 for 10 minutes at 1175° C, a closed box technique being used for this step.

c) Drive-in was conducted at 1175° C for varying periods of time. In each case, this comprised a half hour period in pure oxygen, with the rest of the period in a 97% N_2, 3% O_2 gas mixture.

Initially, wafers were diffused to a junction depth of 10 μ. In later experiments, however, the diffusion depth was reduced to under 5 μ. This had the advantage of considerably reducing diffusion time, and thus reducing the possibility of contamination during the diffusion run.

d) After drive-in, the wafers were washed in HF to remove the boro-silicate glass, and the reverse side was lapped and nickel-plated. Each wafer was quartered; the nickel was stripped off one of these quarters, while the other three were diffused at different diffusion temperatures. In some of the experiments, diffusion temperatures were nominally 1150° C, 1100° C and 1050° C while in yet others, diffusion temperatures of 900° C, 950° C and 1000° C were used. In this manner, the range from 900° C to 1150° C was covered. Adequate time was allowed for the diffusions in each case. Experimental data showed that the diffusion time was relatively unimportant in all cases as long as it was in excess of half an hour. In some of our early experiments, nickel diffusion was done while the boro-silicate glass was still remaining on one side of the wafer. This was found to give extremely variable results, especially for high diffusion temperatures. Often, there was noted a strong gettering effect* at these temperatures, (1000° C upwards) and the procedure was discontinued. All the test data on minority carrier lifetime was thus taken on wafers which were nickel diffused from one side, and free from boro-silicate glass on the other.

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* Ing, S. W., et al, Jour. Electrochem Soc., v. 110, no. 6, p. 533-537, 1963.

This ensured the absence of competing mechanisms of nickel diffusion and nickel gettering, and lead to consistent experimental results.

e) After diffusion, the wafers were air quenched, and back-lapped to remove the nickel-silicon interface region. The upper face of the wafer (in which the boron diffusion was conducted) was vacuum coated with aluminum. The metallized wafers were diced and sintered, and individual dice used to make devices.

f) The individual dice were bonded to TO-5 headers using 0.25% Sb-doped gold-germanium eutectic preforms. Considerable trouble was experienced with this fabrication step. The problem was ultimately traced to the fact that our die-bonder (home-made) had no provisions for scrubbing the die on the header to facilitate the removal of surface oxides. The problem was eliminated by using the following subroutine:

> After sintering, the individual dice were bedded, aluminum face down, on a lap block coated with wax. These dice were lapped for about a minute in 1000 grit, and the freshly lapped dice stored in trichloroethylene (TCE) prior to their use. In addition, the headers were boiled in TCE for five minutes prior to the bonding operation. This series of steps resulted in a consistently successful bonding operation.

g) A nail head bonder was used to make the thermo-compression bond to the wafer. Three-mil gold wire was used, with a preheated capillary. No problems were encountered here, once operator skill was developed. The other end of the bonding wire was spot welded to the post in the TO-5 header.

h) Devices were next etched in CP4. Since the nail head bond is made with gold wire, this served as a mask, while the CP4 etched away the exposed

material. In this manner, a mesa structure was produced. Early devices, with a 10 μ junction depth, required rather heavy mesa-etching. Often, this resulted in undercutting of the aluminum layer below the gold bond, with resultant separation of the bond from the device. This problem was not experienced in the 5 μ structures, where the etching cycle was considerably shorter.

i) After etching, the devices were boiled in deionized water and trichloroethylene, and baked out at 250° C for a short interval of time. Considerable trouble with surface phenomena was encountered at this juncture. The results were quite erratic, with leakage currents ranging from under 1 na to values in excess of 50 μa! In addition, devices with excessive leakage showed excessively low values of breakdown voltage. Since this problem was experienced on over 50% of the devices, experiments were conducted to improve the yields leading to the following processing steps which were found to be successful:

> The devices were rinsed in dilute hydrochloric acid for a few seconds to remove the unmasked aluminum layer. After a brief rinse in deionized water, the devices were etched for 30 seconds in CP-4. Fresh etchant was used with each device. Devices were rinsed in de-ionized water and then air dried. The devices were boiled in Transcene (a proprietary cleaning agent similar to $C\ Cl_4$, available in an ultra-pure grade). A 30 minute bake-out was provided at 250° C.

As a result of the above processing, over 80% of our devices were satisfactory (leakage current $\leq$ 10 na at 10 volts reverse bias). Consequently, no further attempts were made to improve upon this procedure.

j) With a number of devices, angle lap and staining techniques were used to display the junction, which was typically 10 μ deep in the initial diffusions, and 4 μ deep in the more recent devices.

k) Diodes, with "satisfactory" reverse characteristics (under 10 na at 10 volts) were next checked for capacitance at three values of reverse bias (3, 4.5 and 7.5 volts). A plot of the C-V curve showed that the diodes were graded ($n = 1/3$). The capacitance data allowed checking the comparative areas of the different diodes. Only slight variation was seen from device to device (Values of C at 7.5 volts ranged from 4.95 pf to 3.81 pf). Using design curves* for the capacitance of a graded junction, this would indicate junction areas from 105 sq. mils to 81 sq. mils.

For each device, the breakdown voltage was noted as well as the nature of the breakdown characteristics (i.e. hard vs. soft breakdown). In addition, the forward voltage drop was also measured at two values of forward current (10 ma and 50 ma) in order to determine if the forward parasitic resistance had been increased by the introduction of nickel.

At this point the diodes were tested for reverse recovery in a special test jig that was used in conjunction with a sampling oscilloscope. Details of the actual measurement procedure and its theoretical basis are given in Appendix B. Included are also examples of the application of this method to representative devices nickel-doped at temperatures from 900° C to 1150° C. For comparison, data on a high speed gold doped diode (type 1N914) is also shown.

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* Warner, R. M. and Lawrence, H., Bell System Tech. J., vol. 39, p. 389-404 March, 1960.

Figure 4 shows the results of lifetime measurements on various devices that were nickel diffused over the range of 900° C to 1147° C. The individual points correspond to separate devices, with the device number marked in each case. In this manner, the degree of spread in the data is shown in addition to the magnitude of the lifetime.

The following points of interest are noted:

a) The initial material (rotated Czochralski-grown n-silicon) had a lifetime of about 70 nanosecs.

b) On nickel diffusion at 900° C for one hour, the lifetime rose to 400 nanosecs. This is due to the gettering action* of initially present deep lying impurities (such as copper and gold) by the nickel. Since the solid solubility of active nickel is considerably less than that of these impurities, the lifetime enhancement effect due to their removal predominates over the lifetime degredation effect due to nickel diffusion.

c) With increasing temperature, the minority carrier lifetime falls until a diffusion temperature of 1093° C is reached. This is due to the fact that increasingly large amounts of active nickel are present at higher temperatures.

Bakanowski and Forster** have shown that, for gold in low resistivity silicon, the lifetime is inversely proportional to the number of gold centers. We do not find this to be the case with nickel, and ascribe this to the fact that nickel is a two-level recombination center, and also to the fact that nickel provides initially a gettering action for impurities already present in the silicon. A best-fit straight line is drawn through the points over the range 900° C to 1093° C.

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* Silverman, S. J. and Singleton, J. B., Jour. Electrochem. Soc., v. 105, p. 591, 1958.

** Bakanowski, A. E. and Forster, J. H., Bell System Tech. Jour., v. 39, p. 87 (1960).

d) Diffusion at 1147° C results in a rapid increase in lifetime, to a value close to that for the undoped material. This anomaly was verified on a number of devices from different wafers, and has been ascribed to the fact that a large amount of the nickel is essentially combined with the silicon to form nickel silicides, having a lower capture crossection to minority carriers than that of the original active nickel.

It was not possible to show the manner in which the leakage current varied with the nickel doping level. This was due to the fact that this current (in our mesa structures) was often dominated by the presence of surface states. The leakage current was measured on some devices which were heavily doped with nickel, in which surface effects appeared small (i.e., diodes with sharp breakdown characteristics, in the neighborhood of 60 volts). Figure 5 shows the leakage current of a representative diode of this type, nickel diffused at 1047° C. As expected, this leakage current is predominantly due to charge generation* in the depletion layer. This charge generation takes place at various deep lying sites in the forbidden band and is thus enhanced by the presence of nickel. In passing, it should be noted that this leakage current is about 100 times as large as what would be expected for a typical silicon p-n junction diode that was not nickel doped.

2.3.4 Diffusion from a Glassy Source

A number of attempts were made to diffuse nickel from a glassy source. These met with no success at first. However, some success was achieved in our later experiments. These experiments have shown that it is possible to obtain a reasonable quality glass containing nickel on the surface of

* Sah, C. T. et al, "Carrier Generation and Recombination in PN Junctions and PN Junction Characteristics", Proc. IRE, v. 45, p. 1228-1243 (1957).

a silicon wafer. It has also been shown that this glass ($NiO-V_2O_5$ system) can be removed without apparent surface damage to the silicon. In addition, compensation effects have been noted when this glass was used as a diffusion source. Details of these experiments are provided in Appendix C, with suggestions for additional work that is required before a completely satisfactory process can be considered to have been developed.

2.4 Conclusions

This study has investigated the feasibility of using nickel as a substitute for gold in silicon. It has been shown that

a) Nickel can be used to reduce lifetime to the level normally required in high speed switching devices. However, the behavior of nickel in silicon is considerably more complex than that of gold due to effects at both extremes of the diffusion temperature range. In addition, the lifetime degredation effect is a more strong function of temperature than for gold, leading to a more severe control problem during the diffusion step.

b) Compensation effects of nickel in silicon are not of importance in high speed switching devices where low resistivity materials are used ($\leq$ 0.5 ohm-cm). This is true, not withstanding the fact that the active nickel is doubly ionized in these materials.

c) Nickel can be diffused from a glassy source. In addition, this source can be stripped (with difficulty) without apparent damage to the silicon wafer. Thus, it should be possible to diffuse nickel from the top surface of a silicon microcircuit.

3. NOISE IMMUNITY IN MICROCIRCUITS

3.1 The Problem

The microcircuit, with its small size, low power dissipation, and high reliability, has already found wide usage in complex subsystems that were considered impractical a few years ago. The present trend to the integration of even more complex subsystems places an increasing emphasis on the design of microcircuits that can be easily combined in large ensembles. Most present day microcircuits are designed with the emphasis placed on the attainment of performance parameters. These include such terms as propagation delay, fan-in, fan-out, and power dissipation. Of equal (but often considered secondary) importance are those characteristics which will determine the ability of a single circuit to be used in a variety of environments with a minimum of "hand trimming" and "de-bugging". The most important of these characteristics is the ability to have a high degree of immunity to noise, in both the "on" and "off" states. This ability will reduce, or eliminate, the need for attention to precise clocking and phasing, as well as the need for elaborate shielding and grounding.

The saturated logic gate is today the most widely used building block for microelectronic computing elements. It is operable over a wide range of temperatures and parameter spread; while not as fast as its non-saturated counterpart, it operates at lower power dissipation levels, and does not amplify signals (both wanted and unwanted) in their passage through the gate.

At low operating speeds, the noise immunity of a saturated gate can be made arbitrarily high by increasing the threshold at which the gate operates. This technique results in increasing the propagation delay through the gate, but this increase can be avoided by using an inherently faster device in the gate design.

With high speed gates ($\leq$ 4 nsecs propagation delay), it is necessary to effect a trade between the noise immunity and the propagation delay. Thus, it is necessary to critically determine the noise capability of the gate, taking into consideration the nature of the noise signals to which it is subjected.

3.2 The Approach

In this program we have concentrated our study on the saturated transistor-transistor-logic (T^2L) gate. This gate is becoming recognized as the one that has the greatest potential for high speed operation in the saturated mode. Over the last two years, an increasing number of manufacturers have been developing circuit lines using this type of gate.

There are essentially two types of "noise" that can cause malfunction in a digital circuit. The first of these, commonly referred to as d-c noise, is characterized by its presence in the form of pulses that are so wide that they present, in essence, a d-c input to the gates. Such pulses are commonly associated with power supply transients and resistively coupled paths. The second type of noise is known as pulsed noise. Far more frequently encountered, this noise consists of low duty cycle pulses, and is capable of being generated or picked-up whenever short rise-time signals are being transmitted or processed.

In this study we have attempted to evaluate these sources of pulsed noise in microcircuits, and determined the manner in which this noise pick-up can cause a malfunction in the basic T^2L gate. In addition, we have shown a correlation between this pulsed noise immunity and the internal device parameters of the gate. Finally, we have shown that it is possible to design the gate for a specified value of pulsed noise immunity without unnecessarily compromising its performance.

3.3 Program Effort

3.3.1 A Study of Pulsed Noise

A detailed study of pulsed noise has been undertaken. Since the transistor is essentially a charge controlled device, this study has concentrated on determining the charge content of the various forms of noise that may be encountered. Details of the study are outlined in Appendix D.

The following conclusions have been made concerning the nature of noise signals generated in digital circuits:

a) The most serious forms of pulse noise (having wide pulse widths and high charge content) are those generated in coupled interconnection paths between circuit boards, and those caused by mistiming.

b) Other noise sources are of secondary importance. Thus, if the logic stage is capable of tolerating noise signals of the former type, it is not necessary to consider the latter.

3.3.2 D.C. Terminal Characteristics

A T^2L gate was designed and constructed using high speed transistors (2N709) for both the coupling and inverting elements. Under test, this gate was operated with a propagation delay of 3-4 nsecs. into a fan-out of 4. This gate was used as the vehicle for test in the experiments.

An elementary analysis was made of the input and transfer characteristics of this gate. Correlation with the experimentally measured characteristics was sufficiently close so that a more detailed analysis was not found necessary. This analysis, together with the experimental data for this gate, are outlined in Appendix E. Using the analysis, the d.c. noise margin of the gate was obtained.

The noise immunity of a gate of this type is commonly expressed by manufacturers in terms of this d-c transfer characteristic (10% by some and 50% by others). This is quite misleading, since it does not take into account the nature of the malfunction signals that are presented to the gate, and also since it refers to a region of the gate where the characteristics are rapidly changing.

3.3.3 Switching Characteristics

A dynamic analysis was made of the switching characteristics of the gate in order to determine which internal parameters are of significance in computing the propagation delay. This analysis is outlined in Appendix F. It is seen that the turn-on delay is a significant factor in the propagation delay. This term is controlled by the parasitic capacitance at the base of the inverter transistors, and by the base

resistance of the coupling transistor through which it is charged.

In addition, it is seen that the storage time of the inverter transistor Q_2 is controlled by the parasitic resistances associated with the collector of Q_1 and Q_o, and with the base spreading resistance of Q_2. The expression for fall time is complicated since the equation governing this parameter is nonlinear* due to the fact that the base is essentially shorted to ground (through the coupling transistor and the previous inverter stage).

3.3.4 Noise Immunity

The noise immunity for the gate was measured, by feeding into its input narrow pulses with short rise times. A mercury relay pulse generator was used for this purpose, the pulse length being set by means of delay lines of variable length. At the outset, there was considerable difficulty in determining the magnitude of the output signal that should be interpreted as a malfunction indication. (This problem is especially serious with fast rise time pulses where the effect of Miller capacitance in the transistors results in an output for all values of input signal.)

It was decided that a digital indication of malfunction should be used. With this in mind, a sensitive, high speed unloaded flip-flop was hung on the gate to provide this information.

Experiments conducted with this circuit showed that the malfunction signal was a critical function of the malfunction indicator as well as of the gate under test. Accordingly, it was decided that a malfunction indicator, made with gates identical to the one under test, would have

* Thiney, A. "Rise and Fall Times of Transistors in Switching Operation Regardless of the Driving Source Impedance", IEEE Trans. on Elec. Comp., vol. EC-13, p. 616-620, 1964.

significant advantages over the previous indicator. Thus,

a) The noise immunity would now be only a function of the gate (or rather, gates) under test.

b) The results would specify a more functional value of noise immunity. Thus, we consider malfunction to have occurred when the input noise pulse to a gate is sufficiently large so as to transmit logical information to the succeeding stages. In this manner, we define the noise immunity of a gate in terms of its ability to prevent the flow of error-causing signals to successive circuits.

Our experiments were conducted with discrete components, to which parasitic capacitances were added whenever necessary. If actual microcircuit gates are being tested, the measurement of pulse noise immunity should be done by interconnecting them at their terminals, without the necessity of making internal connections. The advantages of this approach for evaluating competitive microcircuits are immediately apparent. The measurement scheme thus takes the form shown in Figure 6.

The analysis for the pulse noise immunity of the T^2L gate is detailed in Appendix G. Here, expressions are derived for the input current as a function of pulse width required to cause malfunction, and excellent correlation is seen to exist between theory and experiment. The experiment was repeated for the same circuit, using 2N706 devices (which are considerably slower) for the individual elements. Again, the results were predictable from the theoretical analysis.

The analysis shows that τ, the width of the pulse required to cause a malfunction, is given by

$$\tau = K/I + \tau_o$$

where τ_o and K are constants for a given circuits, and I is the current. In addition, it is shown that K is a function of the rise time alone, while τ_o is a function of turn on delay and storage time.

The circuit has essentially infinite pulse immunity when the input noise pulse width is less than the sume of the turn on delay and the storage time. On the other hand, the propagation delay through the stage is given by

$$t_{pd} = t_d + 0.5\ t_r, \text{ or}$$
$$t_{pd} = t_s + 0.5\ t_f.$$

whichever is larger*. Thus, there is some degree of independence between these parameters, so that there is design freedome in the choice of these two circuit properties.

It is clear that the proposed method of test can be directly applied, if required, to a measurement of the d.c noise margin of the gate. Because of the feedback action of the cross-coupled gates, the transfer function has an abrupt transition region, and there is thus no problem of interpretation in computing this data from the curve.

3.4 Conclusions

In this program, a study has been made of the sources of spurious noise signals in high speed switching circuits using saturated logic gates. A new method has been proposed for characterising the performance of such gates to noise pulses. This method involves the direct use of three interconnected gates without any additional circuitry, and provides a functional determination of the noise immunity characteristics of the gate.

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* Industry practice is to average these two. This, of course, always gives a more optimistic value for t_{pd}.

The noise immunity has been calculated as a function of device parameters. This calculation has been experimentally verified for both "fast" as well as "slow" gates. It is shown that many of the parameters that govern the propagation delay through the gate also control its noise immunity. On the other hand, there is some freedom in designing a gate with optimum noise immunity for a fixed propagation delay. This may be attained by designing the circuit with a short rise time, and relatively long turn on delay and storage time.

4. OSCILLATION HAZARDS IN ASYNCHRONOUS SEQUENTIAL CIRCUITS

4.1 The Problem

It has been observed that some sequential circuits constructed from very fast nor gates ($\simeq 4$ nanosecond delay) will oscillate when inputs are changed simultaneously. In synchronous circuits this difficulty does not arise since a single clock transition is used to initiate computation of the next state. However, at the interface between computer and external device (i.e. a radar) such synchronization is not possible. It is of considerable interest to determine if such problems can be eliminated by proper design or if fundamental difficulties are involved.

4.2 The Approach

Many special circuits have been investigated and in all cases no design was found which eliminated the possibility of oscillation when the circuit required that a terminal state depends on the sequence of changes of a pair of input variables. It was therefore decided to see if it could be proved that such a design was impossible.

4.3 Program Effort

Two theorems have been proved which show, under assumptions usually valid in the design of sequential circuits, that such a design is in fact impossible without the use of frequency band limiting devices in the feedback loops. The first theorem shows that no state assignment can be found for which the combinational logic is hazard free when simultaneous input changes are allowed. The second theorem indicates that even with hazard free combinational logic, correct sequential action places strigent limitations on the narrowness of pulses which can be passed through the feedback connections.

A detailed discussion of the background of the problem and the statement of the theorems is given in Appendix H, and their proofs in Appendix I.

4.4 Conclusions

It has been concluded that asynchronous circuits cannot be reliably constructed from very fast logical devices if simultaneous input changes are possible, unless some method is available for eliminating short pulses in the feedback loops. The inertial delay of Unger is one element that can be used for this purpose. However, it has been shown that the realization of this device as described by Unger is itself subject to the hazards described here.

Appendix A

Statistical Consideration of Nickel as an Impurity in n-type Silicon

In order to find the free carrier densities which would occur if a sample of n-type silicon were doped with nickel, one needs to know only the original donor concentration M_D and the energy levels of nickel in silicon. From this information the Fermi level, and thus the carrier densities, of the nickel-doped sample can be obtained statistically.

Let M_{Ni} be the total concentration of active nickel, $M_{Ni^{=}}$ be the concentration of nickel in the double acceptor state, and $M_{Ni^{-}}$ be the concentration of nickel in the single acceptor state. It is assumed that the density of nickel states is low, so that interactions between them can be ignored. In addition, considerations of degeneracy can be neglected, since these are only important in determining the limiting resistivity of the doped material.

Using the arguments of Shockley and Last*, it may be shown that

$$M_{Ni^{=}} = \frac{M_{Ni}}{1 + \exp\left[(E_{Ni^{=}} - E_F)/kT\right] + \exp\left[(E_{Ni^{=}} + E_{Ni^{-}} - 2E_F)/kT\right]}$$

$$M_{Ni^{-}} = \frac{M_{Ni}}{1 + \exp\left[(E_{Ni^{-}} - E_F)/kT\right] + \exp\left[(E_F - E_{Ni^{=}})/kT\right]}$$

Writing the charge neutrality equation, assuming that all of the shallow donor states may not necessarily be ionized, we obtain

$$p - n + M_D - N_D - 2M_{Ni^{=}} - M_{Ni^{-}} = 0$$

where N_D is the density of electrons at the donor level.

*Shockley, W. and Last, J. T., Phys. Rev., v. 107, no. 2, p. 392-396, July 15, 1957.

Inserting the known statistical relationships, gives

$$n_i \exp\left[(E_i - E_F)/kT\right] - n_i \exp\left[(E_F - E_i)/kT\right] + M_D \left[1 - \frac{1}{1 + \exp\left[(E_D - E_F)/kT\right]}\right]$$

$$- \frac{2\, M_{Ni}}{1 + \exp\left[(E_{Ni^{=}} - E_F)/kT\right] + \exp\left[(E_{Ni^{=}} + E_{Ni^{-}} - 2\, E_F)/kT\right]}$$

$$- \frac{M_{Ni}}{1 + \exp\left[(E_{Ni^{-}} - E_F)/kT\right] + \exp\left[(E_F - E_{Ni^{=}})/kT\right]}$$

$$= 0$$

where E_i = 0.57 ev above valence band

E_{Ni-} = 0.23 ev above valence band

$E_{Ni=}$ = 0.35 ev below conduction band, and

E_D = 0.04 below conduction band for phosphorous-doped silicon at 300° K.

Graphical solutions to this equation, showing the Fermi level E_F as a function of M_D for various M_{Ni} (at 300° K) are shown in Figure A-1. This figure relates the original donor concentration prior to nickel doping, the concentration of "active" nickel with which the samples are doped, and the resulting free carrier concentrations. The Fermi level for the sample is also displayed in this figure.

In conclusion it must be emphasized that M_{Ni} is the concentration of active nickel, and not the total nickel content given by the solid solubility limit.

Appendix B

The Measurement of Minority Carrier Lifetime

The diode recovery method is commonly used for the measurement of short recovery times (in the nanosecond range) since it is considerably easier to implement than the more common "photoconductive decay" method. The method, as described by Kingston*, consists of applying a step of current, I_F, to a p-n junction and suddenly reversing the current to a new value, I_R. This sudden reversal is maintained until all minority carriers are swept out of the device, resulting in a "flat-top region", denoted by t_s in Figure B-1. Once the carriers are swept out, the current decays to a final value given by the diode leakage current. Knowledge of the length of the flat-top, and of the decay time, can be used to compute device lifetime. The results of Kingston can only be applied to alloy junction devices, and are not applicable to high speed diffused structures with any degree of accuracy.

This method has recently been extended by Kuno** to high speed structures, using the charge control method of analysis. Following the analysis of Kuno, we define forward and reverse recombination rate constants τ_F and τ_R respectively pertaining to the dynamics of decay of stored charge in a diode during the forward and reverse switching time. If the diode is swtiched instantaneously from a forward current of I_F to a reverse current of I_R, Kuno has shown that the "flat-top" region is given by

$$t_s = \tau_F \left[\ln (1 + I_F/I_R) - \ln (1 + \tau_R/\tau_F) \right] .$$

*Kingston, R. H. "Switching Time in Junction Diodes and Transistors", Proc. IRE, v. 42, No. 3, p. 829-834, 1954.

**Kuno, H. J. "Analysis and Characterization of P-N Junction Diode Switching", IEEE Trans. on Electron Devices, ED-11, No. 1, p. 8-14, 1964.

Thus, if we plot t_s as a function of $\ln(1 + I_F/I_R)$, a straight line is obtained with a slope of τ_F. It has also been shown that τ_F is the minority carrier lifetime for the n region of the diode, if $\sigma_p \gg \sigma_n$ (as is the case in our structures).

Figure B-2 shows the test jig used to make these measurements. In each case, the values of forward and reverse current were read directly off the oscilloscope. The method provided a simple check on the accuracy of the measurements, since this curve should be a straight line over a large range of I_F/I_R values. This was indeed found to be the case for our devices.

Figure B-3 to B-9 show representative measurements made on our structure, as well as comparative measurements on a 1N914 diode. In each case, the slope τ_F is marked on the curve. A sampling oscilloscope was used for taking these measurements, with atleast three data points taken in each case as a check on the measurement method.

Appendix C

The Diffusion of Nickel from a Glassy Source

The following is a description of the work conducted to date on investigating the feasibility of diffusing nickel from a glassy source:

a) A study has been made of the chemistry of nickel compounds to ascertain which of these is most suited for this application. This has concentrated our efforts to the use of nickel oxide, NiO. This oxide takes the form of a greenish powder, which melts at 1990° C.

b) A literature search was made for the phase diagram of the $NiO-SiO_2$ system. Such a diagram was not found. Consequently, an attempt was made to see if NiO was soluble in SiO_2 at diffusion temperatures. A wafer of silicon was thermally oxidized at 1000° C (using a dry O_2-steam-dry O_2 cycle). Dry NiO was dusted on the oxidized surface and the wafer heated for one hour at 1150° C. On removal, the wafer was subjected to microscopic examination. While the NiO had sintered to the SiO_2 layer, no signs of a solution were found.

c) The next experiment was conducted in an attempt to dissolve NiO into a glass that is formed on the wafer using SiO_2 and an electronically inactive oxide. The $PbO-SiO_2$ system was selected, since lead is known to be inactive in silicon.

Figure C - 1 shows the phase diagram for the $PbO-SiO_2$ system. It is seen that a liquid phase exists at temperatures above 720° C. A wafer of

silicon was oxidized as described before, and inserted in a closed box with a PbO source. The wafer was heated to 900° C for one hour, and examined. While a $PbO-SiO_2$ glass was certainly formed, the surface condition was very poor with signs of excessive pitting and crazing. It would appear that a suitable technique could most probably be developed for forming a uniform crack-free glass on the wafer. However, time did not permit refining this step, so the experiment was extended to see if nickel would dissolve in this glass. A layer of NiO was dusted on the wafer and the wafer subjected to a one hour diffusion cycle at 1000° C. After diffusion, the wafer was optically inspected for signs of solution of NiO in the glass. Results were inconclusive.

i) A study of the metal-oxide phase diagram literature revealed that NiO can be used with vanadium pentoxide (V_2O_5) to produce a glass at temperatures in excess of 650° C. (The phase diagram for this system is shown in Fig. C-2) Since vanadium is also inactive in silicon, the scheme was attempted as follows: First, V_2O_5 was dusted over a wafer of silicon and placed in a diffusion furnace for an hour at 1000° C. On removal from the furnace, the wafer was cleaned in hot KOH. This removed the V_2O_5 readily, leaving an undamaged silicon surface.

In order to test the feasibility of using this oxide as a carrier of nickel, a freshly etched sample of silicon was coated with a slurry of NiO and V_2O_5 (one part by weight of NiO to ten parts by weight of V_2O_5 in an ethylene glycol base) and diffused for one hour at 1000° C. On removal from the furnace, the glass was removed, with some difficulty, by a hot KOH treatment. The surface of the silicon was inspected visually, and found

to be undamaged. The resistivity of the wafer was found to be increased by the diffusion, and it has been concluded that this is due to the diffusion of Ni from the V_2O_5-NiO source. Time did not permit the detailed investigation of nickel diffusion from this source over a range of typical diffusion temperatures. However, it is concluded that

a) Nickel can be diffused from a NiO-V_2O_5 glass with no damage to the silicon surface.

b) The resulting nickel-vanadium compounds can be removed by the use of hot KOH.

c) The nickel that is diffused in this manner show signs of electrical activity.

Considerable further investigation is needed in order to actually devise a practical process for the diffusion of nickel in silicon. Specifically, it is necessary to search for alternate methods for removing the nickel-vanadium compounds from the surface of the wafer. In addition, it is necessary to conduct an extensive series of compensation experiments to determine the amount of nickel that enters the lattice, and also to determine the optimum NiO-V_2O_5 ratio to be used. Finally, improved methods should be sought for transporting the NiO-V_2O_5 mixture to the silicon wafer.

APPENDIX D

Pulse Noise in Digital Circuits

Large scale digital subsystems are usually composed of a number of iterated, interconnected, logic function blocks. Thus, the problem of pulse transmission in these circuits is one of transmitting high frequency signals in a large, wideband circuit. For any individual logic gate in this circuit, spurious signals presenting themselves at its input are due to one or more of the following reasons:

a) Noise generated in the transmission line between gates,

b) Noise picked up in the transmission line between gates,

c) Noise transmitted from the output of the preceding gate, and

d) Logic Noise

In addition, the transmission line between different gates is of variable length, being under 1/2" long when interconnecting two gates that are side by side, and more than a foot in length when the transmission line connects gates on separate circuit boards.

D.1 Noise Generated in Transmission Lines

Noise generated in transmission lines is a result of reflections from improper terminations at either end of the line. If a short line is used, such as is commonly the case between gates on the same circuit board, this noise has the nature of extremely high frequency ringing, at a frequency determined by the time delay of the line. Thus, a transmission line 1/2" long gives rise to noise components at frequencies of 9 GHz and higher if improperly terminated. Since the fundamental frequency associated with this noise is well beyond the band-width of the

circuit, the problem may safely be ignored. This is especially true in high speed digital circuits which operate at reasonably low impedance levels, and consequently are highly damped.

The situation is quite different with transmission lines whose lengths are comparable to the rise time of the circuit. Here, reflections that occur are sufficiently long in duration that their presence cannot be ignored. Since digital circuits present nonlinear impedances, it is only possible at best to provide a crudely matched termination at both ends of the transmission line. This noise takes the form of distortion of an otherwise rectangular pulse, and also results in spurious pulses, having a width equal to twice the delay time associated with the transmission line.

Pulse distortion in transmission lines may be computed readily* by considering separately the incident and reflected waves on the line.

Figure D-1 shows the equivalent circuit of such a line. At either end of the line,

the Voltage Reflection Coefficient, ρ_v, is given by

$$\rho_v = \frac{Z - Z_o}{Z + Z_o};$$

the Current Reflection Coefficient, ρ_i, is given by

$$\rho_i = \frac{Z_o - Z}{Z_o + Z};$$

the Voltage Transmission Coefficient, t_v, is given by

$$t_v = \frac{2Z}{Z_o + Z};$$

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* Millman, J. and Taub, H. "Pulse and Digital Circuits", McGraw Hill Book Co., New York (1956).

and the Current Transmission Coefficient, t_1, is given by

$$t_i = \frac{2 Z_o}{Z_o + Z}$$

The substitution, $Z = Z_g$ must be made in order for these expressions to apply to the generator end. In like manner, the substitution $Z = Z_1$ will make the expressions applicable to the load end.

Figure D-2 shows a situation that occurs typically in a digital circuit. The line (having a characteristic impedance R_o) is initially charged with the transistor open. At time $t = 0$, the transistor is turned on, thus shorting the previously charged line. Figure D-3 shows the waveforms across the load end (R_1) for the case where $R_1 = R_o$, as well as for the cases where $R_1 = 10\ R_o$ and $R_1 = 0.1\ R_o$. It is assumed that the line is charged to the steady state in each case prior to turning on the transistor, and that the transistor is a perfect switch.

Figure D-3a shows the waveform at the load when the load and transmission line are matched. For this case, the signal across the load terminates after delay of Δ seconds, where Δ is the time delay of the line. Thus, a nett delay of Δ is incorporated into the circuit for this condition.

Figure D-3b shows the load waveform when $R_1 = 10\ R_o$. For this case, the voltage across the load goes through many reversals until it is finally damped. Here, the charge associated with the first of these positive going reversals is given by

$$Q = 0.67\ V_{cc}\ \Delta\ /\ R_1 \text{ coulombs}$$

where V_{cc} is the supply voltage for the transistor. In order to avoid malfunction, it is necessary that the load circuit have a pulse noise immunity in excess of this value.

Figure D-3c shows the case where $R_1 = 0.1\ R_o$. For this termination, we note the absence of pulses that can cause malfunction. However, excessive pulse delay is the result, since the circuit recognizes the cessation of the signal many delay times after its actual termination.

The situation is somewhat more complicated by the fact that the load impedance is, in reality, not constant, but is given by the input impedance of a T^2L gate. Thus, for the first two cases, the load transistor would start to conduct after a time delay of Δ. At this point, the load impedance would abruptly fall, and closely approximate that of a charged line, shorted at both ends. Thus, it is probable that the actual waveform would be rapidly damped after one or two oscillations.

D.2 Noise Pickup in Transmission Lines

One component of this noise is associated with crosstalk between lines. Figure D-4 shows an elementary system of two loosely coupled transmission lines, terminated in their characteristic impedance Z_o.

If C_M and C_S are the mutual and shunt coupling capacitances per unit length, and M and L the mutual and series inductances per unit length, it can be shown* that the charge delivered to Z_3 via the backward wave is approximately given by

$$Q = \frac{M}{L} \cdot \frac{K + 1}{2K} \cdot \Delta \cdot dI$$

where Δ is the delay of the line,

dI is the magnitude of the current excursion at the generator end, and

$$K = \frac{M}{L} \cdot \frac{C_S}{C_M}$$

Following directional coupler theory, it may be shown that the charge delivered to Z_4 is considerably smaller in magnitude. In a practical circuit with varying loads, good design practice indicates that both Z_3 and Z_4 should be capable of tolerating the malfunction charge that is normally delivered to Z_3.

While the expression for malfunction charge indicates that the current level can be adjusted to reduce this type of noise, it is usually found in practice that the high speed pulse circuit designer is limited to a prescribed range of current values in order to achieve the desired system performance. The reason for this is clear in the fundamental equations for the charging time of the various elements of a transistor.

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* Jarvis, D. B. "The Effect of Interconnections on High Speed Logic Circuits," IEEE Trans. on Elec. Comp., v. EC-12, p. 476-487, 1963.

Thus, for any parasitic capacitance that must be charged,

$$\int_{o}^{t_1} I(t)\, dt = \int_{V_1}^{V_2} C(V)\, dV$$

where t_1 is the charging time and V_1 and V_2 are the initial and final values to which the capacitor must be charged. In addition, the time taken to charge the various internal regions of the transistor is given directly by

$$t_2 = \sum_j Q_j/I_j\ (t)$$

where t_2 is the charging time, and Q_j the individual charge elements of the transistor (e.g., base charge, collector storage charge, and so on).

In a typical situation, the mutual inductance is that associated with point to point wiring over a ground plane. Thus, for the configuration of Figure D-5, the mutual coupling inductance is approximately given* (for long wires) by

$$M = 0.2 \ln \sqrt{(1 + 4h^2/D^2)}\ \mu h/\text{meter}.$$

Therefore, as the wiring is brought closer to the ground plane, the mutual inductive coupling is reduced.

For the configuration of Figure D-5, it may also be shown that the capacitance to ground is inversely proportional to $\ln (2h/a) \sqrt{(1 + 4h^2/D^2)}$. Thus, there is, in essence, a trade off between inductive pickup and charging capacitance.

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* Grover, W. C., "Inductance Calculations", D. Van Nostrand Co., Princeton, New Jersey (1946).

It should be noted that the magnitude of the current pickup is a function of the rise time of the transmitted signal. On the other hand, the nett charge pickup is only given by the current excursion alone, and is thus relatively independent of the rise time.

Figure D-6 shows two loops, A B C D and E F G H, both of which are coupled by the mutual impedance associated with the areas of the loops as well as by the self-inductance of the ground line GH, which is common to both. In such a system, it is possible to eliminate the effects of self-impedance by providing separate return paths for both loops, as shown in Figure D-7. Such a system still has mutual inductive pickup, but the self-inductive pickup is eliminated by having separate return paths which are electrically connected at a single point. Figure D-8 shows a crossection through a circuit of this type. For this circuit, assuming parallel wires,

$$M = 0.2 \ln (a_1 b_2/a_2 b_1) \ \mu h/\text{meter}.$$

The use of twisted pairs leads to an almost complete elimination of mutual coupling between two circuit boards. In fact, the mutual coupling of such a system is strictly a function of second order effects, such as non-uniformity of twisting.

More complex schemes may also be used to reduce the mutual coupling between circuits. Thus, the use of coaxial pairs leads to values of mutual inductance that are one decade below the figure normally obtained with twisted pairs.

Stripline techniques provide an increasingly popular alternative to the use of twisted pairs in modern microsystems. This is largely due to the fact that they can be fabricated by photolithographic processes, and are thus compatible with microcircuits in terms of their compactness and ease of fabrication. The most popular technique is microstrip*, where then conductors are printed on one side of a flexible low-loss dielectric such as teflon-loaded fiberglass, about 10 to 20 mils thick. The reverse side of this strip is coated with a conductive layer and serves as a ground plane. Propagation of signals along such a conductor system take place (ideally) in the TEM mode, with essentially all of the power flow being confined to a region of the ground plane equal to approximately three times the strip width. The crosstalk between two parallel conductors in a microstrip configuration is a function of the fringing radiation field from each conductor. This radiation field falls as the square of the spacing between conductors, and can be further reduced by decreasing the thickness of the dielectric layer.

The configuration of two parallel microstrip conductors on a common ground plane is essentially that of a microwave directional coupler, and has been analysed by Jones and Bolljahn**, using coupled mode theory.

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* Grieg, D. D. and Engelmann, H. F., "Microstrip - A New Transmission Technique for the Kilomegacycle Range", Proc. IRE, v. 40, no. 12, p. 1644-1650 (1952).

** Jones, E. M. T. and Bolljahn, J. T., "Coupled-strip Transmission line Filters and Directional Couplers" IRE Trans. on Microwave Theory and Techniques, vol. MTT-4, p. 75-81, 1956.

The work has been extended by Connolly* to the analysis of the response of coupled microstrip lines to a step input pulse. In addition to determining the amplitude of the various signals induced in a coupled line (terminated at both ends in its characteristic impedance), he has shown that the crosstalk pulse appearing at the sending end is 2Δ to 4Δ in width. For his balanced matched-load system, the signal induced at the receiving end is essentially due to end effects and anisotropic behavior of the dielectric constant. In a typical (mismatched) circuit, this signal could be as large as that induced at the sending end.

The mutual impedance of coupled microstrip lines can be made comparable to that of twisted pairs. However, signal pickup due to the common ground return is still present in these structures. The coupling associated with this common ground can be eliminated by resorting to microstrip techniques with separate ground returns. Unfortunately, this leads to a considerable increase in the physical size of the interconnections.

D.3 Noise Transmitted from the Output of the Preceeding Gate

This noise can be generated within a logic gate because of the imperfect nature of circuit elements, both active and passive. The problem with passive elements is due to the nature of the parasitics associated with them. Thus, the offset diodes used to obtain d-c noise

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* Connolly, J. B. "Cross coupling in High Speed Digital Systems", IEEE Trans. on Electronic Computers, v. EC-15, no. 3, p. 323-327, 1966.

immunity in DTL circuits results in the transfer of current pulses because of their parasitic shunt capacitance.

The noise generated in active elements is more serious in nature, and results from the limitations of the devices themselves. Some of these sources are considered here.

Impulse Widening. Impulse widening can sometimes result in converting a very narrow noise pulse into a wider pulse that may be mistaken for a signal. Thus, if an impulse of current, representing a charge q, arrives at the base of a transistor, its collector current is given by

$$I_c(t) = \omega_T q \exp(-\omega_T t / \alpha_{eo})$$

where ω_T is the transistor gain-bandwidth product in radians and α_{eo} is the common emitter current gain. The charge associated with this current waveform is given by $q\alpha_{eo}$. Thus, the effect of impulse widening is to multiply the charge by the transistor current gain, and also to redistribute its frequency components towards the lower end of the spectrum, within the bandwidth of succeeding devices.

Noise Generated in Circuits With Switched Loads. This is one form of noise that occurs when a transistor in the ON condition is suddenly required to feed additional loads. This is a potential problem with both DTL and T^2L circuits where the nature of the load is nonlinear and may suddenly change at random times*.

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* For example, in DTL and T^2L designs when all but one gate input are switched off.

Consider a transistor with a base current of I_B. Let the collector current initially be I_{C1}. Then Figure D-9 shows the charge distribution in the base, with

$$Q_1 = \tau_T \, I_{C1}/\alpha_{eo}$$

$$Q_2 = \tau_s \left[I_B - I_{C1}/\alpha_{eo} \right]$$

where α_{eo} is the common emitter current gain, τ_T is the reciprocal gain bandwidth product, and τ_s is the storage time constant. Thus, the total charge in the base is $Q_1 + Q_2$. At this point, let the demanded collector current be suddenly increased by I_{C2}, and let us assume that the transistor remains saturated. Since this current must be instantaneously supplied by the base charge, it is clear that the charge Q_2 must supply it all, or else the transistor will momentarily drop out of saturation, until the base current re-establishes the base charge to its steady state value.

In order for the transistor to remain in saturation

$$I_{C2} \leq Q_2 / \tau_T$$

Thus, the total collector current that can be handled by this stage without dropping out of saturation is given by

$$I_C = I_{C1} + I_{C2} \leq I_B \, \tau_s / \tau_T + I_{C1} \quad 1 - \left[\tau_s / \alpha_{eo} \tau_T \right]$$

In general,

$$\tau_s / \tau_T < \alpha_{eo}$$

Thus, for the worst case situation

$$I_C \leq I_B \, \tau_s / \tau_T$$

Beaufoy and Sparkes* have defined an "on-demand" current gain for a transistor as

$$\alpha_{es} = \tau_s / \tau_T$$

In typical transistors, $\alpha_{es} = 0.5\alpha_{eo}$. If α_{es} is used as the basis of design instead of α_{eo}, this noise pulse generation can be avoided. Thus, the problem of malfunction due to this cause can be directly avoided by using the on-demand current gain of a transistor instead of its common emitter current gain as a basis of circuit design.

Noise Due to Mistiming. This noise is often present in high speed systems where a signal, after being processed in two channels of slightly different length (i.e., slightly different delay time), arrives at two inputs to a gate with a slight time displacement. In asynchronous systems, care must be taken to minimize the resulting noise signal at all times, with careful attention being paid to equalizing all such delay paths.

The problem is considerably less important in clocked synchronous systems, where clocking is done at regular intervals. In such systems, as long as the delay through any combinational logic path is less than one half of the clock interval, the problem is corrected at each clocking point. In asynchronous circuits, mistiming results in a pulse of amplitude equal to the logical signal, and of width given by the difference in timing delays.

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* Beaufoy and J. Sparkes - Transistor Switching Performance Analyzed in Terms of Base Charge (British) Telecommunications Research LTD., Taplow, England Technical Report, May, 1958.

Consider a signal that must pass through M gates on one channel and N gates on the other, prior to recombination. If $\langle t_{pd} \rangle$ is the average propagation delay of each gate, with a $\pm$ 20% tolerance, and M is greater than N, the maximum pulse width due to mistiming is given by

$$\Delta = (1.2\ M - 0.8\ N)\ \langle t_{pd} \rangle$$

and the charge associated with a current pulse of amplitude I is given by

$$Q = I\ (1.2\ M - 0.8\ N) \langle t_{pd} \rangle$$

Thus, the pulse noise immunity of the gate will determine the number of stage delays that can be tolerated before re-timing is necessitated.

Alternately, as is usually the case, artifical delays are used in order to balance the delay time of the channels. If this is done, and the channels equalized to a delay of M stages, the worst case situation results in a malfunction pulse with a charge given by

$$Q = 0.4\ M\ I \langle t_{pd} \rangle \text{ coulombs,}$$

where I is the peak current associated with the pulse.

D.4 Logic Noise

While this type of noise is also transmitted from the output of a circuit, its presence only occurs at the output of certain types of high speed, asynchronous sequential circuits. These circuits are characterized by the presence of feedback loops and their problems are considered in some detail in the Section 4.

APPENDIX E

Terminal Characteristics of the T^2L Gate

The basic configuration of the T^2L gate is shown in Figure E-1. The operation of the gate is as follows:

When Q_o is driven into the ON condition, the voltage at the point 1 assumes a value equal to its saturation voltage. Assuming a low resistivity collector structure, with a buried layer, this voltage is typically 0.2 volts. For this condition, the base current of Q_1 is driven through its emitter to ground via Q_o, and Q_1 is in the ON condition. The voltage drop across Q_1 can be neglected to a first order approximation, since the current drawn by this stage is much less than that drawn by the inverter transistors (i.e., base drive current as opposed to collector current). At this point, the base of Q_2 is slightly over 0.2 volts to ground, and this transistor is in the OFF condition.

When Q_o is driven into the OFF condition, the base current of Q_1 is diverted through its collector to the base of Q_2, driving this stage ON. For this condition, the final value of the base voltage of Q_2 assumes a value of approximately 0.85 volts. Once again, Q_1 is in the ON condition, and the voltage drop across this stage may be ignored. Thus, the collector voltage of Q_o assumes a value of approximately 0.85 volts at this point. From this point onwards, Q_o goes further into the OFF condition, until it reaches the supply voltage V_B with no additional effect on the inverter transistor.

The state of the transistors as well as the relative voltages are summarized in the following Table.

State of			V_1	V_2	V_3
Q_o	Q_1	Q_2			
ON	ON	OFF	0.2 v	0.2 v	V_B
OFF	ON	ON	V_B	0.85 v	0.2 v

A few significant features of this circuit may be noted.

a) The multi-emitter transistor Q_1 is always ON.

b) The d.c. logic swing at the base of Q_2 is 0.2 volts to 0.85 volts at room temperature.

The values of V_1 and V_2 vary with temperature, as follows: V_1 is directly proportional to the resistivity of the collector body material. Assuming a collector resistivity of 0.1 to 0.25 Ω cm (entirely adequate for a device designed to operate at supply the voltages below 6 volts), the collector resistance at 125° C (and hence V_1), will be about 125% of its value at 25° C. Thus, V_1 increases to about 0.25 volts at 125° C. V_2 is the voltage drop associated with a forward biased diode, and falls at the rate of 1.8 m v/° C. Thus, the lower bound of V_2, obtained at 125° C, is approximately 0.67 volts. Consequently, the logic swing at the base of Q_2 is 0.25 volts to 0.67 volts at 125° C. Since the difference between these levels represents the discrimination of the inverter, (to d.c. signal levels changes), we note that the worst case d.c. noise margin occurs at elevated temperatures.

The input characteristic of the gate may now be assesed. Figure E-2 shows the actual gate used, with the input voltage V_1 as the variable. Initially, Q_o is in the ON condition, and V_1 is approximately 0.2 volts. Thus, $I_1 = -(V_A - V_{EB1} - 0.2)/R_1$ where V_{EB1} is the forward drop across the emitter-base diode Q_1. For the actual values quoted in Figure E-2, $I_1 \cong -4.2$ m a.

As V_1 is increased, the V-I characteristic moves along a straight line with a slope of R_1 until the onset of conduction of Q_2 (at about 0.6 volts). At this point, Q_2 enters its active region, and the input characteristic has a slope given by the sum of the collector body resistance of Q_1 and the input impedance of Q_2. Shortly thereafter, transistor Q_2 becomes saturated.

In saturation, the input impedance of Q_2 is given by

$$R_{in} = r'_{b2} + (kT/qI_{E2})$$

where r'_{b2} is the base spreading resistance of the inverter transistor, and I_{E2} is its emitter current. The slope of the input characteristic during this region is thus given by the sum of the collector saturation resistance of the coupling transistor, the base spreading resistance of the inverter, and the forward impedance of the emitter-base diode of the inverter transistor. Since I_{E2} is large (about 15-20 ma for this circuit), this last term is usually negligible.

This slope is maintained until the current supplied by V_A is all diverted to the base of Q_2, at which point the input impedance rapidly increases to that of a reverse biased emitter-base diode. At this point, the input current of

the gate is given by

$$I_1 = I_{B1}\,\alpha_R/(1 - \alpha_R),$$

where I_{B1} is the base current of the coupling transistor, and α_R is its inverse current gain. In practice, the coupling transistor must be designed to keep this inverse current gain extremely small, since it limits the fan-in and fan-out capabilities of the gate.

Figure E-3 shows the input characteristic obtained by the approximate analysis. A more detailed analysis can be made using the large signal model of Ebers and Moll. However, this analysis serves no useful purpose in our study.

In Figure E-3, the various points are noted as follows:

P_1 - Stage Q_o is saturated, and Q_2 is OFF.

P_2 - Q_o almost completely OFF, Q_2 entering its active region.

P_4 - Q_o almost completely OFF, Q_2 hard in saturation.

P_5 - Q_o completely OFF.

The location of the point P_3, when Q_2 is at the edge of saturation, is somewhat more difficult to determine, and varies with the fan-out of the stage. Assuming a common emitter current gain of 50 for Q_2, the base current required to drive this stage into saturation is given by $(V_B - 0.2)/R_2\alpha_{ei}$. For the component values given, I_{CS2} = 11 ma. when the stage is unloaded. If Q_2 is loaded with a fan-out of 4 (as is typical for the T^2L gate), then $I_{CS2} = (11 + 4 \times 4.2) = 27.8$ ma. Thus, a base current of approximately 0.56 ma. is required to bring Q_2 to the edge of saturation, i.e., to arrive at P_3.

Figure E-4 shows a measured input characteristic obtained for the T^2L gate designed on this program. From this characteristic the following

points may be noted.

a. $r'_{b1} + r_{cs2} = 40$ ohms.

b. Q_2 enters its active region at an input voltage of 0.6 volts.

c. Q_2 is hard in saturation at an input voltage of 0.8 volts.

d. The common emitter inverse gain of the coupling transistor is seen to be 0.12. While this is quite high, it must be remembered that the devices used in these experiments were not specifically made for this application.

The transfer characteristic of this gate may be readily sketched with the aid of Figure E-3. Here, using the same terminology for the various breakpoints, one obtains (see Figure E-5)

P_1 : $V_1 = 0.2$ volts, $V_3 = 1.5$ volts

P_2 : $V_1 = 0.6$ volts, $V_3 = 1.5$ volts

P_4 : $V_1 = 0.85$ volts, $V_3 = 0.2$ volts

P_5 : $V_1 = 1.5$ volts, $V_3 = 0.2$ volts

As before, the location of P_3 is a function of stage gain and loading. Since, however, only 0.56 ma. has to be fed to the base of Q_2, the voltage V_1 is normally somewhere between 0.6 and 0.7 when this point occurs. In view of the fact that the quiescent points of this circuit are at P_1 and P_5, the d.c. margin to noise for this gate is 0.4 volts positive (P_1 - P_2), and 0.7 volts negative (P_5 - P_4). Thus, if the gate is OFF, an input level shift of 0.4 volts (in the positive direction) can be tolerated. On the other hand, when the gate is ON, an input level shift of 0.7 volts (in the negative direction) can be allowed. The d.c. voltage noise margin of the gate is thus 0.4 volts, since this represents the more pessimistic value.

The effect of elevated temperature is to shift points P_2, P_3 and P_4 and P_5 laterally, to the left. Thus, the d.c. noise immunity to positive level changes is somewhat lessened, while the noise immunity to negative going level shifts is relatively unchanged. Since the threshold voltage of the emitter-base diode of Q_2 is reduced by about 0.18 volts at 125° C, the effective d.c. noise margin is also lessened by this value. Thus, the d.c. noise margin is reduced to 0.22 volts at 125° C.

It is worth noting that a more optimistic value of noise margin can be quoted for this gate, by using some other point on the transfer characteristic as a reference point. (For example, noise margin may be measured down to, say, 50% of the transition) This choice will not, however, alter the situation drastically.

Figure E-6 shows the measured transfer characteristic for the T^2L gate. For this measurement the multiple-emitter coupling transistor was replaced by a planar epitaxial unit having a single emitter. It is worth noting that the characteristic in the transition region between P_2 and P_4 is somewhat curved. This is due to the fact that the input characteristic of the inverter diode is exponential, and not a threshold as assumed in the analysis.

APPENDIX F

Switching Characteristics of a T^2L Gate

The switching characteristics of the T^2L gate may now be determined. For simplicity, the circuit will be analysed for a fan in / fan out of unity, since our prime interest is in the development of a method for the characterization of this gate to noise. The manner in which the noise immunity of the gate is affected by other terminal loadings can be readily computed, once the gate has been characterized for any one set of conditions.

The switching properties may be determined by studying the nature of the various parts of the switching cycle, as they occur. At the outset it should be remembered that Q_1 is ON at all times, with its base current changing only slightly during different parts of the switching cycle. Thus, the base charge for this transistor can be conveniently considered as constant, even though it does undergo redistribution (which occurs at a near-instantaneous rate) during the switching cycle. Consequently, only the parasitic elements of Q_1 need be considered in the analysis.

The switching properties are computed for the application of an ideal input signal V_1 to the gate, as shown in Figure F-1 together with the idealized output waveform V_3.

Turn-on Delay

Figure F-2 shows the circuit for the basic T^2L gate, with its transfer characteristic. For this gate, the turn-on delay occurs as the operating point moves from P_1 to P_2. Over this transition, the voltages at the base and collector of Q_1 may be listed as follows for

the circuit values shown:

Operating Point	Voltages at	
	2'	2
P_1	1.05 v	0.2 v
P_2	1.2 v	0.6 v

The various parasitic capacitances that must be charged during this phase of the turn on transient are as follows:

a) C_{TC1}, the collector transition capacitance of Q_1, is subjected to little voltage change, and hence requires a small amount of charge which may be neglected.

b) C_{CS1}, the collector to substrate capacitance of Q_1, is subjected to a voltage change to 0.4 volts.

c) C_{TE2}, the emitter transition capacitance of Q_2, is subjected to a voltage change of 0.4 volts.

Thus, the total charge that must be delivered during the turn on delay phase, P_1 to P_2, is given by 0.4 $(C_{CS1} + C_{TE2})$ picocoulombs, where the capacitance values are given in picofarads.

It should be stressed that the capacitance values must be adjusted for a fan-in in excess of unity. However, since this only serves to <u>increase</u> the capacitance, it will result in a more optimistic value for the resulting pulse noise immunity. As a consequence, a fan-in of unity will be used.

If I is the current used to charge these capacitances, then

$$\int_0^{t_1} I \, dt = 0.4 \ (C_{CS1} + C_{TE2})$$

If the base current is used in this expression, we obtain t_1, the time

taken to bring Q_2 from the OFF region to the edge of the active region. This time is the turn-on delay time of the transistor.

Rise Time

Once the inverter transistor is brought to the edge of the active region, any additional charge contributes to the rise time. It can be shown* that the collector current during this phase is given by

$$I_c(t) = \alpha_E I_B \left[1 - \exp \left\{ - t/\alpha_E \ (\tau_T + R_2 C_2) \right\} \right]$$

where τ_T is the reciprocal of the gain-bandwidth product of the inverter, and C_2 is the total capacitance at its collector. This term includes the collector transition capacitance and the collector to substrate capacitance of the inverter stage, as well as the capacitive loading effects due to wiring and fan-out.

Since the stage is saturated at currents well below $\alpha_E I_B$, the approximate form of this equation is useful, as follows:

$$I_C \cong I_B \ t/(\tau_T + R_2 C_2)$$

Writing I_{CS2} as the saturation current of Q_2, the time taken to attain 50% of this value is given by

$$t_r(0.5) = 0.5 \ I_{CS2} \ (\tau_T + R_2 C_2) / I_B$$

Storage Time

Let τ_s be the charge storage time constant for Q_2. Once the inverter transistor has reached the edge of saturation, the charge build up in this device is given by

$$Q = Q_{max} (1 - e^{-t/\tau_s})$$

where $Q_{max} = \tau_s \left[I_{CS2}/\alpha_{E2} - I_{B2} \right]$

* Phillips, A. B. "Transistor Engineering, Chapter 16, McGraw Hill Book Co., New York, 1962.

Thus, the transistor is fully saturated (to its 95% value) in a time equal to $3\tau_s$. If the input signal is maintained for a time that is greater than $3\tau_s$, and removed, the storage time may be shown to be given by*

$$t_s = \tau_s \ln \frac{I_{B2} - I}{I_{SAT2}/\alpha_{eo} - I}$$

Here, I is the reverse current that flows during this phase, and is shown in Figure F-3. While this current flows, the emitter base voltage of Q_2 is 0.85 volts, while the saturation voltage of Q_o is 0.2 volts. Hence,

$$I = 0.65/(r'_{b2} + r_{cso} + r_{csl}) \text{ amps.}$$

where r'_{b2} is the base spreading resistance of Q_2, and r_{cso} and r_{csl} are the collector resistances of Q_o and Q_1 respectively.

Fall Time

The analysis of fall time is complicated by the fact that the emitter-base diode is shorted to ground through a small resistance R, where

$$R = r'_{b2} + r_{cso} + r_{csl}$$

For this case, it may be shown** that the fall time, to the 50% point, is given approximately by

$$t_f\ (0.5) \cong \frac{q\ I_B}{kT} \cdot \frac{R}{\exp\ (qV_{EB}/kT)} \cdot (\tau_T + R'_2\ C_2)$$

* Ibid, p. 54.

**Thiney, A. IEEE Trans. on Elec. Computers, v. EC-13, p. 616-620, 1964.

Here, R_2' is the parallel connection of the load resistance of Q_2 as well as the base resistances of the various multiple-emitter coupling transistors to which the gate is connected. Also, C_2 is the sum of the collector transition capacitance of Q_2, the collector-to-substrate capacitance of Q_2, and the capacitance loading effects due to wiring and fan out.

APPENDIX G

Calculation for the Pulse Noise Immunity of a T^2L Gate

Figure G-1 shows the block diagram of a T^2L gate, together with a malfunction indicator consisting of two identical cross-coupled gates. A high speed T^2L circuit arrangement, used in the experiments to simulate the block diagram, is shown in Figure G-2. For simplicity, the coupling transistors were removed in the test version. However, their effect can be readily included in the analysis, as shown. All the transistors used in this circuit were type 2N709. Since these devices are heavily gold doped (as are all devices used in high speed saturated logic gates), the charge stored in the collector may be neglected in the analysis.

A rectangular current pulse, of amplitude I and width τ, is applied to the input of the circuit of Figure G-2. It is required to determine the current amplitude at which transistor Q_4 is turned OFF, resulting in an indication of malfunction. Alternately, the problem may be stated in the following terms: Given a rectangular pulse of amplitude I, what is its minimum time duration in order that Q_4 be turned OFF? This problem may be solved by considering in sequence the various aspects of circuit operation as follows:

a) With Q_2 in the OFF condition, its emitter-base voltage is essentially the sum of the saturation voltage of Q_1 and the voltage drop across R. If the gate were fed from a preceeding gate, the voltage drop across R would be replaced by the saturation voltage of its inverter transistor.

During the turn on delay time interval t_d, the voltage at the base of Q_2 is raised until this transistor is on the edge of conduction. In this interval, the various capacitances between the base of Q_2 and ground must be charged. These include C_{TE2}— the emitter transition capacitance of Q_2, C_{CS1}— the collector-substrate capacitance of Q_1, and any stray wiring capacitances C that may be present at this point. Since the charging current during this phase is I_B, we obtain

$$t_d = \frac{dV_{BE2}\,(C_{TE2} + C_{CS1} + C)}{I_B} \qquad (1)$$

where dV_{BE2} is the emitter-base voltage excursion between the OFF condition and the edge of saturation. (At room temperature, these are typically 0.2 and 0.6 volts respectively.) Since the base resistance R_B is well in excess of the collector saturation resistance of Q_1 and the base spreading resistance of Q_2, a constant current source may be assumed.

b) The transistor Q_2 is brought from the edge of conduction to the edge of saturation. During this rise time, t_r, Q_2 is in its active region, and we may write

$$(\tau_T + R_{L2}\,C_{C2})\,\frac{dI_{C2}}{dt} + \frac{I_{C2}}{\alpha_{eo2}} = I$$

where τ_T is the reciprocal gain-bandwidth product of the inverter averaged over the rise time, R_{L2} and C_{C2} are the effective values of its load resistance and capacitance respectively. I_{C2} is the collector current, and I is the input current supplied to its base.

Solving,

$$I_{C2} = \alpha_{eo2}\,I\left[1 - \exp\left\{-t/\alpha_{eo2}\,(\tau_T + R_{L2}\,C_{C2})\right\}\right]$$

If the transistor saturates at $I_S \ll \alpha_{eo2} I$, we may write

$$t_r = \frac{I_S (\tau_T + R_{L2} C_{C2})}{I} \qquad (2)$$

During this rise time interval, Q_3 is OFF, and thus all of the current in the load resistor is supplied to Q_2.

c) Once Q_2 is saturated, it acts as an effective short circuit on Q_4, and aids in removing its stored charge. All of this stored charge must be removed before the collector voltage of Q_4 starts to rise from its ON value. During this interval, the effective loop voltage aiding the removal of stored charge is $V_{BE(SAT)4} - V_{CE(SAT)2}$, where $V_{BE(SAT)4}$ is the base voltage of Q_4 when it is saturated, and $V_{CE(SAT)2}$ is the collector voltage of Q_2 in its saturated condition. For typical high speed transistors having a buried layer under the collector, $V_{BE(SAT)4}$ is about 0.85 to 0.9 volts, while $V_{CE(SAT)2}$ is about 0.15 to 0.3 volts.

The only resistance in the loop path is r'_{b4} and r_{CS2}. In the event that the malfunction circuit is synthesized from a pair of complete logic gates, the saturation resistance of a multi-emitter coupling transistor must also be included in this loop.

Thus, loop current, I_L, (see Figure G-2) is given by

$$I_L = \frac{V_{BE(SAT)4} - V_{CE(SAT)2}}{r'_{b4} + r_{CS2}}$$

The stored charge in Q_4 is given by

$$Q_s = \tau_s \left[I_{B4} - \frac{I_{(SAT)4}}{\alpha_{eo4}} \right] \cong \tau_s I_{B4}$$

where τ_s is the charge storage time constant of Q_4, and I_{B4} and $I_{(SAT)4}$

are the base and collector currents respectively when Q_4 is saturated.

Then, t_s, the time taken to dissipate the stored charge in Q_4, is given by

$$t_s = \frac{\tau_s I_{B4} (r'_{b4} + r_{CS2})}{V_{BE(SAT)4} - V_{CE(SAT)2}} \qquad (3)$$

d) Once the stored charge in Q_4 is dissipated, its collector voltage begins to rise until Q_3 reaches the edge of the active region. The computation of this time involves the solution of a nonlinear differential equation. However, since the base of Q_4 is essentially shorted to ground through Q_2, this time can be ignored.

e) Once Q_3 enters its active region, the feedback action of the flip-flop is initiated and a permanent indication of malfunction is obtained. The precise point at which the balance of the flip-flop is altered is open to question. However, this time can be conveniently ignored, as is noted experimentally by the fact that the malfunction indication is extremely sensitive to any input current change at this point. (In the experimental study, it was not possible to hold the circuit on the verge of malfunction.)

If all these events occur in sequence, the minimum pulse width required is given by $t_d + t_r + t_s$. It is easily seen that the turn-on delay interval and the rise time interval of Q_2 do indeed occur in sequence. On the other hand, some of the charge in Q_4 begins to be dissipated the moment the collector voltage of Q_2 becomes equal to $V_{BE(SAT)4}$.

The fraction of the rise time during which this occurs is given by

$$t_1 = t_r \cdot \frac{V_{BE(SAT)4} - V_{CE(SAT)2}}{V_B - V_{CE(SAT)2}}$$

During this time interval, the loop voltage varies from zero to a maximum of

$$V_{BE(SAT)4} - V_{CE(SAT)2}$$

To a first approximation, this variation may be assumed to occur linearly during the time interval.

The effective resistance in the loop is

$$r'_{b4} + R_L$$

Consequently, during this interval, the loop current may be assumed to rise linearly from zero to a value given by

$$i_1 = \frac{V_{BE(SAT)4} - V_{CE(SAT)2}}{r'_{b4} + R_L}$$

Integrating this current over the time t_1 results in the charge dq that is dissipated during the risetime interval. Thus,

$$dq = \frac{1}{2} i_1 t_1$$

$$= \frac{1}{2} \cdot \frac{t_r}{(r'_{b4} + R_L)} \cdot \frac{\left[V_{BE(SAT)4} - V_{CE(SAT)2}\right]^2}{V_B - V_{CE(SAT)2}}$$

The base stored charge $\tau_s I_{B4}$ is reduced by dq during this part of the risetime interval.

It has been shown previously (see P. 60) that the time interval t_s required to dissipate the stored charge in Q_4 is given by

$$t_s = \text{Stored Charge} \cdot \frac{r'_{b4} + r_{CS2}}{V_{BE(SAT)4} - V_{CE(SAT)2}}$$

Consequently, if we consider the dissipation of stored charge <u>after</u> the transistor rise time interval, the time for this event to occur is $t_s - dt_s$,

where

$$dt_s = \frac{1}{2} \; t_r \left[\frac{V_{BE(SAT)4} - V_{CE(SAT)2}}{V_B - V_{CE(SAT)2}} \right] \left[\frac{r'_{b4} + r_{CS2}}{r'_{b4} + R_L} \right] \quad (4)$$

It is seen that there is an approximately inverse relation between dt_s and V_B, if the term $V_{CE(SAT)2}$ is ignored.

The term dt_s may be ignored in medium speed circuits, since these normally operate at large values of collector supply voltage. This is not the case in high speed circuits, however, where very low values of supply voltage, and correspondingly large values of supply current, are common.

Thus, the total time that the pulse must be maintained to cause malfunction is given by

$$\tau = t_d + t_r + t_s - dt_s$$

Of these terms, both t_d and t_s are only functions of the power supply voltage and of the circuit, while t_r and dt_s are functions of the noise current amplitude. Thus, the noise pulse width takes the form of

$$\tau = K/I + \tau_o$$

where τ_o is a constant for the circuit.

These computations have been carried out for the high speed gate of Figure G-2, using 2N709 transistors. Since discrete components were used for this experiment, the value of the collector-to-substrate capacitance of the coupling transistor has been ignored.

The various circuit and parameter values used for these devices is given in Table 1. Most of these were taken off the manufacturers specification sheet. The base spreading resistance is unfortunately not specified and was thus obtained from the experimentally derived input impedance curve shown in Figure E-4.

For this case,

$$\tau = (24/I + 1.08) \text{ nsecs.}$$

where I is in milliamperes.

Figure G-3 shows a plot of I as a function of τ, obtained experimentally on the circuit of Figure G-2. The input current to the coupling transistor was monitored with the aid of a current transformer and a sampling oscilloscope, and was seen to be nearly rectangular for all values of pulse width above 3.5 nsces. It is seen that there is close correlation between the calculated and experimental values.

The circuit was retested, using a slower speed transistor (2N706) in place of the 2N709. Parameter values for this circuit are also given in Table 1. Figure G-4 shows the experimental and calculated values. For this version,

$$\tau = (197/I + 2.55) \text{ nsecs.}$$

Again, close correlation is seen between theory and experiment.

A final comment is in order concerning the nature of these curves. At large values of τ, the theoretical expressions indicate that the current approaches zero. Clearly, this is not true, since it must reach a finite value.

With microcircuits, complete logic blocks are interconnected in the manner of Figure G-1. The circuit arrangement for this connection is shown in Figure G-5. The relations governing the noise immunity of this gate are very similar to those of the circuit of Figure G-2, with minor modifications. Thus,

$$t_d = \frac{dV_{BE2}\,(C_{TE2} + C_{CS1} + C)}{I_B}$$

as before. Also,

$$t_r = \frac{I_S\,(\tau_T + R_{L2}\,C_{C2})}{I}$$

as before, except that $C_{C2} = C_{TC2} + C_{TE6}$ for this configuration.

The storage time is given by

$$t_s = \frac{s\, I_{B4}\, (r'_{b4} + r_{cs2} + r_{cs6})}{V_{BE(SAT)4} - V_{CE(SAT)2} - V_{CE(SAT)6}}$$

where I_{B4} is supplied via R_B and not R_L as in the previous circuit. Finally,

$$dt_s = \frac{1}{2}\, t_r \left[\frac{V_{BE(SAT)4} - V_{CE(SAT)2} - V_{CE(SAT)6}}{V_B - V_{CE(SAT)2}} \right] \left[\frac{r'_{b4} + r_{cs2} + r_{cs6}}{r'_{b4} + R_L + r_{cs6}} \right]$$

Thus, the primary change is that due to the inclusion of the voltage drop across Q_6 and to its parasitic series resistance.

TABLE 1

Parameter	Values for 2N709	Values for 2N706	Remarks
$V_{BE(OFF)2}$	0.15 v	0.3 v	In the OFF condition
V'_{BE2}	0.5 v	0.6 v	At the edge of saturation
$V_{BE(SAT)4}$	0.9 v	0.9 v	In saturated condition
$V_{CE(SAT)2}$	0.15 v	0.3 v	
V_B	1.5 v	1.5 v	See Figure G-2
C_{TE2}	4 pf.	8 pf.	For a collector current of about 10 ma.
C_{TE4}	4 pf.	8 pf.	For a collector current of about 10 ma.
C_{TC2}	2.5 pf.	5 pf.	
C_{TC3}	2.5 pf.	5 pf.	
C_{CS1}	0 pf.	0 pf.	For this circuit
C	0 pf.	0 pf.	For this circuit
$r'_{b4} + r_{CS2}$	40 ohms	15 ohms	Measured, as in Figure E-4
α_{eo4}	50	20	
f_T	500 mc	50 mcs	Averaged over the rise time
τ_T	2 nsec	20 nsec	
τ_s	3 nsec	16 nsec	
R_{L2}	30	13	Figure G-2
I_B	4.7 ma	4.35 ma	Figure G-2 (during t_d phase)

TABLE 1 (continued)

Parameter	Values for 2N709	Values for 2N706	Remarks
I_{B4}	5 ma	5 ma	To drive Q_4 into saturation
$I_{(SAT)4}$	11.25 ma	10 ma	
I_s	11.25 ma	10 ma	Since initially Q_3 is OFF
t_d	0.38 nsec	0.55 nsec	Equation 1
t_s	0.705 nsec	2.0 nsec	Equation 3
t_r	25.8/I	225.2/I	Equation 2 I in ma
dt_s	.074 t_r	.028 t_r	Equation 4
τ	24/I + 1.08	197/I + 2.55	In nsecs.

APPENDIX H

Oscillation Hazards in Asynchronous Sequential Circuits

Introduction

The investigation and results described here originated with the observation that with very fast nor gates having very low output capacitance, the circuit of Figure H-1 will oscillate when the signals at both A and B of Figure H-1 are simultaneously changed from 1 to 0. This behavior is a property of a model in which each gate is replaced by an instantaneous calculation of the "nor" function of its inputs followed by a delay. If the circuit is redrawn as shown in Figure H-2, it is readily apparent that if the nor gates are modelled as ideal logical devices followed by pure delays that oscillation will result when the signals at A and B are simultaneously changed from 1 to 0. Such a model does not accurately represent a practical nor gate. However, to the extent that the rise time of the gate plus output wiring is small compared to the delay of the same configuration, the model becomes increasingly valid. Alternatively, the transfer function of the two gates with the output wire must have greater than unity gain at 360 phase shift.

If the transfer functions of the gates with their output wires are known, the possibility of such oscillation would be indicated by the Nyquist criterion. If the devices themselves have no phase shift this would require greater than unity loop gain at a frequency for which the interconnecting wires are a wavelength long.

In the course of further work with the same circuits a very fast counter was required to measure the duration of a pulse whose width was determined by radar range. It was discovered that the readout circuit for such a counter could not be designed to avoid the possibility of oscillation for a certain relation between the time of the read-out signal and the transitions of the clock signal driving the counter. After some investigation it was found that many standard synchronizing circuits suffered from this difficulty.

An <u>inertial</u> delay of length D has the property that no input pulse of length less than D appears at the output of the inertial delay and any input pulse of length greater than D appears at the output delayed by D. A circuit which has this property was described by Unger (1) and is shown in Figure H-3.

The device labelled M in Figure H-3 is a "majority" gate. Such a gate produces an output of one if and only if two or more of its inputs are one.

The logical function computed by the majority gate of Figure H-3 can also be computed using nor logic as shown in Figure H-4.

It is readily seen that if the output Y is identified with the input C as is required for the realization of the inertial delay of Figure H-3 and if each nor gate has a small pure delay then the circuit can be caused to oscillate in a variety of ways. For example, the circuit of Figure H-3 with the majority logic of Figure H-4 is stable if the output of the majority logic is zero (and hence C is zero) while A = 0 and B = 1. If A changes to 1 one gate delay before B changes to zero, the closed loop

will oscillate. Since this transition could occur in normal operation of the inertial delay, the circuit of Figure H-3 with the majority logic of Figure H-4 cannot be regarded as reliable under asynchronous operation.

It was observed that an ideal inertial delay of more than one gate delay inserted in series with one of the nor gate outputs of Figure H-1 would prevent the oscillation of that circuit. It should be observed that two identical inertial delays in series with both nor gate outputs will not prevent oscillation. It was therefore conjectured that reliable asynchronous circuits can not be constructed from logical devices having pure delays and pure delays alone. In addition to such components, a component having low pass filtering properties or properties similar to an inertial delay is necessary for the reliable operation of such asynchronous circuits. This does not seem to be generally recognized as the use of capacitors is frequently forbidden in the use of high speed gates without the provision of any alternative device which can function in a manner similar to an inertial delay.

Results

The theorems proved in this paper are pertinent to this question. The theorems are not completely general in that a flow tables are assumed for which the transition between two stable states involves at most one transient. No effort has been made as yet to generalize the results beyond this case.

The concept of a critical input race is central to the investigation. An asynchronous flow table is said to contain a critical input race if there is a pair of input lines and values of the signals on these lines and an internal state which is stable for the pair of signal values with the property that the stable state resulting from a change of both values depends upon the order of the change.

Under these assumptions we have

Theorem 1 If a critical race exists in an asynchronous flow table, then there is no secondary assignment such that the combinational logic which computes the next state is free from functional hazards.

The proof of this theorem is given in the Appendix I. The definition of a functional hazard is due to Eichelberger (2) and is discussed in the reference given. Roughly, a Boolean function with a functional hazard cannot be mechanized in such a way as to insure no undesirable transients in the output of the mechanization when certain inputs change simultaneously.

Of course, such transients could be eliminated by placing an ideal inertial delay in series with each output of the combinational logic if the magnitude of the delay were greater than the difference between the maximum and minimum delay through the logic.

For the proof of Theorem 2 it is assumed that all transitions between stable states involve the change of only a single secondary variable. That such secondary assignments are always possible has been shown by Huffman (3). The argument can be generalized, but becomes very tedious. The principal difficulty is clear from the argument in the

limited context and such assignments are usually used in practice. We will call such assignments Huffman secondary assignments.

Theorem 2 If an asynchronous circuit with a Huffman secondary assignment contains a critical input race then even if the combinational logic which computes the next state is hazard free, appropriate input change timing may cause oscillation for certain combinations of stray delay in the combinational logic unless sufficiently large inertial delays are placed in the feedback loops. A sufficient condition for stability is that such delays be larger than the longest logic delay.

The proof of this theorem is contained in the Appendix I. The proof exhibits the range of input change timing which yields unreliable results and specifies the magnitude of the inertial delays required to insure that such unreliability does not occur.

The theorems can of course be applied to the construction of the inertial delay itself. If such a delay is constructed from logical devices and a pure delay in the form shown in Figure H-5 then it is readily seen that the flow table for the asynchronous circuit contains a critical input race and could hence only be reliably designed with the aid of an inertial delay. We conclude, therefore, that under the assumptions made here that a complete set of devices for the design of reliable asynchronous circuits must include some device which will serve the function of an inertial delay. A capacitor will serve since it can fulfill the function of a low pass filter but only at the expense of deterioration of output rise times.

APPENDIX I

Proofs on Theorems on Hazards in Asynchronous Sequential Circuits

Proof on Theorem 1

The combinational logic of an asynchronous sequential switching circuit must compute a set of n Boolean functions defined by a table which is formed by substituting a sequence of n binary digits for each state of its flow table. A particular choice of such a sequence for each state is called a secondary assignment. The portion of such a table corresponding to the most complex form of critical input race is shown in Figure I-1.

We will be concerned with the values of the n Boolean functions defined by such a table on a subset of the total states where a total state is defined as a pair consisting of an input combination and the secondary assignment for an internal state. For example, the pair aN10 defines a total state, where "a" is an abbreviation for the sequence $a_1 a_2 \ldots a_n$ of binary digits and N denotes a fixed combination of values for all inputs except those involved in the critical input race which are specified by the final ordered pair of binary digits.

To each pair of total states there corresponds a subset of total states called a subcube of which the pair are diagonally opposite vertices. This subset is defined as follows.

Definition: Given two arbitrary total states, the set of total states which have the same binary digits as the two given total states in the positions where the binary digits of the two given states are identical,

is called the subcube determined by the pair of given total states. This subcube will be denoted by (x,y) where x and y are the designations of the given total states. The total states x and y are diagonally opposite vertices of the subcube.

Eichelberger (3) has defined a Boolean function as having a subcube of sets of argument values such that the function values agree on a pair of diagonally opposite vertices and are not identical on all sets of argument values in the subcube.

Eichelberger has shown for Boolean functions having function hazards that no mechanization can insure the absence of undesireable output transients for arbitrary input changes regardless of stray logic delays.

With these definitions the argument proceeds as follows.

Since there is a critical input race it must be true that $a_j \neq b_j$, $a_k \neq d_k$ for some $j \neq k$. There are then two possibilities for c_j.

If $c_j = a_j$ then $c_j \neq b_j$ and the jth Boolean function has a function hazard on the (aN01, cN10) subcube as shown in Figure I-2 since the value a_j is assumed on the total states aN01 and cN10 while the value $\bar{a}_j$ is assumed on aN00.

An exactly analogous argument demonstrates the existence of a function hazard if $e_k = a_k$ by considering the values for the kth function on the subcube

(aN01, cN10)

Therefore if a function hazard is not to exist we must have

$$a_j \neq c_j \qquad a_j \neq b_j \qquad j \neq k$$
$$a_k \neq e_k \qquad a_k \neq d_k$$
$$c_i \neq e_i$$

A number of cases will now be considered which are easily followed if the constraints above are described in the form of Figure I-3.

Case (1) If $a_j = f_j$ or $a_k = f_k$ then since $a_j \neq b_j$ and $a_k \neq d_k$, a function hazard exists on the (aN01, aN10) subcube since the value b_j is assumed on this subcube by the jth function and the value d_k is assumed by the kth function on this subcube while the values on the diagonally opposite total states are $a_j = f_j$ and $a_k = f_k$ respectively.

Case (2) If $c_k = a_k$ then since the value $\bar{a}_k$ is assumed on (aN01, cN10) a function hazard exists.

Case (3) If $e_j = a_j$, then since the value $\bar{a}_j$ is assumed on the subcube (a N01, eN10) a function hazard exists.

Case (4) If $d_j = \bar{a}_j$ then since the value a_j is assumed on the (aN00, aN11) subcube, a function hazard exists.

Case (5) If $b_k = \bar{a}_k$ then since the value a_k is assumed on the (aN00, aN11) subcube a function hazard exists.

No reference is made to the ith position in these arguments.

Case (6) If $c_i = a_i$ and it is not true that $a_i = b_i = d_i = f_i$ a function hazard exists on the (aN01, cN10) subcube since all the values a_i, b_i, d_i, f_i are assumed there.

Case (7) Similarly if $c_i = \bar{a}_i$ a function hazard exists on the (aN01, cN10) subcube unless $a_i = b_i = d_i = f_i$.

The only possibilities remaining if no function hazard is to exist are

$$a_j \neq c_j, \quad a_j \neq b_j$$
$$a_k \neq e_k \quad a_k \neq d_k \qquad j \neq k$$
$$c_i \neq e_i \qquad \text{some } i$$

case (1) $\quad a_j \neq f_j, \; a_k \neq f_k$

case (2) $\quad c_k \neq a_k$

case (3) $\quad e_j \neq a_j$

case (4) $\quad d_j \neq \bar{a}_j$

case (5) $\quad b_k \neq \bar{a}_k$

case (6) and (7) $\quad a_i = b_i = d_i = f_i$

It is easily verified that these conditions require $i \neq j$, k, and that this assumption has not been previously required.

The value of the ith, j^{th} and k^{th} functions in the positions relevant to the critical input race can now all be written in terms of the values of a_i, a_j, a_k and c_i as shown in Figure I-4.
If $c_i = a_i$ then the d and c rows must not be included in the (aN01, fN10) if no function hazard is to exist since otherwise the function value $\bar{c}_i$ would occur on this subcube.

It follows that the a, b, c, f rows must be coded

$$a = \ldots a_i \ldots a_j \ldots a_k \ldots$$
$$d = \ldots a_i \ldots a_j \ldots \bar{a}_k \ldots$$
$$e = \ldots \bar{a}_i \ldots a_j \ldots \bar{a}_k \ldots$$
$$f = \ldots a_i \ldots \bar{a}_j \ldots \bar{a}_k \ldots$$

With no further constraint on the secondary assignment, the d row might be included in the (aN01, fN10) subcube. Since this would lead to a function hazard, if there is to be no function hazard there must be an integer $l \neq i, j, k$ such that

$$a = \ldots a_i \ldots a_j \ldots a_k \ldots a_l \ldots$$
$$d = \ldots a_i \ldots a_j \ldots \bar{a}_k \ldots \bar{a}_l \ldots$$
$$f = \ldots a_i \ldots \bar{a}_j \ldots \bar{a}_k \ldots a_l \ldots$$

eliminating the d row from the (aN01, fN10) subcube. However, this coding results in a function hazard on the (aN01, aN10) subcube since the lth function has values $a_l = f_l$ on diagonally opposite total states and the value $d_l = \bar{a}_l$ on the subcube.

Similarly, if $c_i = \bar{a}_i$ then the b and c rows must be included in the (aN01, fN10) subcube if a functional hazard is not to exist. Then the a, b, c, f rows must be coded

$$a = \ldots a_i \ldots a_j \ldots a_k \ldots$$
$$b = \ldots a_i \ldots \bar{a}_j \ldots a_k \ldots$$
$$c = \ldots \bar{a}_i \ldots \bar{a}_j \ldots \bar{a}_k \ldots$$
$$f = \ldots a_i \ldots \bar{a}_j \ldots \bar{a}_k \ldots$$

If the b row is in the subcube a function hazard would be present. Hence if no function hazard is to exist there must be an integer $m \neq i, j, k$ such that the a, b, f rows are coded

$$a = \ldots a_i \ldots a_j \ldots a_k \ldots a_m \ldots$$
$$b = \ldots a_i \ldots \bar{a}_j \ldots a_k \ldots \bar{a}_m \ldots$$
$$f = \ldots a_i \ldots \bar{a}_j \ldots \bar{a}_k \ldots a_m \ldots$$

However, this coding results in a function hazard on the (aN01, aN10) subcube since the mth function has the value $a_m = f_m$ on diagonally opposite total states and $b_m = \bar{a}_m$ on the total state (aN00).

The critical input race of Figure I-1 has the maximum number of transient states assuming direct transitions from stable states to stable states. Strictly speaking other cases involving fewer transient states should be considered. These arguments will be left to the reader since they are much simpler than the one given here and involve the same techniques.

Proof of Theorem II

Since it is assumed that the flow table contains a critical race, there must be a sub-table of the form of Figure I-5 or of a form which can be derived from the form of Figure I-5 by state identification. However, s_2 cannot be identified with s_5 or s_1 with s_4 if a critical input race is to exist.

The following notation will be used

T_d : Length of inertial delay in the feedback lines

T_s : Time between the change of input I_1 and the change of input I_2. It is assumed without loss of generality that the sequence of input changes is N01→N11→N10 since the argument for the sequence N01→N00→N10 is identical.

$T_c(s_i \xrightarrow{ab} s_j)$: The time required for the combinational logic to compute the internal state s_j after a change in input occurs when the sequential machine is in the internal state s_i which results in the input state ab.

We will first distinguish three cases.

I (classical) $T_c\ (s_o \xrightarrow{11} s_1) + T_d < T_s$

II (ambiguous)

$$T_d + T_c\ (s_o \xrightarrow{11} s_i) - T_c\ (s_o \xrightarrow{10} s_3) < T_s < T_d + T_c\ (s_o \xrightarrow{11} s_1)$$

III (simultaneous)

$$T_s < T_d + T_c\ (s_o \xrightarrow{11} s_1) - T_c\ (s_o \xrightarrow{10} s_3)$$

Case I: When I_1 changes in the stable state s_o the circuit will compute s_1 which will arrive at the outputs of the inertial delays after an interval of time $T_d + T_c\ (s_o \xrightarrow{11} s_1)$. Since s_1 is stable with input 11 no further change will occur until I_2 changes, at which time the circuit will compute the stable state s_2. This is the classical case of input change separation sufficiently large to allow stabilization after each input change.

Case III: When I_1 changes the combinational logic will compute s_1 after $T_c\ (s_o \xrightarrow{11} s_1)$. However, I_2 changes when the output of the inertial delays is still s_o. The combinational logic will then compute s_3 which will reach the inputs to the inertial delays at $T_s + T_c\ (s_o \xrightarrow{10} s_3)$ after the first input change. The difference in time of arrival at the inertial delays is $T_s + T_c\ (s_o \xrightarrow{10} s_3) - T_c\ (s_o \xrightarrow{11} s_i)$ which is less than the inertial delay so that the delay outputs will change from $s_o \rightarrow s_3$. If the input changes are close enough to satisfy the inequality of case III they are regarded as simultaneous by the sequential circuit.

Case II: In case II the result of the changes is ambiguous and depends upon the relative size of T_s and

$$T_c\ (s_o \xrightarrow{11} s_i) + T_c\ (s_i \xrightarrow{10} s_2) - T_c\ (s_o \xrightarrow{10} s_3)$$

First we assume that

(1) $T_s > T_c\,(s_o \xrightarrow{11} s_1) + T_c\,(s_1 \xrightarrow{10} s_2) - T_c\,(s_o \xrightarrow{10} s_3)$. It is readily verified that the state s_1 will get through the inertial delays after the change in I_2 if and only if the inequalities of Case II are valid. In Case I s_1 gets through the delays before I_2 changes and in Case III s_1 does not get through the delays. In the state s_1 with input 10 the state s_2 is computed and arrives at the inertial delays at

$$T_c\,(s_o \xrightarrow{11} s_i) + T_c\,(s_1 \xrightarrow{10} s_2) + T_d$$

However, at the time of the second input change the outputs of the delay held s_o and the circuit computed s_3 which arrived at the delay inputs at

$$T_c\,(s_o \xrightarrow{10} s_3) + T_s$$

If

$$T_d > T_c\,(s_o \xrightarrow{11} s_1) + T_c\,(s_1 \xrightarrow{10} s_2) + T_d - T_c\,(s_o \xrightarrow{10} s_3) + T_s$$

s_3 will not pass through the inertial delays and the circuit will become stable in s_2. But this is precisely the inequality (1) which was assumed.

On the other hand, if the inequality (2) is true

(2) $T_s < T_c\,(s_o \xrightarrow{11} s_i) + T_c\,(s_1 \xrightarrow{10} s_2) - T_c\,(s_o \xrightarrow{10} s_3)$ then both s_3 and s_2 will pass through the inertial delays and since both s_3 and s_2 are stable the entire process will be repeated indefinitely if the time required to establish each of the stable states at the output of the combinational logic when that logic has computed the other exceeds the magnitude of the inertial delay. If the maximum logic delay is T_{max} then this will not occur if $T_d > T_{max}$. It is readily verified that if this condition holds even the first oscillation

will not occur since if

$$T_c\ (s_o \xrightarrow{11} s_1) + T_c(s_1 \xrightarrow{10} s_2) - T_c\ (s_o \xrightarrow{10} s_3)$$
$$T_d + T_c\ (s_o \xrightarrow{11} s_1) - T_c\ (s_o \xrightarrow{10} s_3)$$

the inequality (2) cannot be satisfied in case II which is equivalent to

$$T_d > T_c\ (s_1 \xrightarrow{10} s_2)$$

and is insured by $T_d > T_{max}$.

It should be noted that the argument only requires that any two of the states s_2, s_3, s_5 be distinct which is a slightly weaker condition than the existence of a critical input race. However, normally s_3 will be identical to either s_2 or s_5, in which case a critical input race is required.

References

(1) S. H. Unger, Hazards and Delays in Asynchronous Sequential Circuits, IRE Trans. on Circuit Theory, vol. CT-6, no. 1, pp. 12-25, 1959.

(2) E. B. Eichelberger, Hazard Detection in Combinational and Sequential Switching Circuits, IBM Journal of Research and Development, Vol. 9, No. 2, March 1965.

(3) D. A. Huffman, A Study of the Memory Requirements of Sequential Switching Circuits, Technical Report No. 293, Research Laboratory for Electronics, Massachusetts Institute of Technology, April 1955.

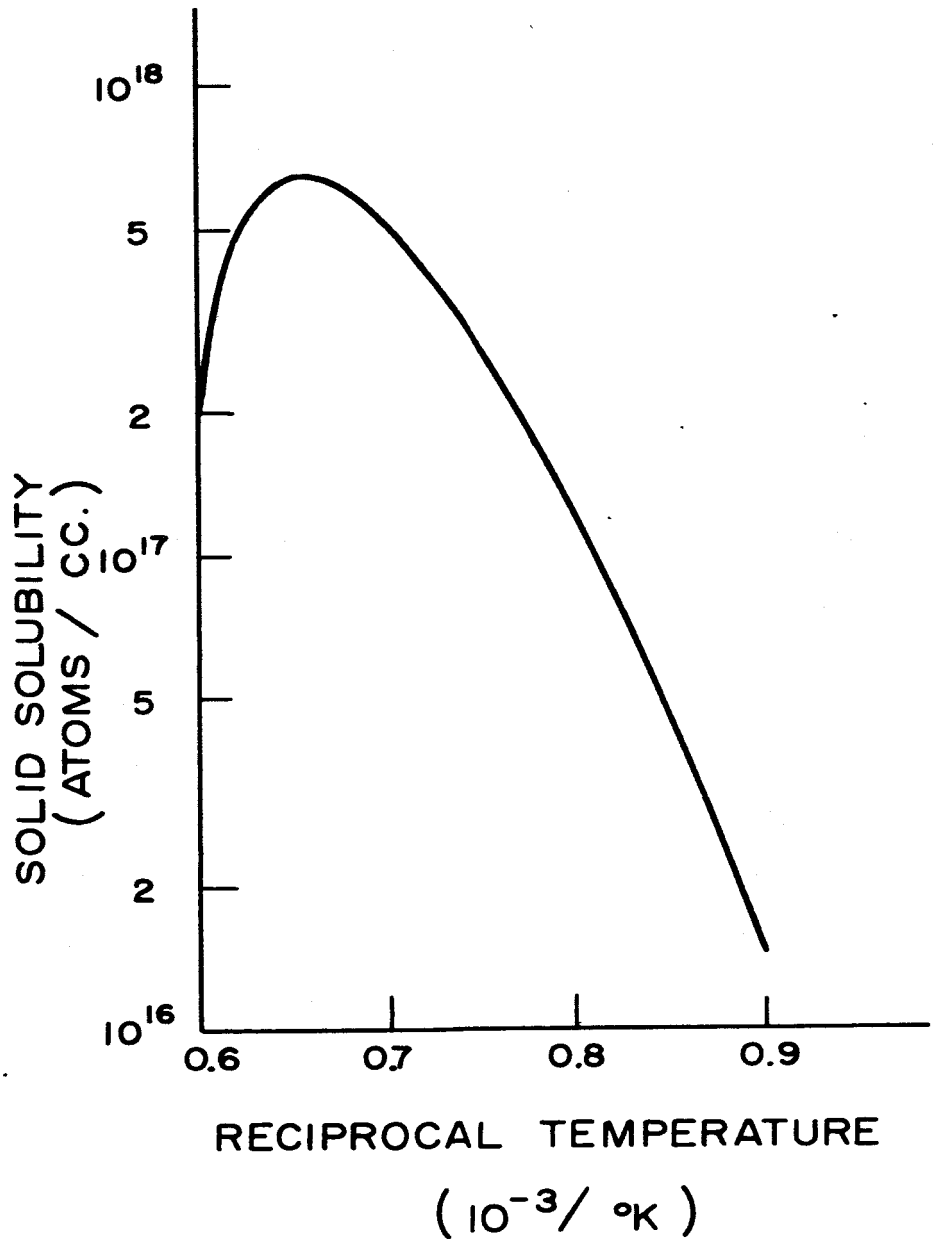

SOLID SOLUBILITY
(ATOMS / CC.)
10^{18}
5
2
10^{17}
5
2
10^{16}
0.6
0.7
0.8
0.9
RECIPROCAL TEMPERATURE
(10^{-3}/ °K)

FIG. 1

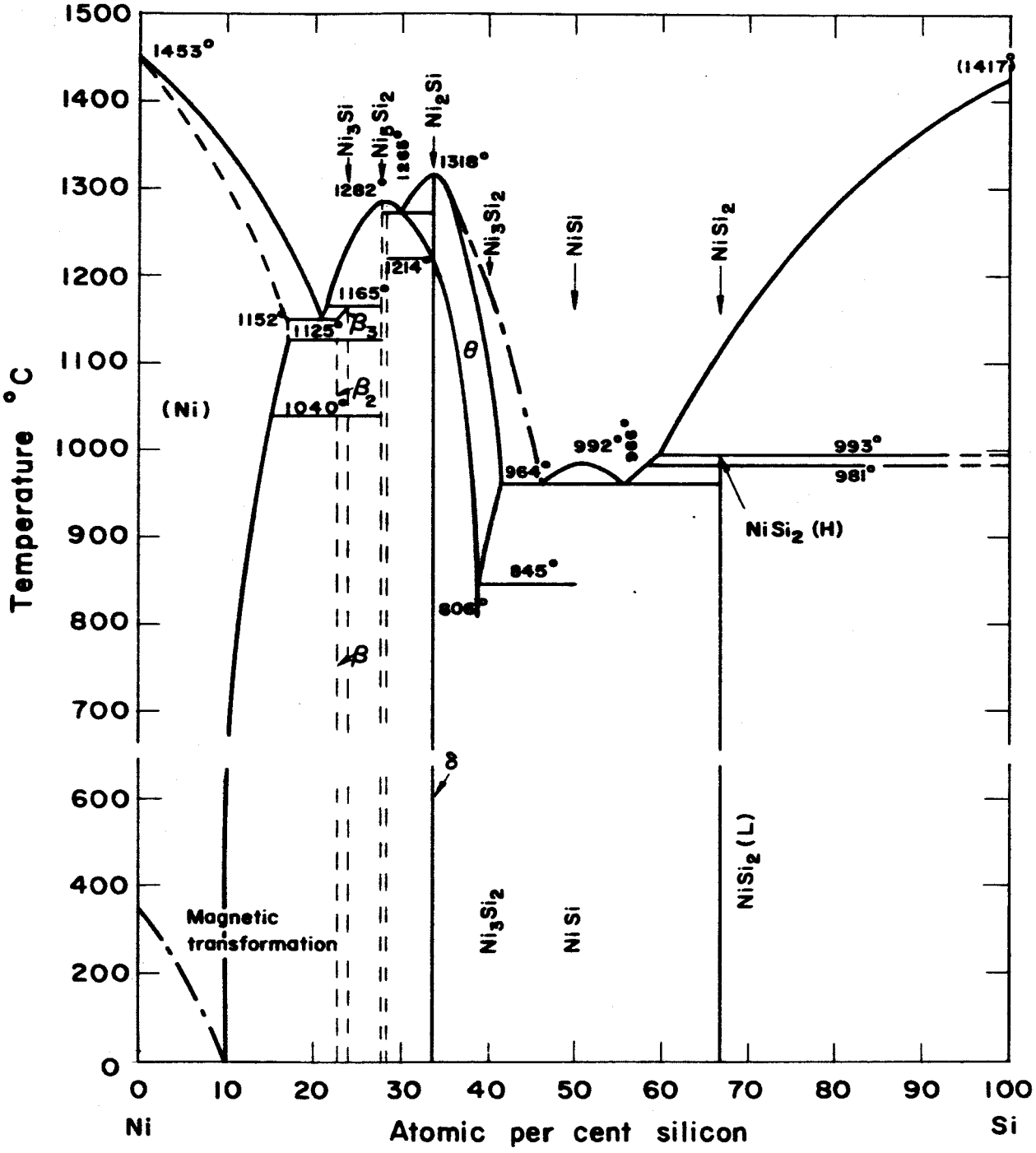

1500
1400
1300
1200
1100
1000
900
800
700
600
400
200
0
Temperature °C
1453°
(1417°)
Ni_3Si
Ni_3Si_2
Ni_2Si
1282°
1318°
1214°
1165°
1152°
1125°
β_3
β_2
1040°
β
θ
Ni_3Si_2
NiSi
$NiSi_2$
(Ni)
992°
964°
993°
981°
$NiSi_2$ (H)
845°
806°
δ
$NiSi_2$ (L)
Magnetic transformation
Ni_3Si_2
NiSi
0
10
20
30
40
50
60
70
80
90
100
Ni
Atomic per cent silicon
Si

FIG. 2

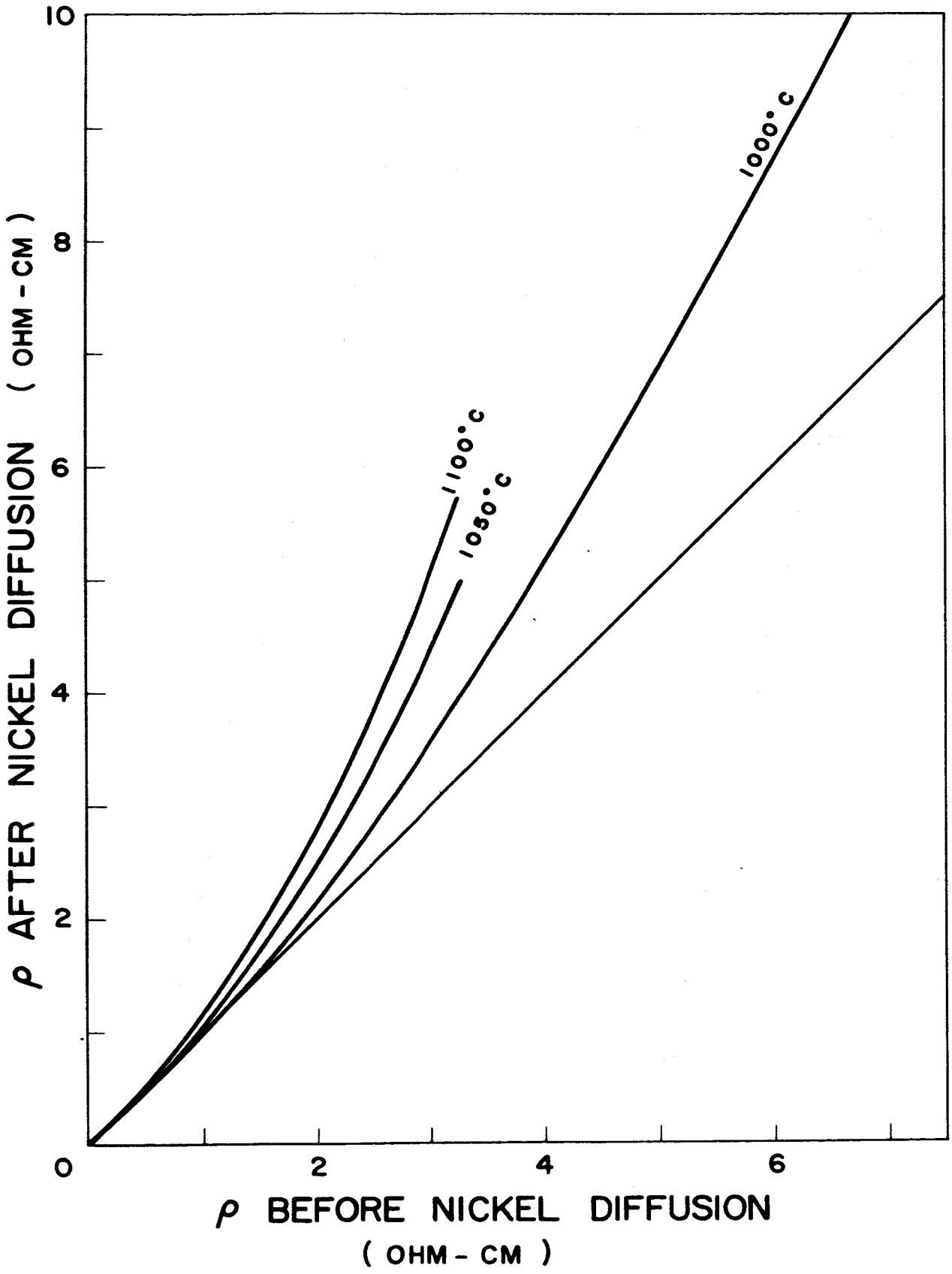

10
8
6
4
2
0
2
4
6
ρ AFTER NICKEL DIFFUSION (OHM - CM)
ρ BEFORE NICKEL DIFFUSION
(OHM - CM)
1000°C
1100°C
1050°C

FIG. 3

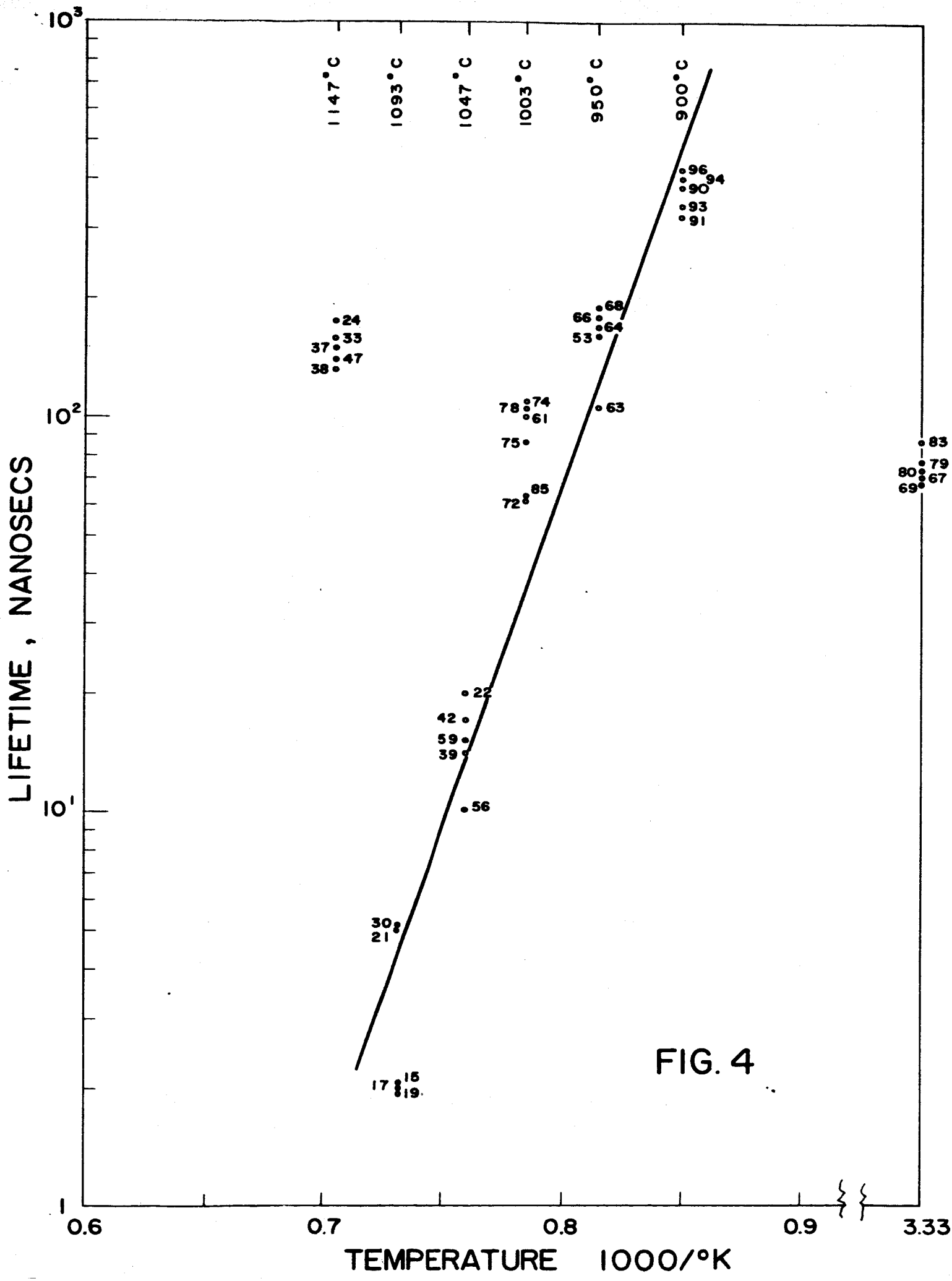

LIFETIME, NANOSECS
TEMPERATURE 1000/°K
1147°C
1093°C
1047°C
1003°C
950°C
900°C
10^3
10^2
10^1
1
0.6
0.7
0.8
0.9
3.33

FIG. 4

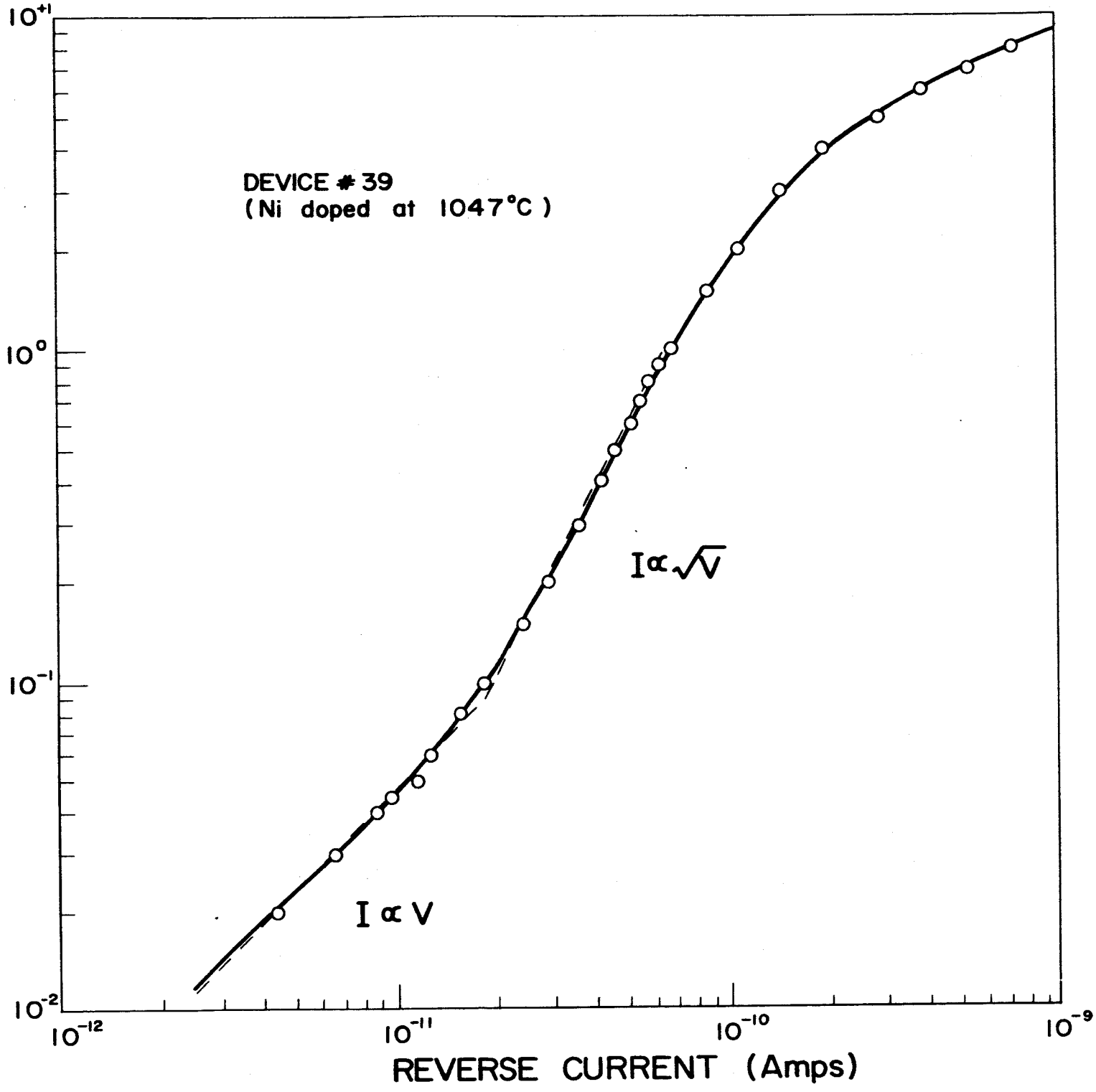

DEVICE # 39
(Ni doped at 1047°C)
I ∝ V
I ∝ √V
REVERSE VOLTAGE (Volts)
REVERSE CURRENT (Amps)
10^+1
10^0
10^-1
10^-2
10^-12
10^-11
10^-10
10^-9

FIG. 5

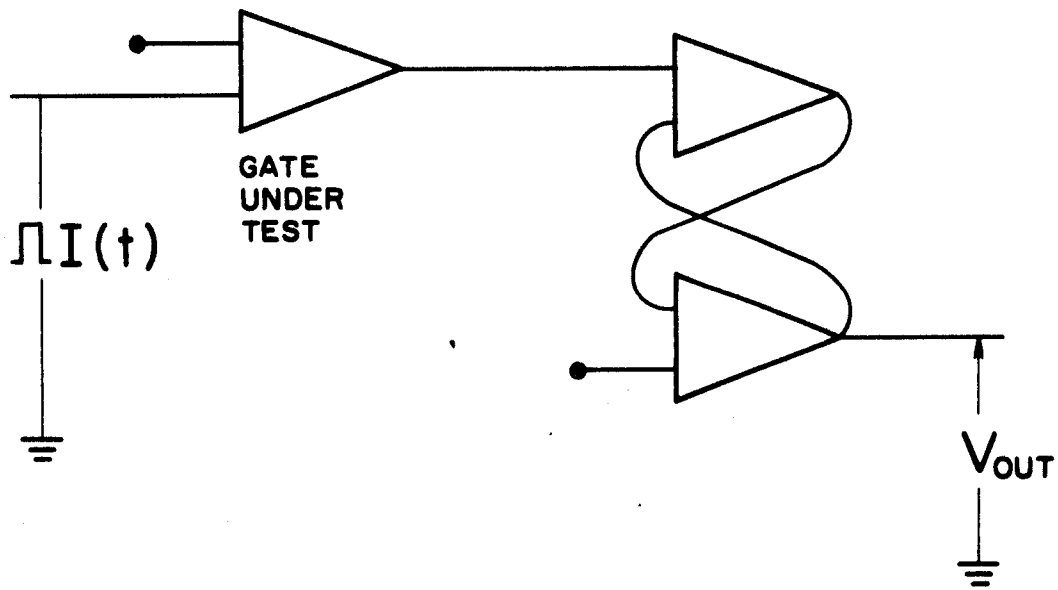


FIG. 6

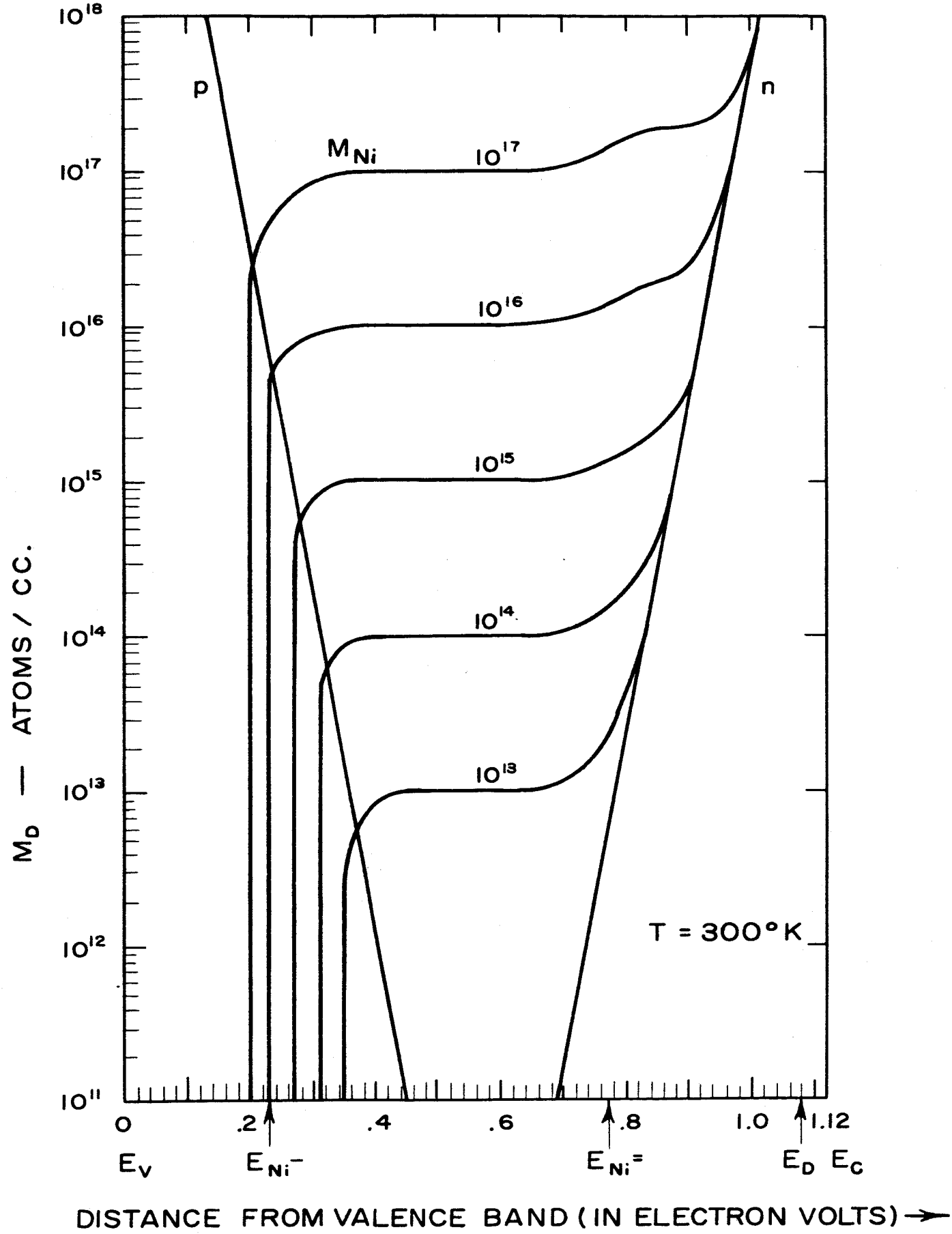

10^{18}
10^{17}
10^{16}
10^{15}
10^{14}
10^{13}
10^{12}
10^{11}
M_D — ATOMS / CC.
p
n
M_{Ni}
10^{17}
10^{16}
10^{15}
10^{14}
10^{13}
T = 300° K
0
.2
.4
.6
.8
1.0
1.12
E_V
E_{Ni^-}
$E_{Ni^=}$
E_D
E_C
DISTANCE FROM VALENCE BAND (IN ELECTRON VOLTS) →

FIG. A-1

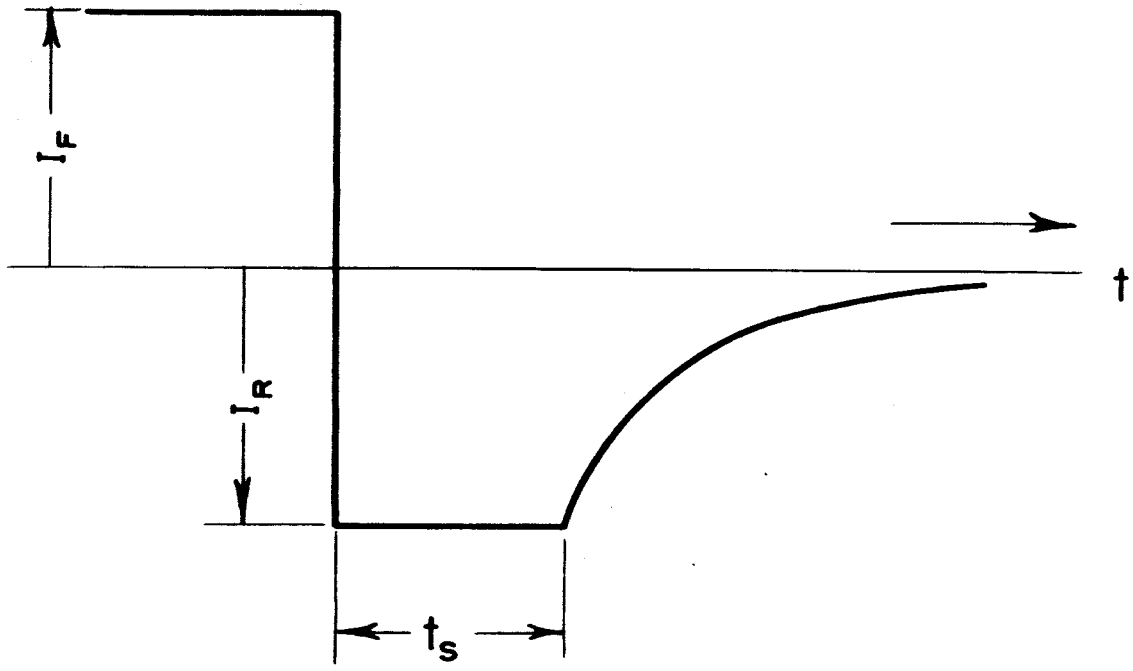


FIG. B-1

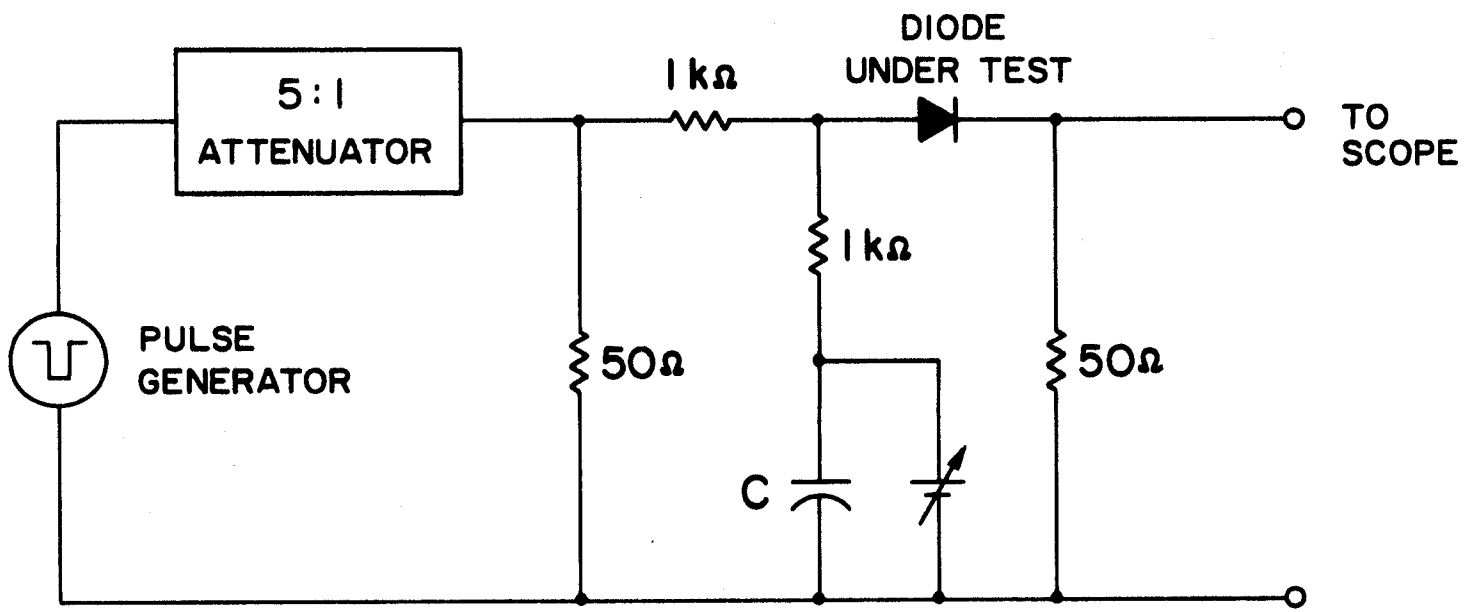

5 : 1
ATTENUATOR
1 kΩ
DIODE
UNDER TEST
TO
SCOPE
1 kΩ
PULSE
GENERATOR
50Ω
50Ω
C

FIG. B-2

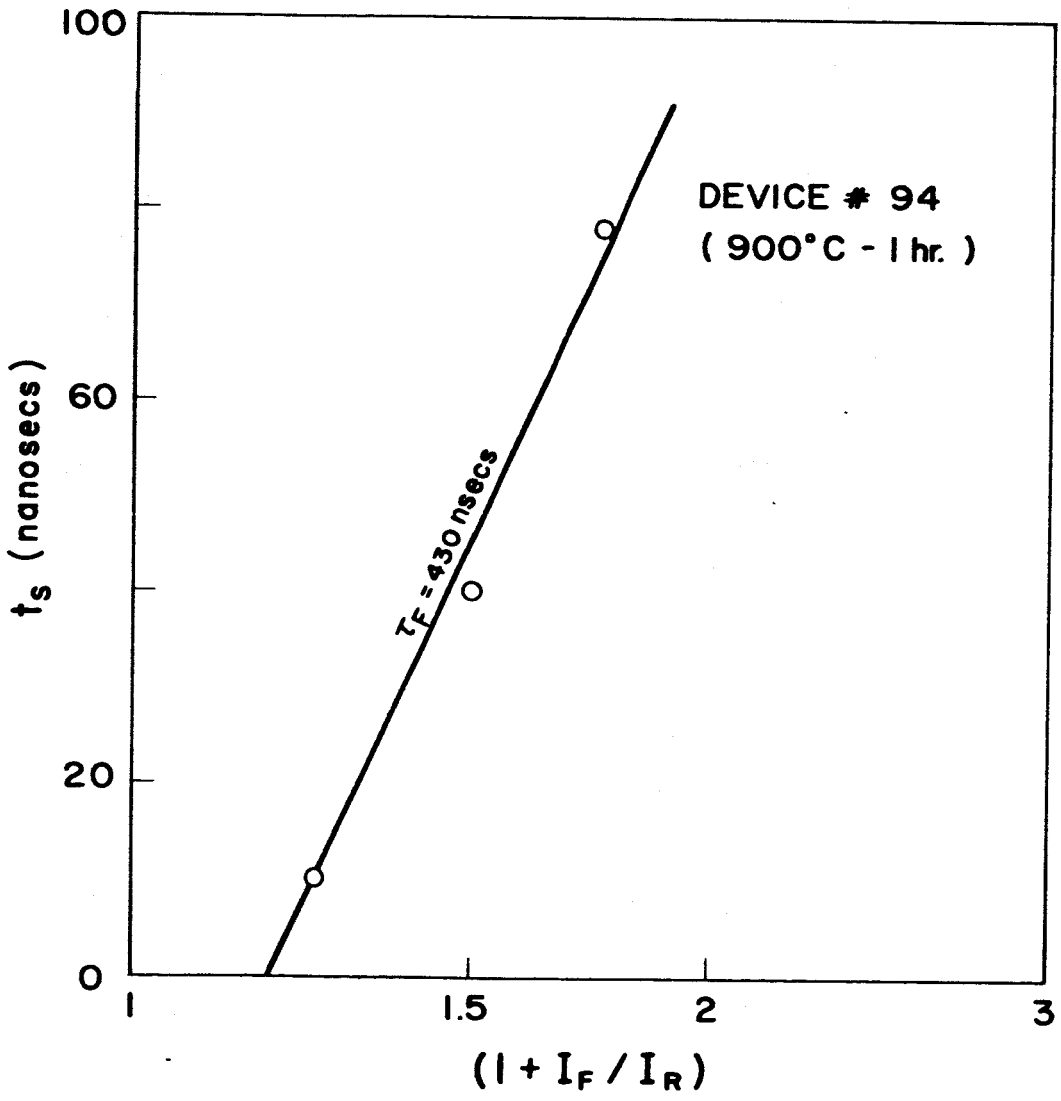

100
60
20
0
1
1.5
2
3
t_s (nanosecs)
$(1 + I_F / I_R)$
DEVICE # 94
(900°C - 1 hr.)
τ_F = 430 nsecs

FIG. B-3

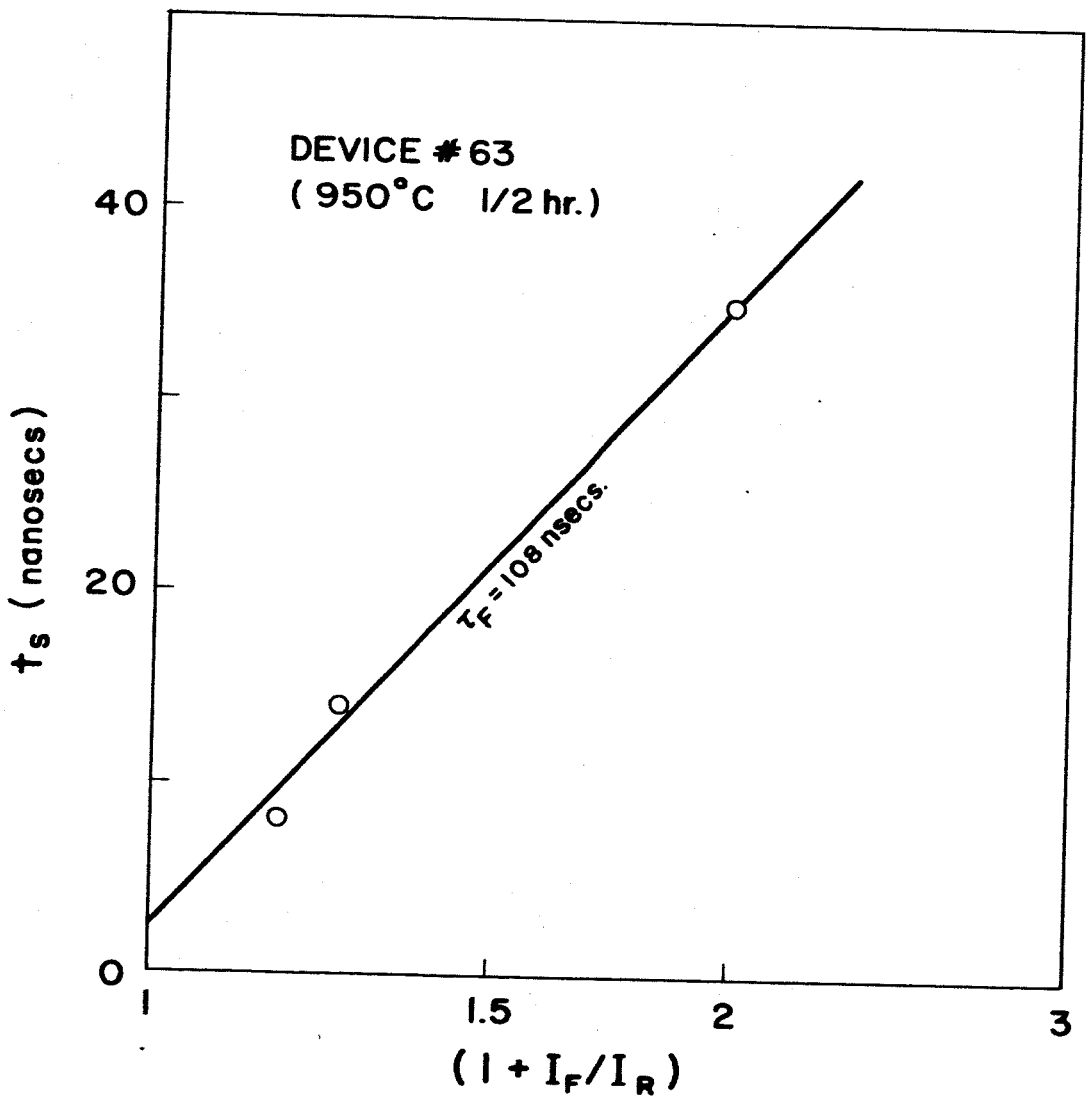

DEVICE # 63
(950°C 1/2 hr.)
τ_F = 108 nsecs.
40
20
0
t_s (nanosecs)
1
1.5
2
3
(1 + I_F/I_R)

FIG. B-4

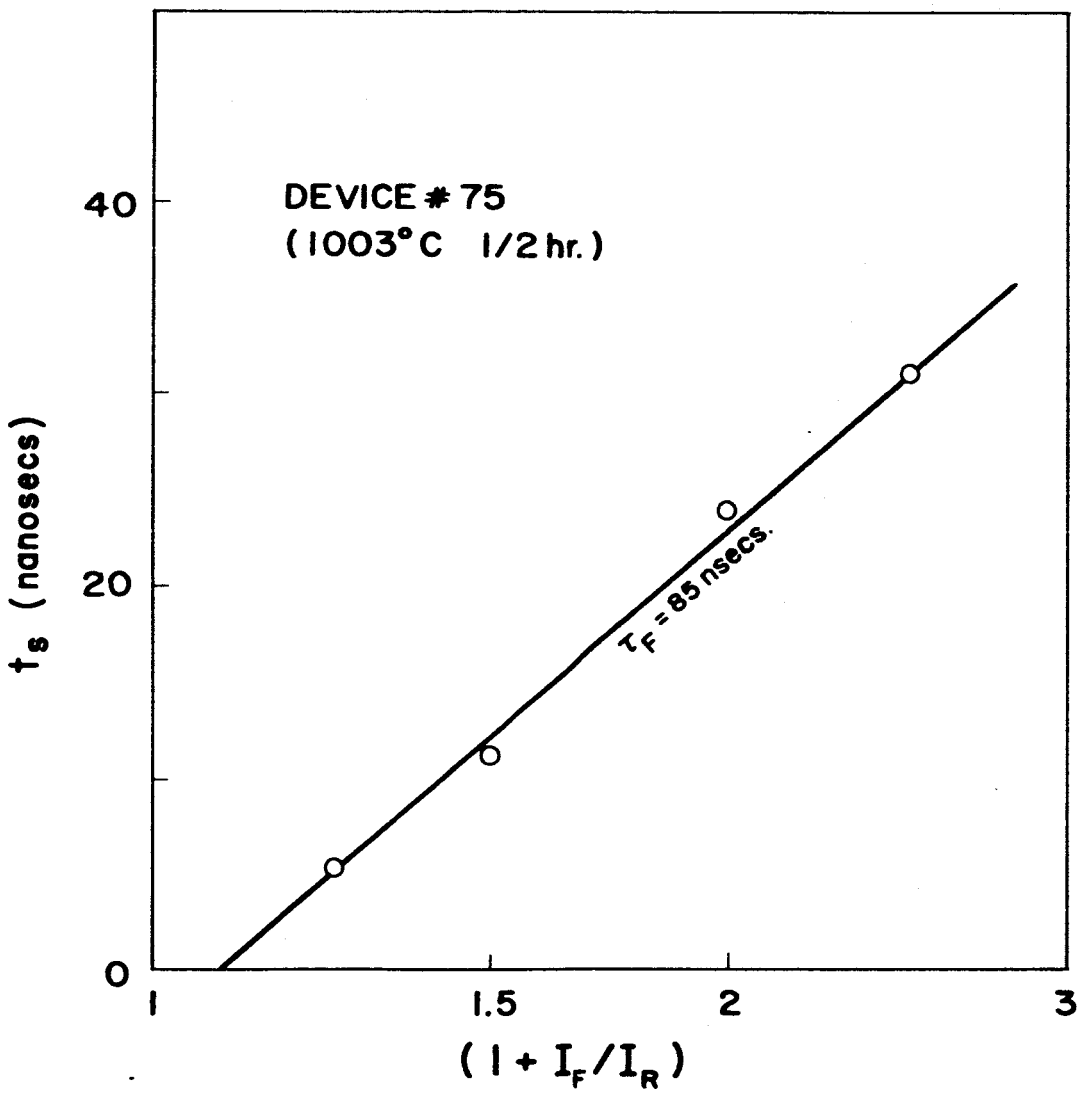

DEVICE # 75
(1003°C 1/2 hr.)
τ_F = 85 nsecs.
40
20
0
t_s (nanosecs)
1
1.5
2
3
$(1 + I_F/I_R)$

FIG. B-5

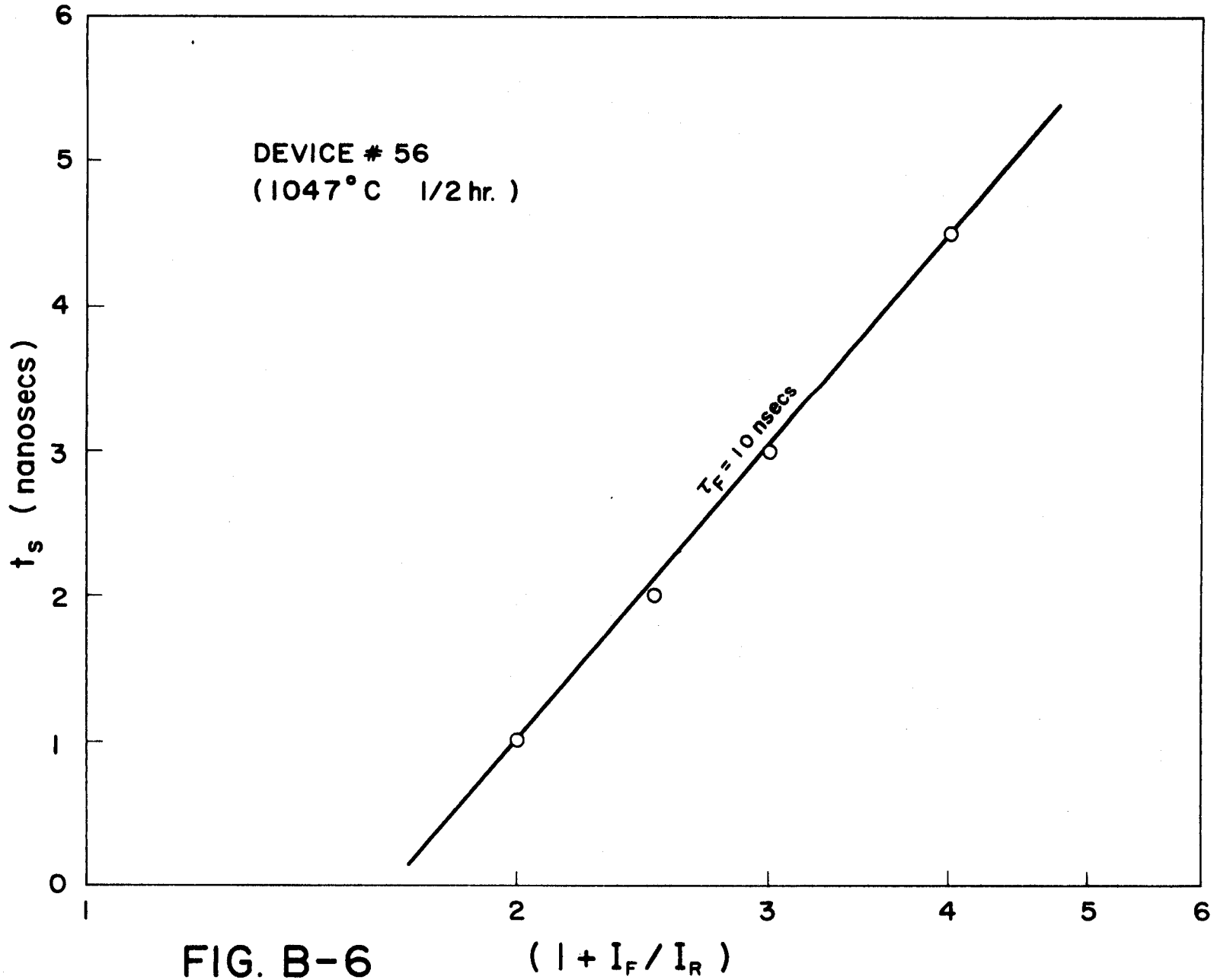

DEVICE # 56
(1047° C 1/2 hr.)
τ_F = 10 nsecs
t_s (nanosecs)
$(1 + I_F / I_R)$
0
1
2
3
4
5
6

FIG. B-6

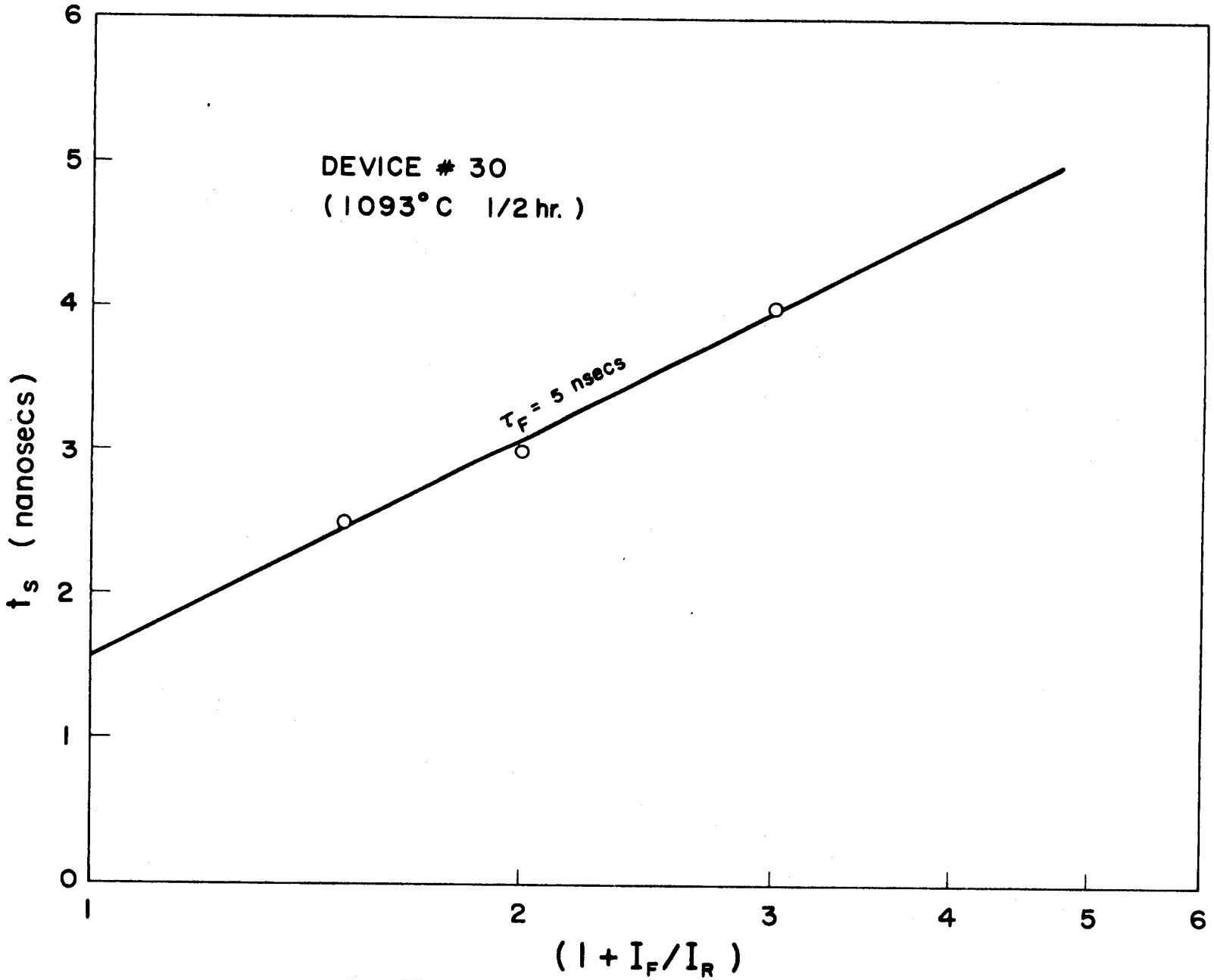


FIG. B-7

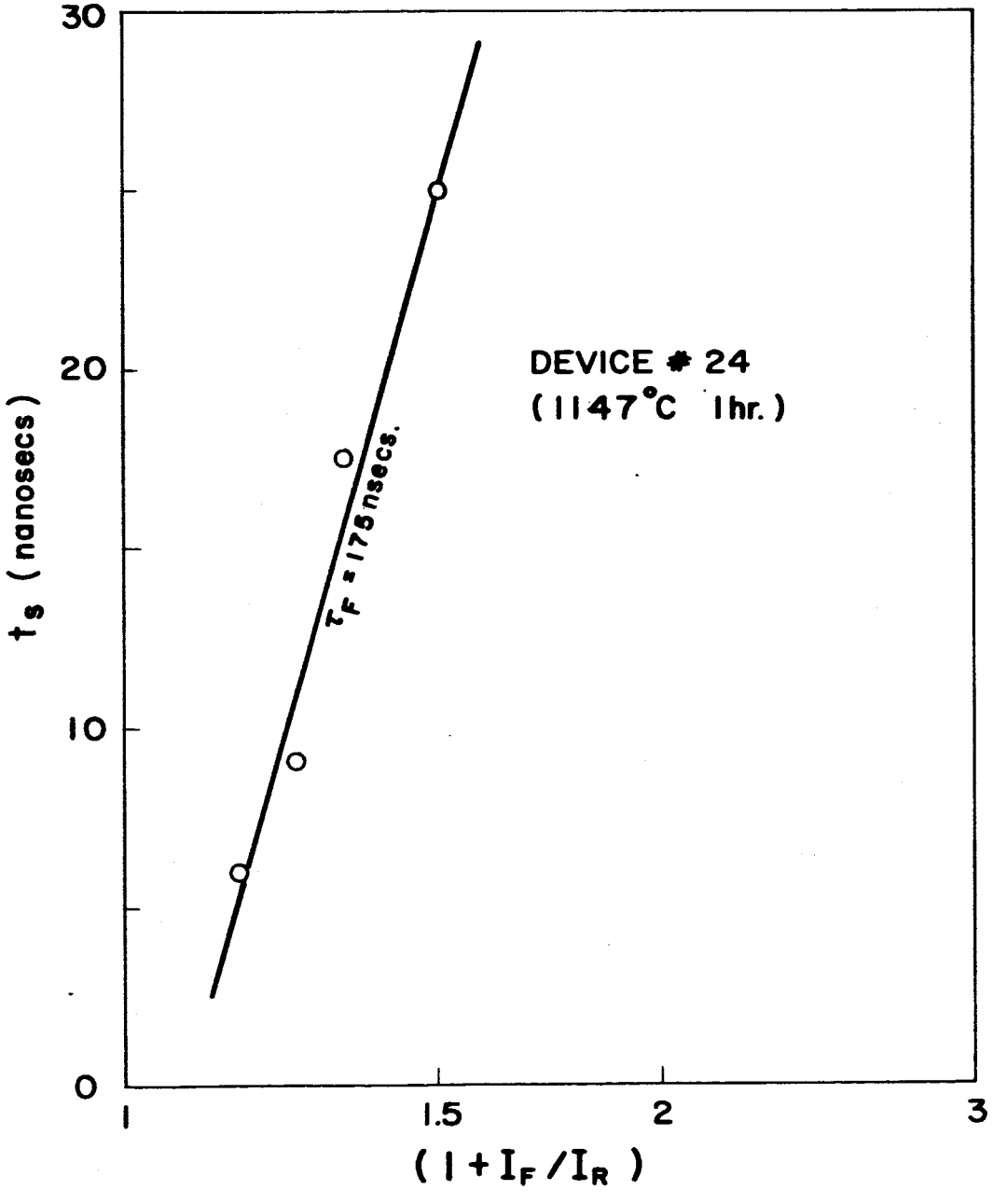

30
20
10
0
1
1.5
2
3
t_s (nanosecs)
$(1 + I_F/I_R)$
τ_F = 178 nsecs.
DEVICE # 24
(1147°C 1hr.)

FIG. B-8

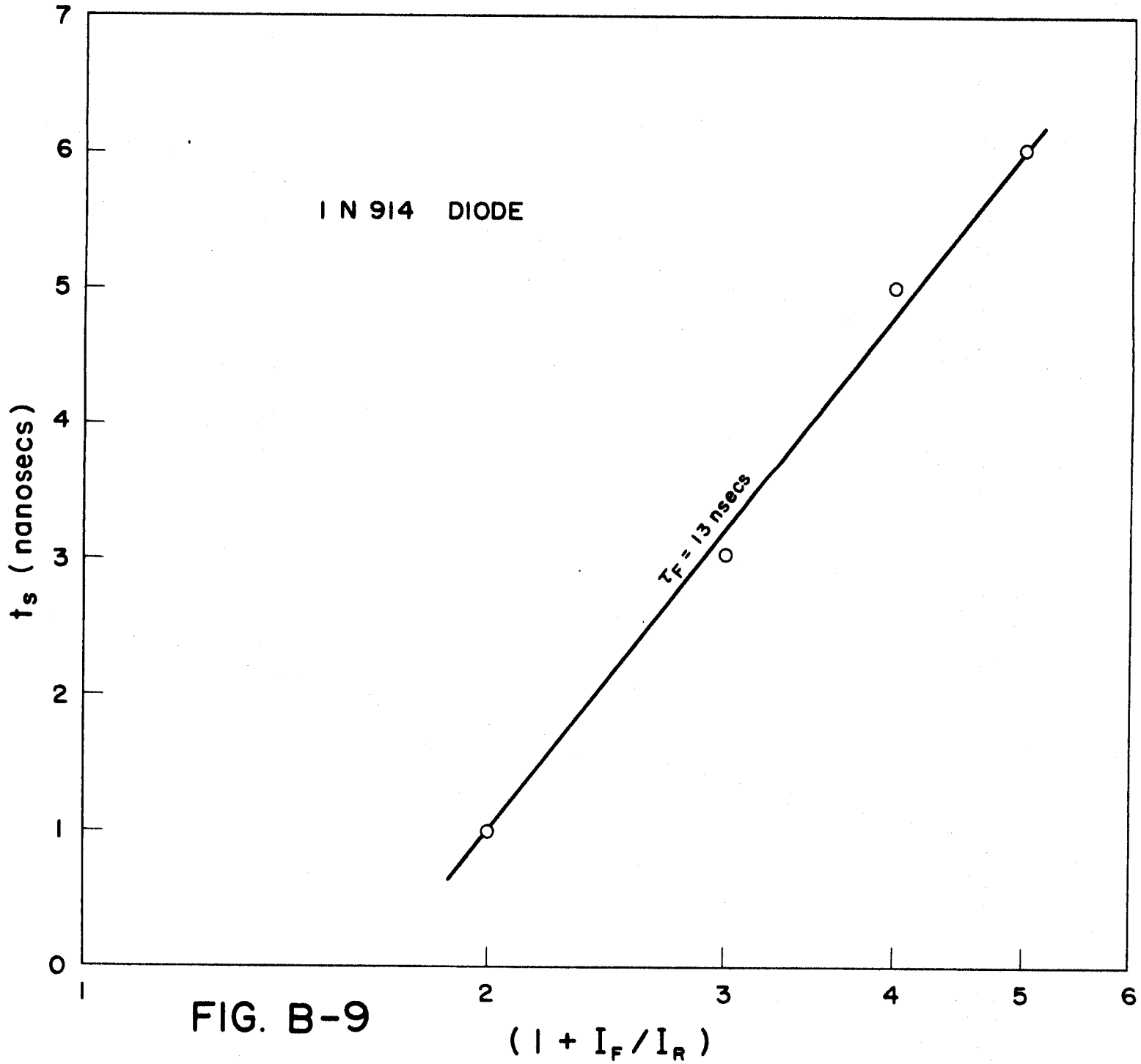

1 N 914 DIODE
τ_F = 13 nsecs
t_s (nanosecs)
$(1 + I_F/I_R)$
0
1
2
3
4
5
6
7
1
2
3
4
5
6

FIG. B-9

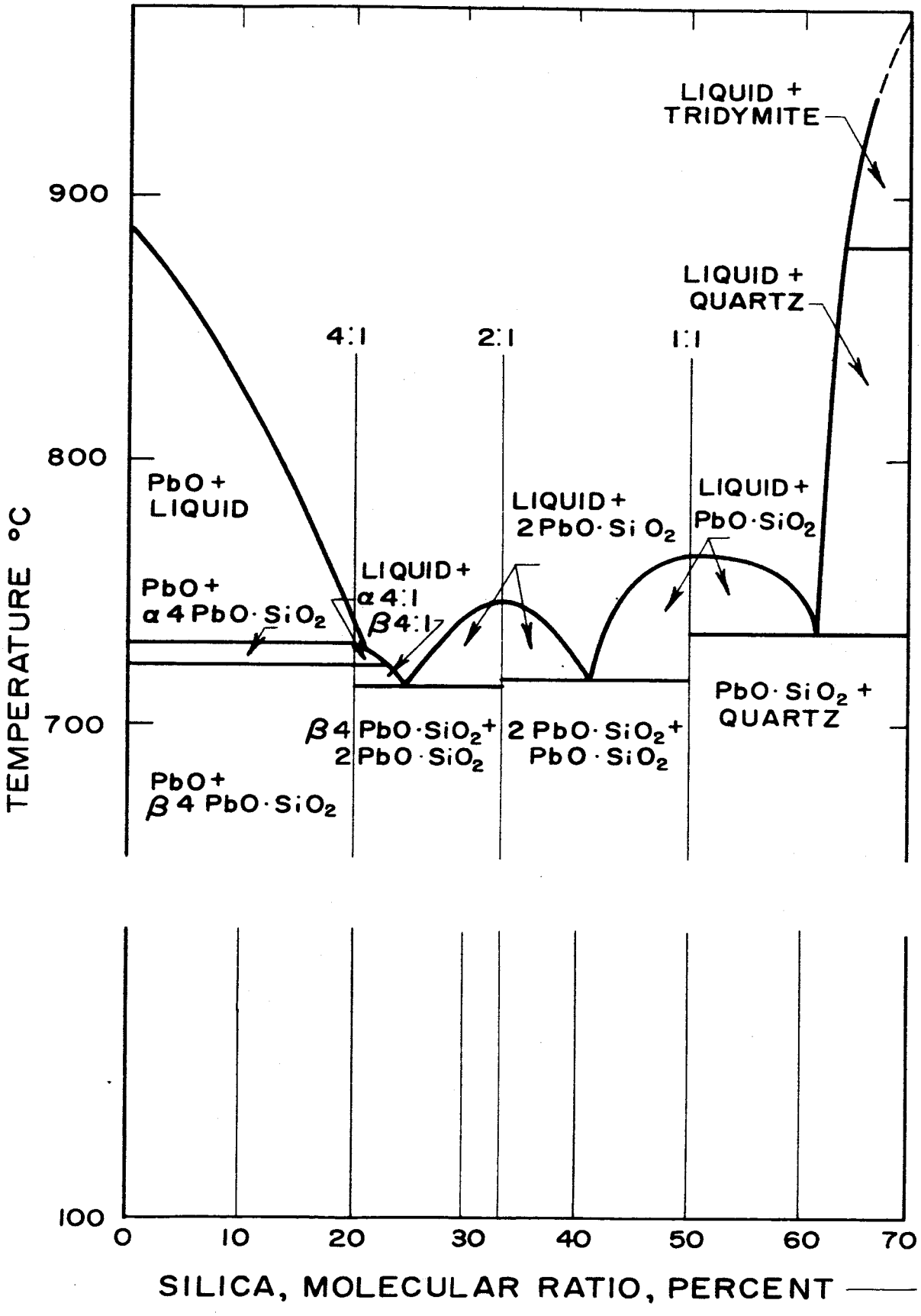

LIQUID +
TRIDYMITE
LIQUID +
QUARTZ
4:1
2:1
1:1
900
800
700
100
TEMPERATURE °C
PbO +
LIQUID
PbO +
α 4 PbO · SiO2
LIQUID +
α 4:1
β 4:1
LIQUID +
2 PbO · SiO2
LIQUID +
PbO · SiO2
PbO · SiO2 +
QUARTZ
β 4 PbO · SiO2 +
2 PbO · SiO2
2 PbO · SiO2 +
PbO · SiO2
PbO +
β 4 PbO · SiO2
0
10
20
30
40
50
60
70
SILICA, MOLECULAR RATIO, PERCENT

FIG. C-1

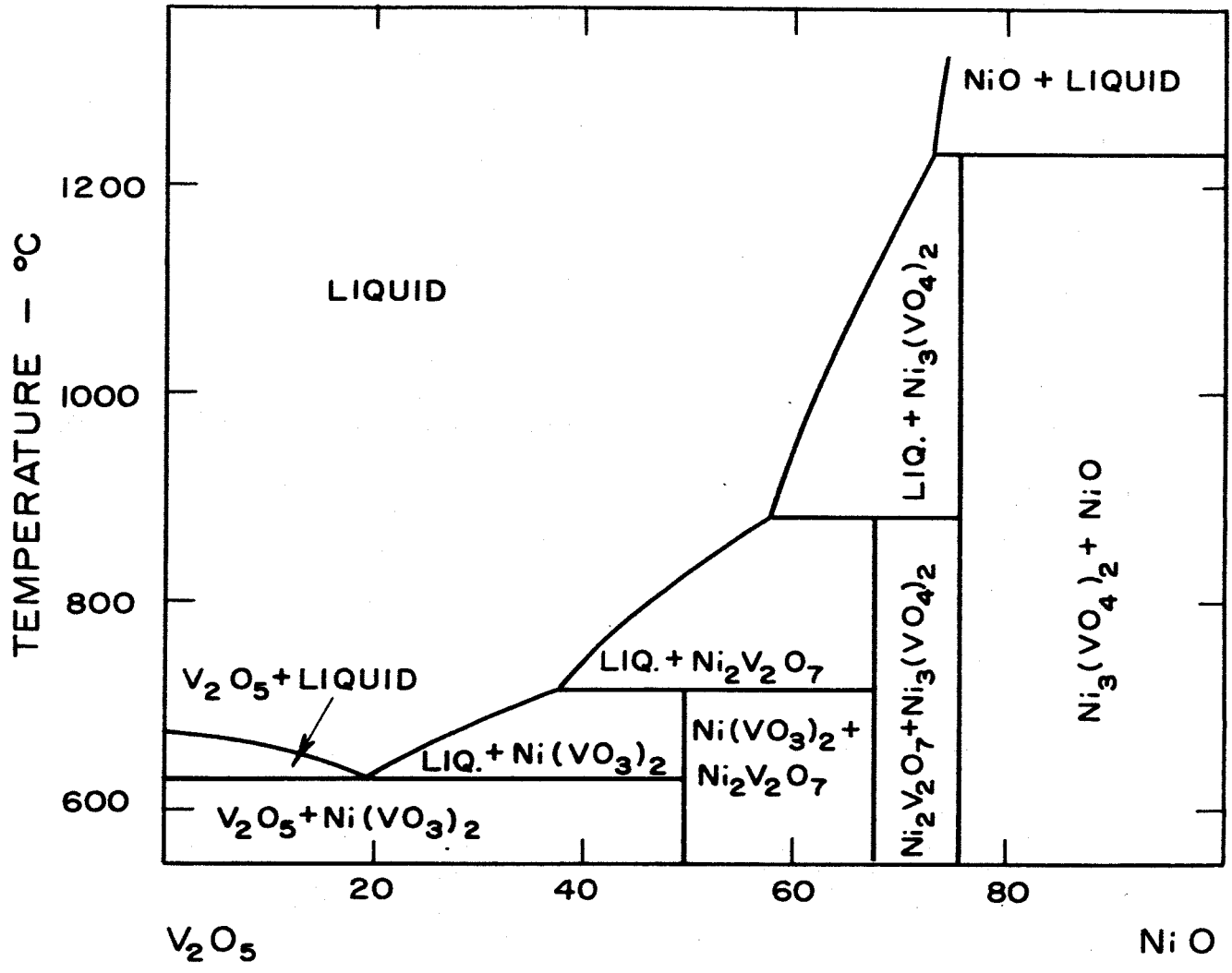

NiO + LIQUID
LIQUID
LIQ. + $Ni_3(VO_4)_2$
$Ni_3(VO_4)_2$ + NiO
LIQ. + $Ni_2V_2O_7$
V_2O_5 + LIQUID
LIQ. + $Ni(VO_3)_2$
$Ni(VO_3)_2$ + $Ni_2V_2O_7$
$Ni_2V_2O_7$ + $Ni_3(VO_4)_2$
V_2O_5 + $Ni(VO_3)_2$
TEMPERATURE – °C
1200
1000
800
600
20
40
60
80
V_2O_5
NiO

FIG. C-2

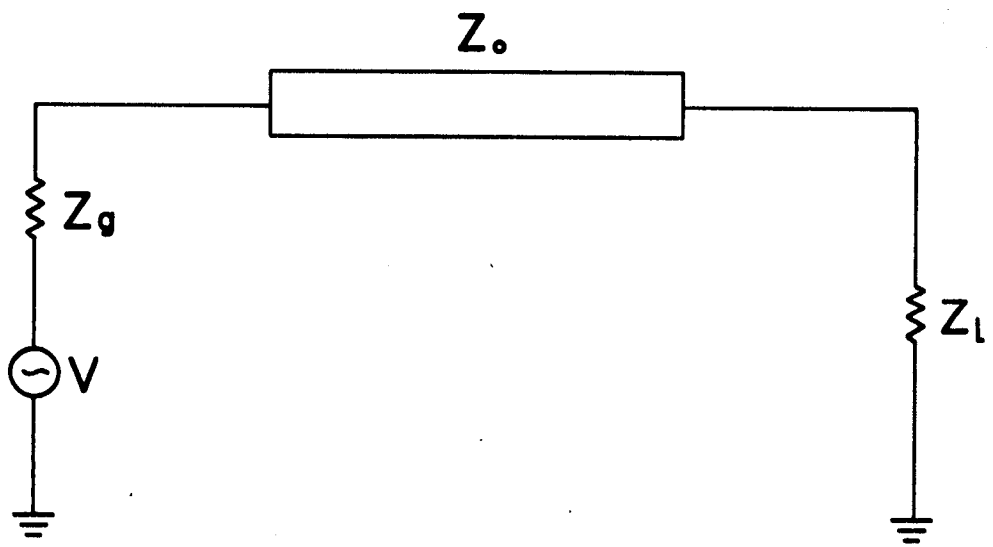


FIG. D-1

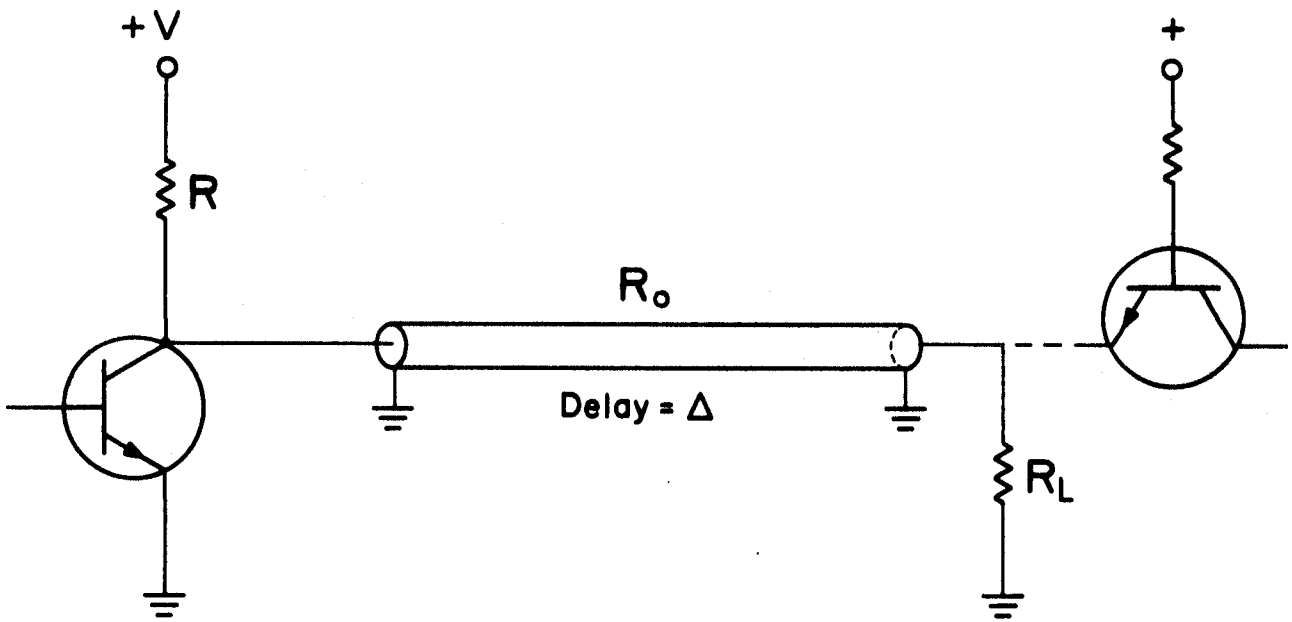


FIG. D-2

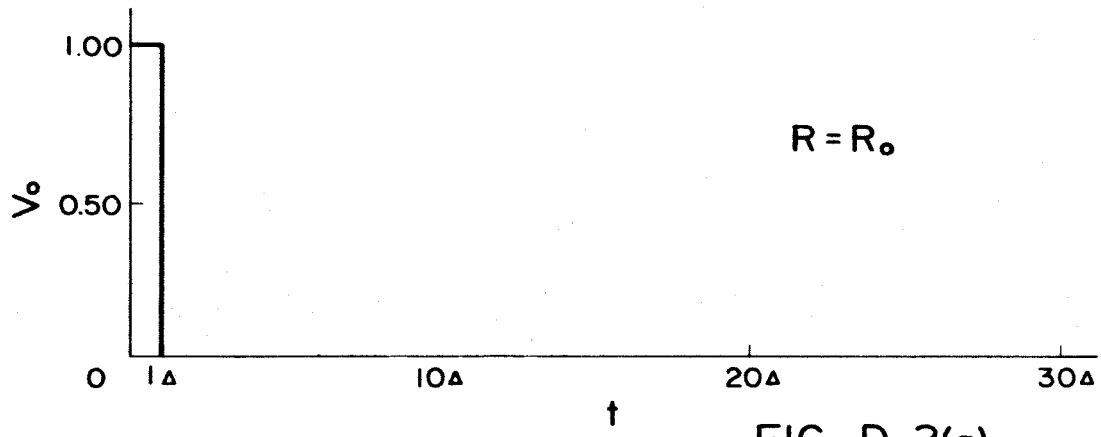


FIG. D-3(a)

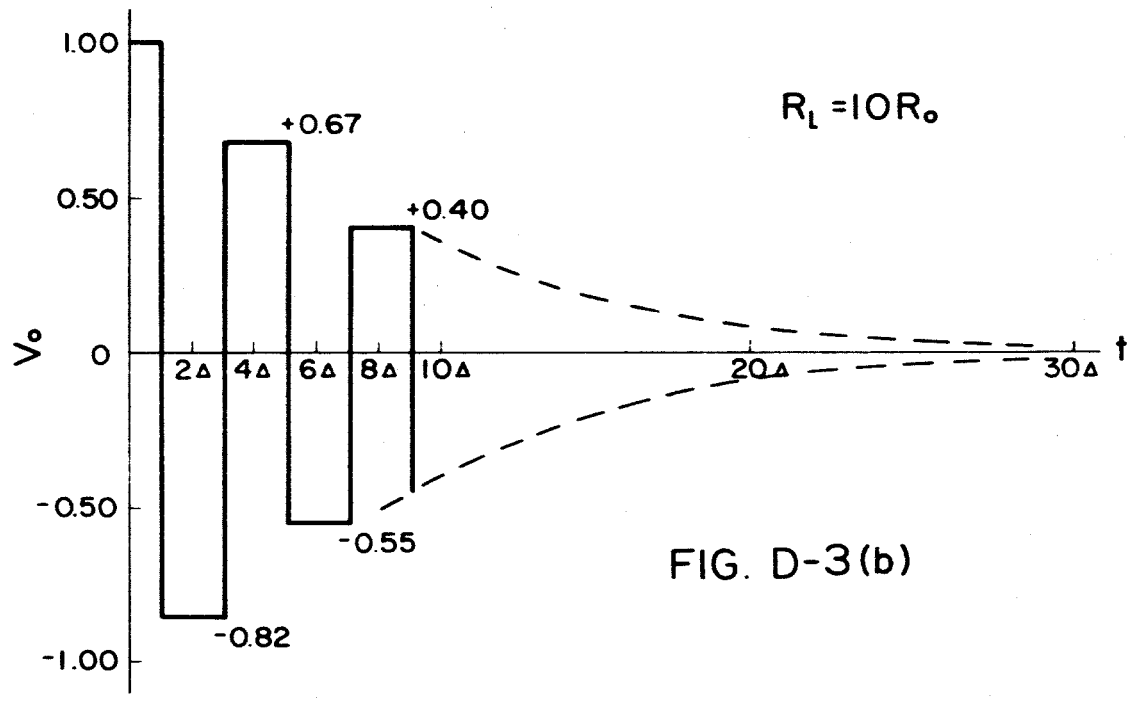


FIG. D-3(b)

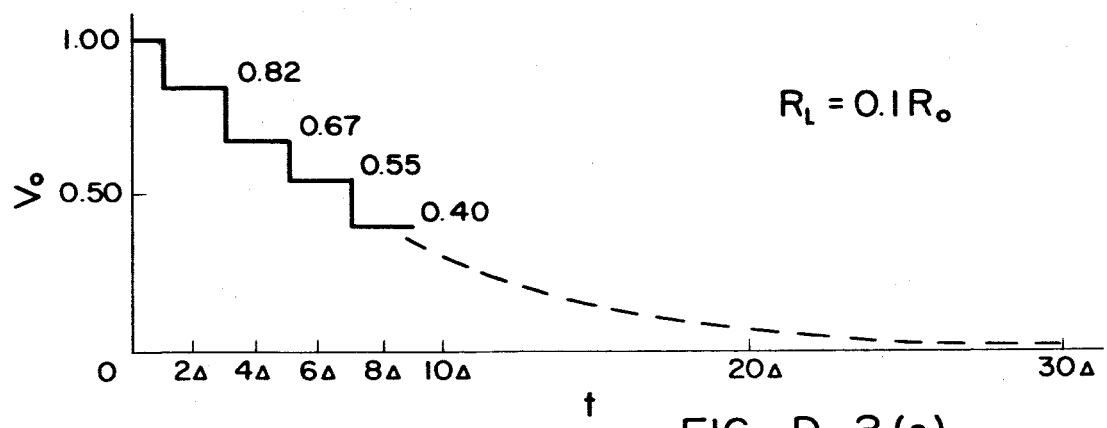


FIG. D-3(c)

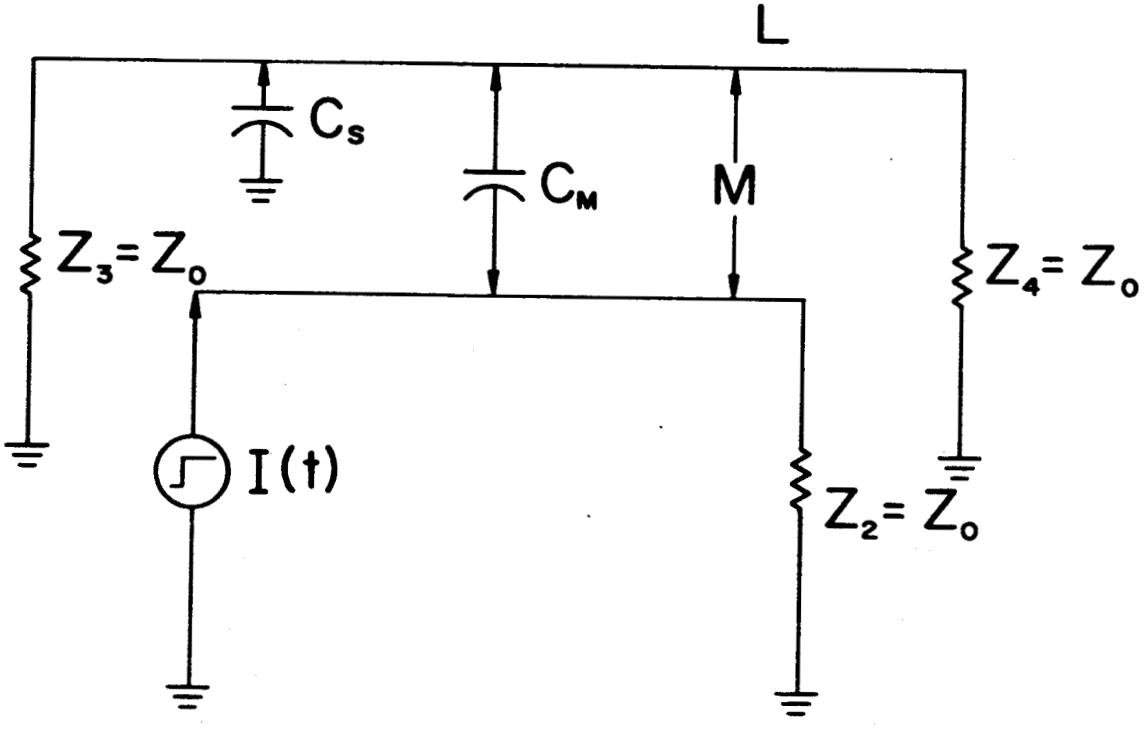


FIG. D-4

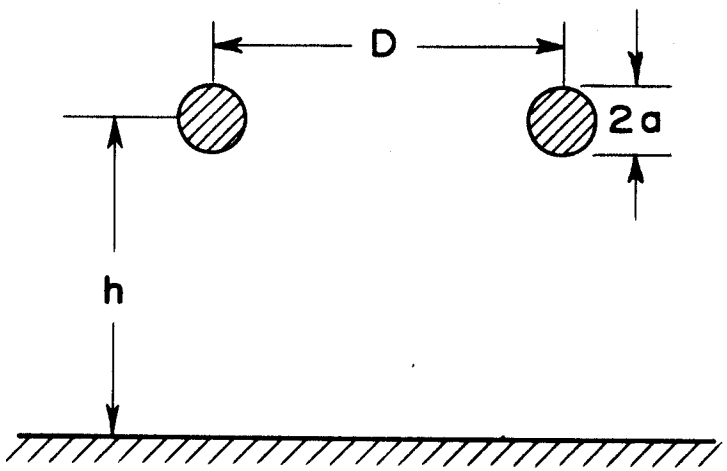


FIG. D-5

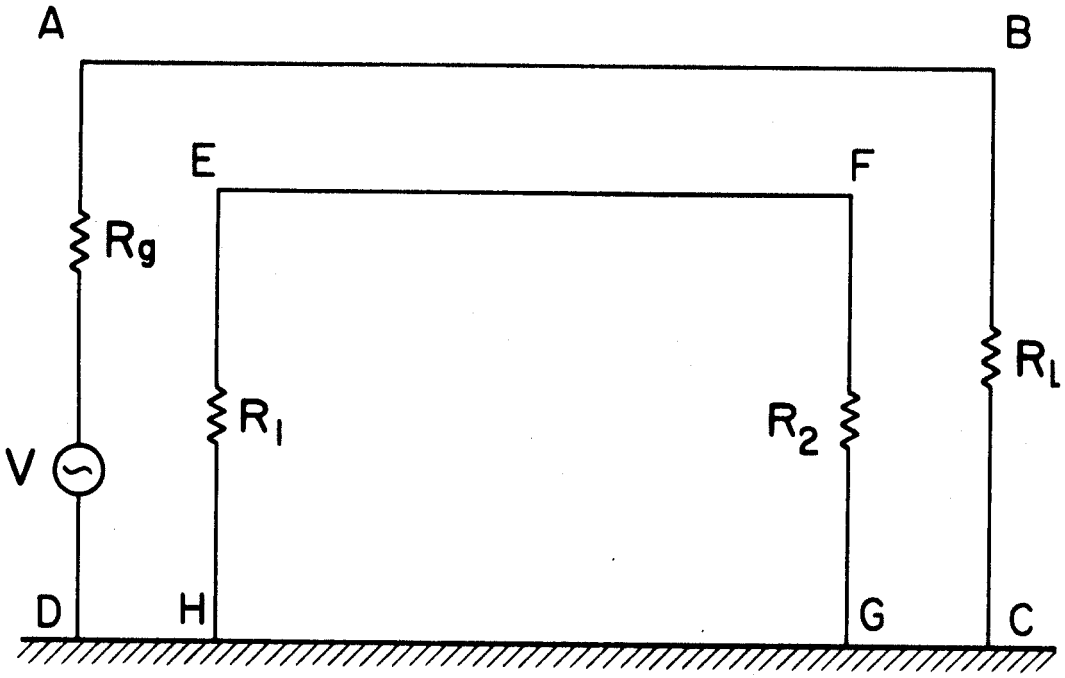


FIG. D-6

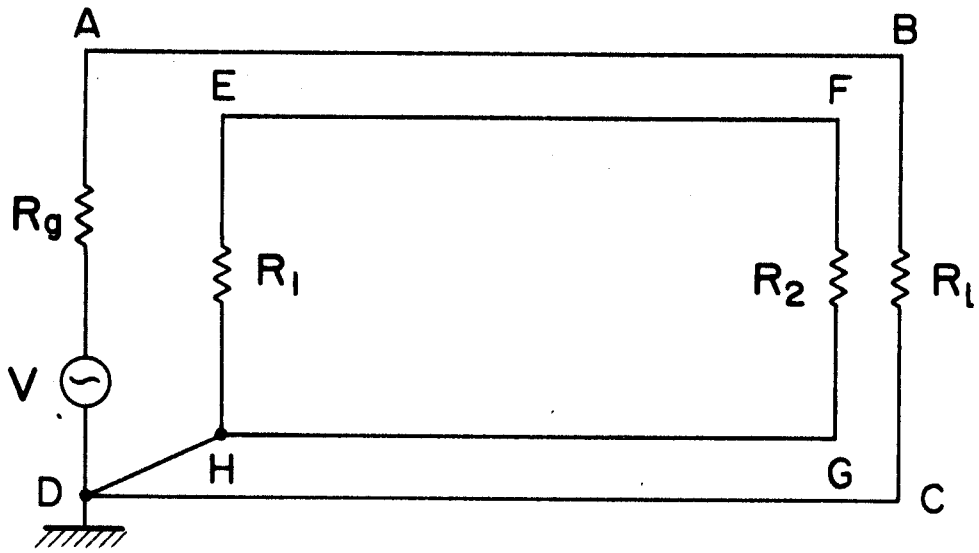


FIG. D-7

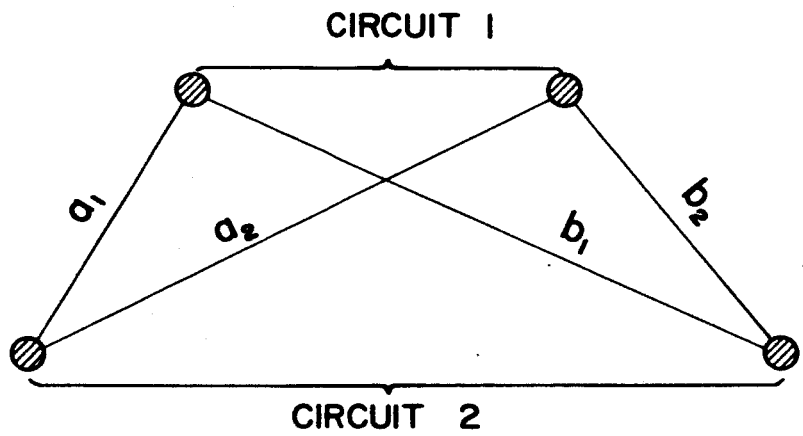


FIG. D-8

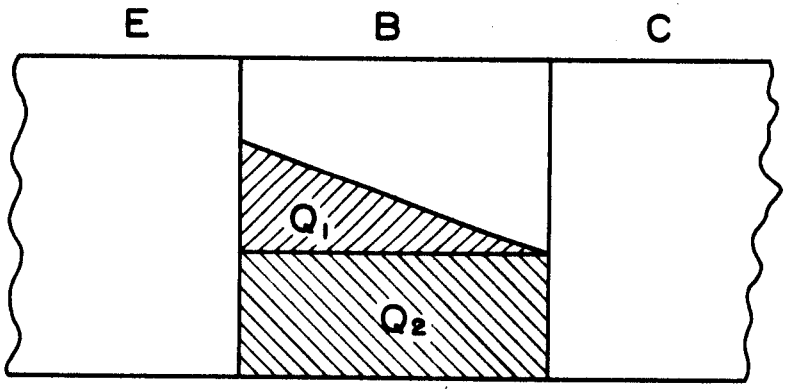


FIG. D-9

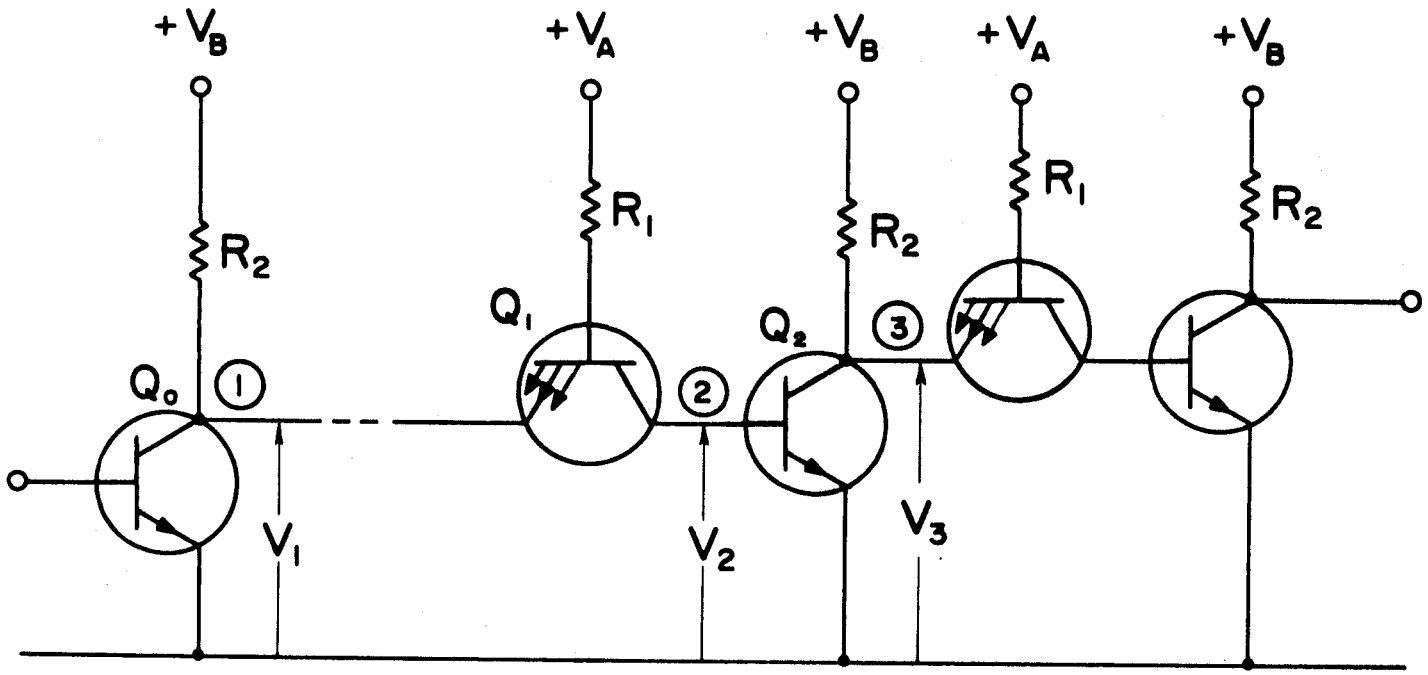


FIG. E-1

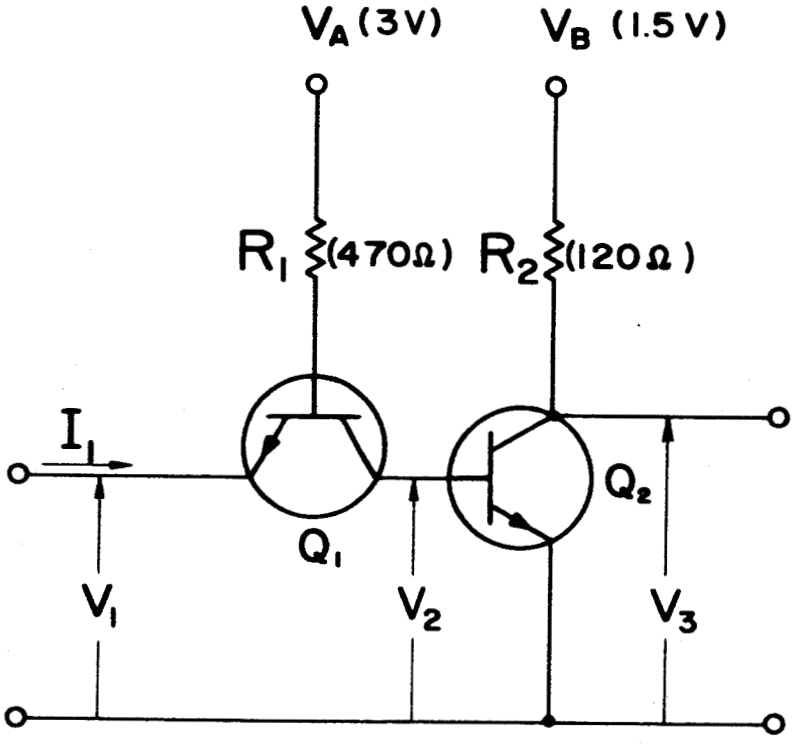


FIG. E-2

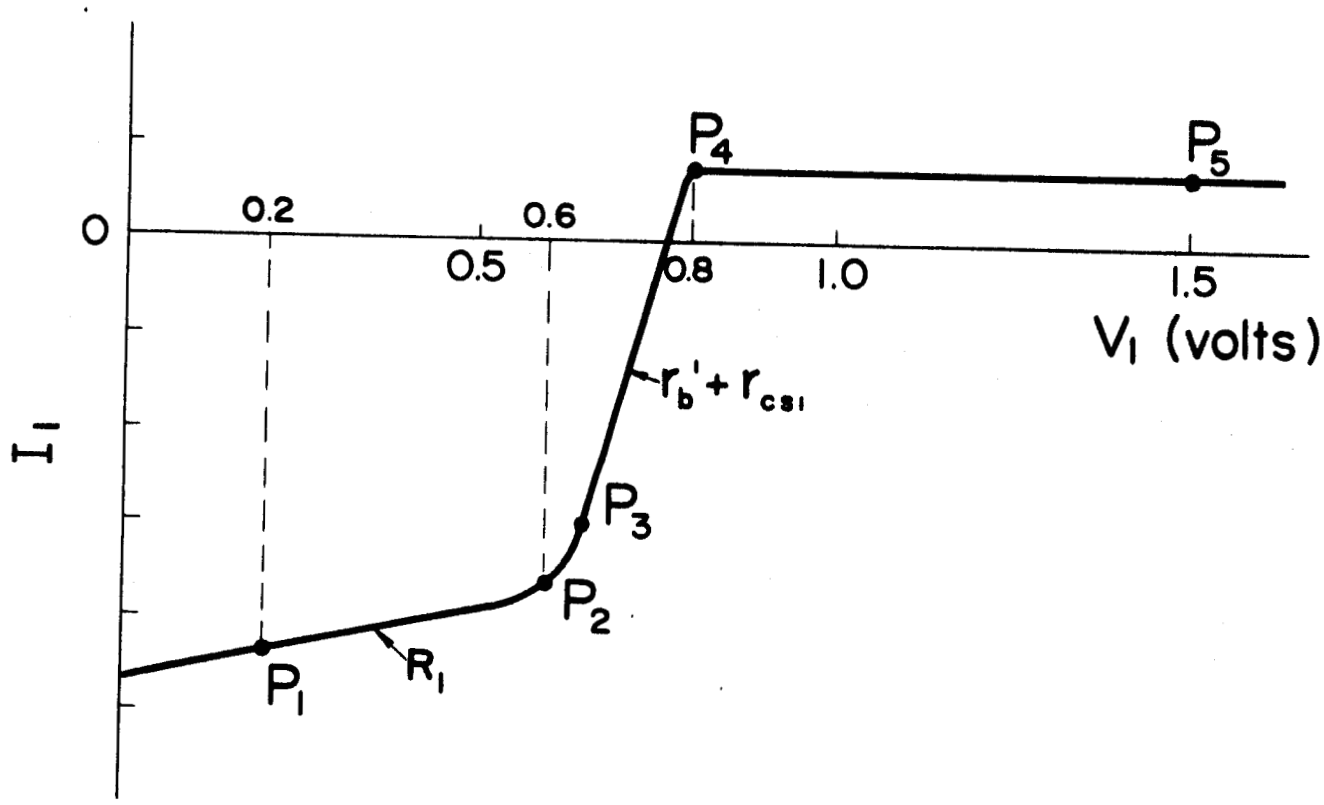


FIG. E-3

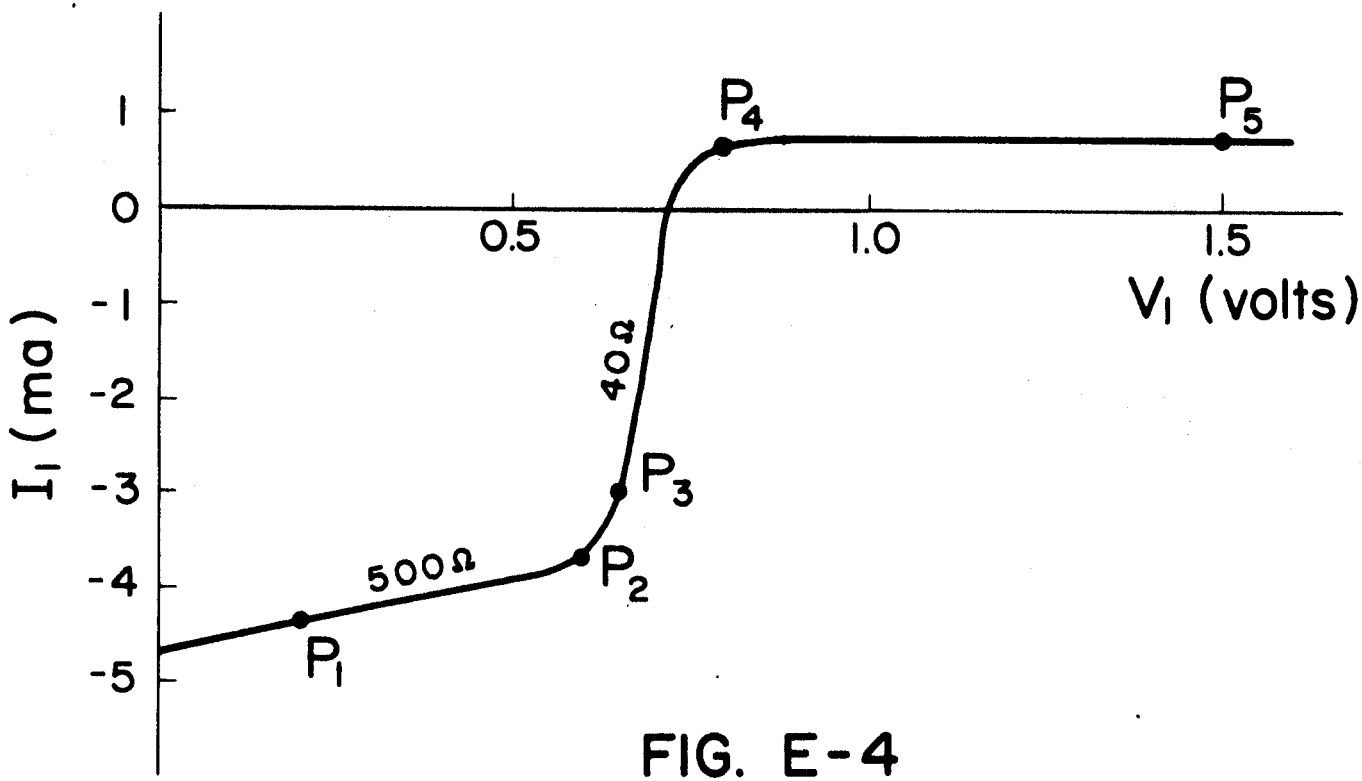


FIG. E-4

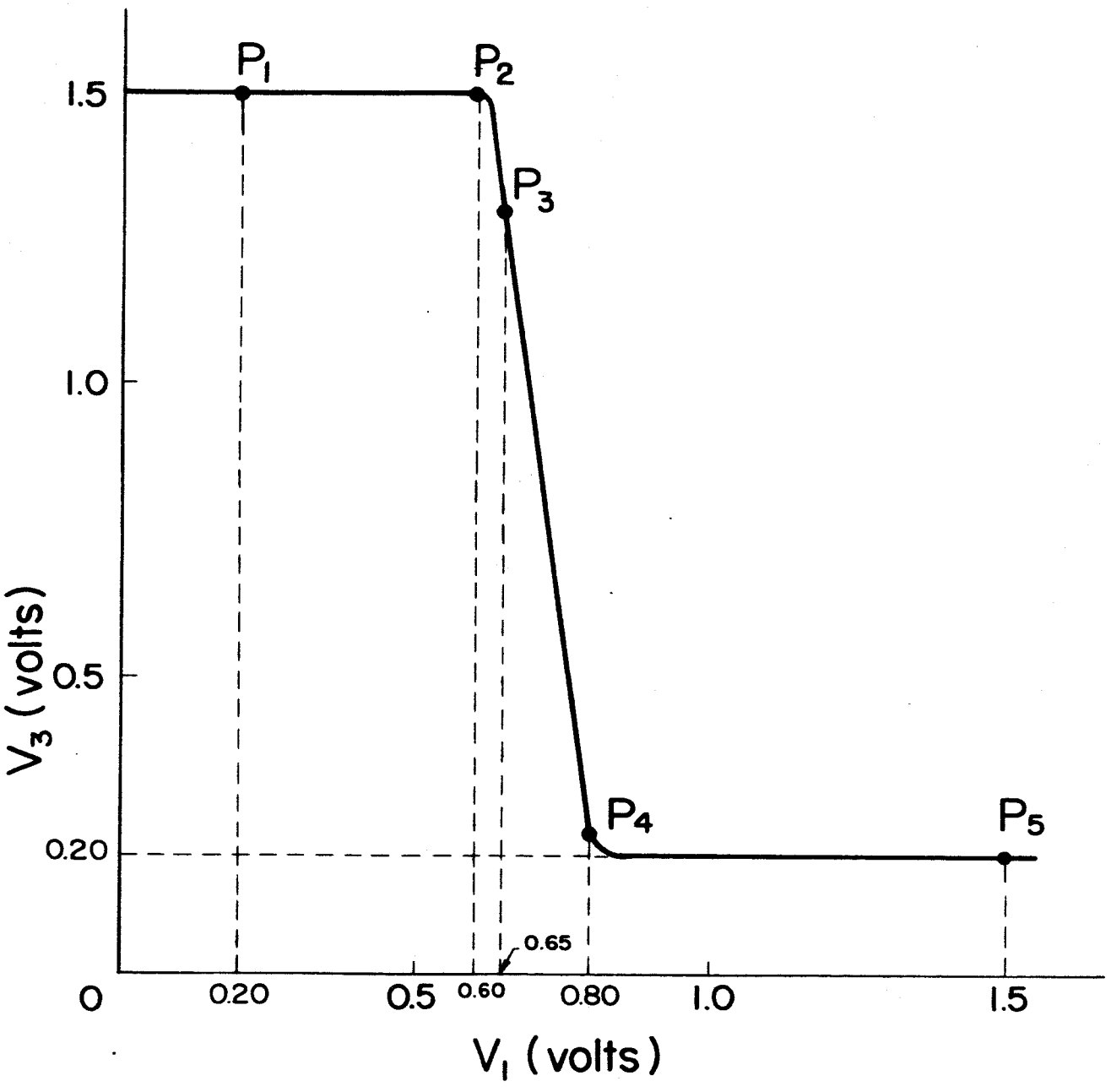

P1
P2
P3
P4
P5
1.5
1.0
0.5
0.20
0
0.20
0.5
0.60
0.65
0.80
1.0
1.5
V3 (volts)
V1 (volts)

FIG. E-5

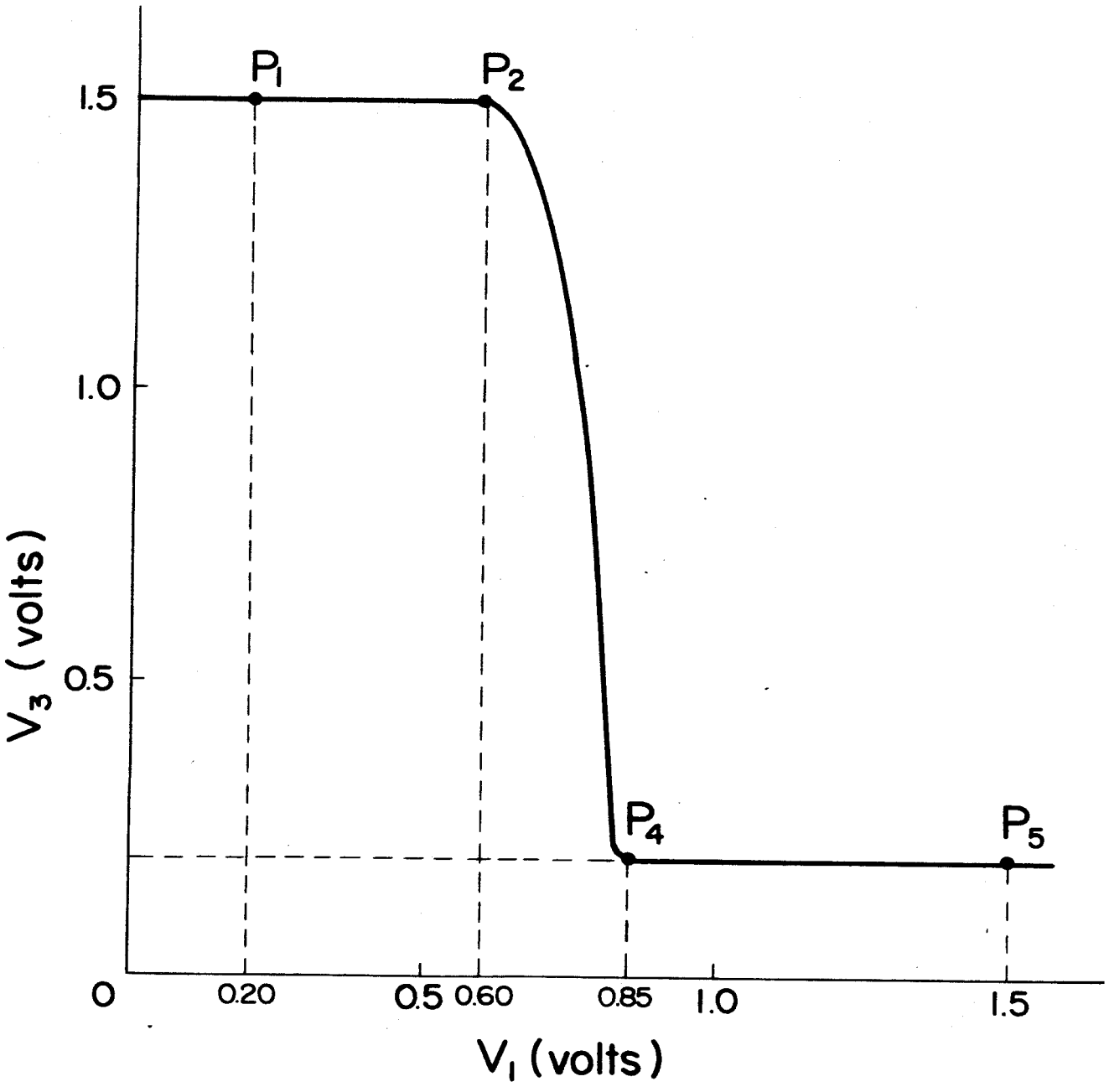


FIG. E-6

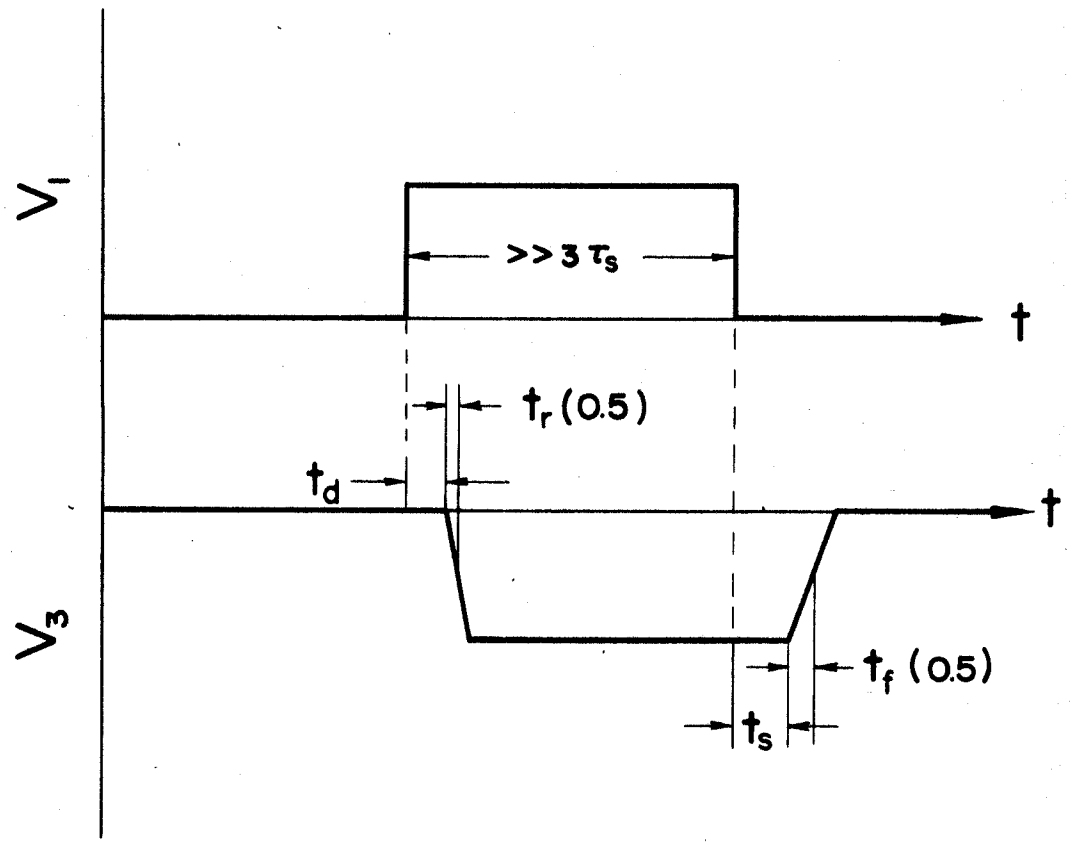


FIG. F-1

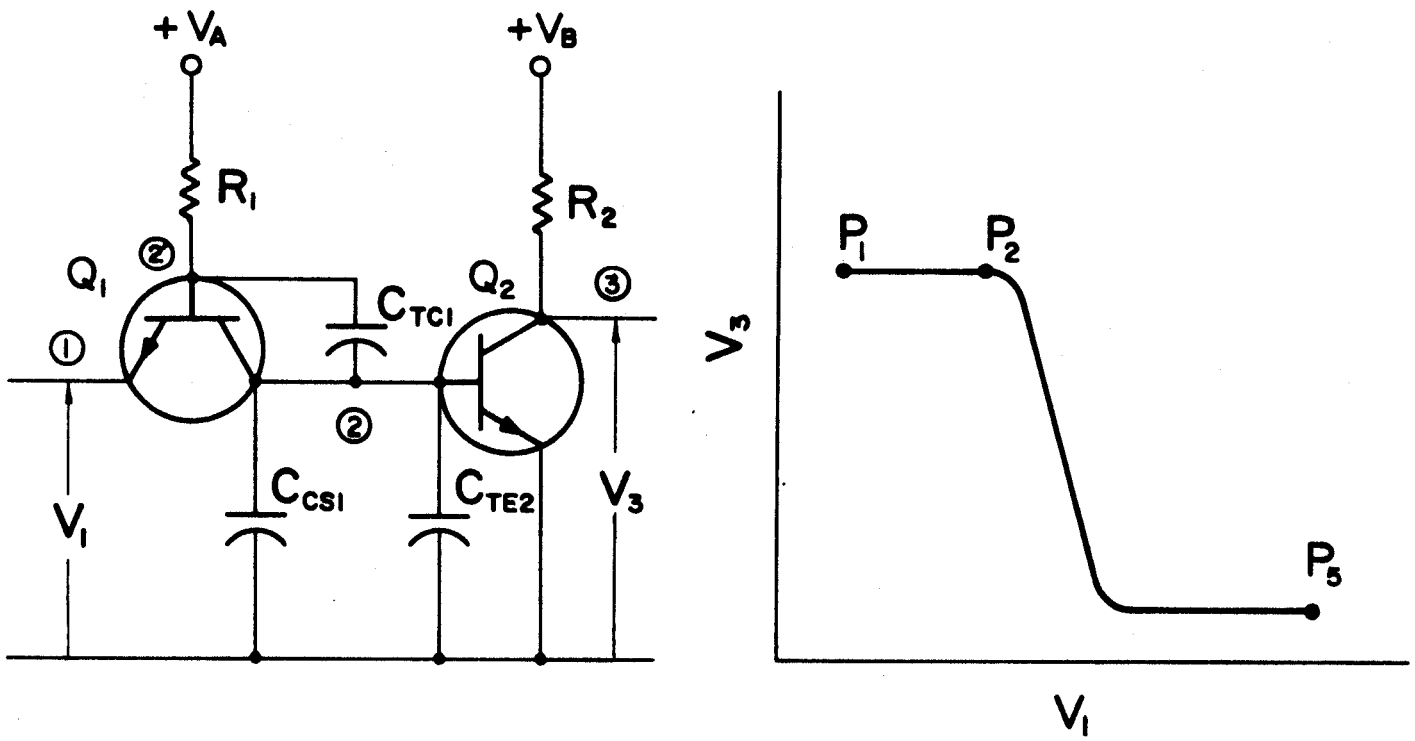


FIG. F-2

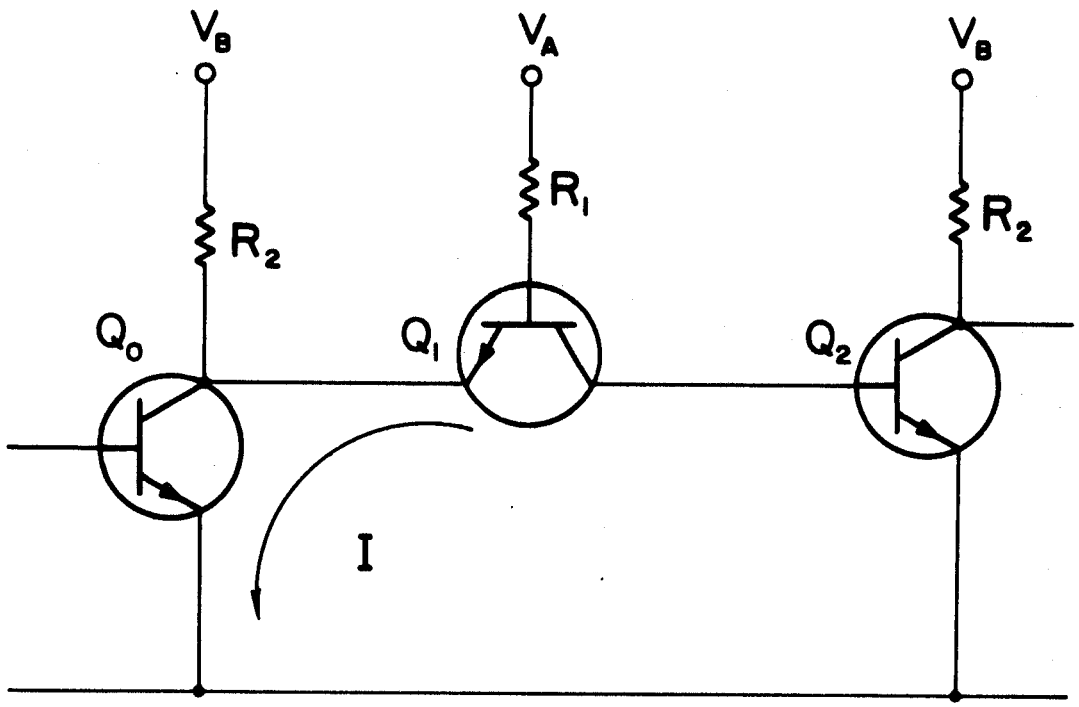


FIG. F-3

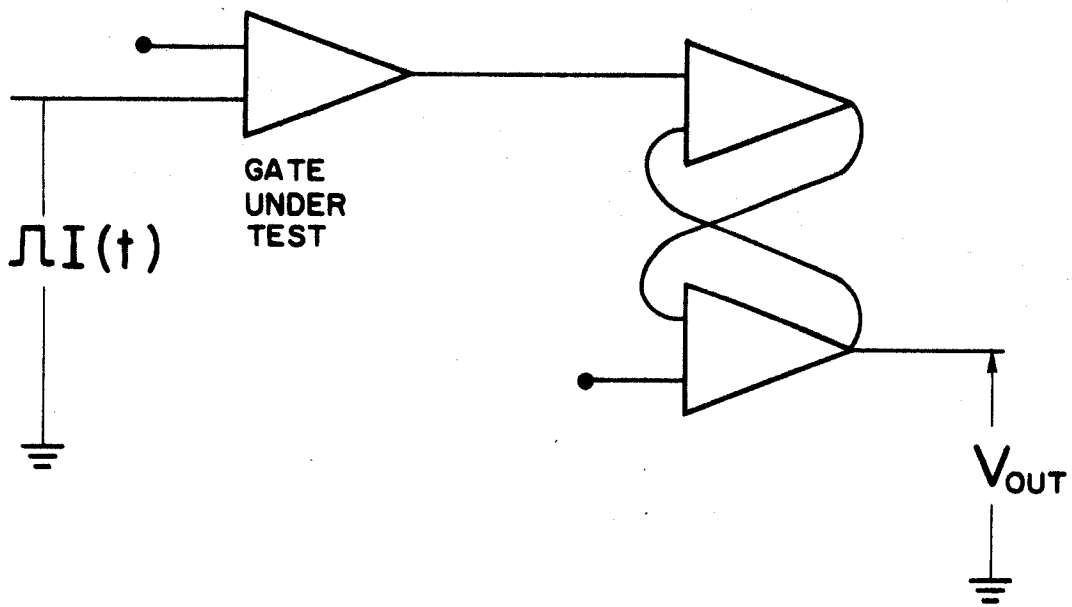


FIG. G-1

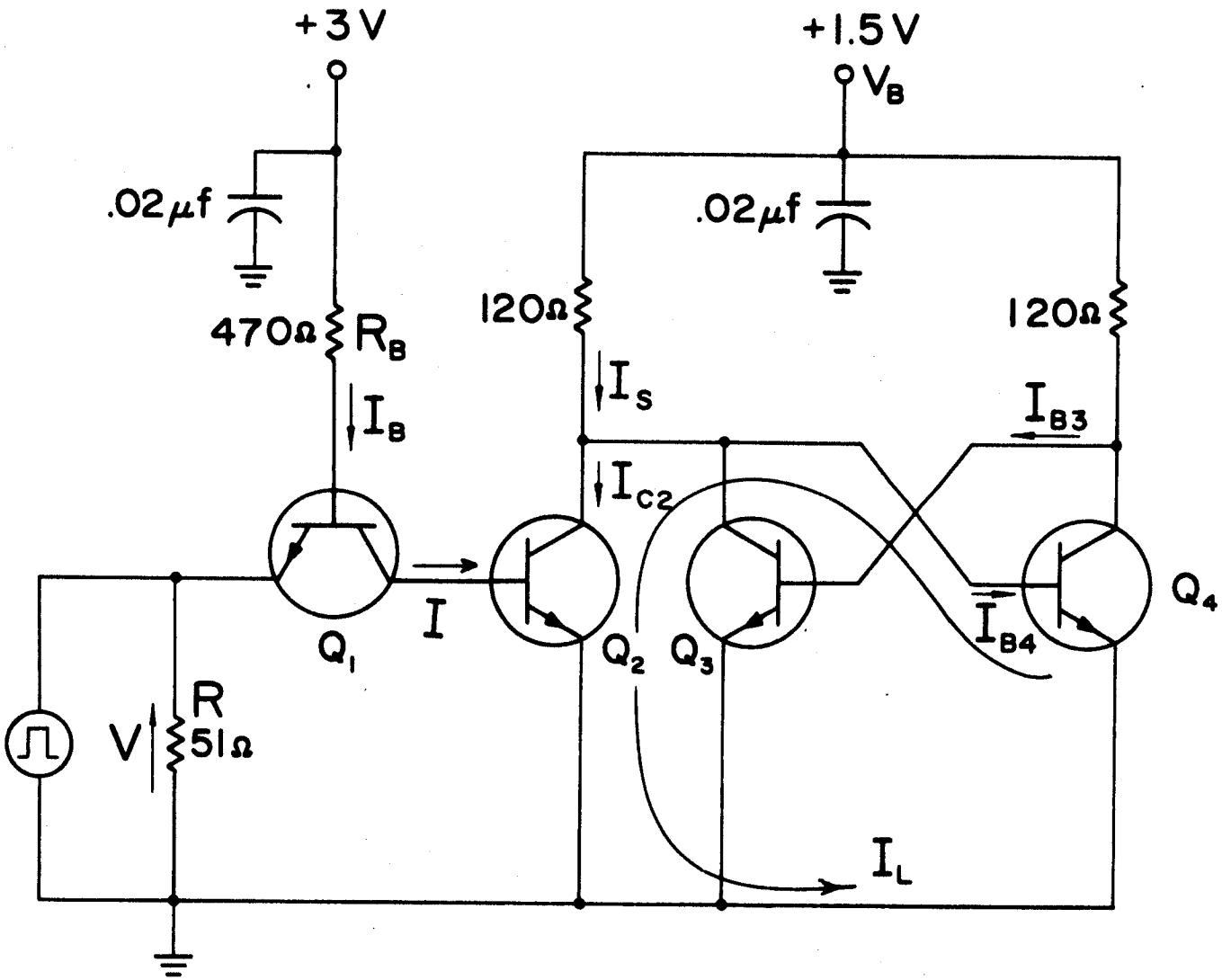

+3V
+1.5V
V_B
.02μf
.02μf
470Ω
R_B
I_B
120Ω
120Ω
I_S
I_{B3}
I_{C2}
Q_1
I
Q_2
Q_3
I_{B4}
Q_4
V
R
51Ω
I_L

FIG. G-2

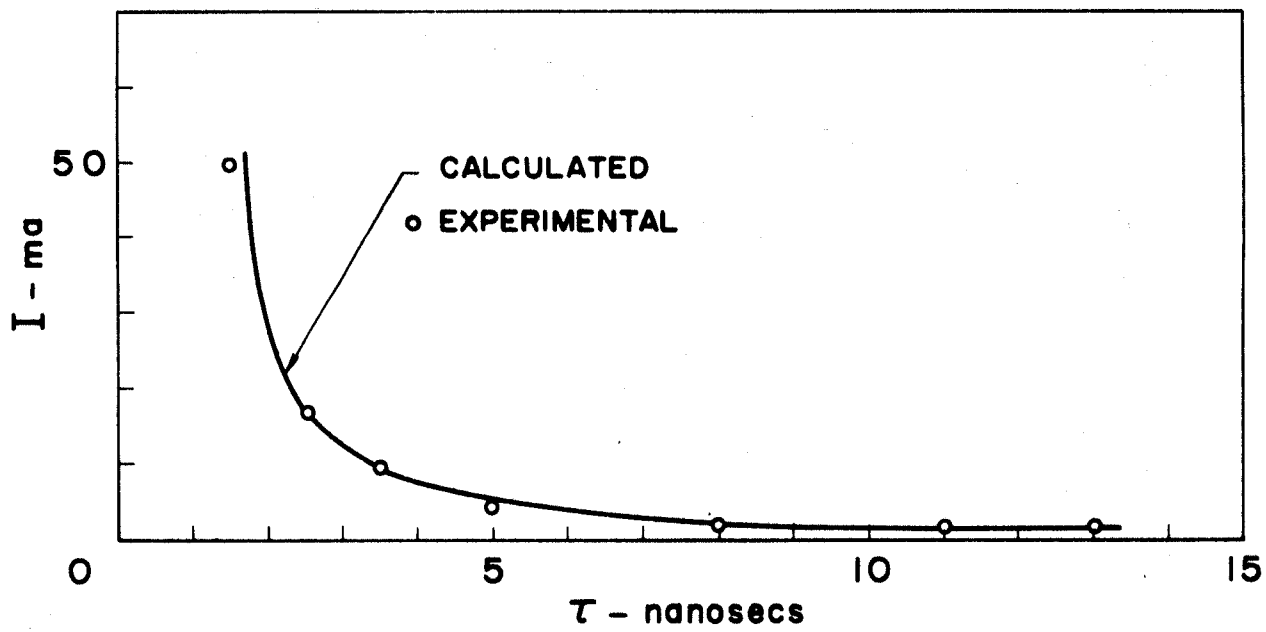


FIG. G-3

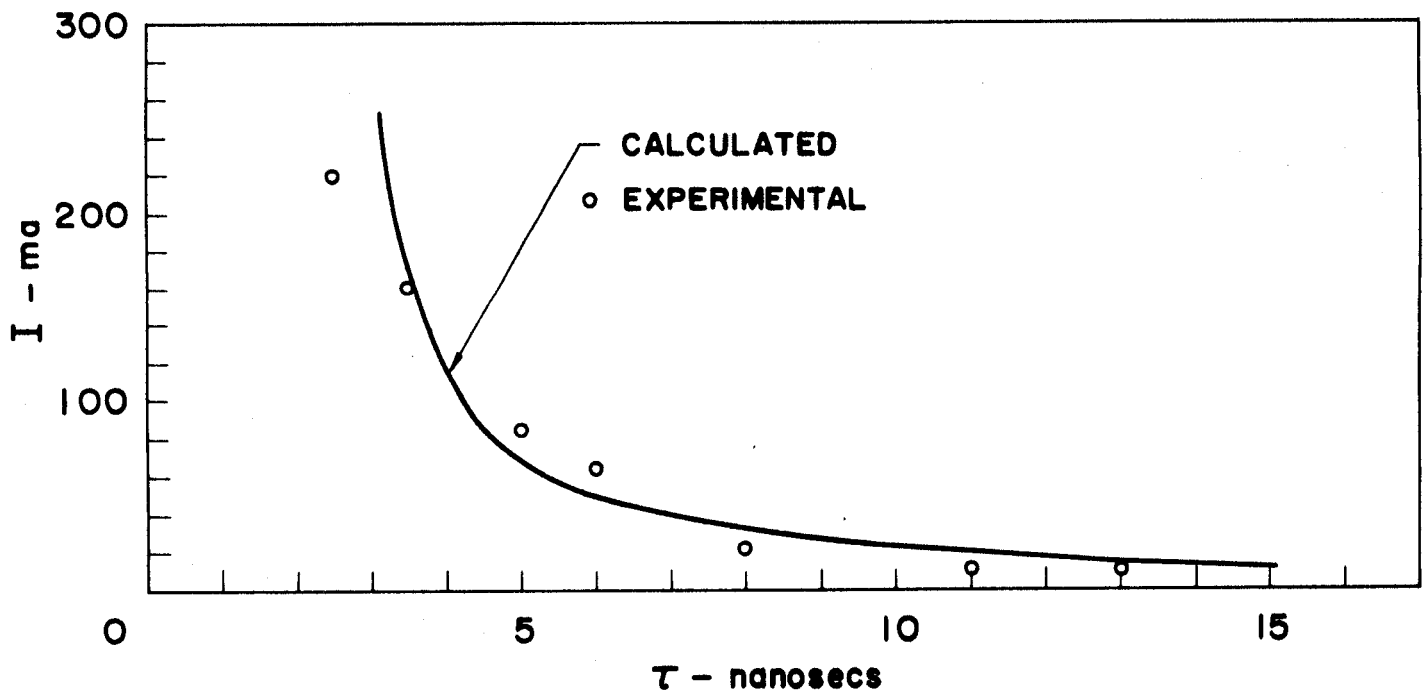


FIG. G-4

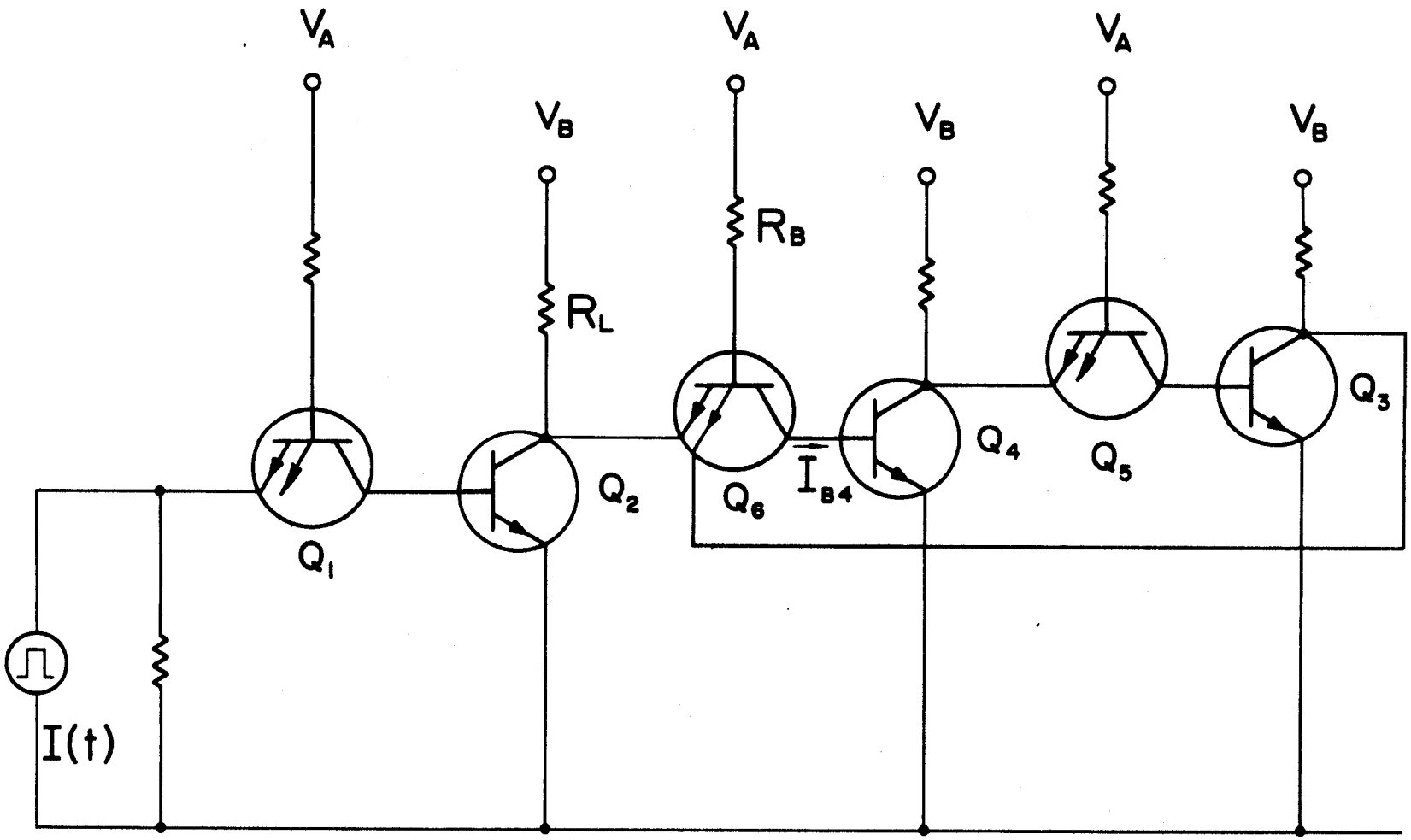


FIG. G-5

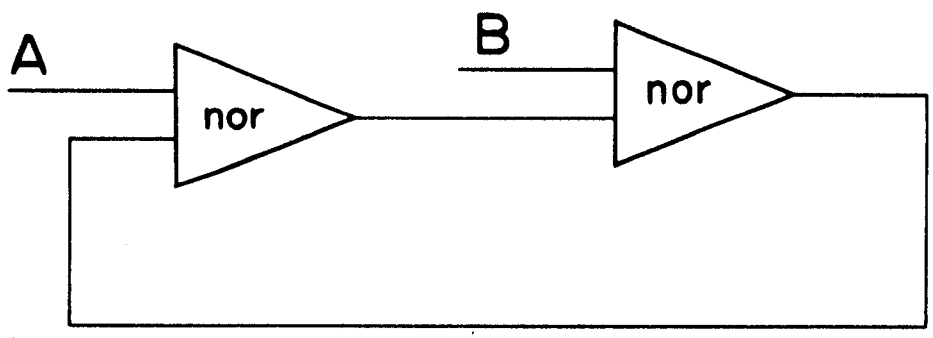


FIG. H-2

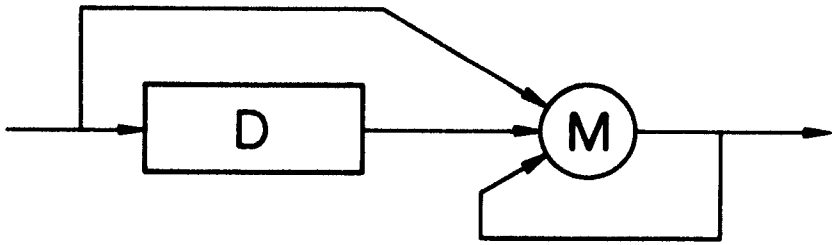
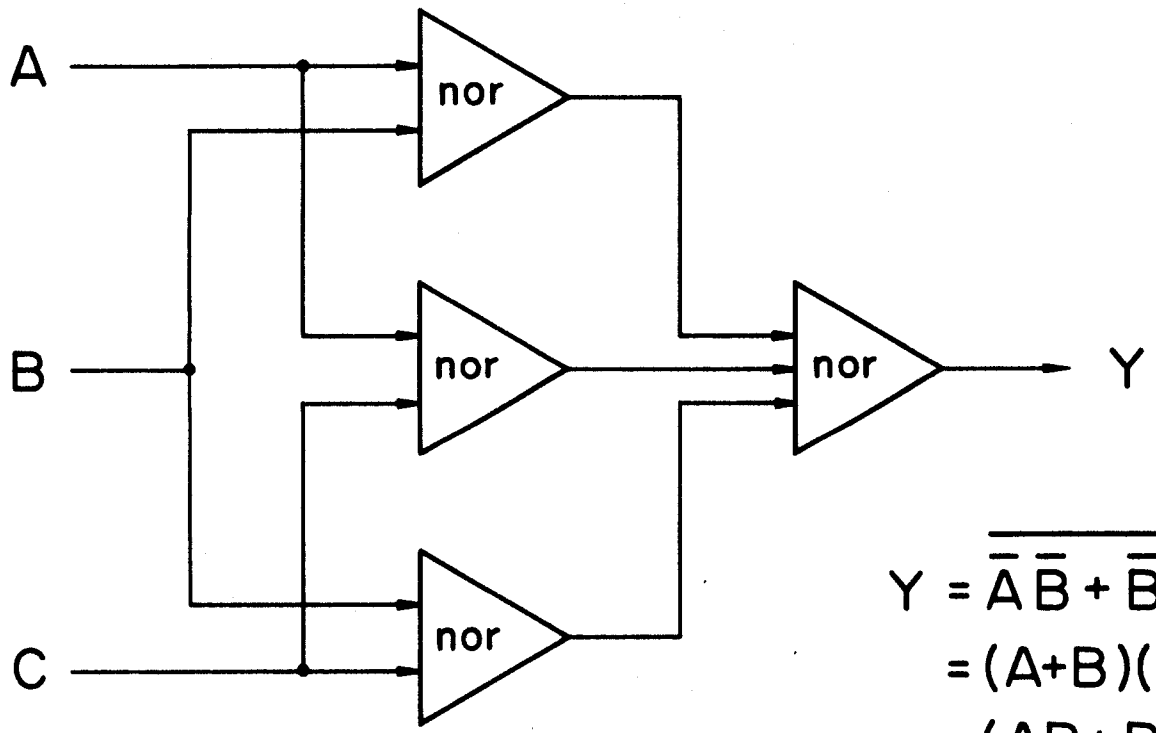


FIG. H-3



$$Y = \overline{\bar{A}\bar{B} + \bar{B}\bar{C} + \bar{A}\bar{C}}$$
$$= (A+B)(B+C)(A+C)$$
$$= (AB+B+AC+BC)(A+C)$$
$$= AB+AC+BC$$

FIG. H-4

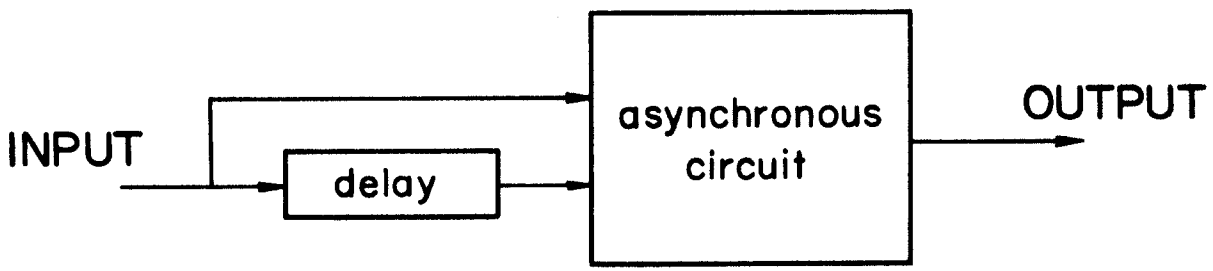


FIG. H-5

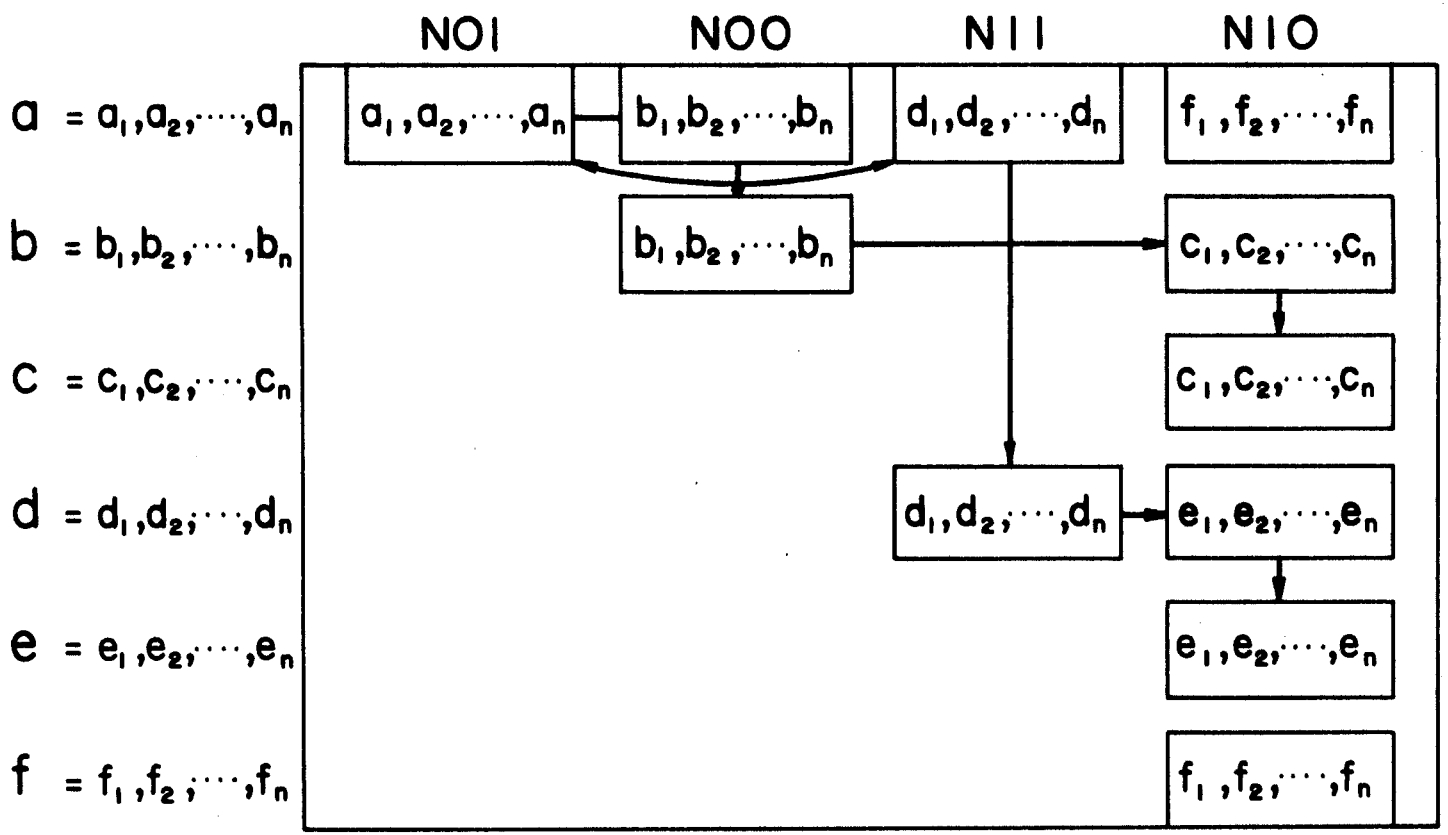

NOI
NOO
NII
NIO
a = a1,a2,···,an
b = b1,b2,···,bn
c = c1,c2,···,cn
d = d1,d2,···,dn
e = e1,e2,···,en
f = f1,f2,···,fn
a1,a2,···,an
b1,b2,···,bn
d1,d2,···,dn
f1,f2,···,fn
b1,b2,···,bn
c1,c2,···,cn
c1,c2,···,cn
d1,d2,···,dn
e1,e2,···,en
e1,e2,···,en
f1,f2,···,fn

FIG. 1-1

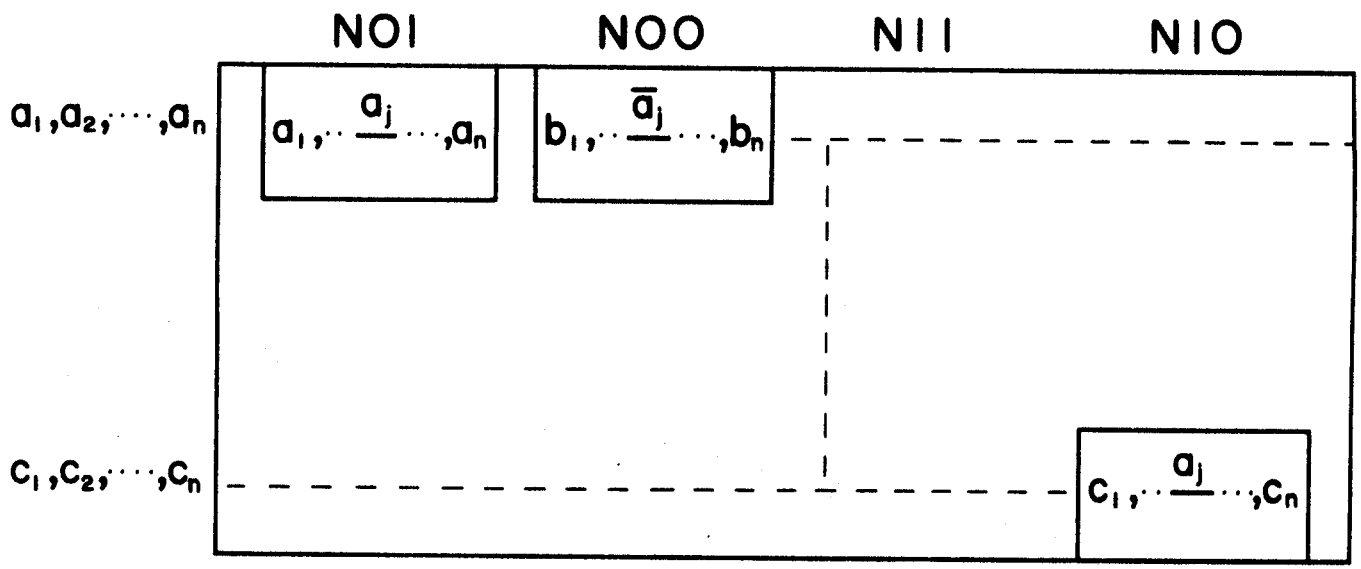


FIG. 1-2

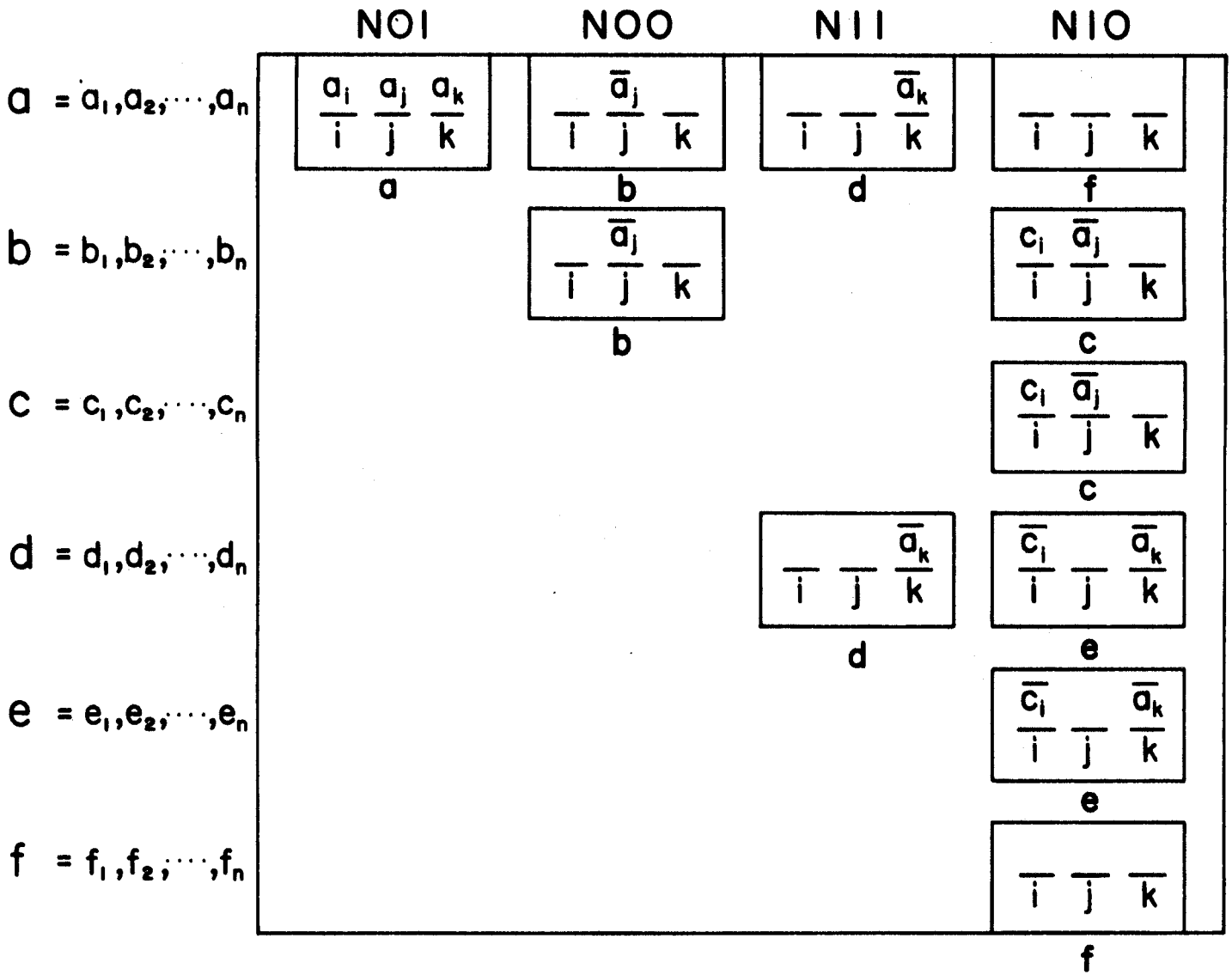

NOI
NOO
NII
NIO
a = a1,a2,···,an
b = b1,b2,···,bn
c = c1,c2,···,cn
d = d1,d2,···,dn
e = e1,e2,···,en
f = f1,f2,···,fn
ai aj ak
i j k
a
āj
i j k
b
āk
i j k
d
i j k
f
b
ci āj
i j k
c
c
ci āj
i j k
c
d
āk
i j k
d
ci āk
i j k
e
e
ci āk
i j k
e
i j k
f

FIG. 1-3

	NOI	NOO	NII	NIO
$a = a_1, a_2, \cdots, a_n$	$\frac{a_i}{i}\ \frac{a_j}{j}\ \frac{a_k}{k}$ a	$\frac{a_i}{i}\ \frac{\bar{a}_j}{j}\ \frac{a_k}{k}$ b	$\frac{a_i}{i}\ \frac{a_j}{j}\ \frac{\bar{a}_k}{k}$ d	$\frac{a_i}{i}\ \frac{\bar{a}_j}{j}\ \frac{\bar{a}_k}{k}$ f
$b = b_1, b_2, \cdots, b_n$		$\frac{a_i}{i}\ \frac{\bar{a}_j}{j}\ \frac{a_k}{k}$ b		$\frac{c_i}{i}\ \frac{\bar{a}_j}{j}\ \frac{\bar{a}_k}{k}$ c
$c = c_1, c_2, \cdots, c_n$				$\frac{c_i}{i}\ \frac{\bar{a}_j}{j}\ \frac{\bar{a}_k}{k}$ c
$d = d_1, d_2, \cdots, d_n$			$\frac{a_i}{i}\ \frac{a_j}{j}\ \frac{\bar{a}_k}{k}$ d	$\frac{\bar{c}_i}{i}\ \frac{\bar{a}_j}{j}\ \frac{\bar{a}_k}{k}$ e
$e = e_1, e_2, \cdots, e_n$				$\frac{\bar{c}_i}{i}\ \frac{\bar{a}_j}{j}\ \frac{\bar{a}_k}{k}$ e
$f = f_1, f_2, \cdots, f_n$				$\frac{a_i}{i}\ \frac{\bar{a}_j}{j}\ \frac{\bar{a}_k}{k}$ f

FIG. 1-4

NI_1I_2

	N_{00}	N_{01}	N_{11}	N_{10}
S_0	S_4	S_0	S_1	S_3
S_1	—	—	S_1	S_2
S_2	—	—	—	S_2
S_3	—	—	—	S_3
S_4	S_4	—	—	S_5
S_5	—	—	—	S_5

FIG. 1-5