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A STUDY ON THE EFFECTS OF Co^{60} γ-RADIATION ON STEAM-GROWN SiO_2 MOS STRUCTURES

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Theoretical and Experimental Studies of Radiation Induced Damage to Semiconductor Surfaces and the Effects of this Damage on Semiconductor Device Performance

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by

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ABSTRACT

MATTAUCH, ROBERT JOSEPH. A study on the effects of Co^{60} γ-radiation on the steam-grown SiO_2 MOS structures. (Under the direction of ROBERT WALTER LADE).

MOS capacitors were fabricated on both p- and n-type silicon substrates which had been thermally oxidized in a steam atmosphere. Capacitance-bias voltage curves were obtained with a measuring frequency of 100 kHz for both type devices.

Divice curve shift along the bias voltage axis yielded data from which it was deduced that the oxide charge moved by a diffusion mechanism. That charge was found to be positive and have an activation energy very near that of sodium in fused silica.

Exposure of the devices to a gamma ray flux from a Co^{60} source had the effects of both shifting the device curves along the voltage axis and decreasing the slope of those curves. A surface state density determination technique was employed and it was learned that the exposure of 3.6×10^6 roentgens caused the density of charges located at the oxide-semiconductor interface to increase from $10^{11} cm^{-2} eV^{-1}$ by an order of magnitude.

It was learned from Co^{60} irradiation and elevated temperature studies that the surface state density can be

decreased to its initial value but the oxide charge density is permanently decreased from approximately 10^{12} cm^{-2} to approximately $5 \times 10^{11} cm^{-2}$. A model based upon the Compton effect in the oxide is presented to explain the noted oxide charge change.

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1. INTRODUCTION

The metal-oxide-semiconductor (MOS) configuration has become invaluable as a tool in the study of oxide and oxide-semiconductor interface properties. The metal-oxide-semiconductor transistor was first proposed by Lilienfeld (1928) and has since that time gained acceptance as an operational amplifying circuit element.

The device is a capacitor consisting of one metal plate and one semiconductor plate with a thin dielectric placed between the two and in intimate contact with each. A metal contact is made to each of two opposite sides of the semiconductor exterior to the capacitor region as is seen in Figure 1. A voltage applied between the metal and the semiconductor will cause either holes or electrons to be drawn to the oxide-semiconductor interface region of the semiconductor. Thus the conductivity of the silicon between the two metal contacts designated as a "source" and "drain" is a function of the metal-to-semiconductor bias magnitude and polarity.

The operation of this device is strongly dependent upon the properties of the region of the semiconductor directly adjacent to the oxide-semiconductor interface, the oxide, and also the interface itself. Hence, study of these properties and their dependence upon externally controllable parameters is necessary in understanding the operation and behavior of the MOS transistor. To this end the MOS capacitor has been

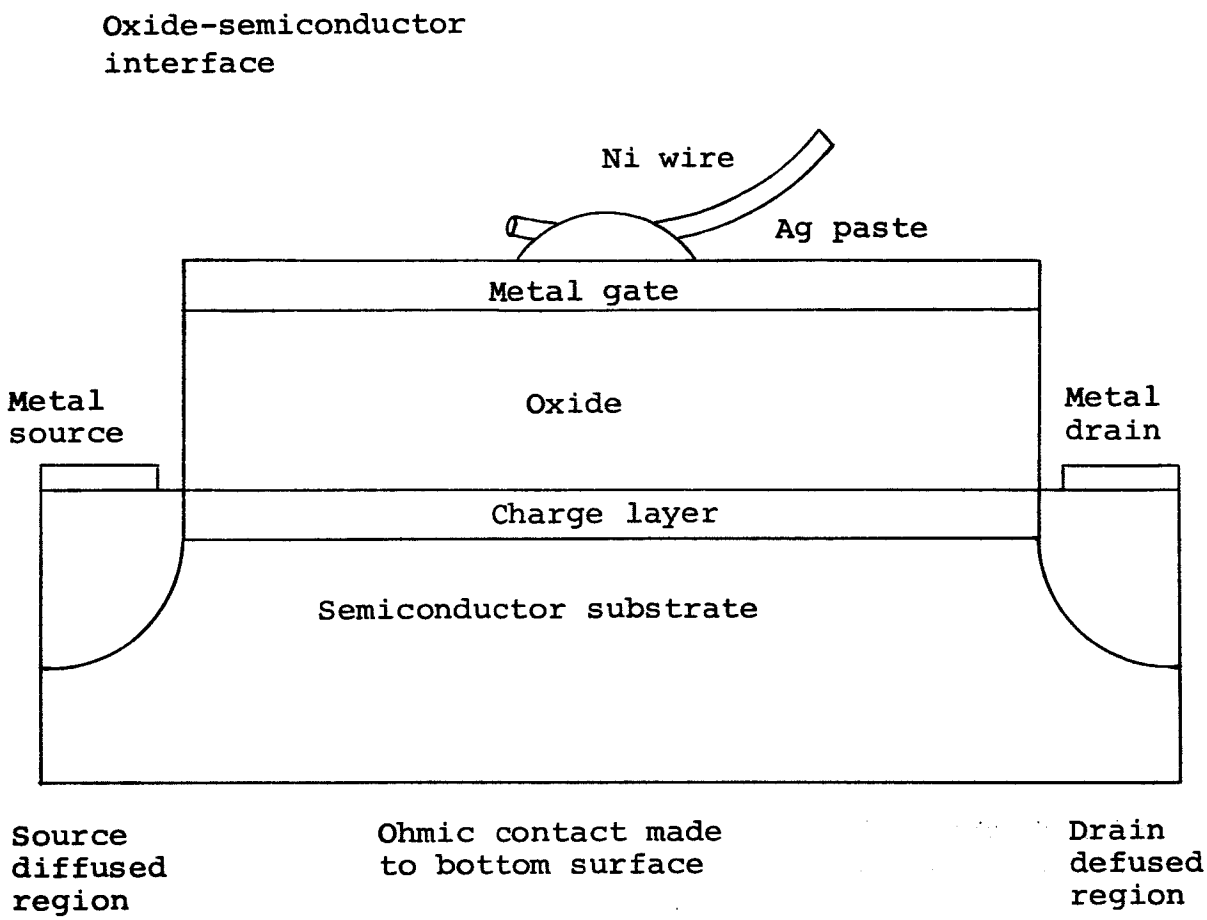


Figure 1.1. A typical MOS transistor Structure

used as a tool for such study. This capacitor (having the MOS configuration) is simply the MOS transistor with the source and drain contact delieted in fabrication.

It is impossible to fabricate this transistor or capacitor without causing a layer of charge to be located at the oxide-semiconductor interface. This is to be expected on the basis that a "clean" semiconductor surface is strongly p-type due to broken or "dangling" host atom bonds as discussed by Atalla et al. (1959). The polarity and concentration of the charge in this layer are factors of great importance in the operation of the MOS transistor.

Methods have been devised whereby this charge polarity and magnitude are determinable. These methods involve capacitance measurements as a function of metal-to-semiconductor bias voltage and will be discussed at length in Chapters 3 and 4 of this thesis.

The amount, polarity and distribution of charge located in the oxide dielectric are also strong factors in the operation of this transistor. Since fabrication techniques for this device involve oxide growth at a high temperature in either a wet oxygen or steam atmosphere any impurities such as alkali ions which are commonly found to some extent in even the purest water will act as impurities in the oxide. An oxide of the order of 1.0 micron in thickness containing a charge of 10^{12} cm^{-2} has a charge contamination of approximately 1.0 ppm as reported by Snow et al. (1965). If an oxide

is grown in a dry oxygen atmosphere at elevated temperatures hydrogen ions (protons) will be present in the oxide. A method of determining oxide charge polarity and change has been devised and will be discussed in detail in Chapter 4.

The purpose of this thesis is to determine the nature of the oxide charge, to determine both the pre- and post-Co^{60} gamma irradiation silicon surface state densities, and to determine the effect of such radiation on the oxide charge. These studies were carried out on MOS capacitors fabricated on both p- and n-type silicon. Device oxides were grown at elevated temperatures in a steam atmosphere. The externally observable capacitance as a function of bias voltage was used to determine the silicon surface charge density and also the changes in oxide charge density.

The nature of the oxide charge was determined by annealing studies at various temperatures. The change in the oxide charge density due to the gamma radiation is explained on the basis of neutralization of positive oxide charges by electrons which were freed by that radiation. A change in the silicon surface charge density due to the radiation is noted. It is determined, however, that the charge density can be returned to very nearly its original value by elevated temperature annealing under a bias potential.

2. LITERATURE REVIEW

2.1 Non Radiation

The existence of surface charge states on semiconductor materials was born out of the now classic field effect experiment performed by Shockley and Pearson (1948). The experimental configuration used by these authors was basically that of an MOS transistor which allowed them to monitor surface conductance as a function of an electric field applied normal to that surface. Kingston (1956) summed up rather thoroughly the work done on germanium up to 1955.

The dependence of the capacitance of the MOS structure upon bias was noted by Brown et al. (1956) but it was not until Atallia et al. (1959) developed an effective technique for growing a surface passivation oxide on silicon that a thermally grown oxide dielectric was feasible. Preliminary studies were carried out on the frequency dependence of the experimentally observable capacitance-bias voltage relations of the MOS capacitor by Lehovec et al. (1961), Terman (1962), Lehovec et al. (1963), Lehovec (1963), and Lehovec and Slobodskoy (1964).

The introduction of the silicon insulated-gate-field-effect transistor by Hofstein and Heiman (1963) essentially marked the beginning of silicon MOS studies on a large scale. Heiman (1964) developed a physical model for the MOS diode by extending the work of Rose (1963). Zaininger (1964) carried out experimental work on the determination of silicon

surface state density with respect to energy by investigating the depletion and accumulation portions of the observable capacitance-bias relations. Hofstein (1965) investigated the inversion region of the capacitance-bias curves for the silicon MOS diode and found that the first order, one dimensional equivalent circuit proposed by Lehovec and Slobodskoy (1964) did not explain two anomalies, thus a two dimensional model was proposed.

Outgrowths of these investigations were the development of a method for determining conductivity type from MOS capacitance measurements of Heiman et al. (1964) and information on hydrogen induced surface states at a Si-SiO_2 interface by Zaininger and Warfield (1964). Instability of MOS transistor operating characteristics led to the search of a SiO_2 stabilization technique. Kerr et al. (1964) reported on such a technique in which the oxide was doped with phosphorous. The success of this technique is believed dependent on the ability of the phosphorous to act as a getter for any positive space charge located in the oxide as reported by Kooi (1965b). Investigations into MOS instability by the study of oxide properties were carried out by Snow et al. (1965), Kooi (1965b), Whelan (1965), and Hofstein (1966).

2.2 Radiation

Szedon and Sandor (1965) irradiated MOS diodes with low energy (10-20-keV) electrons and noted not only a horizontal

shift but also a change in derivative of the experimental capacitance-bias curves. They attributed these changes to an increase in the number of surface states at the Si-SiO_2 interface. Mattauch and Lade (1965) reported the occurance of similar changes in the capacitance-bias characteristics caused by the irradiation of MOS diodes with 1.175 MeV gamma rays.

Kooi (1965a) investigated the influence of X-ray irradiation on the charge distribution in metal-oxide-semiconductor structures by means of the field effect experiment. This led to further studies by Kooi (1965c) in which the MOS structure was fabricated with and without a phosphate glass coating on the oxide dielectric. The devices were subjected to X-ray, gamma rays, and ultraviolet radiation. The ionizing effects of these exposures were detected in all cases by the field effect measurement and in a number of cases by capacitance-bias voltage measurements. It was noted that the radiation caused not only a change in the oxide charge density but also an increase in the density of charge located at the Si-SiO_2 interface. The latter effect was seen to be more pronounced on devices for which the oxide had been thermally grown in a wet ambient. Kooi (1965c) concluded by discussing a few possible relations between the SiO_2 structure and the observed effects.

Zaininger (1966) carried out an investigation of the effect of high energy electron radiation on MOS diodes and

concluded that the changes observed in surface stated density were caused for the most part by secondary electron emission from the Cr-Ag electrode situated upon the oxide.

The articles mentioned in the above literature review are those which the author feels present a complete background in the area of this thesis.

3. THE CALCULATION OF SURFACE STATE DENSITY

3.1 Device Structure, Band Diagram, and Equivalent Circuit

A theoretical treatment of the MOS structure is carried out in this chapter. The end product of this mathematical analysis is a method of calculating the density of surface charges located at the oxide-semiconductor interface by the use of experimentally obtainable capacitance-bias voltage relations.

The mathematical model which represents this device is based upon the assumptions that the oxide is perfectly insulating and that any effects due to space charge, tunnel currents, or polarized molecules are negligible. It is generally true that a small number of charges are distributed throughout oxides which have been fabricated by any of the present means, such as wet or dry thermal oxidation or anodic oxidation. If a voltage is applied across the device, causing an electric field in the oxide, it is a good assumption that any voltage drop due to the presence of such oxide charges is small with respect to the overall oxide voltage.

The potential band diagram of Figure 3.1 is applicable to the MOS structure with an externally applied voltage and the above assumptions invoked. The following potential expression results from Figure 3.1.

$$V = \phi_m + V_{ox} - x + \psi_s - \phi_f , \qquad (3.1)$$

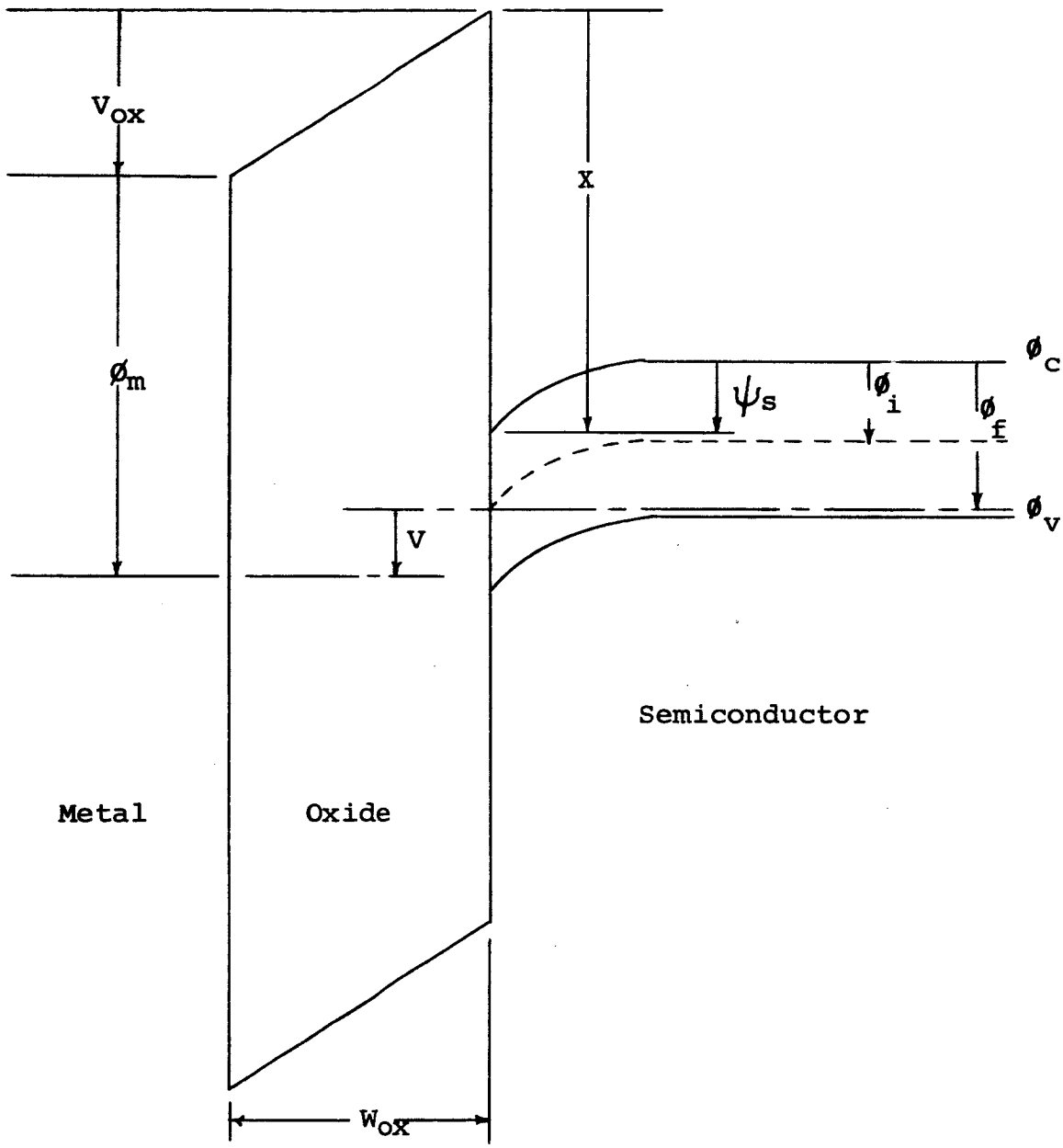


Figure 3.1. Potential band diagram for a p-type substrate MOS capacitor with an applied voltage, V

where V = voltage applied across the MOS device

ϕ_m = work function of the metal (volts)

V_{ox} = total voltage drop across the oxide

X = electron affinity of semiconductor (volts)

ψ_s = surface potential (volts

ϕ_f = potential difference between conduction band and Fermi level (volts)

ψ_i = intrinsic Fermi potential (volts)

ϕ_c = conduction band potential (volts)

ϕ_v = valance band potential (volts)

It is necessary for the following discussion of an equivalent circuit and also for the calculation of surface state density that the above listed oxide voltage be assumed to have a constant gradient throughout the oxide. Thus, even though space charge regions occur at both the metal-oxide and the oxide-semiconductor interfaces, the ratios of the oxide thickness to the extent of these space charge regions into the oxide is assumed much greater than unity. The assumption will also be made that there exists no work function difference between the metal and the semiconductor. Thus

$$\phi_m - x - \phi_f = 0, \tag{3.2}$$

and equation 3.1 becomes

$$V = V_{ox} + \psi_s . \tag{3.3}$$

This assumption will be discussed in more detail in chapter 5.

An applied voltage will cause the total metal (gate) charge counterpart to be distributed both in the semiconductor

near the surface and also at the oxide-semiconductor interface. Hence,

$$Q_t = Q_{ss} + Q_{sc} \tag{3.4}$$

where Q_{tot} is the charge on the gate, Q_{ss} is the charge located at the oxide-semiconductor interface, and Q_{sc} is the charge in the semiconductor. The total capacitance of the MOS structure is defined as

$$C = \frac{dQ_t}{dv} . \tag{3.5}$$

The following capacitance and potential definitions are also needed for the discussion of an equivalent circuit.

$$C_{ss} = \frac{dQ_{ss}}{d\psi_s} \tag{3.6}$$

$$C_{sc} = \frac{dQ_{sc}}{d\psi_s} \tag{3.7}$$

$$C_s = \frac{dQ_t}{d\psi_s} \tag{3.8}$$

$$C_{ox} = \frac{dQ_t}{dV_{ox}} \tag{3.9}$$

$$V_{ss} = \frac{Q_{ss}}{C_{ox}} \tag{3.10}$$

$$V_{sc} = \frac{Q_{sc}}{C_{ox}} \tag{3.11}$$

The following expression can also be written by the use of equations (3.4), (3.6), and (3.7),

$$C_s = C_{ss} + C_{sc} \cdot \tag{3.12}$$

This exhibits the fact that the surface state capacitance and the semiconductor capacitance act as though they are effectively in parallel.

The defining equation for the total capacitance between the gate and the semiconductor substrate, (3.5) may be expanded by the use of the chain rule as follows:

$$C = \frac{dQ_t}{dv} = \left(\frac{dQ_t}{d\psi_s}\right)\left(\frac{d\psi_s}{dv}\right) . \tag{3.13}$$

Equations (3.1), (3.8), and (3.9) allow one to reduce equation (3.13) to

$$C = \frac{C_s\ C_{ox}}{C_s + C_{ox}} . \tag{3.14}$$

This equation leads one to the conclusion that the C_s and C_{ox} are effectively in a series configuration. As Zaininger (1964) pointed out, care must be taken in viewing this series configuration in the usual circuit-element sense. Two distinct capacitors connected in a series circuit each have a distinct set of charges. In the case of the C_s and C_{ox} series configuration only one set of charges is present.

The above work, specifically equations (3.12) and (3.14), along with the realization that a resistance will exist between the semiconductor surface and the back contact, leads to the equivalent circuit shown in Figure 3.2 where R_{ox} is the leakage resistance from the gate to the semiconductor and R_B is the bulk resistance and the accumulation region resistance.

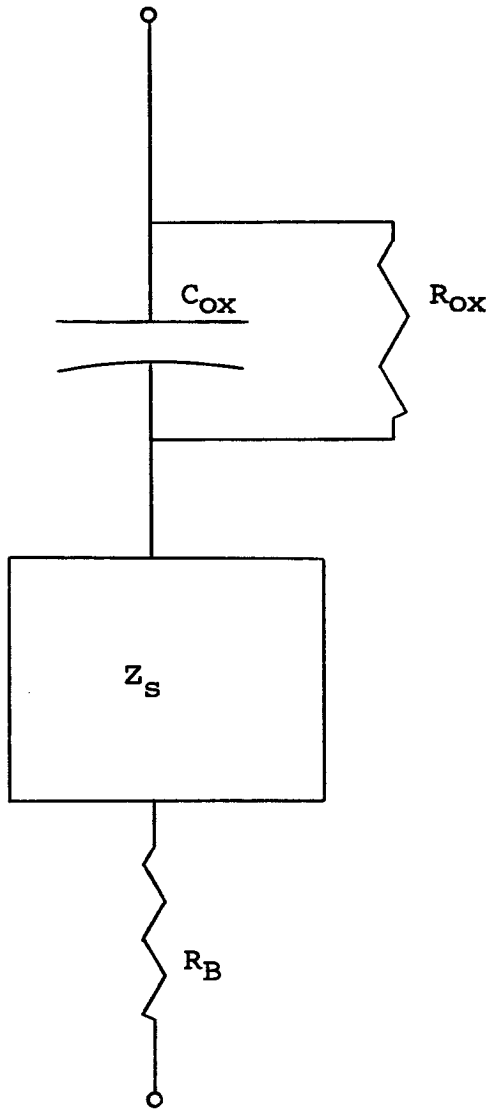


Figure 3.2. The basic MOS equivalent circuit (Source: Zaininger (1964), p. 76)

The latter which includes both spreading resistance and the accumulation region resistance will be treated in detail in the next paragraph. The semiconductor surface impedance, Z_s, is a function of the type of carriers in abundance at the surface. It will be discussed further and illustrated by equivalent circuits for both depletion and inversion regime operation later in this chapter.

Figure 3.3 illustrates the positions of both the accumulation region resistance R_a and the spreading resistance R_s. Since this work treats radiation effects on MOS structures as made apparent by the investigation of accumulation and depletion regime capacitance-bias voltage measurements, it is a good assumption that R_a be neglected and R_s be calculated using the entire semiconductor thickness in order to obtain an estimate of the greatest possible value of the series R_a and R_s resistance. A device with circular symmetry is utilized in the laboratory and is the basis for a calculation of R_s using the method of Zaininger (1964). It can be seen from Figure 3.3 that the radius of the current carrying region is

$$r = a + y \frac{(b - a)}{W} \tag{3.15}$$

where a is the radius of the metal electrode and b is the assumed effective radius of the ohmic contact on the back side of the device. The differential spreading resistance is given by

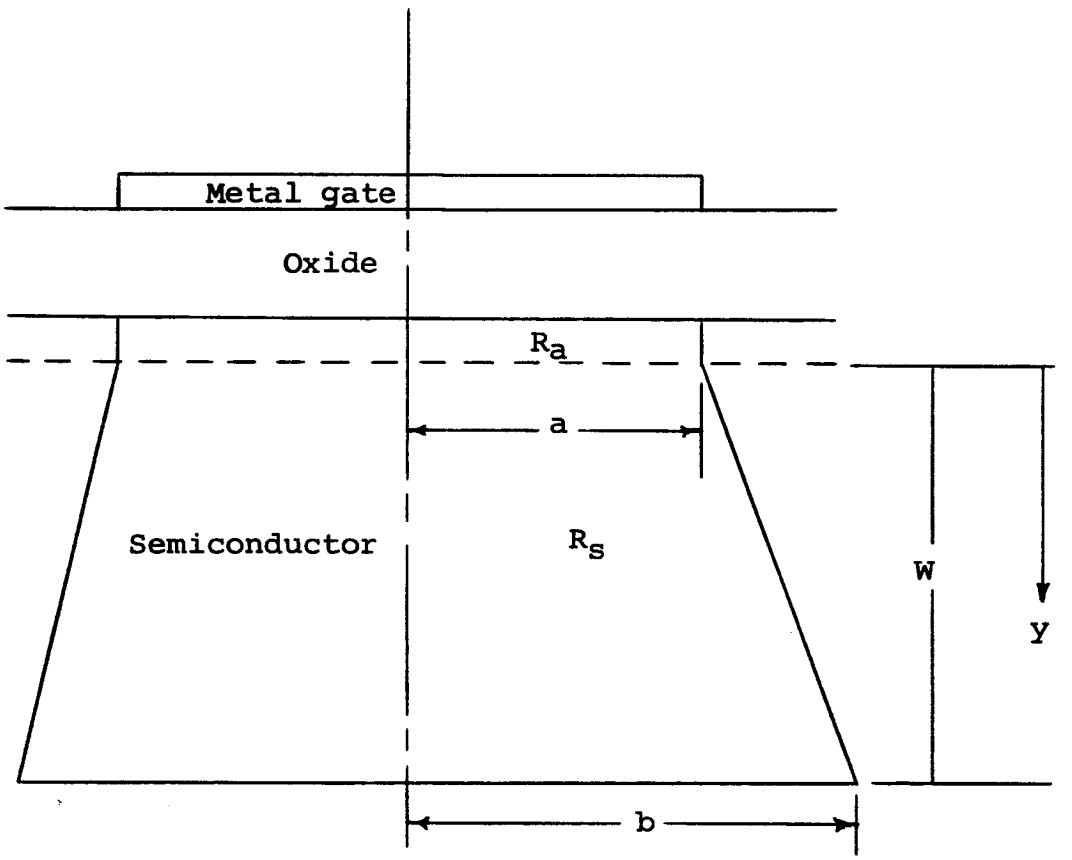


Figure 3.3. Diagram showing substrate resistances (Source: Zaininger (1964), p. 77)

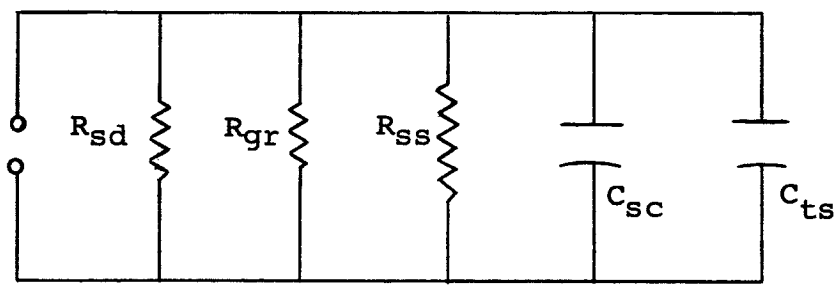
$$dR_s = \frac{\rho dy}{A} = \frac{\rho dy}{\pi r^2} = \frac{\rho dy}{\pi(a + y(b - a)/W)^2} \quad . \tag{3.16}$$

This expression can be integrated to obtain the total spreading resistance.

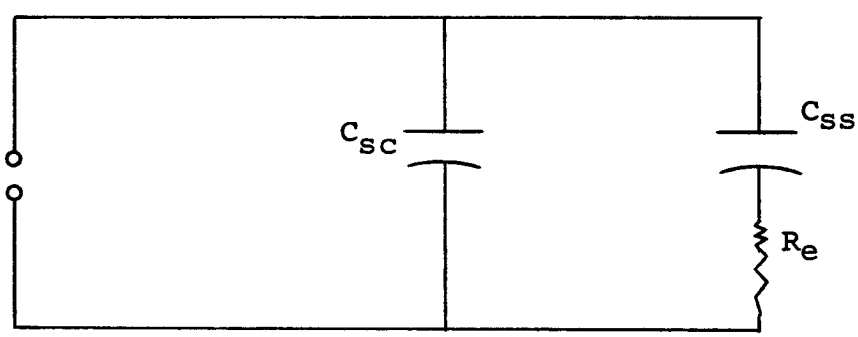
$$R_s = \int_0^W \frac{\rho dy}{\pi(a + y(b - a)/W)^2} = \frac{\rho W}{\pi ab} \tag{3.17}$$

The "worst-case" spreading resistance for a typical device is on the order of 50 ohms. This resistance is important in processing the capacitance-bias voltage data as will be seen in following sections.

Lehovec and Slobodskoy (1964) have investigated the impedance of the MOS device in the accumulation, depletion, and inversion regimes and have developed circuit models based upon both their experimental data and the physics of charge transfer at the semiconductor surface. The equivalent circuits are, however, so complex that, in data processing, little, if any meaningful information can be gleaned from them concerning the physical processes at the surface. Hofstein (1965) and Zaininger (1964) have developed, in a manner similar to that found in the first portion of this chapter, simple equivalent circuits which lend themselves nicely to interpretation of data. Figure 3.4 illustrates the simplified equivalent circuit for the device in the inversion regime and the simplified circuit representing the device in the accumulation



(a)



(b)

Figure 3.4. Surface equivalent circuits (a) for surface inversion and (b) for surface depletion and accumulation (Source: Zaininger (1964), p. 83)

and depletion regimes. Since the accumulation and depletion regimes of operation are of interest in this work the equivalent circuit of Figure 3.4 (part b) will be used as the impedance Z_s of Figure 3.2. Resistance R_e characterizes the losses of the device due to charge transitions into and out of surface states, C_{ss} is the previously defined surface state capacitance, and C_{sc} is the previously defined semiconductor capacitance.

3.2 Prediction of Capacitance-Bias Curves

An examination of the statistics governing charge carrier density at the semiconductor surface as a function of applied bias voltage will indicate that the MOS capacitance is bias voltage dependent. Such a dependence is shown by the typical normalized capacitance-bias voltage curve in Figure 3.5. This curve is for a p-type device, thus, operation in the accumulation regime indicates the presence of an excess of majority carriers, or holes, at the surface. This is caused by the negative gate voltage just as a positive gate voltage causes an excess number of minority carriers (electrons) to reside at the surface for inversion regime operation. A device, when operated in the depletion regime, has a surface which is practically devoid of both holes and electrons. Whether the solid or dotted capacitance curve of Figure 3.5 is seen in inversion regime operation is dependent upon the frequency of the applied test voltage. As discussed by Hofstein (1965), a low frequency test signal

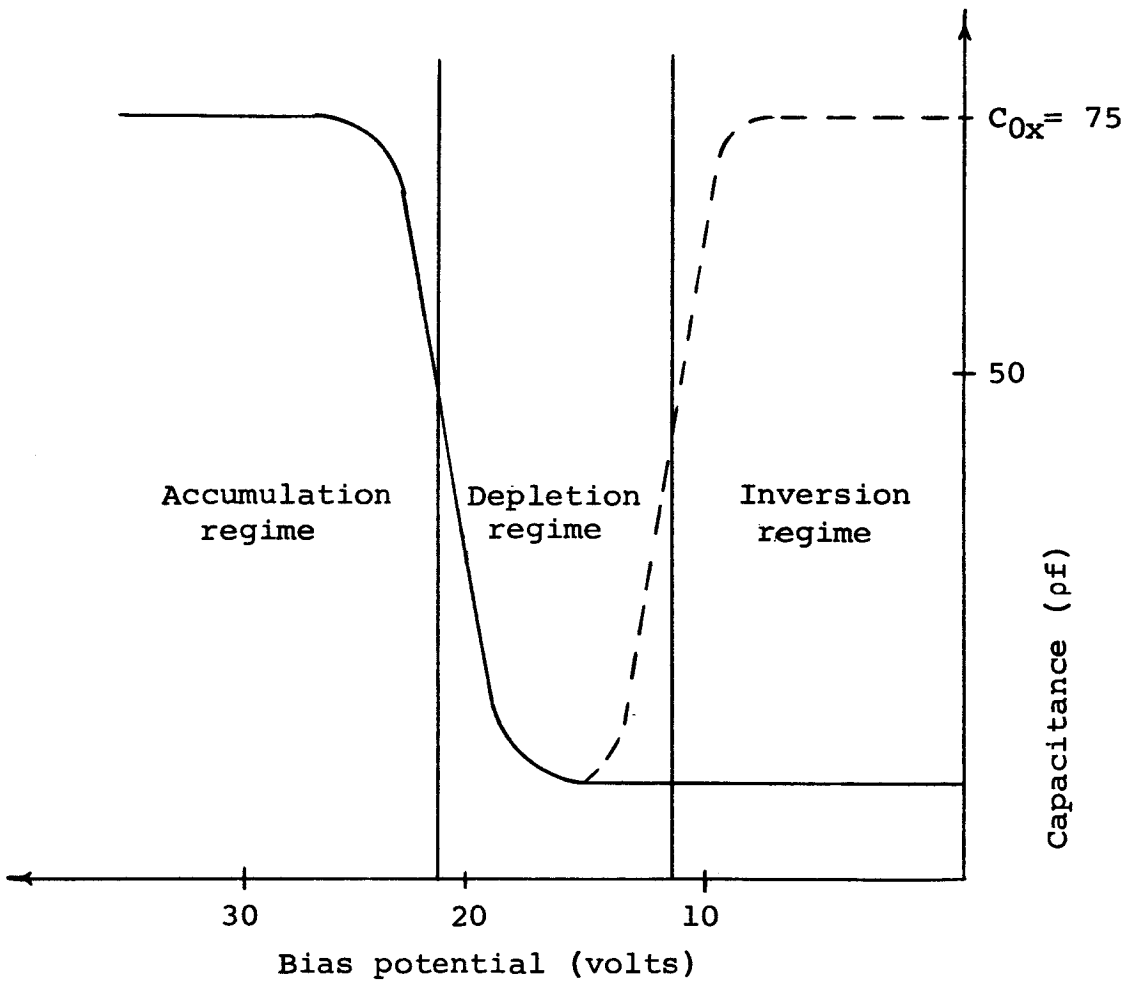


Figure 3.5. A typical capacitance-bias voltage curve for a p-type device with the three modes of operation shown

may have a period sufficiently long that the minority carriers can follow the varying potential; whereas a high frequency test signal will have a period much shorter than the response time of the minority carriers. One other way exists by which the inversion layer at the semiconductor surface can remain in equilibrium with the bulk. This will be discussed in chapter 7.

3.3 Determination of Surface State Density

The method used herein to calculate surface state density as a function of surface potential, ψ_s, is based on the fundamental potential equation (3.1) which may be written

$$V = V_{ss} + V_{sc} + \psi_s. \tag{3.18}$$

In general V and V_{sc} are determined as functions of $_s$ which then allows the relation existing between V_{ss} and ψ_s to be determined. The knowledge of V_{ss} (ψ_s) readily yields the number of surface charges as a function of surface potential on a unit surface area basis.

The applied voltage V is related to the surface potential in a manner similar to that of Heiman (1964) by means of Poisson's equation and Gauss's law. The latter allows one to write

$$D_{ox} = \epsilon E_{ox} = \frac{\epsilon_{ox}}{W_{ox}} (V - \psi_s) = Q_t. \tag{3.19}$$

This equation along with (3.5) then enables one to write

$$C = C_{ox} \left(\frac{1 - d\psi_s}{dv}\right) \tag{3.20}$$

where $C_{ox} = \frac{\epsilon_{ox}}{W_{ox}}$, which can be utilized along with equation (3.18) to obtain

$$C = C_{ox} \left[\frac{(dV_{sc}/d\psi_s)+(dV_{ss}/d\psi_s)}{1 +(dV_{sc}/d\psi_s)+(dV_{ss}/d\psi_s)}\right] . \tag{3.21}$$

At this point it must be assumed that the applied test signal is of a frequency sufficiently high so that its period is much shorter than the response time of the surface states. This being the case, one notes that

$$\frac{dV_{ss}}{d\psi_s} \cong 0,$$

and equation (3.21) becomes

$$C = C_{ox} \left[\frac{dV_{sc}/d\psi_s}{1 +(dV_{sc}/d\psi_s)}\right] . \tag{3.22}$$

Equation (3.22) allows $dV_{sc}/d\psi_s$ to be written in terms of C and C_{ox}

$$\frac{dV_{sc}}{d\psi_s} = \frac{C}{C_{ox} - C} . \tag{3.23}$$

Since C is a function of bias voltage so also is $dV_{sc}/d\psi_s$. $dV_{sc}/d\psi_s$ can, however, be calculated as a function of $_s$ on a theoretical basis from Poisson's equation. This enables one to relate the applied voltage to the surface potential. If it is assumed that the Fermi level always

remains at least 3 kT from the conduction and valence band edges, Maxwell-Boltzmann statistics may be used. Poisson's equation for p-type material with a concentration, N_a, of acceptor atoms which are all assumed ionized, then becomes

$$\frac{d^2\psi}{dx^2} = -\frac{q}{E}\left[p - n + N_D^+ - N_A^-\right] \tag{3.24}$$

which is

$$\frac{d^2\psi}{dx^2} = -\frac{q}{E}\ N_A(e^{-\beta} - 1) - N_o(e^{\beta} - 1) \tag{3.25}$$

where

$$p = N_A\ e^{-\beta\psi} \tag{3.26}$$

$$n = N_o e^{\beta\psi} \tag{3.27}$$

$$N_D^+ = N_o \tag{3.28}$$

$$N_A^- \approx N_A \tag{3.29}$$

and

$$\beta = \frac{q}{kT}. \tag{3.30}$$

By means of the substitution

$$\frac{d\psi}{dx} = u, \tag{3.31}$$

the second derivative term in (3.25) becomes

$$\frac{d^2}{dx^2} = u\ \frac{du}{d\psi}. \tag{3.32}$$

This greatly facilitates the integration of (3.25) in the following manner.

$$\int_0^u u\,du = -\int_0^{\psi_s} \frac{q}{E}\left[N_A(e^{-\beta}-1) - N_O(e^{\beta}-1)\right] d\psi \tag{3.33}$$

The result is

$$\frac{u^2}{2} = -\frac{q}{E}\left[\psi_s(N_A - N_O) + N_A\left(\frac{kT}{q}\right)(\ ^{-\beta\psi}-1) + N_O\left(\frac{kT}{q}\right)(\ ^{\beta\psi}+1)\right]. \tag{3.34}$$

Hence

$$\left.\frac{d\psi}{dx}\right|_s = \pm\sqrt{\frac{2N_A kT}{E}}\left[\beta\psi_s - 1 + e^{-\beta\psi_s} + \frac{N_O}{N_A}(e^{\beta\psi_s} - 1 - \beta\psi_s)\right]^{\frac{1}{2}} \tag{3.35}$$

But

$$E_s = -\left.\frac{d\psi}{dx}\right|_{x=x_s}, \tag{3.36}$$

and since

$$E_{ox}\,\epsilon_{ox} = E_s\,\epsilon_s \tag{3.37}$$

$$E_{ox} = \frac{\epsilon s}{\epsilon_{ox}}\sqrt{\frac{2N_A kT}{s}}\left[\beta\psi_s - 1 + e^{-\beta x_s} + \frac{N_O}{N_A}(e^{\beta x_s} - 1 - \beta x_s)\right]^{\frac{1}{2}} \tag{3.38}$$

where this field is due to the semiconductor band bending at the surface and has no connection with surface states. Since this is the case

$$V_{sc} = \pm\, 2\left(\frac{kT}{q}\right)\left(\frac{E_s}{E_{ox}}\right)\left(\frac{W_{ox}}{L_s}\right)\left[\beta\psi_s - 1 + e^{-\beta\psi_s} + \frac{N_O}{N_A}(e^{\beta\psi_s} - 1 - \beta\psi_s)\right]^{\frac{1}{2}} \tag{3.39}$$

where

$$L_s = \left[\frac{2kT\epsilon_s}{q^2 N_A}\right]^{\frac{1}{2}}. \tag{3.40}$$

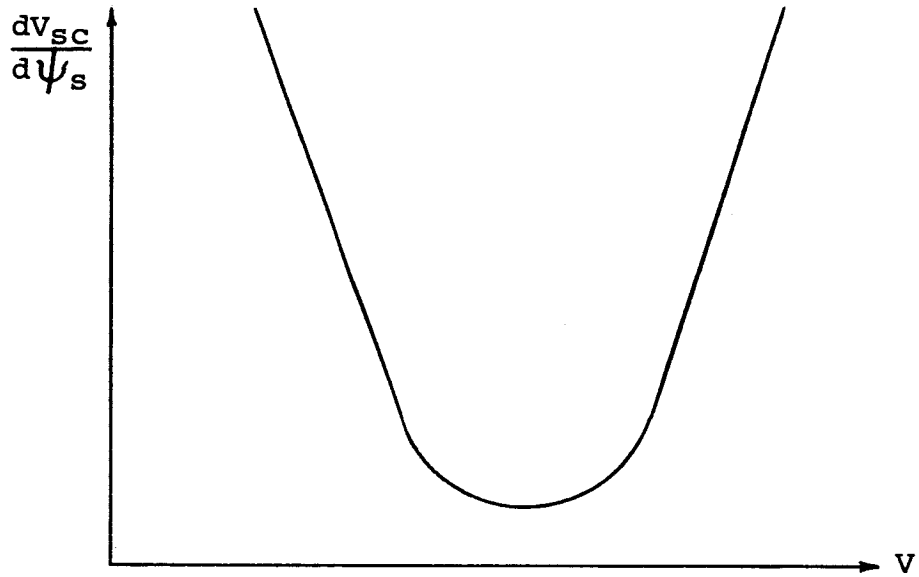
One differentration of (3.39) yields

$$\frac{dV_{SC}}{d\psi_S} = \pm \left(\frac{E_S}{E_{OX}}\right)\left(\frac{W_{OX}}{L_S}\right) \left\{ \frac{1 - e^{-\beta\psi_S} + N_O/N_A(e^{\beta\psi_S} - 1)}{\left[\beta\psi_S - 1 + e^{-\beta\psi_S} + N_O/N_A(e^{\beta\psi_S} - 1 - \beta\psi_S)\right]^{\frac{1}{2}}} \right\} . \quad (3.41)$$

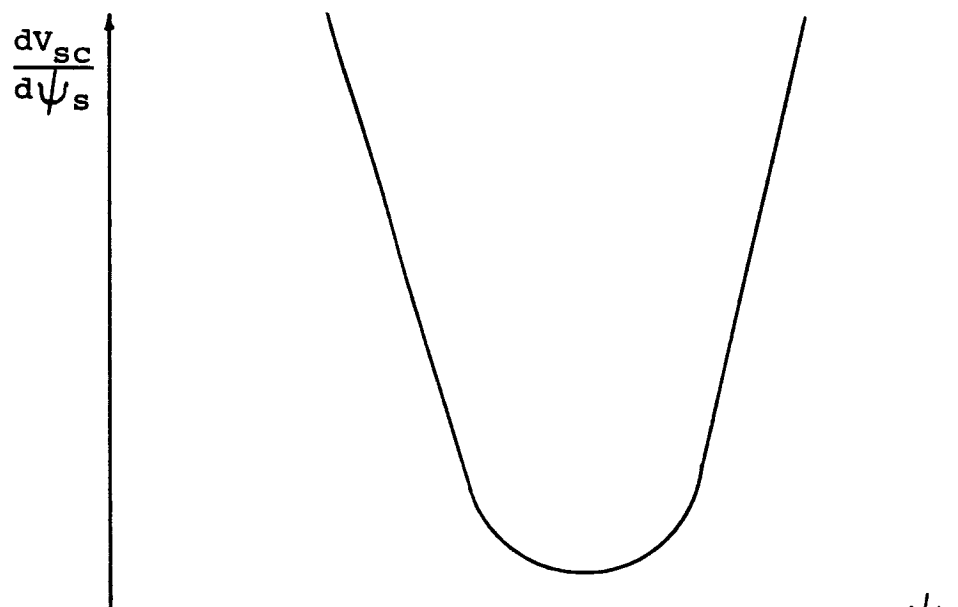
This is the desired equation for $dV_{SC}/d\psi_S$ in terms of ψ_S which allows one to relate V directly to ψ_S through equation (3.32). This can be done since C is a function of the bias voltage. Figure 3.6 (part a) shows a curve of $dV_{SC}/d\psi_S$ as a function of V which was obtained from capacitance-bias voltage data similar to that shown in Figure 3.5, while Figure 3.6 (part b) shows $dV_{SC}/d\psi_S$ as a function of ψ_S. As is pointed out by Zaininger (1964) the value of $dV_{SC}/d\psi_S$ for which the minima occur in each of these curves must be the same in order to avoid a discontinuity in surface potential and a misinterpretation of data. This matching of the minima is accomplished by varying N_A in the expression for L_S and in equation (3.41) and also yields the exact value of N_A at the surface which is not obtainable from the bulk material data.

The method used in this thesis to relate V to ψ_S was that of first choosing N_A so that the two minima coincided, and then using a computer program to store the complete $dV_{SC}/d\psi_S$ vs. ψ_S curve for use in a comparison with the $dV_{SC}/d\psi_S$ vs. V curve.

As can be seen from equation (3.39) the relationship expressing V_{SC} in terms of ψ_S is a direct by-product of the development of equation (3.41) which expresses $dV_{SS}/d\psi_S$ in terms of ψ_S. The facility for expressing both V and V_{SC} in terms of ψ_S which has now been developed allows one to determine the existing relationship between V_{SS} and ψ_S. The



(a)



(b)

Figure 3.6. Typical curves showing the general shape of (a) $dV_{sc}/d\psi_s$ as a function of applied bias voltage, and (b) $dV_{sc}/d\psi_s$ as a function of surface potential

determination of the surface state density from this relationship by the method of Zaininger (1964) requires a differentiation of V_{ss} with respect to ψ_s as follows.

$$\frac{dV_{ss}}{d\psi_s} = \frac{1}{C_{ox}} \frac{dQ_{ss}}{d\psi_s} = \frac{q}{C_{ox}} \frac{dN_{ss}}{d\psi_s} = \frac{q}{C_{ox}} N'_{ss} \tag{3.42}$$

hence

$$N'_{ss} = \frac{C_{ox}}{q} \frac{dV_{ss}}{d\psi_s} \text{ cm}^{-2} \quad \text{eV}^{-1} . \tag{3.43}$$

Figure 3.7 shows a curve of N'_{ss} vs. ψ_s for a typical p-type device. As can be seen, the range of surface potential over which such calculations can be made and remain within the framework of the assumption concerning non-degeneracy is approximately one half the forbidden gap potential.

It is assumed in the above determination of N'_{ss} that the capacitance data used is directly applicable to the equivalent circuits of Figures 3.2 and 3.4. That this is in fact true will be demonstrated in chapter 6. The following list of steps in the calculation of N'_{ss} from the data is presented in summary.

1. Obtain high frequency capacitance-bias voltage data which is directly applicable to the appropriate equivalent circuit.
2. Assuming that C_{ox} is the true oxide capacitance[1] obtain a curve of $dV_{sc}/d\psi_s$ as a function of bias voltage.

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[1] The value of capacitance asymptotically approached in the accumulation regime region of the data is the true

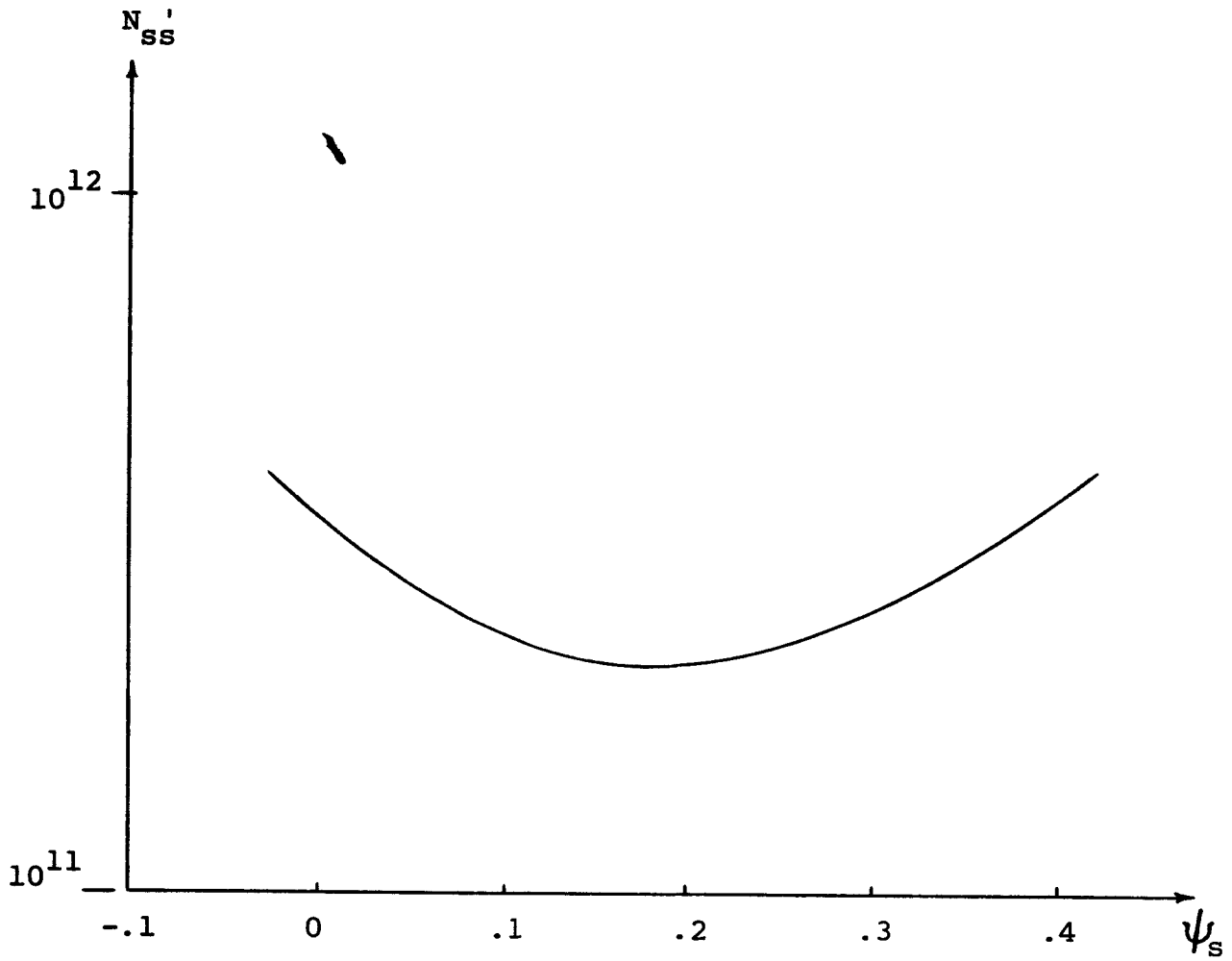

Figure 3.7. A typical curve of surface state density, N_{ss}', as a function of surface potential, ψ_s

3. Obtain a curve of $dV_{sc}/d\psi_s$ as function s using the value of N_A or N_d which causes the minima of that curve and the one mentioned in step two above to occur for the same value of $dV_{sc}/d\psi_s$.
4. By use of the curves of steps two and three above, obtain a relation between V and ψ_s.
5. Utilize equation (3.39) to obtain an expression for V_{sc} in terms of ψ_s.
6. Utilize the fundamental potential expression given by equation (3.18) to determine V_{ss} as a function of ψ_s.
7. Utilize equation (3.43) to determine the actual surface state density as a function of surface potential.

It is possible to use the above method to make an absolute determination of the surface state density if the oxide charge density is known and can be accounted for in the data. The next chapter deals with the oxide charge in a theoretical manner.

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capacitance of the oxide layer itself if its magnitude in invarient with frequency as was pointed out by Zaininger (1964).

4. OXIDE CHARGES

4.1 Horizontal Curve Displacement Due to Oxide Charges

The mathematical model developed in the previous chapter was based on several assumptions. The one which was perhaps the most unrealistic concerned charges distributed throughout the silicon oxide. Charge is always present in an oxide to some extent no matter what the preparation technique might have been. This charge has the effect of simply shifting the capacitance-bias voltage curve of the device horizontally away from the position it would normally occupy were there no such charge in the oxide. The direction and amount of this voltage shift is dependent upon the polarity and distribution of this oxide charge as will now be shown.

Change in capacitance of the MOS device with applied bias as shown in Figure 3.5 is due to the change in semiconductor surface charge distribution and density caused by the bias voltage. The presence of charge in the oxide will cause a change in semiconductor surface charge density and distribution. Hence the same capacitance as seen for a given voltage V_O for the case in which no oxide charge is present will be seen for a different voltage V_O' when an oxide charge is present. This charge, if it remains constant with applied voltage, does not change the shape of the capacitance curve but simply acts to shift the curve along the voltage axis as is mentioned above. The dependence of the amount of charge

induced in the semiconductor surface upon the oxide charge polarity and distribution will now be shown in the manner of Snow et al. (1965).

Figure 4.1 shows an arbitrary charge distribution in an oxide and corresponding charges induced in the metal and semiconductor by that oxide charge. The incremental charges induced at the metal gate, Q_g', and semiconductor, Q_s', due to an increment of change in the oxide, $\rho(x)$, can be calculated by the use of Green's reciprocity theorem given by Panofsky and Phillips (1955):

$$dQ_g' = \left[(x - x_o)/x_o\right] \rho(x)\ dx, \tag{4.1}$$

$$dQ_s' = \left[x/x_o\right] \rho(x)\ dx. \tag{4.2}$$

An integration over the oxide thickness yields the total charge at either oxide boundary due to the oxide charge.

$$Q_g' = \int_o^{x_o} \left[(x - x_o)/x_o\right] \rho(x)\ dx \tag{4.3}$$

$$Q_s' = \int_o^{x_o} \left[x/x_o\right] \rho(x) dx \tag{4.4}$$

It can be easily shown that the sum of the charges induced at the gate and in the semiconductor by the oxide charge must equal, in magnitude, the total charge in the oxide.

$$\left[Q_g' + Q_s'\right] = -\int_o^{x_o} \rho(x)\ dx \quad . \tag{4.5}$$

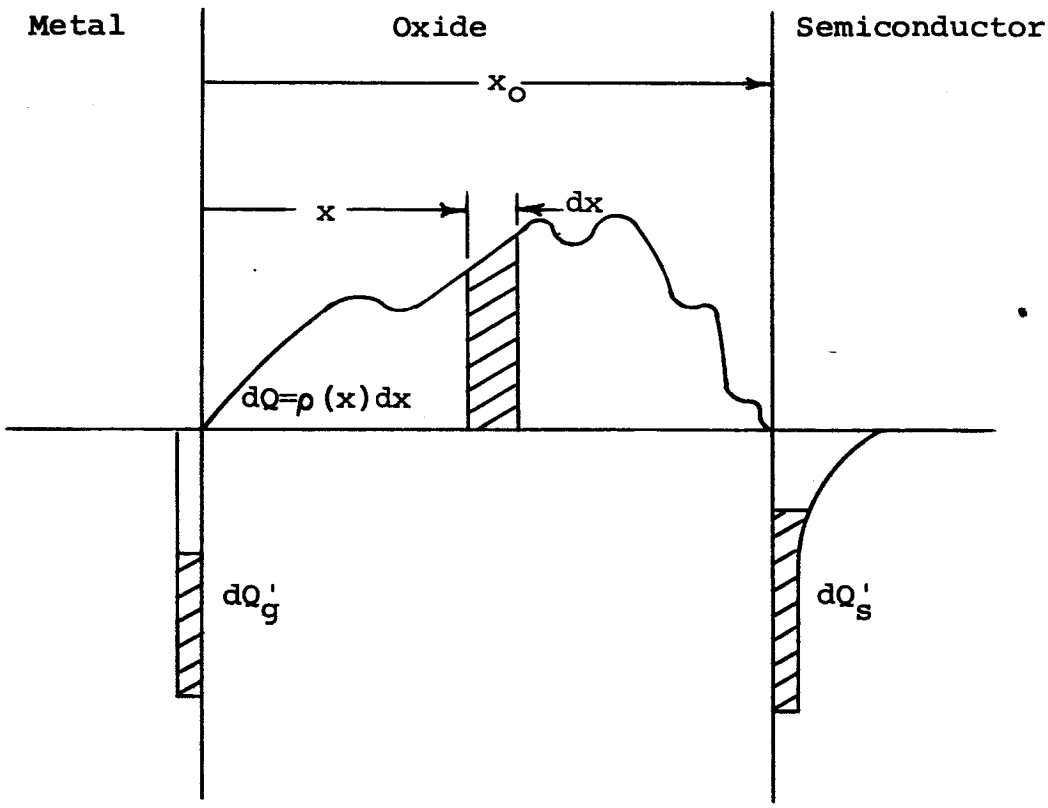


Figure 4.1. Charge induced in the gate, dQ_g', and in the semiconductor, dQ_s', due to an arbitrary charge distribution, $\rho(x)$, in the oxide

One can see from equation (4.4) that practically no charge will be induced in the semiconductor by the oxide charge if all of that charge appears in an incremental layer located at $x' = 0$. On the other hand, the existance of all the oxide charge in an incremental layer at $x' = x_o'$ would cause a charge to be induced in the semiconductor nearly equal in magnitude to the total oxide charge and of opposite polarity. Similar conclusions can be drawn concerning the charge induced on the metal gate by a similar type of limiting investigation of equation (4.3).

If one would now assume that there exists a zero bias charge Q_o on the semiconductor surface it becomes apparent that the addition of an oxide charge $\rho(x)$, which would induce some additional charge Q_s at the semiconductor surface, would make it necessary to apply a bias equal in magnitude to

$$V = \frac{Q_s}{C_{ox}} \tag{4.6}$$

in order to cause the semiconductor surface charge to return to Q_o. Since the capacitance of the MOS device is dependent upon the charge present at the semiconductor surface, one may conclude that the addition of a surface charge of magnitude Q, by induction from an oxide charge, will have the effect of simply shifting the device capacitance-bias voltage curve along the voltage axis by an amount $V = Q/C_{ox}$. Equation (3.39) can be used to show that the total charge at the

semiconductor surface is dependent upon the normal electric field at the surface. By the application of Gauss's law one may conclude, in the case of a device with an oxide charge, that the polarity of the shift of the capacitance-bias voltage curve along the voltage axis due to that charge is opposite the polarity of the oxide charge.

4.2 Annealing Results for Sodium Contamination

Snow et al. (1965) thermally oxidized both p- and n-type silicon substrates in a dry oxygen atmosphere to a thickness of 0.2μ. These were then used in the fabrication of MOS devices but some were first contaminated by a rinse in a diluted NaCl solution prior to the deposition of metal gate electrodes. These structures along with a group of non-contaminated control devices were put through a series of thermal annealing tests while various magnitudes and polarities of potential were impressed across them. It is the purpose of this section to discuss the pertinent details of the experiments along with salient features of the results obtained.

It was found that little or no drift occurred in the capacitance-bias voltage curves of the contaminated devices when the temperature of those structures was raised as high as 200°C under open circuit, short circuit, or negative bias conditions. The application of a positive bias during annealing periods at ≠150°C did however cause gross horizontal shifts in

the curves. These shifts were always towards more negative bias values and were as great as 100 volts, depending upon the duration of the annealing period. It was found that these drifted curves could always be recovered to their initial positions but never beyond by annealing the corresponding devices at an elevated temperature under short circuit conditions. The recovery of the curves was found to be accelerated by an elevated temperature anneal with a negative bias impressed on the device. These facts lead Snow et al. to the conclusion that nearly all of the positive charges, which were initially at the metal-oxide interface, could be drifted at elevated temperatures to the oxide-semiconductor interface by the application of a positive bias, and subsequently drifted back to their initial positions by the application of a negative bias as is illustrated respectively in Figure 4.2 by capacitance versus bias voltage curves and Figure 4.3 by probable charge distributions.

By the use of a charge integration technique these investigators were able to confirm the predicted surface charge changes which were calculated by means of equation (4.6). This technique and that employing curve shift data indicated that the charge flowed from the metal-oxide interface to the oxide-semiconductor interface in a manner proportional to the square-root of time. This was true until a certain total charge had been transferred after which a saturation was noted in the

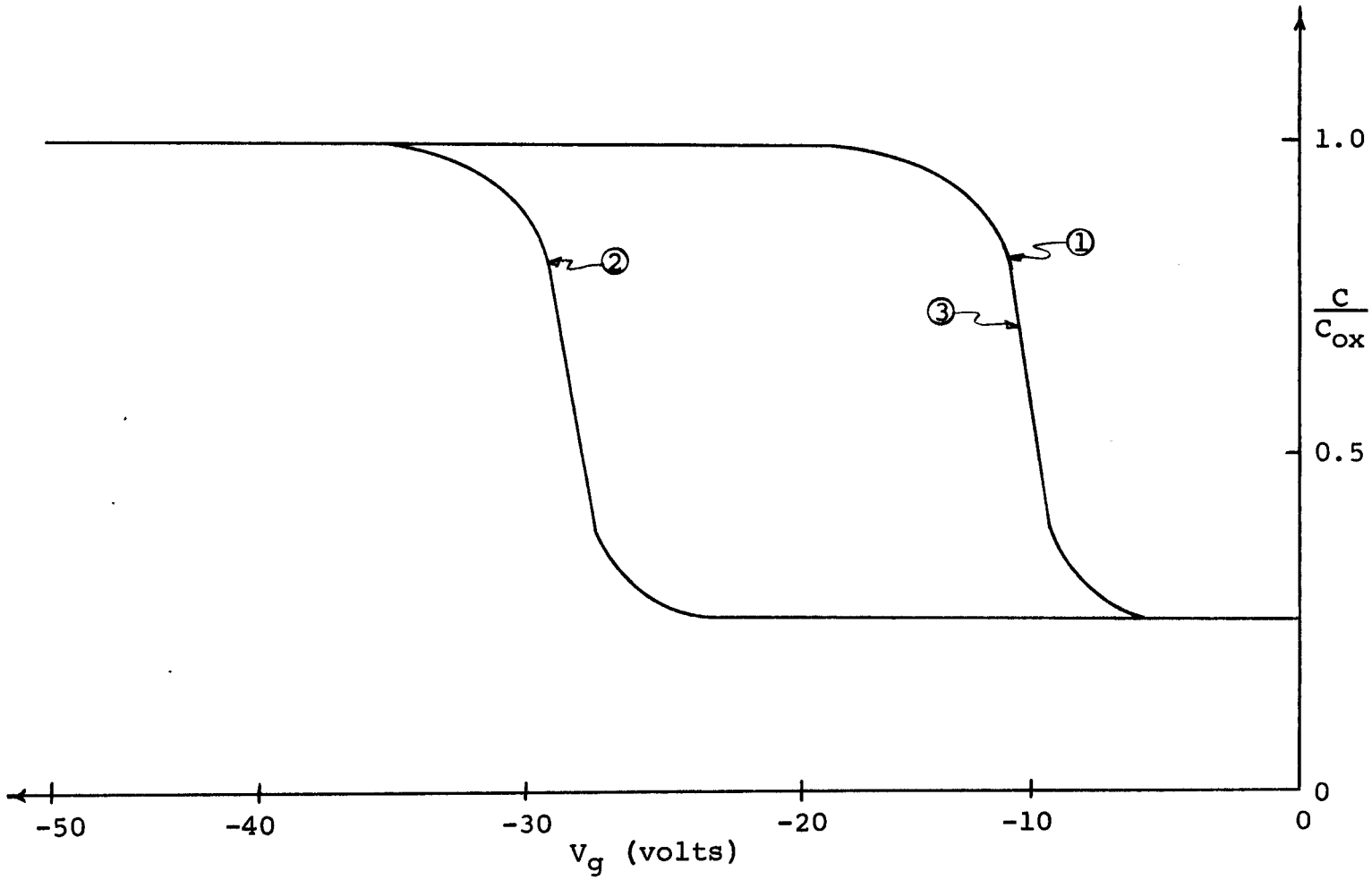


Figure 4.2. Experimentally obtained capacitance-bias voltage curves illustrating the effects of elevated temperature annealing with an applied bias voltage: (1) original curve; (2) curve after a 5 minute anneal at 150°C with +10 v applied; (3) curve after 5 minutes at 150°C with gate short-circuited to substrate (Source: Snow et al. (1965), p. 1666

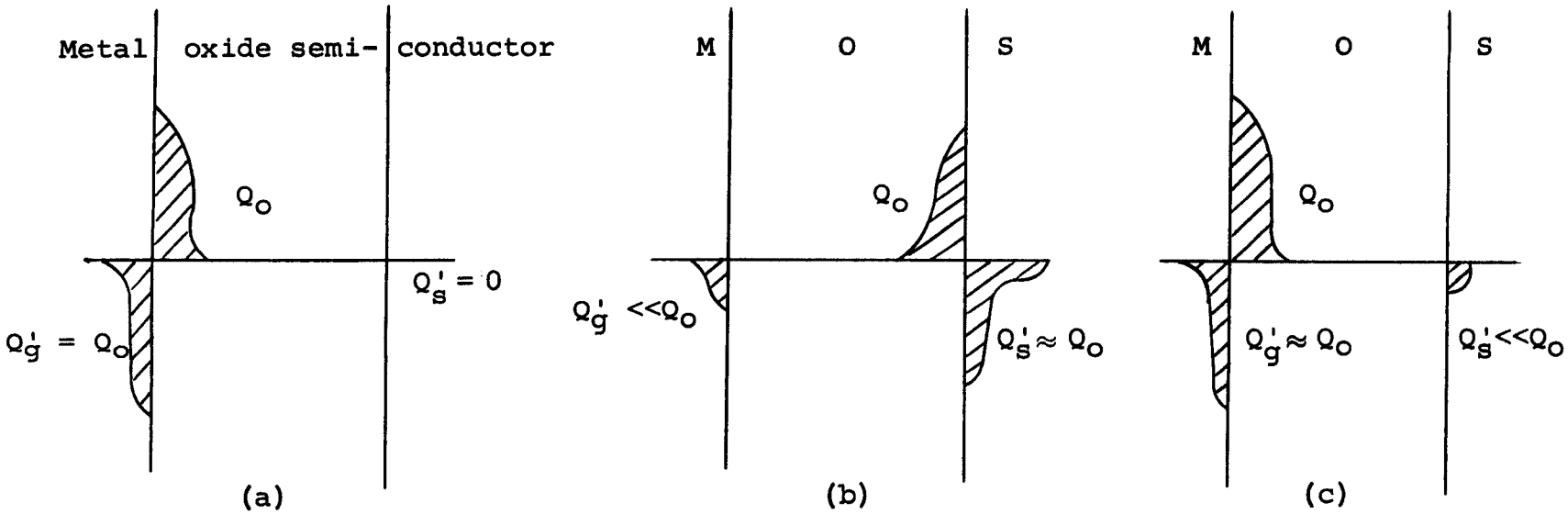


Figure 4.3. Hypothesised charge distribution for a contaminated MOS device oxide. The initial distribution corresponding to curve (1) of Figure 4.2 is shown in (a) while the distribution corresponding to curve (2) of Figure 4.2 is shown in (b) and the distribution corresponding to curve (3) of Figure 4.2 is shown in (c) (Source: Snow et al.(1965),p.1667)

amount of charge at the semiconductor surface. Recovery flow in the reverse direction due to a negative bias anneal was found to have essentially the same time dependence as did the initial drift. Such data taken at various temperatures yielded activation energy information for the flow of the mobile charges in amorphous silicon dioxide. The activation energy found experimentally was approximately 0.7 eV which is near that of sodium ions in amorphous silica as reported by Snow et al. (1965). Finally, profiling experiments were carried out on a device after it had been annealed with a positive bias to determine the charge distribution in the oxide. Only about one-half of the oxide was able to be removed by the authors without causing short circuits from the gate to the semiconductor. It was, however, found by capacitance-bias voltage plots that virtually none of the positive ions were located in that removed portion. This fact confirmed the original hypothesis which implies that essentially all of the charge flows to the oxide-semiconductor interface due to an applied positive bias during the annealing period.

These experimental facts were used to fabricate a mathematical model which predicts, quite well, the experimentally observed phenomena. The following section will present and discuss this model.

4.3 A Diffusion Model for Ion Transport in Silicon Dioxide

Snow et al. (1965) assumed that the one-dimensional flux of charged particles or ions, in the oxide in the presence of both an electric field, E, and a concentration gradient can be given by

$$F = \mu EN - D(\partial N/\partial x), \tag{4.7}$$

where F is the flux in $cm^{-2}sec^{-1}$, μ is the mobility in cm^2 $volt^{-1}sec^{-1}$, E is the electric field in volt cm^{-1}, N is the ion concentration in cm^{-3}, D is the diffusion constant in cm^2sec^{-1}, and x is the distance into the oxide from the gate in cm. Upon combining this with the continuity equation

$$(\partial N/\partial t) = - (\partial F/\partial x), \tag{4.8}$$

they obtained the following relation which governs the time dependent concentration of the ions

$$\partial N/\partial t = D(\partial^2 N/\partial x^2) - \mu\, \partial (EN)/\partial x. \tag{4.9}$$

Because of the method employed in contamination, discussed in the previous section, the initial ion concentration was assumed, constant throughout a thin layer at the metal-oxide interface and zero elsewhere in the oxide as shown in Figure 4.4. The electric field in the oxide was assumed initially zero everywhere except for a thin region near the metal gate where a negative field exists due to the image in the gate of the initial charge Q_o. Hence the oxide electric field varied from zero in the bulk to Q_o/C_{ox} at the surface as is shown in Figure 4.4. Because Q_o/C_o was always at least 30 volts while V_g was usually 10 volts in the authors'

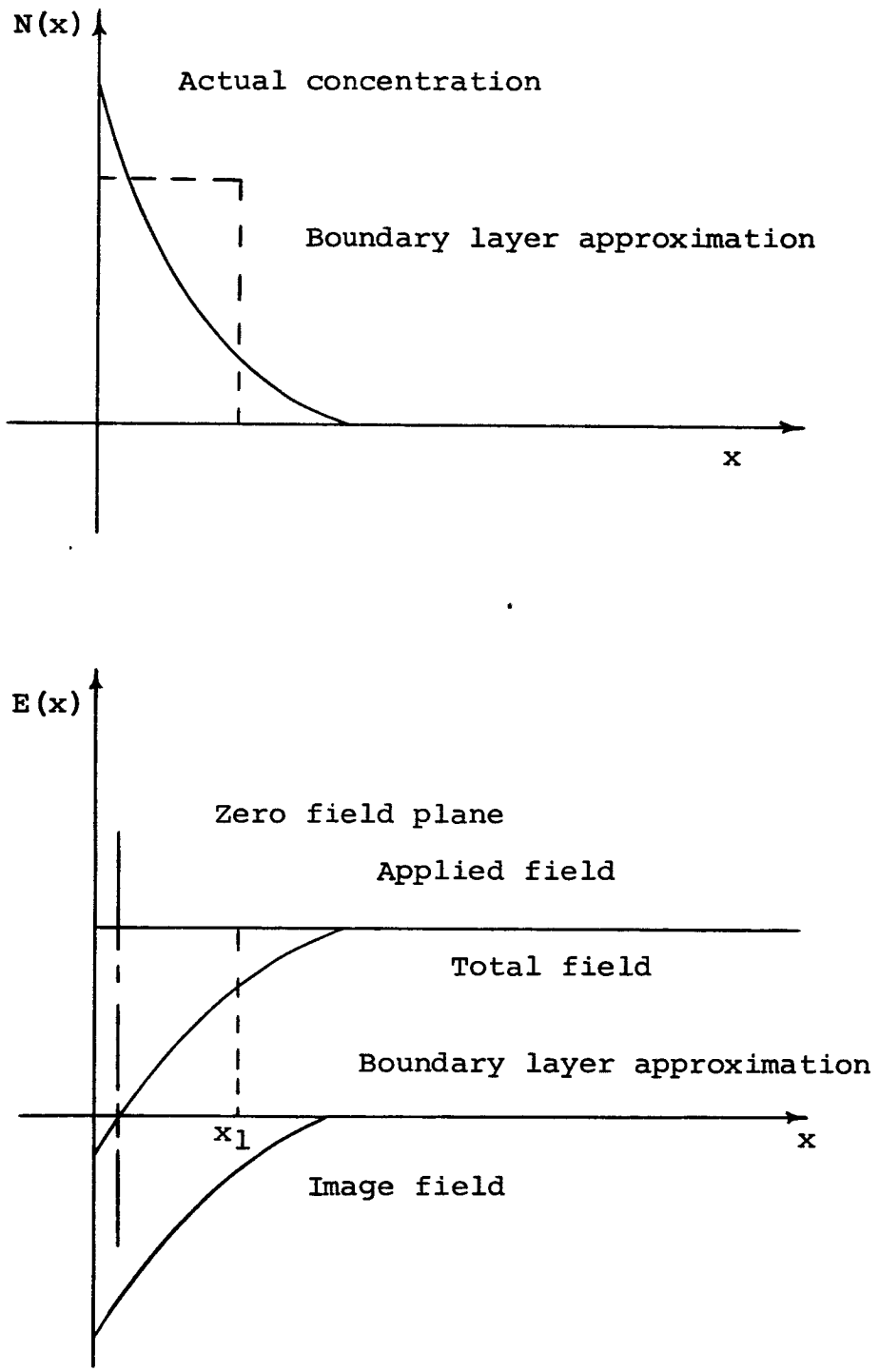


Figure 4.4. The ion concentration, N(x), and the electric field E(x), in the oxide near the metal-oxide-interface (Source: Snow et al. (1965),p.1670)

experimental work, a zero field plane existed in the oxide at some non-zero distance from the metal-oxide interface.

For ease in the solution of equation (4.9) the oxide was divided into two sections. The first section which includes the zero-field plane extends from the metal-oxide interface a distance x_1 into the oxide. Since this region is one of relatively low electric field and high concentration gradient it was assumed that ion transport took place therein only by diffusion. For mathematical simplicity the electric field was assumed zero within the thin boundary layer and a constant, V_g/x_o, elsewhere, while the ion concentration was assumed initially constant, Q_o/gx_1, in the boundary layer and zero elsewhere.

These assumptions having been made by Snow et al. the problem became:

Inside the boundary layer,

$$\frac{\partial N}{\partial t} = D \frac{\partial^2 N}{\partial x^2}, \quad 0 < x < x_1, \ t > 0 \tag{4.10}$$

which states that ions are transported by diffusion only. The initial condition

$$N(x,0) = \frac{Q_o}{qx_1} \ ; \ 0 < x < x_1 \tag{4.11}$$

was imposed which simply stated that the total number of ions Q_o is distributed uniformly throughout the boundary layer. The imposed boundary condition

$$\frac{\partial N}{\partial x} = 0; \quad x = 0, \quad t > 0 \tag{4.12}$$

which states that the flux of ions at the metal-oxide interface is zero.

Outside the boundary layer

$$\frac{\partial N}{\partial t} = D\frac{\partial^2 N}{\partial x^2} - \mu E_o \frac{\partial N}{\partial x} \ , \ x_1 < x < x_o \ , \ t > 0. \tag{4.13}$$

which states that ion transport is by both drift and diffusion.

The initial condition

$$N(x,0) = 0; \quad x_1 < x < x_o \tag{4.14}$$

which was imposed states that no ions are initially outside the boundary layer.

The boundary condition

$$-D \frac{\partial N}{\partial x} + \mu E_o N = 0 \ ; \quad x = x_o, \quad t > 0 \ . \tag{4.15}$$

which was imposed states that the flux of ions at the oxide-semiconductor interface is zero. It can be noted that boundary conditions imposed by equations (4.12) and (4.15) imply that there is no loss of ions from the oxide.

In addition to the above boundary conditions a set of solution matching conditions were imposed at x_1 in order that there be no discontinuity in ion concentration or flux.

Those conditions are

$$N(x_1^-, t) = N(x_1^+, t), \tag{4.16}$$

and

$$- D\frac{\partial N}{\partial x}\Big|_{x_1^-} = - D\frac{\partial N}{\partial x}\Big|_{x_1^+} + \mu E_o N(x_1^+, t). \tag{4.17}$$

Further simplification was achieved by noting that

$$-D\frac{\partial N}{\partial x}\Big|_{x_1^-} > \mu E_o N (x_1^-, t), \tag{4.18}$$

and since the transport of ions within the boundary layer was assumed to be by diffusion, the greatest part of the ion concentration variation will be over a region on the order of $(Dt)^{\frac{1}{2}}$. Hence this inequality was written, where the normalization

$$\hat{N} \equiv \frac{N}{(Q_o/qx_1)} \tag{4.19}$$

was used, as

$$D\,\frac{1-\hat{N}(x_1,t)}{(Dt)^{\frac{1}{2}}} \gtrsim \mu E_o \hat{N}(x_1, t) \tag{4.20}$$

which gave rise to

$$\hat{N}(x_1, t) \lesssim \left[\mu E_o \left(\frac{t}{D}\right)^{\frac{1}{2}} - 1\right]^{-1}. \tag{4.21}$$

The author noted that for times much greater than

$$t = \frac{D}{\mu^2 E_o^2} = \left(\frac{1}{D}\right)\left(\frac{kT}{qE_o}\right)^2 \tag{4.22}$$

the ion concentration at and beyond x_1 was negligibly small. On the basis of available data on sodium diffusion in fused quartz that time was found to be 10^{-3} hours which was much less than any of the annealing periods used. Thus, the matching conditions given in equations (4.16) and (4.17) were replaced by the boundary condition

$$N(x_1, t) = 0 \; ; \quad t > 0. \tag{4.23}$$

It was necessary then to solve equation (4.10) subject to the initial condition given by equation (4.11) and the boundary conditions given by equations (4.12) and (4.23).

The solution to this problem was given as

$$\hat{N}(x,t) = 1 - \sum_{n=0}^{\infty} (-1)^n \left[\operatorname{erfc} \frac{(2n+1)x_1 - x}{2(Dt)^{\frac{1}{2}}} + \operatorname{erfc} \frac{(2n+1)x_1 + x}{2(Dt)^{\frac{1}{2}}} \right. \tag{4.24}$$

$$= \frac{4}{\pi} \sum_{n=0}^{\infty} \frac{(-1)^n}{(2n+1)} \exp\left[\frac{-D(2n+1)^2 \pi^2 t}{4x_1^2}\right] \cos\left[\frac{(2n+1)\pi x}{2x_1}\right]. \tag{4.25}$$

where the first form is a more rapidly convergent representation for small times while the second is more rapidly convergent for larger times.

Since it can be shown by means of the above order of magnitude calculation that the ion concentration outside the boundary layer is negligibly small, the authors assumed that whenever an ion diffused out of the boundary layer it was rapidly transported through the bulk of the oxide to the oxide-semiconductor interface. That assumption stated that the rate of disappearance of ions from the boundary layer is equal to the rate of appearance of ions at the oxide-semiconductor interface. The amount of ionic charge present at the oxide-semiconductor interface is measurable by means of capacitance-bias voltage curve shift. Hence this time dependent interface charge was given by

$$\left|Q_s'/q\right| = -\int_0^t D\left[\partial N(x,t')/\partial x\right] dt' \tag{4.26}$$

where $N(x,t')$ is given by equations (4.24) and (4.25).

Snow _et al_. differentated and integrated the first term of each of the two expressions for $N(x,t)$ and obtained

$$\left|Q_s'/Q_o\right| \cong \frac{4}{\pi^{\frac{1}{2}}} (t/\tau)^{\frac{1}{2}} \text{ for } t \ll \tau \ , \tag{4.27}$$

and

$$\left|Q_s'/q\right| \cong 1 - \frac{8}{\pi^2}\exp\ (-t/\tau) \text{ for } t \gg \tau \ , \tag{4.28}$$

where

$$\tau = 4\ x_1^2/\ \pi^2 D. \tag{4.29}$$

These two asymptotic expressions of charge appearance at the interface as a function of time along with data are reproduced from the work of Snow _et al_. (1965) in graphical form in Figure 4.5. It can be seen from that figure that this simple model satisfactorily accounts for most features of the observed phenomena.

Another assumption was made by the authors which gave rise to a new model. This assumption was that a constant electric field appeared across the oxide and would be applicable in the absence of a zero field plane in the boundary layer. This occurs at some time during each complete drift of ions from the boundary layer to the oxide-semiconductor interface. Although the solution of the equation governing the time dependent concentration of ions based upon this

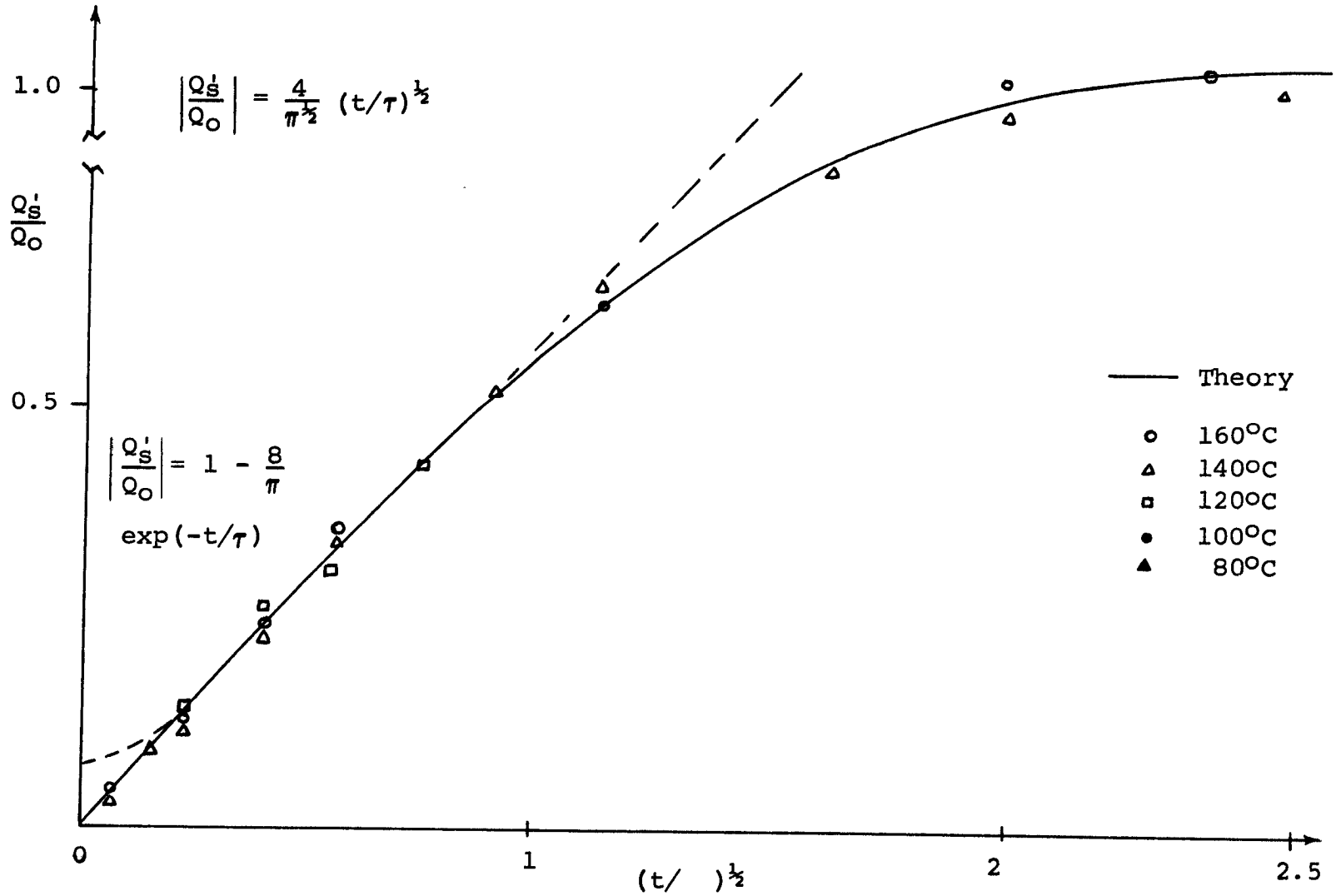


Figure 4.5. Normalized excess charge induced in the silicon as a function of the square root of time (Source: Snow et al. (1965) p. 1672)

model is rather instructive and the obtained results quite applicable; the author of this thesis feels it not nearly so important to the main body of this work as the above presented model and solution. For this reason the solution and results of the latter model of Snow et al. are presented in Appendix A of this thesis.

4.4 A Trapping Model for Ion Transport in Silicon Dioxide

Hofstein (1966) has investigated instabilities in thermally grown oxides by a modified field-effect technique. The oxides used were grown in a dry oxygen atmosphere to a thickness of 0.1μ, approximately one-half that of the oxides used by Snow et al. Hofstein used several methods of surface contamination including immersion of the oxidezed substrates in a saturated NaCl solution at 90°C for 15 minutes. He found in general that the time taken to restore the oxide of a device to its initial condition after a positive bias annealing period was approximately 1/1000 of that necessary for the initial drift; and attributed the long initial drift time-constant to ionic trapping at the metal-oxide interface.

It was also reported by Hofstein (1966) that only after the removal of two hundred angstroms of oxide and a subsequent immersion of the oxidized substrate in a sodium chloride solution, was a quasi-semmetric drift and recovery cycle noted. The only apparent difference in Hofstein's fabrication technique as compared to that of Snow et al. (1965) is that Hofstein

did have phosphorous present in some surface regions of the devices from the first step of fabrication, whereas Snow et al. (1965) did not report such oxide contamination at any region of the surface during any step of device fabrication. Phosphorous was shown by Yon et al. (1966) to act as a getter for sodium atoms in the oxide.

Since device fabrication techniques are all-important in determining the behavior of that device, as is evidenced by the above, the following chapter will be devoted to a discussion of the structures used for data acquisition in the remaining chapters.

5. MOS CAPACITOR FABRICATION TECHNIQUES

5.1 Introduction

The termination of a silicon crystal lattice must necessarily result in the breaking of covalent bonds. Figure 5.1 is a schematic diagram of a clean silicon surface showing the dangling bonds at that surface which result from the termination of the periodic lattice. Chemisorption of foreign species on that surface will make the surface properties strongly dependent upon that species. For example, it is known that surface treatment with oxygen, ozone, halides, or any oxidizing agent will create acceptor states at that surface while treatment with ammonia, acetone, water or methonal will create donor states at that same surface.

This strong dependence of surface properties on atmosphere and other variables which are controlled only with difficulty can be greatly decreased by coating the semi-conductor surface with a layer of passivating material. Such a material is thermally grown silicon dioxide which renders the silicon surface passive to most treatments at standard temperature and pressure. Any impurities incorporated in the silicon dioxide during its growth or introduced later by some means will influence the substrate properties. It is for this reason that the following sections, on materials used and preparation techniques employed in the growth of a silicon

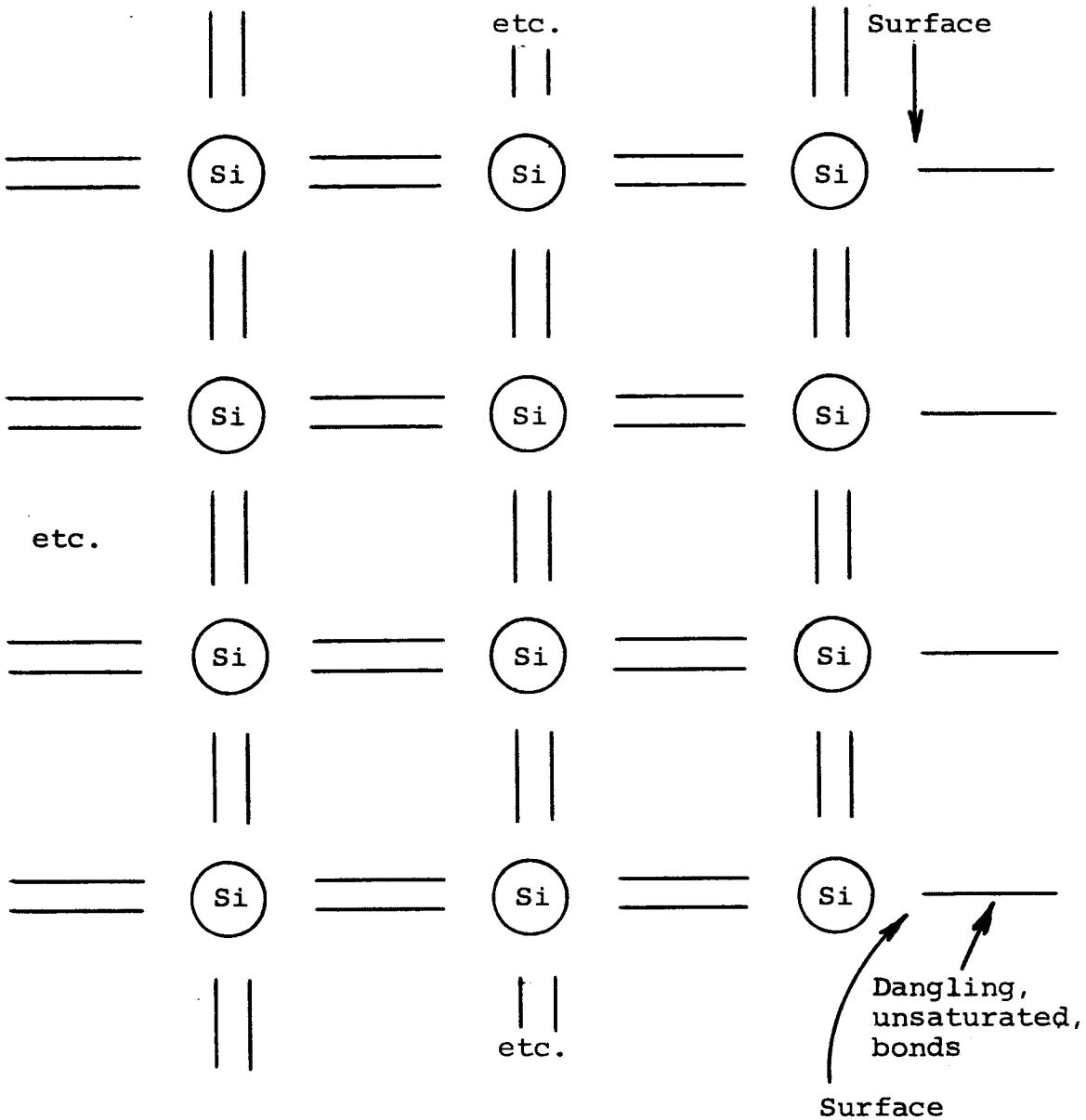


Figure 5.1 Diagram of a clean silicon surface

dioxide layer on both n- and p-type silicon, and on the use thereof in the fabrication of MOS capacitors, will give very specific details on all materials and processes.

5.2 Materials Used

Ingots of both n- and p-type Czochralski-pulled silicon were obtained from the Monsanto Company. Each was fastened to ceramic tile by means of glycolphthiolate wax. These tiles were then clamped in a Micro-Mech wafering machine and the ingots were sliced perpendicular to the (111) axis. This process produced 35 mil wafers of silicon approximately one inch in diameter.

5.3 Surface Lapping

These wafers were initially lapped in a slurey of 400 grit silicon carbide lapping compound and water to remove work damage caused by the wafering machine. The wafers were subsequently lapped in 600 grit, 800 grit, and 10 micron lapping compound-water slurries. After each of the lapping steps the wafers were examined by means of a metallographic microscope to insure that the lapping had been uniform. The wafers were lapped with each compound until the work damage done by the previous step had been removed. This was necessary since the surfaces were finally chemically polished with a solution which had a tendancy to attack crystalline dislocations at those surfaces. The entire lapping sequence removed approximately ten mils of silicon from one side of each wafer.

5.4 Surface Polishing

There are two possible surface polishing techniques available. Mechanical polishing produces a mirror-like surface which is virtually an optical flat, but which has Al_2O_3 polishing compound imbedded in it. Chemical polishing produces a somewhat irregular surface which is clean. Mechanically polished wafers were used in device fabrication several times but the devices failed probably due to unclean surfaces. Stickler and Faust (1964) showed that the aluminum oxide present on the surface of a mechanically polished wafer after polishing was not removable by the usual rinses in organic solvents and immersions in boiling acids. They found also that a ten percent sodium hydroxide solution removed all traces of the Al_2O_3 but etched the surfaces leaving sodium behind.

The devices and oxidized substrates reported on in the remainder of this work were polished by a chemical technique to insure surface cleanliness and reproducability. The technique used will now be described.

A wafer was first rinsed in distilled dimineralized water, boiled in reagent grade tricloroethylene and then reagent grade methyl alcohol to remove any remaining ten micron lapping powder. The sample was then ultrasonically cleaned in a methonal bath for five minutes. The container was then decanted and fresh methanol added for a final ten minute period in the ultrasonic cleaner. Upon removal, the

device was dryed with a hot air blast and then placed in a polypropylene beaker of polishing solution situated on an angled turntable as is shown in Figure 5.2. It was found empirically that a more even polish could be obtained by shining an incandescent microscope lamp on the surface of the wafer while it was rotating in the bath of polishing solution. Small bubbles of hydrogen formed during the polishing period and sometimes adhered to the surface of the wafer causing the areas which they covered to be protected against the polishing solution. A small variable-speed motor with a mass fastened eccentrically to its shaft was mounted to the frame of the turntable. It caused enough vibration during the polishing period to quickly remove any hydrogen bubbles which formed.

The polishing solution was composed of 95% concentrated nitric acid and 5% concentrated hydroflouric acid by volume. The nitric acid acts as an oxidizing agent and forms a silicon oxide at the surface while the hydroflouric acid acts to remove the silicon oxide. Thus the amount of hydroflouric acid present in the polishing solution mentioned above is the surface polishing, or etching, rate determinant. The turn-table speed was approximately 33 rpm and the light intensity at the silicon surface was approximately 100 foot-candles.

The time necessary for a good polish was dependent upon the sample but was usually no longer than twenty minutes. When it was determined that the polishing was complete the beaker was removed from the turntable and the solution was

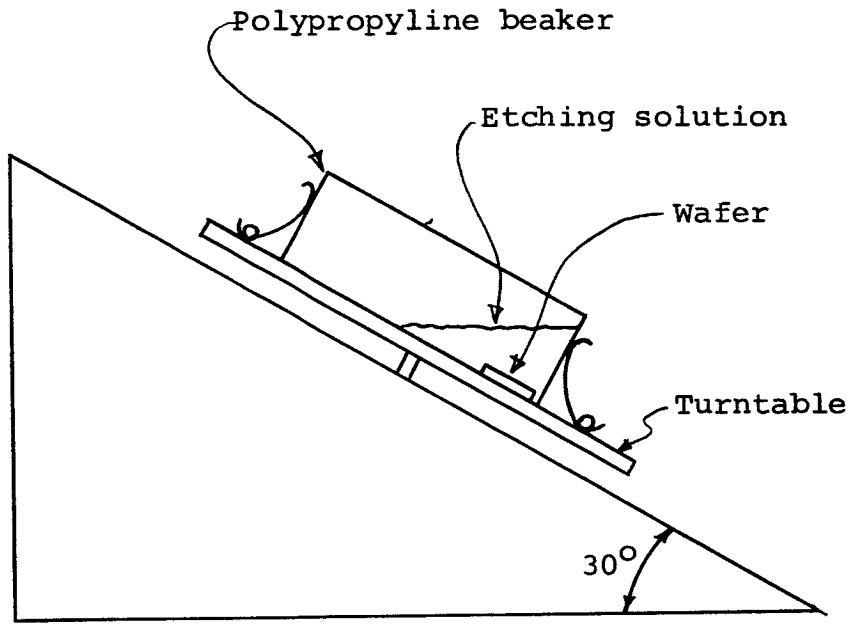


Figure 5.2. Diagram of the angled turntable used for wafer polishing

decanted until just enough remained in the bottom of the beaker to cover the wafer. Distilled, demineralized water was then slowly added to the acid and kept in constant agitation. This resulting solution was decanted as above and the container refilled with water several times until the acid concentration was negligibly small. It was found that, if air was allowed to touch the wafer while the acid concentration was still relatively high, stains of a milky appearance were formed on the wafer surface.

The wafer was removed from the polishing beaker and thoroughly washed in running, distilled, demineralized water. It was then rinsed with a spray of absolute methanol and dried with a blast of hot air. The polished wafer was then stored between two pieces of filter paper until its preparation for oxidation.

5.5 Glassware Cleaning

Prior to thermal oxidation of the silicon wafers the quartz furnace tube along with all other system glassware had to be clean and free from any possible contaminating agents. The general cleaning procedure used was that of rinsing the glassware with distilled dimmeralized water to remove any small dust particles present and then soaking the glassware in a solution composed of 50% aqua regia and 50% pure water for approximately two hours. The steam generator assembly as seen in Figure 5.3 was the first portion of the glassware

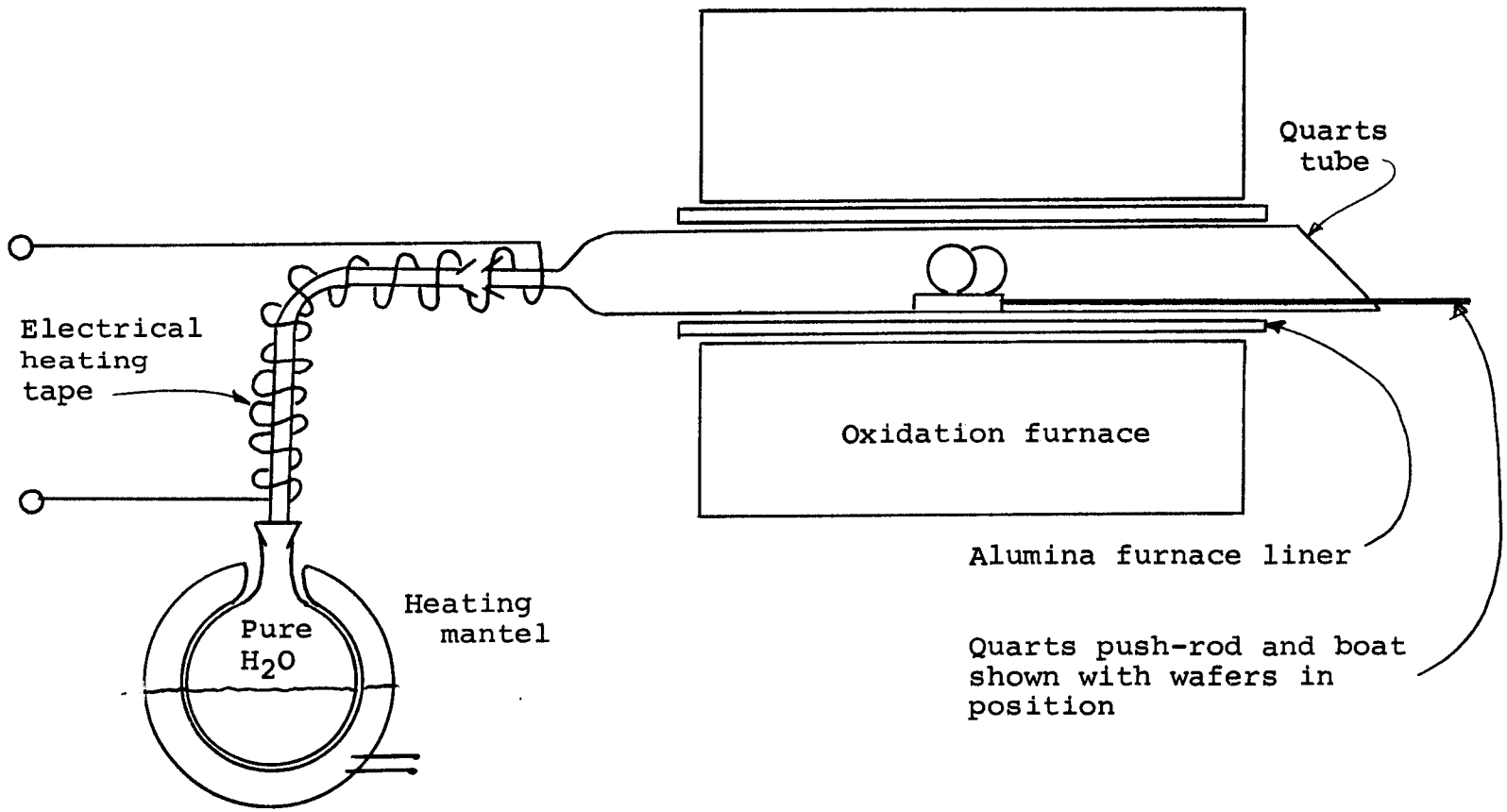


Figure 5.3. Steam oxidation equipment diagram

to be thoroughly rinsed with pure water and made ready for use. It was then filled half full of distilled demineralized water and placed in a zipper type heating mantel which was subsequently energized. The furnace tube and boat were then thoroughly rinsed with purified water and slowly inserted into a special oxidation furnace which was at the temperature necessary for oxidation. By the time the furnace tube had been fully inserted into the furnace the steam generator was in operation and immediately connected to the furnace tube. This configuration of equipment which was then ready for the oxidation of silicon wafers is shown in Figure 5.3.

The furnace used was a "Diffusation 50" manufactured by the Lindberg Hevi-Duty Company and was used exclusively for the thermal oxidation of silicon. Neither the alumina furnace liner nor the quartz furnace tube had ever been used for any other high or low temperature process.

5.6 Wafer Cleaning

It was necessary to carefully clean the polished surface of a wafer to be oxidized in order that a homogeneous, pinhole-free oxide be formed. The cleaning technique consisted of boiling the wafer for one minute in trichloroethylene and then decanting and boiling for one more minute in the same organic solvent. The wafer was then immersed in room temperature reagent grade methyl alcohol for one minute and rinsed in distilled demineralized water. This was followed by a 30 minute

immersion in 80°C concentrated sulfuric acid, a water rinse and 30 minute immersion in concentrated 80°C nitric acid. The wafer was then thoroughly rinsed in running distilled demineralized water at least five times and finally stored in methyl alcohol until being loaded into the furnace.

5.7 Oxidation

The thermal oxidation of silicon at 1100°C obeys the following relation as given by Donovan (1965)

$$x^2 = 7.26\ t \exp(-0.8/kT) \tag{5.1}$$

where

x = oxide thickness (microns)

t = time of oxidation (minutes)

T = temperature (°K)

k = Boltzmann's constant (V °K^{-1})

for times greater than five minutes. This relation between oxide thickness, time, and temperature is shown in Figure 5.4 as obtained from Donovan (1965). The wafer was placed in the 1100°C steam atmosphere for a period of 30 minutes. During that time an oxide was formed approximately 0.35μ in thickness. At the end of the oxidation period that wafer was rapidly withdrawn from the furnace and quenched to room temperature in the atmosphere. It was stored between two pieces of filter paper until the next step in the fabrication process.

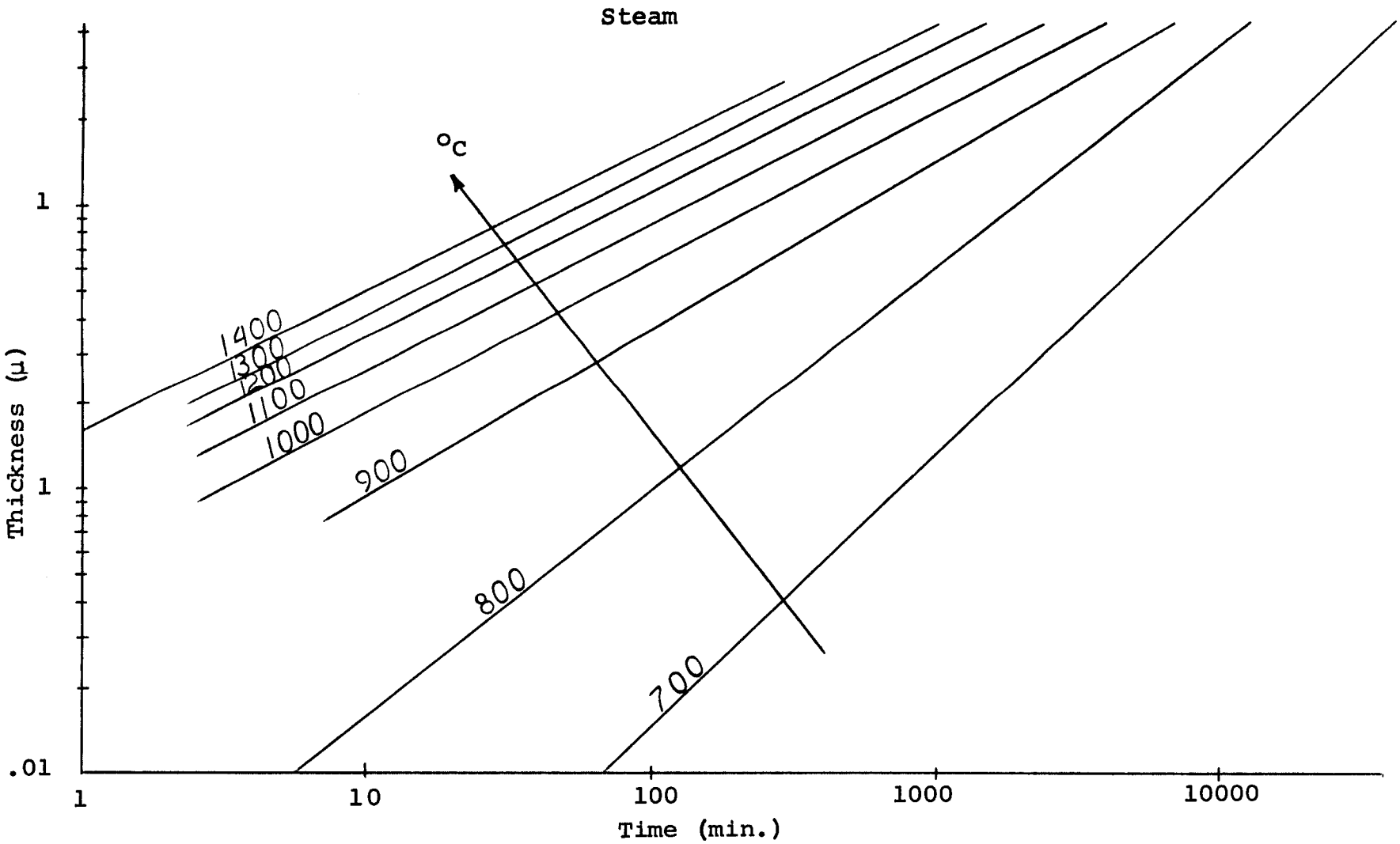


Figure 5.4. Silicon oxide thickness as a function of oxidation time for various temperatures in a steam atmosphere (Source: Donovan (1965), p.49)

5.8 Gate Electrodes and Ohmic Contacts

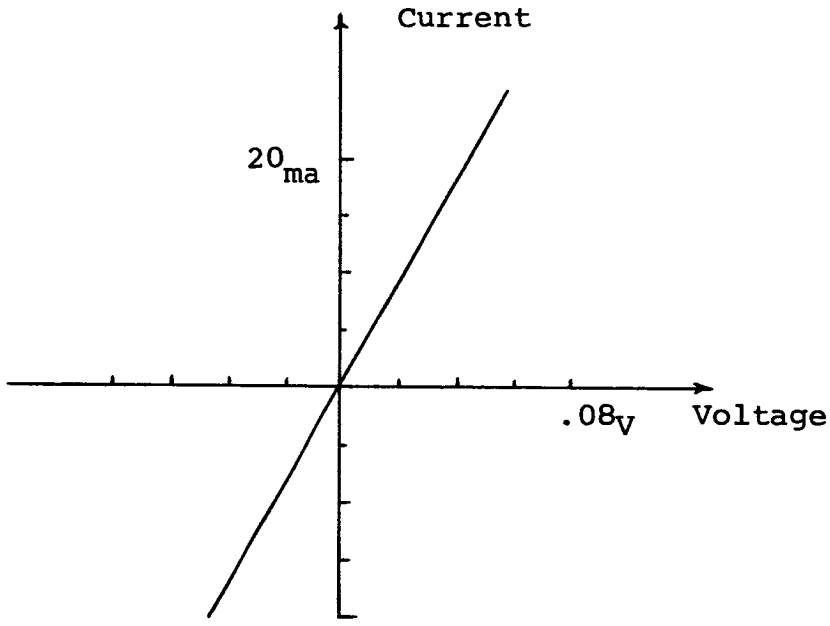
Following the oxidation the oxide was removed from the back, unfinished side, of the wafer by means of sandblasting with 27 micron aluminum oxide. During sandblasting the wafer was held in a vacuum chuck with only the back side exposed so as to protect the oxide on the polished surface. The oxidized substrate was then cleaned by a methanol spray five times in preparation for the vacuum deposition of gate and substrate contacts.

Filaments wound with 99.999+% pure gold and 99.99+% pure aluminum were degreased by boiling in trichloroethylene and then placed in the vacuum chamber as sources for the depositions. The wafer was placed, sandblasted surface up, 14 inches below the filaments in the chamber which was then pumped down to approximately 2×10^{-5} Torr. The aluminum-bearing filament was energized for approximately two minutes. Then both the aluminum- and gold-bearing filaments were simultaneously energized for one minute transition period after which the gold-bearing filament was energized alone for approximately two minutes. The deposition of the ohmic contacts to the substrate was then complete.

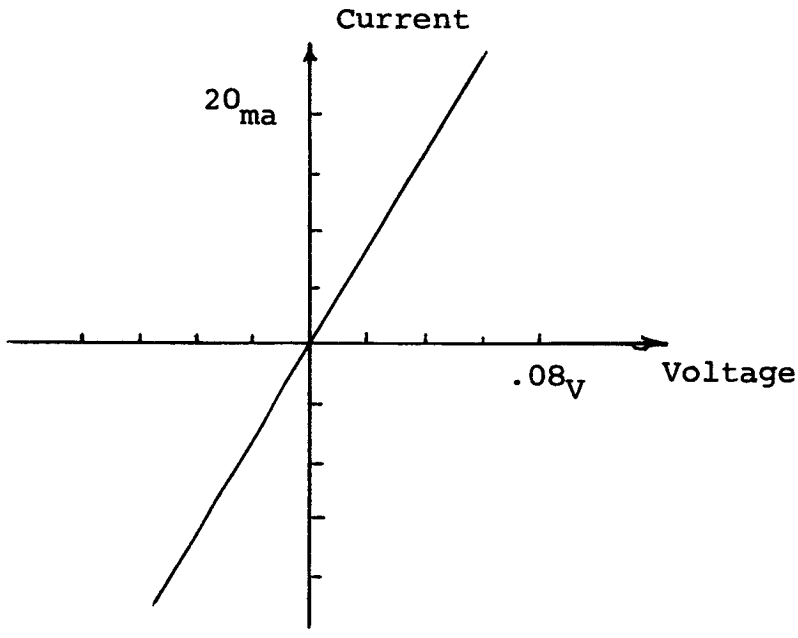
In order to check the ohmicity of the contacts, three n- and three p-type test devices were fabricated. Both sides of the two different type wafers were sandblasted and metal layers evaporated thereon by the process mentioned above. The wafers were then scribed and broken yielding several small

chips with a test surface on each side. Both n- and p-type chips were fastened to TO-5 headers by means of conducting silver paste. Top surface contacts were made by means of five mil nickel wire and conducting silver paste. Current versus voltage curves were taken for these ohmic "sandwich" test devices. The results indicated rather good ohmic contacts as can be seen by the straight-line current-voltage relationships shown in Figure 5.5.

In order to deposit the metal gates on the wafer a one mil thick brass mask having five 40-mil diameter holes in each of five rows was used. The wafer was placed in the vacuum chamber 14 inches below the filaments with the oxidized polished surface facing the electrodes and the mask placed thereon. The evaporation sequence used was exactly the same as that described for the deposition of the ohmic back contacts in which both aluminum and gold were used in that order. Aluminum was vapor deposited initially onto the silicon-dioxide for two reasons. It adheres to the oxidized surface quite well and has a work function very near 4.0eV which is approximately the same as that of the silicon used. The work function similarity allows one to simplify equations (3.1) to (3.3). A gold coating was deposited on the aluminum since it is easy to make electrical contact with. This is due to the absence of any insulating oxide coating on the gold similar to that which forms on aluminum. Special care was taken



(a)



(b)

Figure 5.5. Current-voltage curves for test ohmic contacts: curve (a) is for p-type material and curve (b) is for n-type material

to insure that during a gate deposition the oxidized surface and mask were at least 12 inches from the metal source filaments in the vacuum chamber. This was done to prevent the occurance of a frequency dependent oxide capacitance due to the "penumbra effect" as discussed by Zaininger (1964).

5.9 Mounting and Storage of MOS Capacitors

The wafer bearing five metal gate electrodes in each of five rows was mounted with glycolphthiolate wax, sandblasted side down, on a graphite block which was clamped into position in a wire dicing machine. A continuous wire loop coated with a slurry of glycerine, 400 grit lapping powder, and water was slowly drawn across the wafer first cutting it into five rows of five devices each and then subsequently dividing each row into five separate devices. The wire dicing machine was used in preference over the diamond wheel Micro-Mech wafering machine since the wire of the former essentially slowly lapped its way through the wafer without causing crystal chipping and microcracks and also because it would separate all the devices on a wafer without contaminating the surface of the device with lubricant.

The individual devices were then removed from the graphite block and washed in a spray of acetone to remove the glycolphthiolate wax from the substrate contact. A device was finally rinsed in a spray of absolute methyl alcohol, dried in a blast of hot air, and fastened, ohmic contact side down,

by means of conducting silver paste to a TO-5 header. Contact was made to the metal gate by means of a five mil nickel wire and conductive silver paste. A mounted device is shown in Figure 5.6.

The completed MOS-capacitors were stored at room temperature in a closed glass or plastic dessicator containing anhydrous $CaSO_4$ as the dessicant.

5.10 Oxide Thickness Measurement

An edge section of the oxidized wafer, not bearing any devices, was used for the oxide thickness determination. A multiple-beam interferometric technique utilizing Fizeau fringes was applied. A schematic diagram of the equipment necessary for such a thickness determination is shown in Figure 5.7 as given by Donovan (1965). Preparation of the oxide specimen was accomplished by covering a portion thereof with Apiezon wax and then removing the exposed oxide by the use of commercial 48% concentration hydroflouric acid. This acid was much better to use than a slow acting, buffered hydroflouric acid oxide-etch in this specific application since it rapidly undercut the oxide under the protective wax region; hence, forming a wide transition wedge between the oxidized and non-oxidized portions of the specimen. Such a wedge is necessary for determining the exact interference fringe displacement across the oxide-non-oxide discontinuity on the observed specimen.

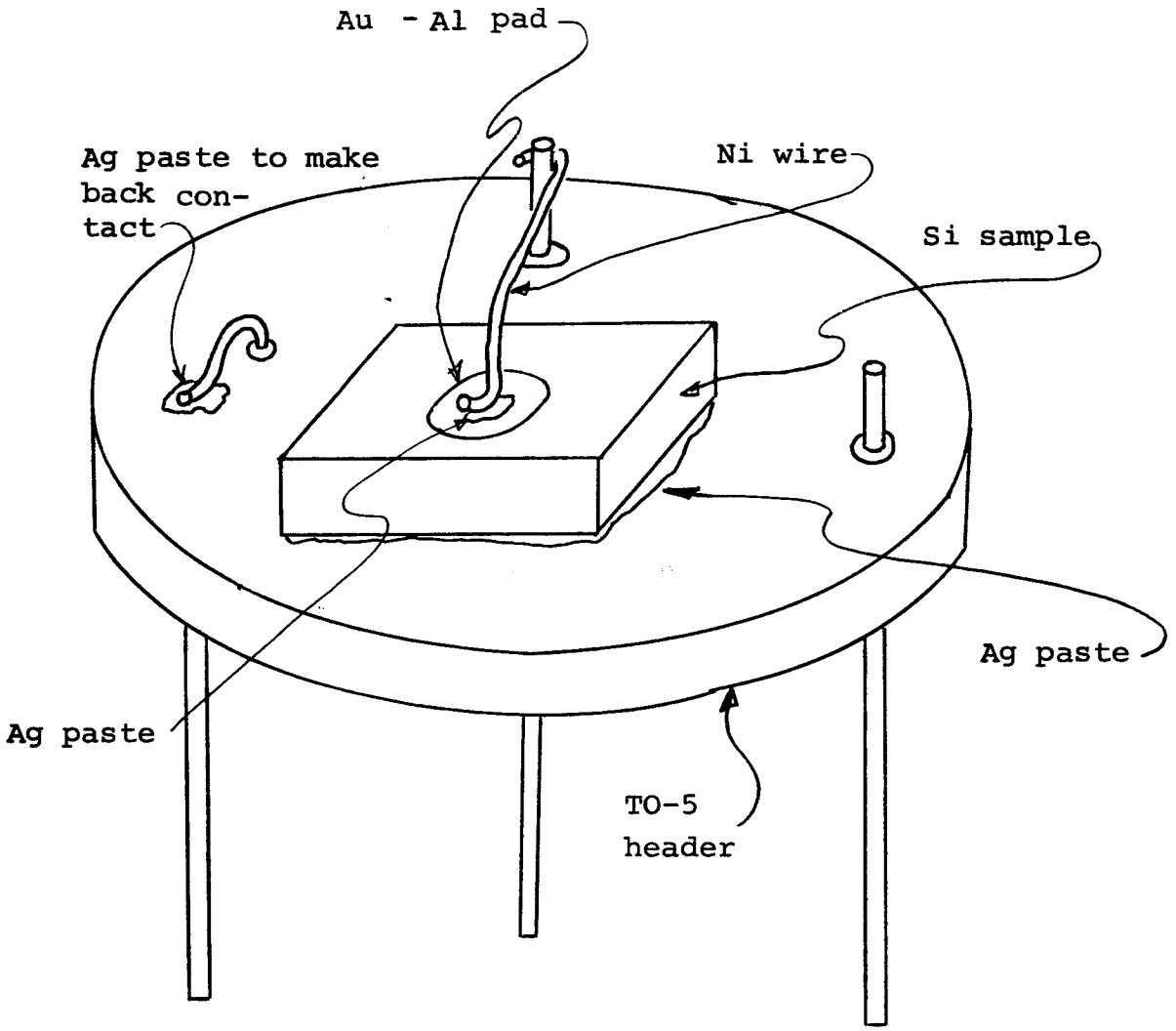


Figure 5.6. Mounted MOS capacitor

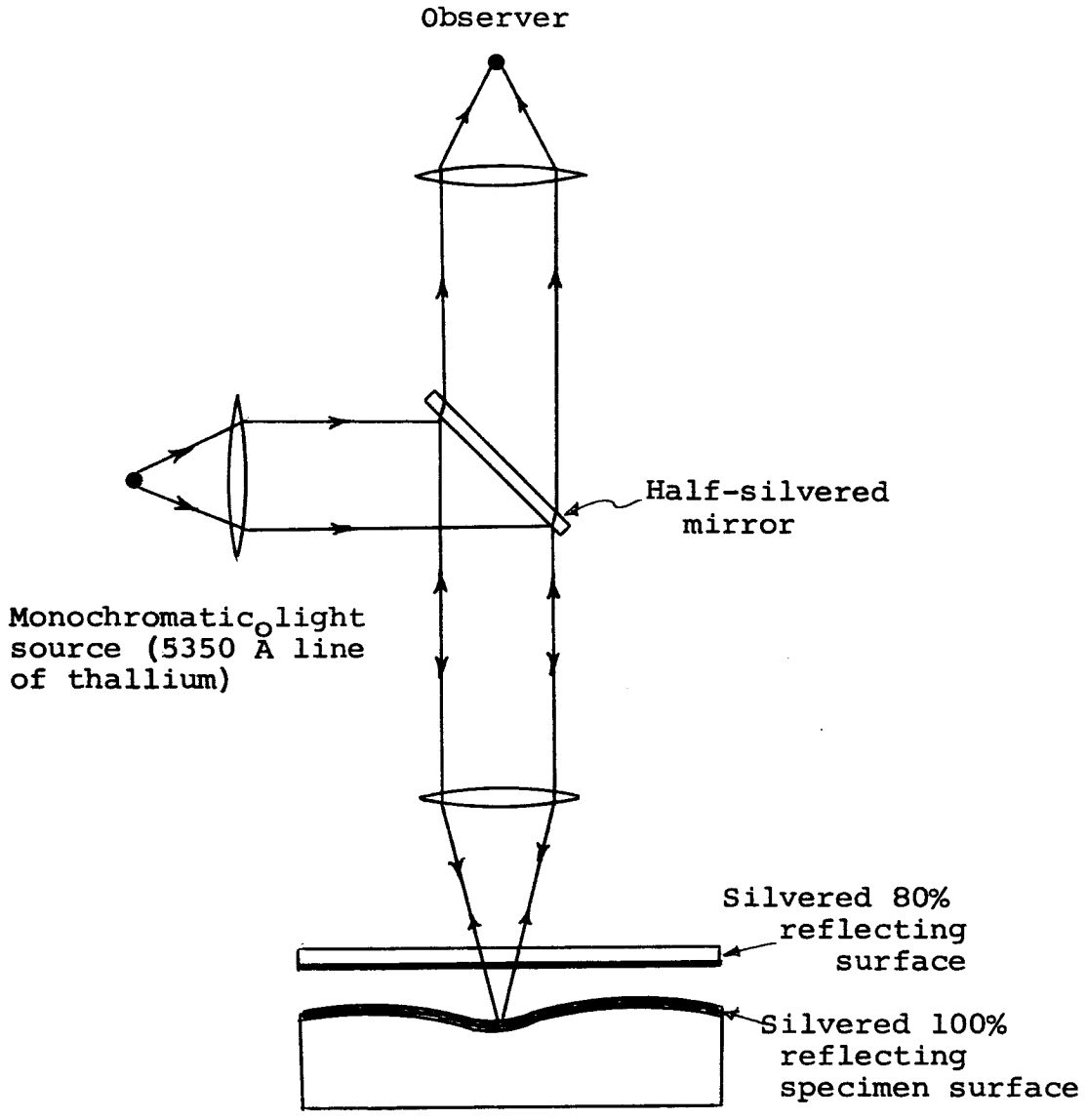


Figure 5.7. Diagram of equipment used in forming multiple-beam interference patterns (Source: Donovan (1965), p. 197)

The oxide, which was prepared as above, was then given an aluminum coating over the oxide discontinuity by means of vapor deposition. This aluminum coating was assumed homogeneous in thickness and hence possessed the same discontinuity as did the oxide but one which was totally reflecting. The specimen was then placed in position in the interferometer and an interference pattern similar to the one shown in Figure 5.8 was obtained. In determining the oxide step height by this technique, the author noted that the fringe pattern displacement corresponded to twice that step height since the fringe displacement represented a change in optical path which is twice the separation between the reflecting plates. Hence the oxide thickness is given by:

$$W_{ox} = f\lambda/2\mu \tag{5.2}$$

where

W_{ox} = oxide thickness (angstroms)

f = fringe displacement (mils)

λ = wavelength of monochromatic light (angstroms)

μ = fringe separation (mils)

In each case the measured oxide thickness and that calculated from the basic parallel plate capacitor relation (using ϵ_r = 3.85 as reported by Owen and Douglas (1959)) corresponded to within five percent. Donovan (1965) also gives information leading to the oxide thickness relation for a non-perfect reflecting oxide surface

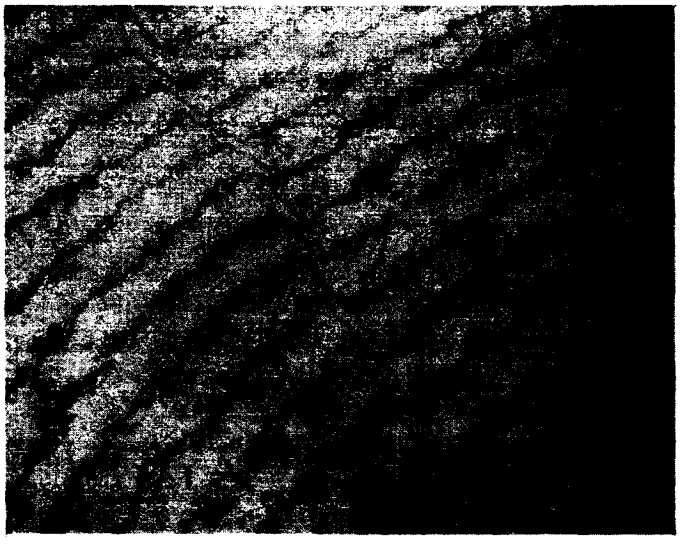


Figure 5.8 Typical interference pattern obtained when measuring oxide thickness using the Fizeau fringes technique

$$f\lambda/\mu = W_{ox}\ (n - 1), \tag{5.3}$$

where

n = the index of refraction of an oxide film

which can be used in conjunction with information gained from the coated oxide case to determine the index of refraction of the oxide.

Hence one can see that oxide thickness determination by a multiple beam interferometry method can be used as a check on the measured value of oxide capacitance assuming the relative permitivity of the oxide is known.

The method used in device capacitance measurement as a function of bias are discussed in the following chapter.

6. MEASUREMENTS

6.1 Introduction

The method described in chapter 3 for determining the silicon surface charge density of an MOS structure assumes a knowledge of the device capacitance as a function of applied voltage. This chapter explains the methods used in determining such information for the fabricated MOS structures. Specifically it explains how the value of C_{sc} of Figure 3.4 and equation (3.7) was determined as a function of applied bias voltage and how overall capacitance-bias voltage plots to be used in oxide charge calculations were obtained.

6.2 Correspondence Between the Data And the Equivalent Circuit

As is shown by Hofstein (1965), surface charge states cannot follow an applied signal if the frequency is equal to or greater than approximately 100 kHz. Thus for a 100 kHz test signal it was assumed that the surface charge would not change at all with a change in applied voltage and as a consequence the surface capacitance C_{ss} would be zero by defining equation (3.6). The equivalent circuit of an MOS capacitor operating in accumulation and depletion regimes thus became simply the series configuration of R_B, C_{ox}, and C_{sc}. Since Q_{sc} is the only charge in the semiconductor or at the oxide-semiconductor interface which is a function of bias voltage, C_{sc} was the only element of the equivalent circuit

which would likewise vary with bias. Due to the very strong dependence of the semiconductor capacitance, C_{sc}, on the bias voltage, a small signal, 20 millivolts rms or less, was used for the device capacitance measurements.

The capacitance bridges used for such measurements yielded device capacitance and resistance information in terms of an effective parallel resistor and capacitor circuit element configuration. Since the equivalent circuit for an MOS capacitor is in a series configuration which can, for simplicity, be assumed to be composed of one bias dependent capacitor, C, in series with a fixed resistor, R_B; the admittance of that circuit can be written as

$$Y = \frac{\omega^2 C^2 R_B + J \quad C}{1 + \omega^2 C^2 R_B^2} \tag{6.1}$$

where

ω = the excitation frequency (radians sec^{-1})

$j = \sqrt{-1}$

From this the effective parallel capacitance and conductance of the device can be written as

$$C_p = \frac{C}{\omega^2 C^2 R_B^2 + 1} \tag{6.2}$$

and

$$G = \frac{\omega^2 C^2 R_B}{\omega^2 C^2 R_B^2 + 1} \tag{6.3}$$

where

C_p = the effective parallel capacitance (farads)

G = the effective parallel conductance (mhos)

Since the capacitance-bias voltage measurements used in surface state density calculations were made at 100 kHz for devices with an effective series capacitance which was never greater than 100 picofarads and an effective series resistance which was never over 200 ohms, it became apparent that the approximation

$$C = C_p \tag{6.4}$$

was quite good. It was thus possible to use the values of capacitance obtained directly from the measurements in the calculations for surface charge density outlined in Chapter 3.

6.3 Point by Point Capacitance Data Acquisition

A general Radio 716-C Capacitance Bridge was used to obtain individual values of capacitance versus bias voltage. A block diagram of the entire measuring circuit along with the associated bias circuitry is shown in Figure 6.1. The device container used as a metal cylinder closed at the bottom with a removable metal top. A device socket was rigidly mounted inside the container. One terminal of that socket was grounded to the container and also to the measuring circuitry. A General Radio 1422-MD Presicion Capacitor was shunted across the "Unknown-Direct" bridge terminal pair along with

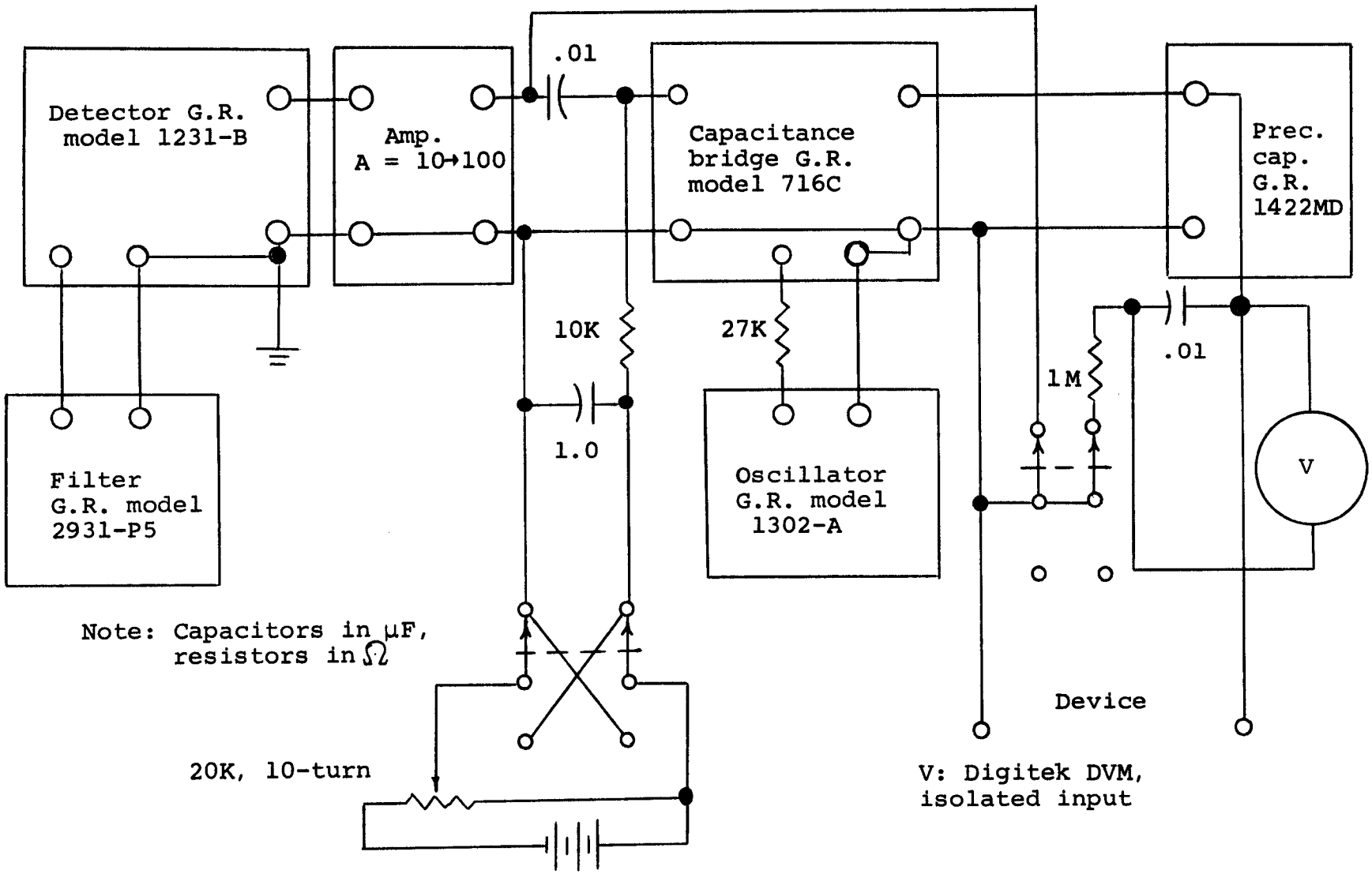


Figure 6.1. Diagram of circuitry used in acquisition of point-by-point capacitance-bias voltage data

the shielded sample container device socket leads. A simplified circuit of the bridge and biasing arrangement is shown in Figure 6.2.

In taking point-by-point capacitance data the author generally used one-tenth volt bias potential increments. A TO-5 header without a device mounted on it was placed in the socket of the device container just as a normal device and header would be for device measurement purposes. The container was then closed and the precision capacitor was set to some convenient reference value and that value recorded. The capacitance and dissipation factor controls of the bridge were then adjusted so that the bridge was balanced.

A device-bearing header was then placed in the holder in place of the empty header and the bias was set to the desired value. The precision capacitor and bridge dissipation factor controls were then adjusted to obtain a bridge balance and the set points of those controls were recorded. The device capacitance for that given bias voltage was the difference between the precision capacitor reference setting and that necessary for a null with the device in place and the bias applied.

In general, once the bridge was balanced without a device, the device was placed in the container and the bias advanced in ½ volt increments between zero and 11 volts and the bridge balanced for each bias value by means of the

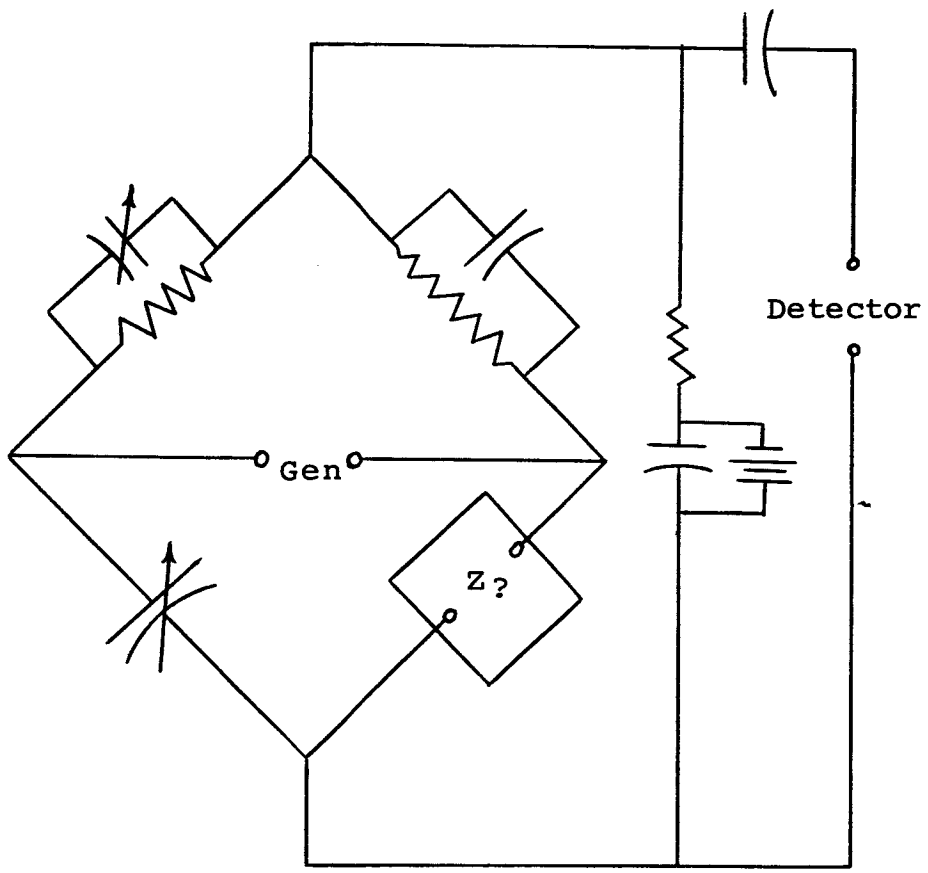


Figure 6.2. Simplified bridge circuit showing biasing arrangement

precision capacitor and the dissipation factor adjustments. Between 11 and 19 volts the vias potential was advance in one-tenth volts increments and the bridge balanced for each bias value. In this way, value pairs of capacitance and bias voltage were obtained for the entire range of bias potential and a capacitance bias curve as is shown in Figure 6.3 resulted. These value pairs were then used in the manner outlined in chapter 3 to obtain surface state density information.

6.4 Automatic Data Acquisition Technique

The General Radio 716-C Capacitance Bridge described above was used in essentially the same circuit for automatic data taking. The only modifications made to the circuit were the connection of the null meter output through a detector to the y-axis input of a Mosley, Model 3, Autograf x-y Recorder and the connection of the x-axis input of the recorder to the device terminals. The null meter output was proportional to the bridge unbalance and therefore to the device capacitance. The voltage appearing across the device was simply the bias potential which, in this case, swept linearly with time by means of a motor driven linear variable resistor and a battery. A second variable resistor allowed changing the maximum value of the voltage sweep. The time taken for the voltage to sweep from zero to its maximum value by means of the motor driven resistor was approximately

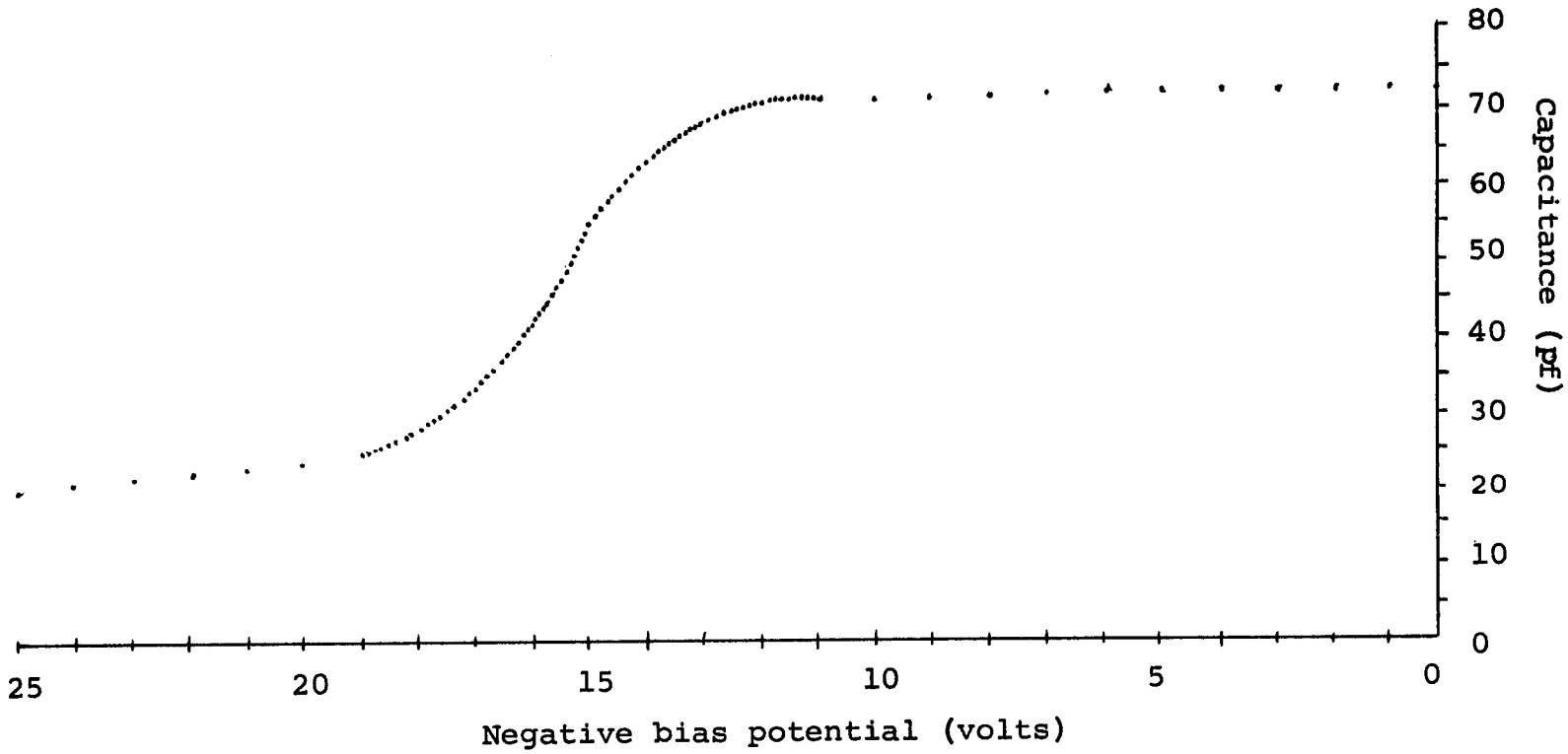


Figure 6.3. A typical point-by-point capacitance-bias voltage curve taken for an n-type device

20 seconds. A block diagram of the measurement equipment along with a schematic diagram of the bias circuitry and the x-y recorder connections is shown in Figure 6.4.

The input impedance of the x-channel of the x-y recorder was 2 megohms resistive. This value was much smaller than the effective parallel resistance of the device itself and hence acted to "mask-out" any changes in bridge output to the detector which might have been due to small changes in the series resistance, R_B, of the device. The capacitance calibration of the obtained curves was accomplished by the removal of the device from its holder and the deliberate changing of the precision capacitor from its reference setting by a known amount to cause bridge unbalance. The magnitude of that change was then noted as the capacitance increment causing the bridge to unbalance and the y-axis output of the recorder to indicate the noted amount. Generally, the precision capacitor was changed by increments of ten picofarads to calabrate a curve taken on the x-y recorder as is shown in Figure 6.5.

Since only twenty seconds were necessary to obtain a capacitance-bias voltage curve by means of the recorder whereas approximately four and one-half hours were necessary to obtain the same curve by the point-by-point method, the automatic curve plotting equipment proved invaluable in obtaining, trend, confirmation, and oxide charge change data.

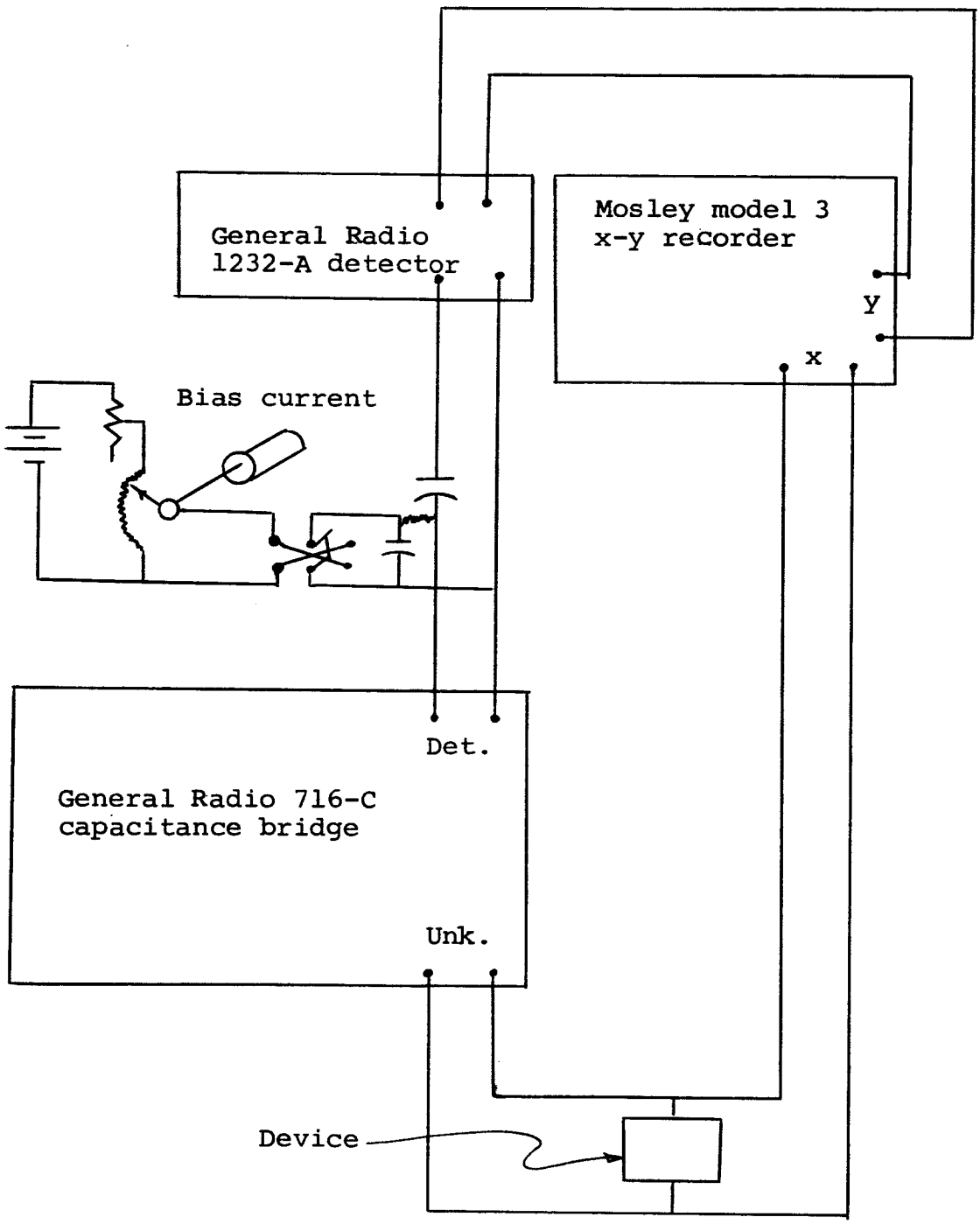


Figure 6.4. Diagram of automatic capacitance-bias voltage plotting equipment

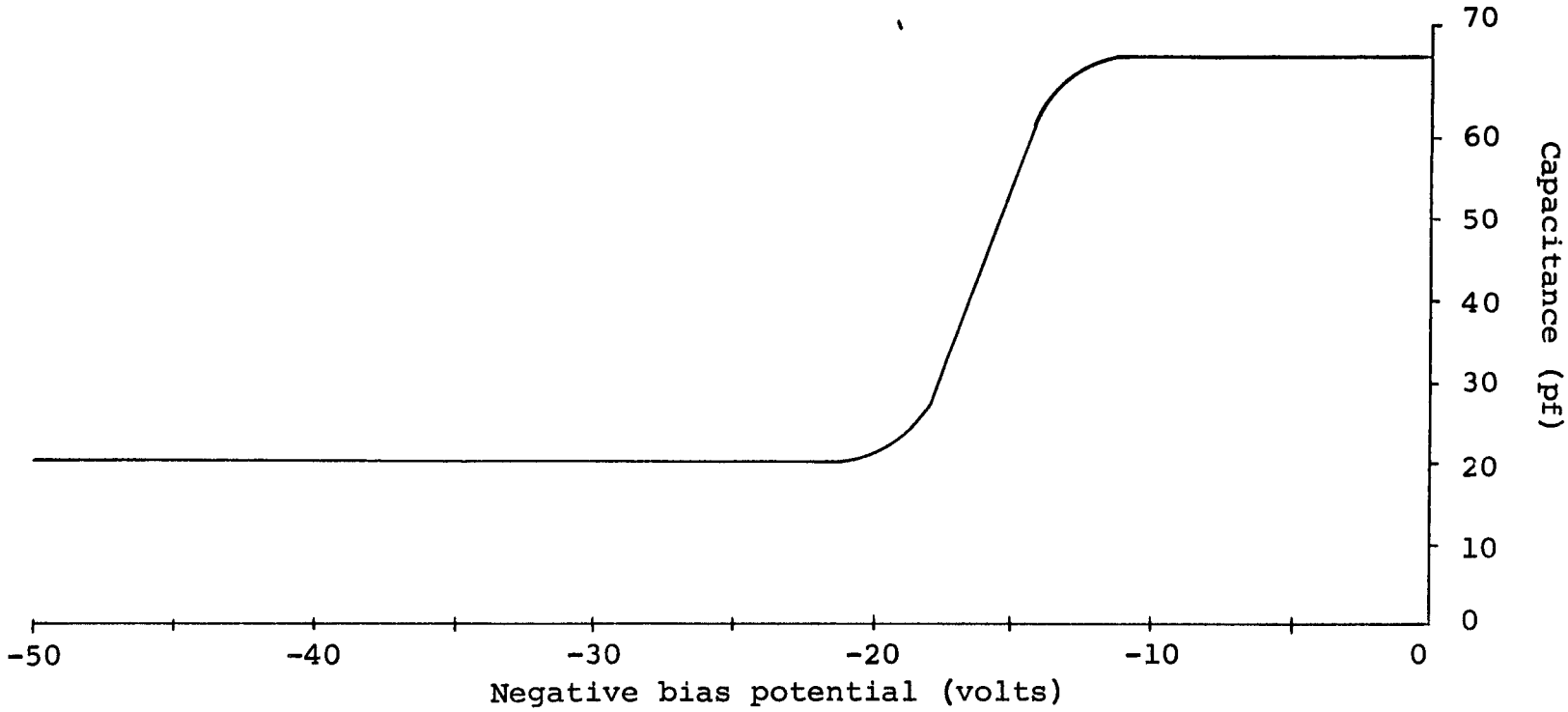


Figure 6.5. A typical capacitance-bias voltage curve for an n-type device obtained by means of the x-y recorder

6.5 Accuracy of Measurements

Since the General Radio 1422-MD Precision Capacitor was used as the capacitance indicating element in the point-by-point data system described in section 6.3, and as the capacitance calabration element in the automatic data systems described in section 6.4, its accuracy will be discussed first. The manufacturer states that the 1422-MD capacitors are calibrated by comparison at 1kHz to a precision better than $\neq$ (0.01% $\neq$ 0.00001 pF) with working standards whose absolute values are known to an accuracy typically $\neq$ 0.01%. This being known, the item next in importance is the resolution with which one can read the capacitance dial. This is nominally 1/50 of a small division or 0.1pF for the range used by the author. The manufacturer states also that the capacitance change with time is less than one scale division or 0.2 picofarads per year.

The normal bridge balancing technique of adjusting the dissipation factor indicator and the precision capacitor several times to be sure of the null was used. The final movement of the precision capacitor dial in each of the two measuring techniques and in setting the reference value of capacitance was always made in the direction of an increasing dial reading in order to prevent any backlash error.

A common source of error in low capacitance, high frequency measurements is the failure of the person doing the

measuring to take into account the capacitance of the device leads and its variation with lead placement and position. Such a source of error was circumvented by using a device holder which insured the same lead position each time, and also by balancing the bridge with all components except the actual silicon device in place.

The voltmeter used to set the bias values for the point-by-point data acquisition was a "Digiatec 220" digital voltmeter manufactured by the United Systems Corporation and guaranteed to have an accuracy of 0.1% full scale. Its internal impedance was 2.2 megohms resistive. The fact that the relatively low internal impedance of the meter did not cause erroneous bias settings due to resistor voltage drops in the bridge or bias circuit was born out by confirming voltage readings made with a Keithley 610-B Electrometer which had an internal impedance greater than 10^{14} ohms.

The voltage scale on the x-axis of the x-y recorder was set by an internal standard. That voltage calibration was checked against the Keithley 610-B Electrometer. Both were found to correspond exactly as far as could be determined from the recorder.

Finally, the frequency of the generator, a General Radio 1302-A Oscillator, was measured by means of a General Radio 1130-A Digital Time and Frequency Meter. The accuracy of this meter is reported by the manufacturer to be $\neq$ 0.01% at 1 volt rms for 10 period measurements.

6.6 High Frequency Measurements

The capacitance value which the capacitance-bias voltage curve is asymptotic to when the device is operated in the accumulation regime is called the oxide capacitance only if it is invariant with frequency as is shown by Zaininger (1964). The main cause for this capacitance to be frequency dependent is the presence of a wedge-shaped boarder at the edge of the metal gate-electrode. It was believed that the large spacing used between the metal-bearing filaments and the wafer in the vacuum system and also the intimacy with which the evaporation mask contacted the oxidized wafer would prevent such a "penumbra effect" on the gate electrodes and thus a frequency dependence of the oxide capacitance. To be sure that the asymptotic accumulation-regime-capacitance seen at 100 kHz was the oxide capacitance; that same device was used in measurements at 1 kHz, 10 kHz, 50 kHz, and 1 MHz. A Boonton 250-A, R-X Meter was used for the 1 MHz measurement while the General Radio 716-C Capacitance Bridge was used for all others. A biasing circuit was not necessary since an n-type device which was in the accumulation regime of operation at zero bias was measured with zero gate biasing potential. Figure 6.6 shows the capacitance which was truly invariant with frequency. Because of the results of the above measurements, the capacitance value which the capacitance-bias voltage curve was found

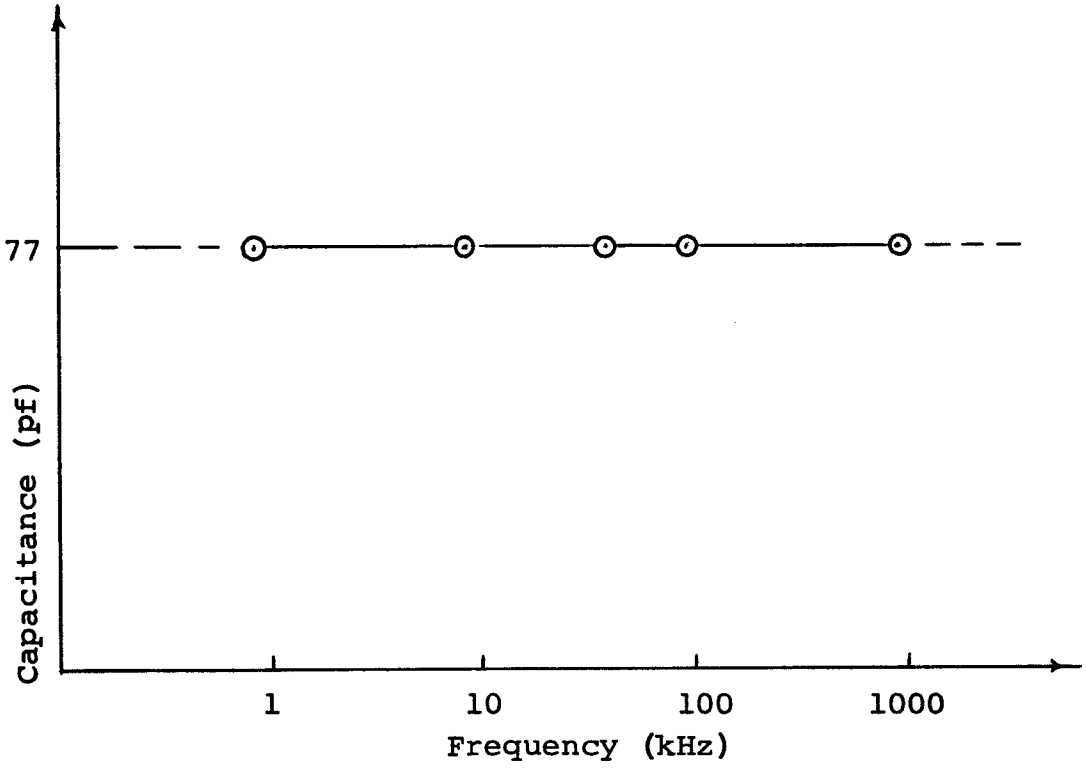


Figure 6.6. Measured accumulation regime capacitance versus measurement frequency for a typical device

asymptotic to at 100 kHz, was used as the oxide capacitance. The necessity of knowing the true oxide capacitance for each device can be explained by noting from equation (3.23) that the $dV_{sc}/d\psi_s$ versus V curve would be shifted vertically if the oxide capacitance value were changed. Such a shift would cause the incorrect semiconductor surface doping concentration to be used in the subsequent calculations which would thus yield incorrect surface charge density versus surface potential information. The calculations and conclusions of the remaining chapters depend strongly upon the details of device construction and measurements outlined thus far.

7. NON-IRRADIATION ANNEALING DATA

7.1 Introduction

Both n-and p-type MOS diodes fabricated according to the techniques of Chapter 5 were investigated by thermal annealing techniques. These investigations indicated the presence of highly mobile ions in the dielectric SiO_2. The polarity of the majority of the oxide ions was seen to be positive since devices fabricated on both n-and p-type substrates exhibited n-type surface properties with zero bias potential applied to the gate. The following sections explained the annealing techniques used, present the annealing data for both n-and p-type devices, and indicate the results of calculations based on that data.

7.2 Annealing Procedures

A Lab-Line 3620 Vacuum Oven was used as the temperature chamber for the annealing process. The oven temperature ranged from 50 to 100°C while the annealing periods ranged in length from one minute to three days. After the capacitor was placed in the oven device holder the oven was sealed, the bias applied from gate to substrate, and the oven pumped down to approximately 20 inches of water. After exactly one minute of pump-down time the oven was backfilled to atmospheric pressure with argon to provide an inert atmosphere and prevent any elevated temperature surface reactions. During the remainder of the annealing period argon was allowed

to flow into the chamber at a rate of approximately two cubic centimeters per minute. This was done to keep atmospheric air from entering the chamber through the small cracks which appeared around the oven door when the oven pressure was not below atmospheric.

At the end of the annealing period the device was moved from the oven to a thermal quenching chamber which maintained the annealing bias across the device while flushing it with pre-purified nitrogen for one minute. The cooling gas was at room temperature and flowed at the rate of approximately 45 cubic feet per minute. In moving the device from the oven to the thermal quenching chamber the author took care not to short-circuit the device header leads since the oxide field perturbation caused by such an action would no doubt have caused some oxide ionic charge redistribution in cases where the anneal just completed had not been done under short-circuit bias conditions. At the end of the thermal quenching period the device was placed in the measurement chamber described in the previous chapter, and a capacitance-bias potential curve was automatically plotted for that device. The following section will discuss the obtained results.

7.3 General Annealing Results For n-type Material

In all, 25 n-type and 25 p-type devices were fabricated and individually mounted. Of the 25 n-type devices six were

investigated by means of a sequence of annealing tests. The results obtained were the same in each case and are presented for one representative device in this section.

Figure 7.1 shows capacitance-bias voltage curves for an n-type device which has been annealed with both positive and negative gate bias applied during different annealing periods. Curve 1 was taken before any annealing was carried out. Curve 2 was taken after a 12-hour anneal at 75°C with a -5.0 volt bias applied to the gate. The movement of curve 2 toward a less negative bias voltage with respect to curve 1 indicated that less bias voltage was necessary to deplete the semi-conductor surface of electrons. This implied that fewer electrons were initially present at that surface after the negative bias anneal since the corresponding positive charge in the oxide was drifted to the metal-oxide interface. It was found that the capacitance-bias voltage curve for the device could not be moved to a less negative bias value by means of a longer annealing period, a higher temperature, or a more negative bias potential. Hence the curve was said to be located at the "negative saturation" position for the device. Snow et al. (1965) noted the same effect due to device annealing with a high temperature and negative bias applied to the metal gate electrode as is discussed in chapter 4.

The application of a positive 5.0 volt bias for an annealing period of one hour at 75°C caused the positive oxide

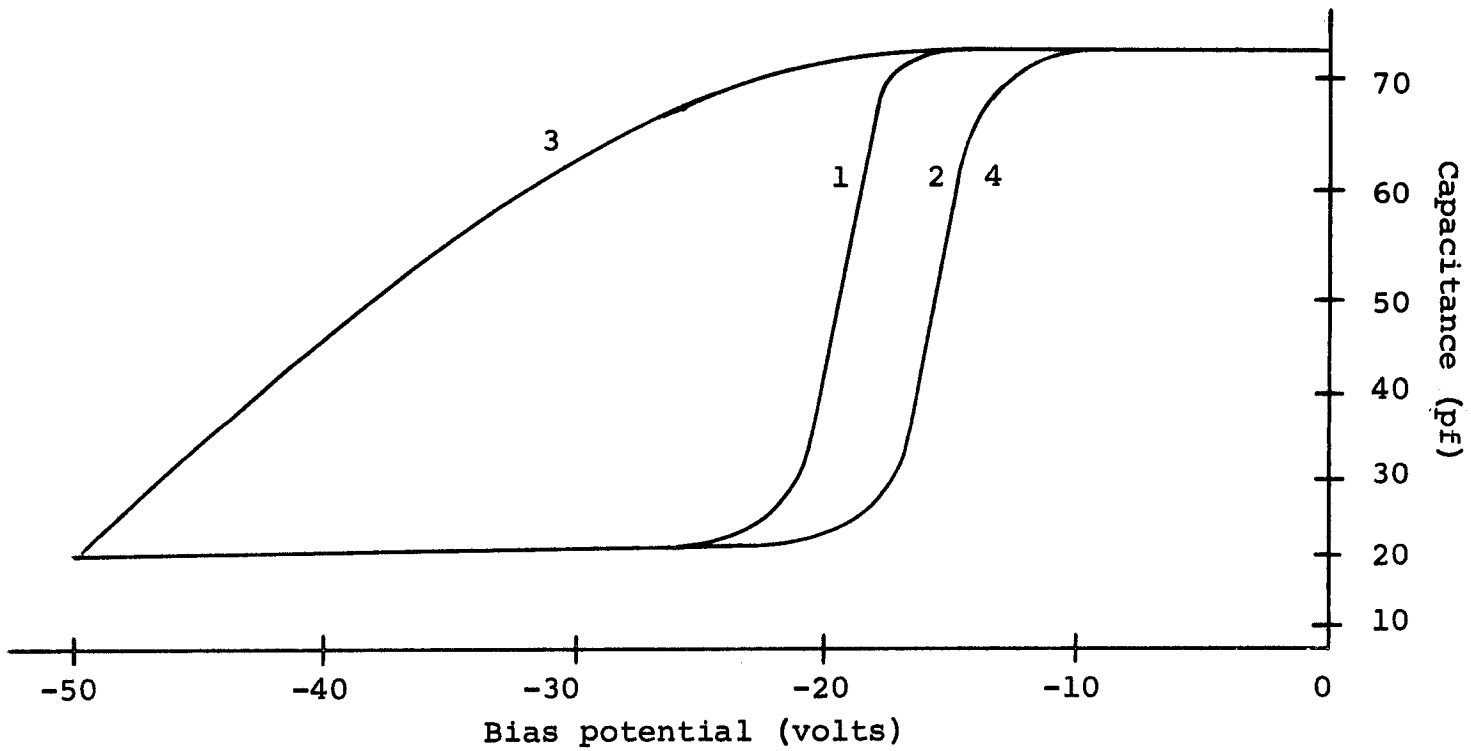


Figure 7.1. Capacitance-bias voltage curves for a typical n-type device: curve (1) was taken prior to annealing; curve (2) was taken after a 12 hour, 75°C anneal with -5.0 volt bias applied; curve (3) was taken after a 1 hour, 75°C anneal with +5.0 volt bias applied; curve (4) was taken after a 4 hour, 75°C anneal with a -5.0 volt bias applied

charge to drift to the oxide-semiconductor interface and thus attract a negative charge of equal magnitude to the semiconductor surface. A much larger negative bias was thereafter needed to achieve the same degree of semiconductor surface charge depletion as was possible with curves 1 and 2 for smaller bias values as can be seen from curve 3 of Figure 7.1.

Chapters 3 and 4 show that a parallel horizontal shift of a capacitance-bias voltage curve is evidance of a change in oxide charge distribution wereas a change in derivative of the more nearly vertical, accumulation to depletion transition, portions of the curve is evidence of a change in the density of charge states located at the semiconductor surface. It can be seen from curve 3 of Figure 7.1 that the positive-bias anneal caused not only a change in the oxide charge distribution but also an increase in the silicon surface charge density. A subsequent negative-bias anneal for a period of four hours caused both the oxide charge and the silicon surface charge to return to their negative saturation distributions and densities as can be seen from the resulting curve 4 of Figure 7.1.

Since the oxide charge distribution of a device is not always the same before an elevated temperature anneal the negative saturation oxide charge configuration was chosen as a reference or initial distribution for a series of

capacitance-bias voltage curve movement studies which will now be discussed. The device was originally annealed at 100°C with a -5.0 volt bias in order to affect the charge changes necessary for the movement of the capacitance-bias voltage curve to the negative saturation position as shown by curve 1 of Figure 7.2. A +5.0 volt bias applied during each of four five minute annealing periods at 100°C caused the curve to move, each time, toward a more negative bias voltage as is shown in Figure 7.2 by curves 2, 3, 4, and 5. This data shows that the positive charge located in the oxide was drifted from its initial negative-saturation position at the metal-oxide interface to the oxide semiconductor interface where it caused stronger surface inversion and an increase in silicon surface charge density.

The device was annealed for a period of one hour at 100°C with a -5.0 volt bias applied in order to cause the capacitance-bias voltage curve to return to its negative saturation position. The device curve was then in the position of curve 1 of Figure 7.2. A -5.0 volt bias was applied for annealing periods ranging in length from five minutes to 24 hours during which the device temperature was maintained at 100°C. No noticeable change was found in the shape or position of the device capacitance-bias voltage curves. It is evident from this data that the initial negative-bias anneal was sufficient to drift nearly all of the positive oxide charge

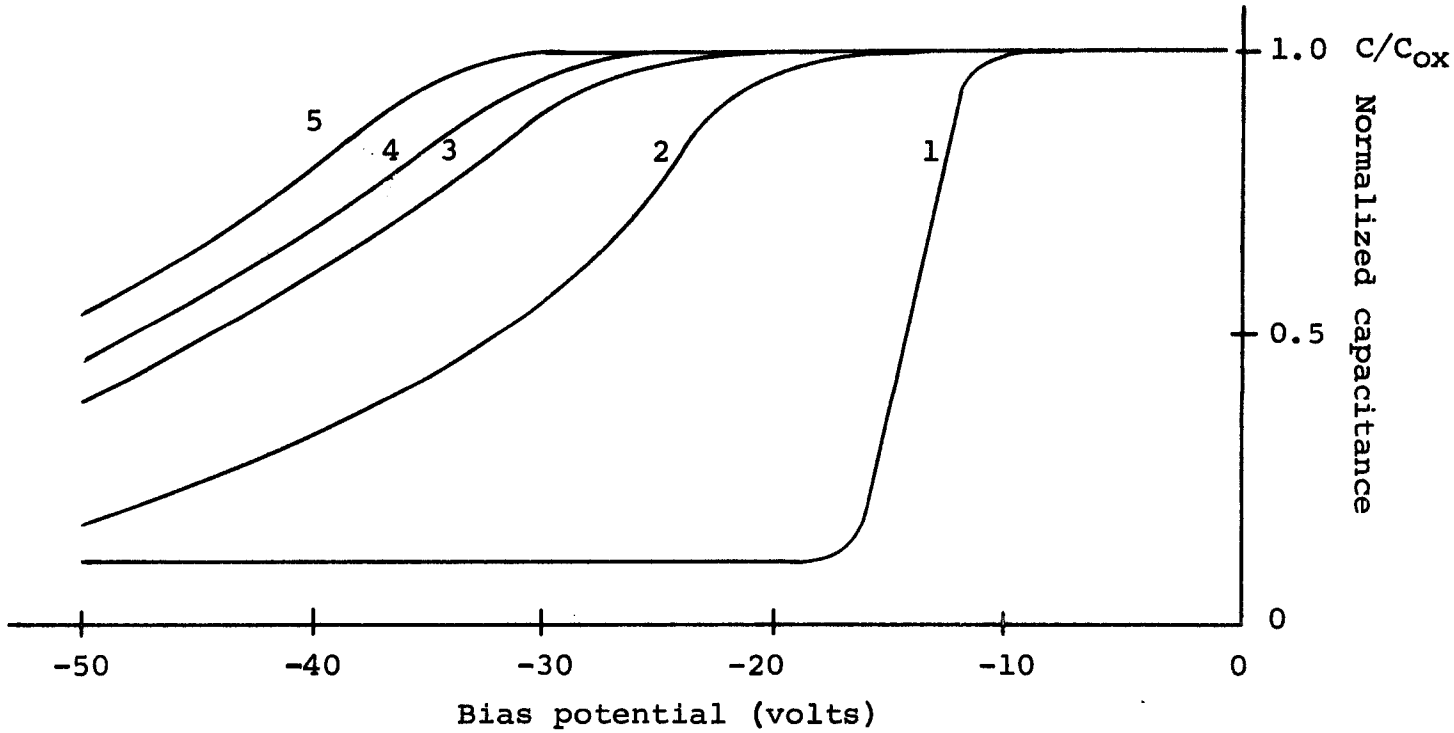


Figure 7.2. Capacitance-bias voltage curves for an n-type device: curve (1) was taken after a 1 hour, 100°C, -5.0 volt anneal; curves (2) through (5) were each taken after a 5 minute, 100°C, +5.0 volt anneal

to the metal-oxide interface and that any further annealing with a negative gate bias voltage had no noticeable effect.

The device was once again annealed at 100°C with a -5.0 volt bias applied in order to return it to its negative saturation condition. A series of 100°C anneals were then carried out during which the device was short circuited. It was found that after each short circuit anneal, the device capacitance-bias voltage curve was in the negative saturation position. This is to be expected on the basis of the work of Snow et al. (1965), and specifically upon equation (4.1) which gives the metal gate electrode image charge for a general oxide charge distribution.

The device was finally returned to its negative saturation condition by a 100°C anneal during which a -5.0 volt bias was applied to the gate electrode. It was then annealed at 100°C for various amounts of time while being open circuited. The general movement of the curve was from the negative saturation position to some intermediate position to the left of the former as shown by curve 1 and 2 in Figure 7.3. A certain amount of instability was noted in that the capacitance-bias voltage curve taken at different time intervals oscillated about an intermediate position shown in curve 2 of Figure 7.3. This indicates that the oxide charge which was originally situatied quite closely to the metal gate in the negative saturation condition was redistributed due to the thermal agitation in the absence of any fixed bias. It is believed

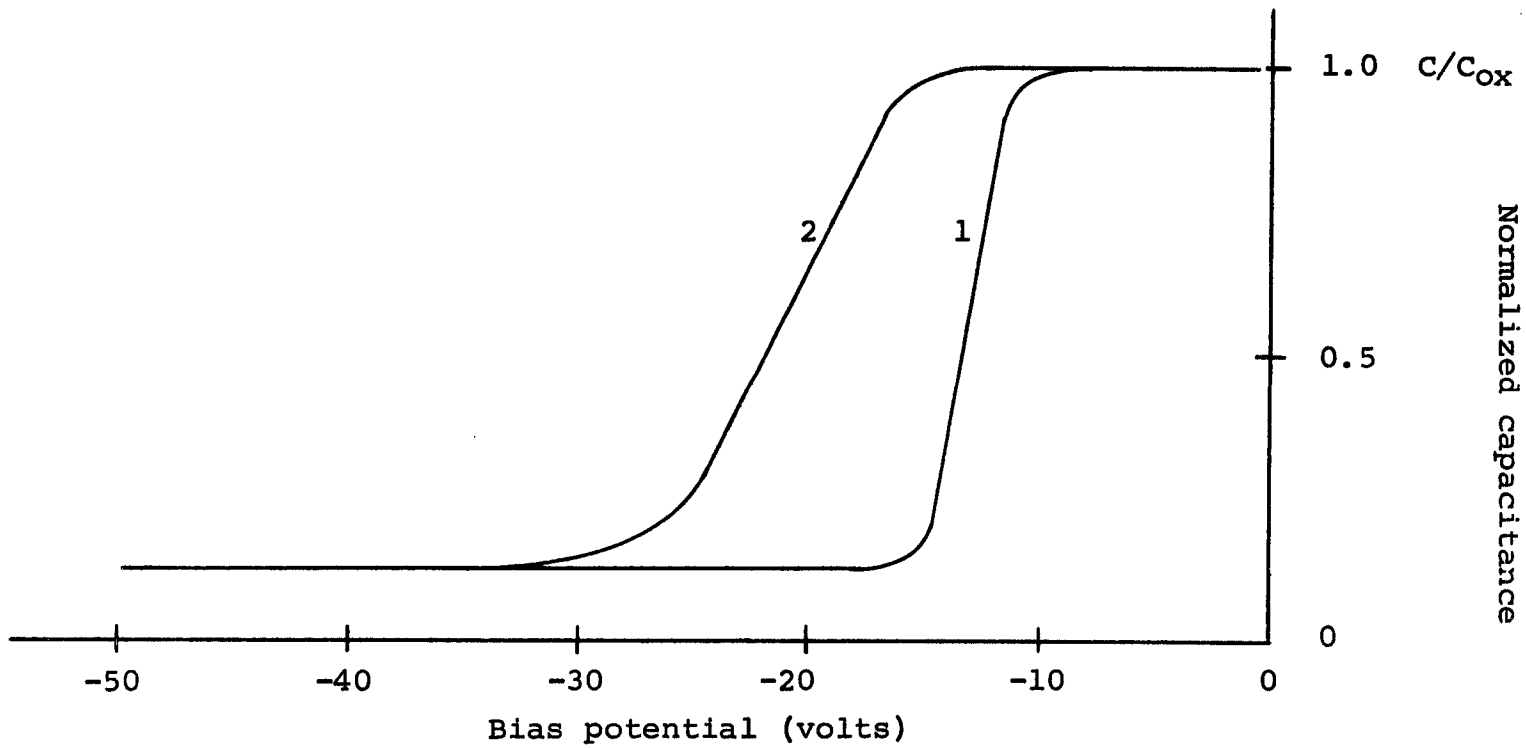


Figure 7.3. Capacitance-bias voltage curves for an n-type device: curve (1) was taken after a 100°C, negative bias anneal and is in the negative saturation position; curve (2) is in the intermediate position resulting after a 100°C, open-circuit anneal

that the instability of the capacitance-bias voltage curves during the open-circuit anneal is closely related to the semiconductor surface noise reported on by Jordan and Jordan (1965).

Although there was no well-defined obtainable positive saturation position of the capacitance-bias voltage curve; it was found that, by the application of a positive bias under elevated temperature conditions for a sufficiently long period of time, the curve did move to a completely horizontal position located at the oxide value of capacitance. This curve was very reproductable and hence used as the initial curve for positive, negative, open circuit, and short circuit bias annealing studies similar to those which were reported above for the negative saturation position. The expected results were obtained and are presented in summary in Table 7.1.

7.4 General Annealing Results for p-type Material

MOS capacitors fabricated on p-type substrates were examined in much the same way as were those fabricated on n-type material discussed in the foregoing sections. In general, the mobile ion model proposed above was confirmed by the findings. p-type structures were, however, found to be inherently unstable under thermal stress. The same annealing temperature range as was used for n-type substrate devices

Table 7.1 Summary of annealing trends for n-type substrate MOS capacitors

Annealing bias	Initial position: From a negative saturation position	Initial position: From a position saturation position
After positive bias	Move toward greater negative bias	No movement
After negative bias	No movement	Move toward less negative bias
After short-circuit	No movement	Move toward less negative bias
After open-circuit	Move to intermediate position	Move to intermediate position

was found to cause many of the p-type substrate devices to develop gate-to-substrate short circuits. Because of this inherent instability, it was impossible to obtain the amount of data for these devices as was obtained for the n-type substrate structures. The salient features of the obtained data will now be discussed.

The surface of a p-type substrate device was always found to be inverted to n-type as can be seen from the

characteristic capacitance-bias voltage curve shown in Figure 7.4. It was noted in Chapter 3 that the value of capacitance to which the curve was asymptotic in the inversion regime was a function of how well the substrate minority carriers could follow the applied test signal. If only the section of substrate under the gate electrode is considered, Hofstein (1965) has shown that typical response cutoff frequencies for minority carriers are between 10 and 100 Hz. For this reason one should observe the dotted portion of the capacitance-bias voltage curve of Figure 7.4 in the depletion and accumulation regimes of operation. The solid portion of that curve can however be seen because of coupling of the inversion layer under the gate to the remaining semiconductor surface as is explained by Zaininger (1964) and is shown in Figure 7.5. Such inversion layer coupling can be eliminated by a polarization of the surface external to the gate area is also shown in Figure 7.5. This surface polarization technique was used in most of the data acquisition on p-type material in order that only the actual device region located under the gate be allowed to contribute minority carriers and hence be a part of the measurement.

It was found that the application of a negative gate bias to the device during elevated temperature annealing caused the capacitance-bias voltage curve to shift toward less negative values of gate bias. This is shown in Figure 7.6

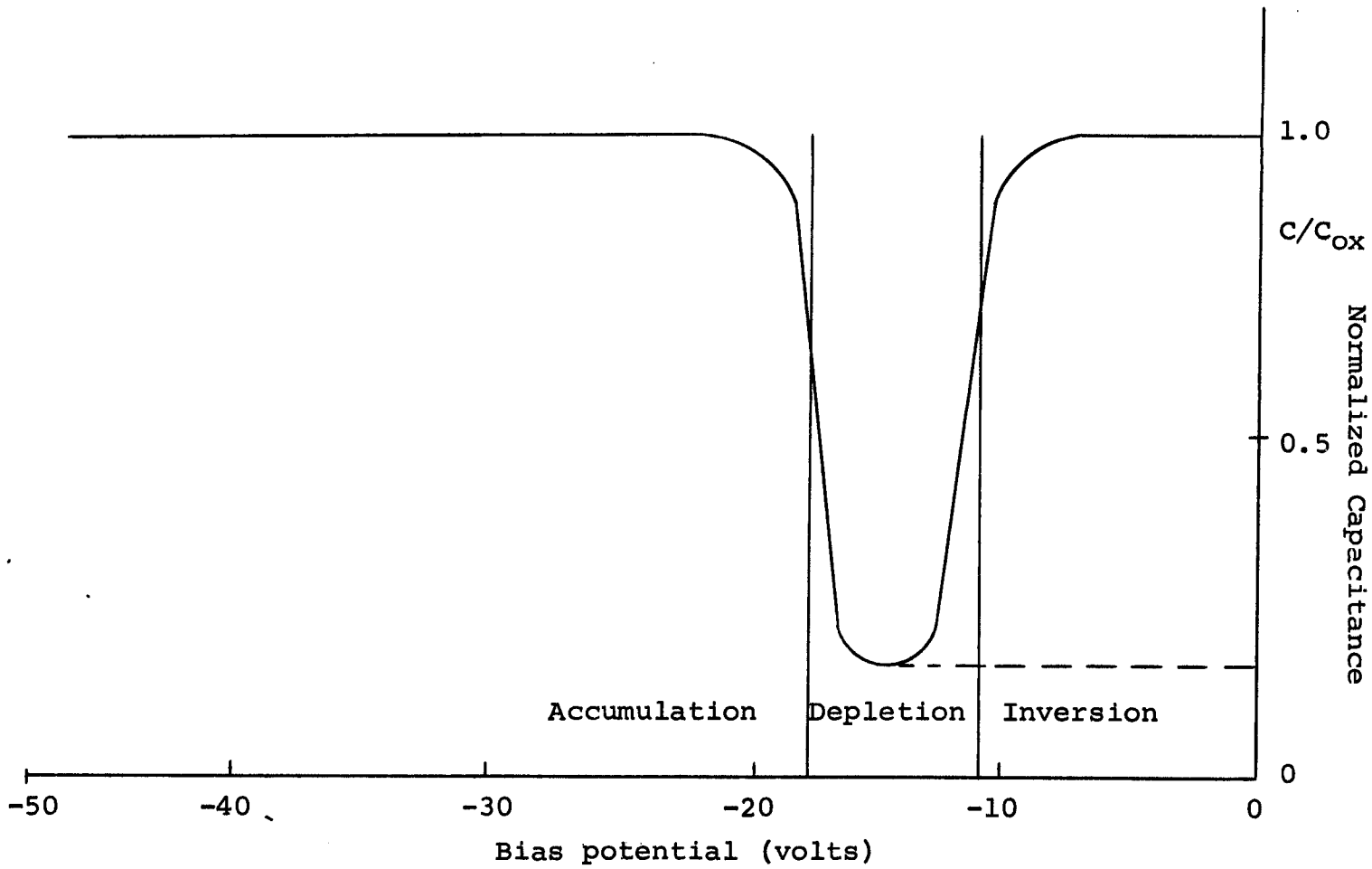
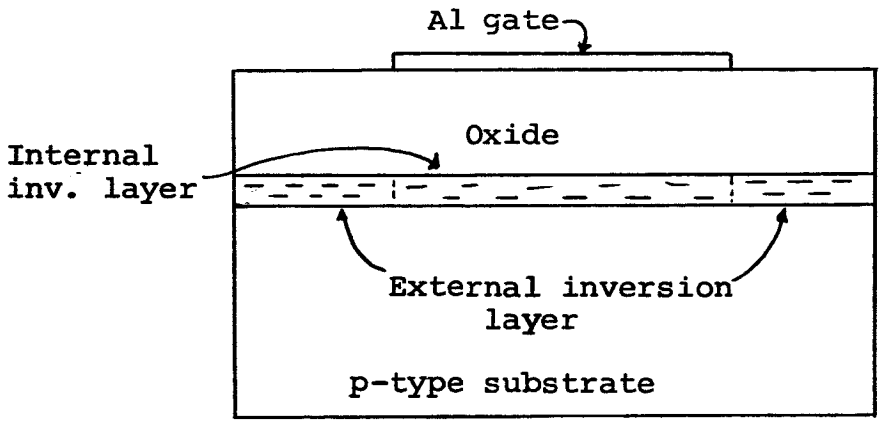
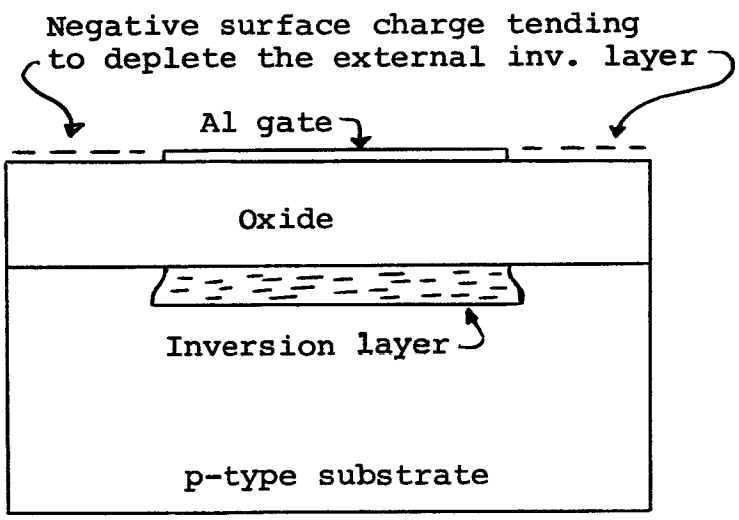


Figure 7.4. A typical capacitance-bias voltage curve for a p-type device with the operation regimes shown



(a)



(b)

Figure 7.5. MOS device diagrams showing the device coupled to the external wafer in (a) and a decoupled device in (b)

where curve 1 is the original device curve while curve 2 was taken after a negative bias anneal. It was also found that an increase of time, temperature, or negative bias voltage for the annealing period would not cause further curve movements. Thus, curve 2 of Figure 7.6 is said to be in the "negative saturation" position. This data indicates that the electric field in the oxide due to the negative gate bias caused the mobile positive oxide charges to move toward the metal gate and thus cause less negative charge to appear at the semiconductor surface. This is predicted by equation (4.2) which gives the semiconductor surface charge as a function of the oxide charge.

The application of a positive bias during an annealing period caused the device-capacitance curve to invert to that of an n-type device. Figure 7.7 shows curve 1 in the negative saturation position and curve 2 which resulted after a positive bias anneal. This data indicates that the positive oxide charge, made mobile by the elevated temperature, drifted to the oxide-semiconductor interface region of the oxide due to the impressed electric field. Equation (4.1) shows that a sheath of charge located within a strip consisting of 1% of the oxide, at the semiconductor surface, will cause that same magnitude of charge to be attracted to the semiconductor surface. The corresponding negative charge located at the semiconductor surface was present in such a copious quantity

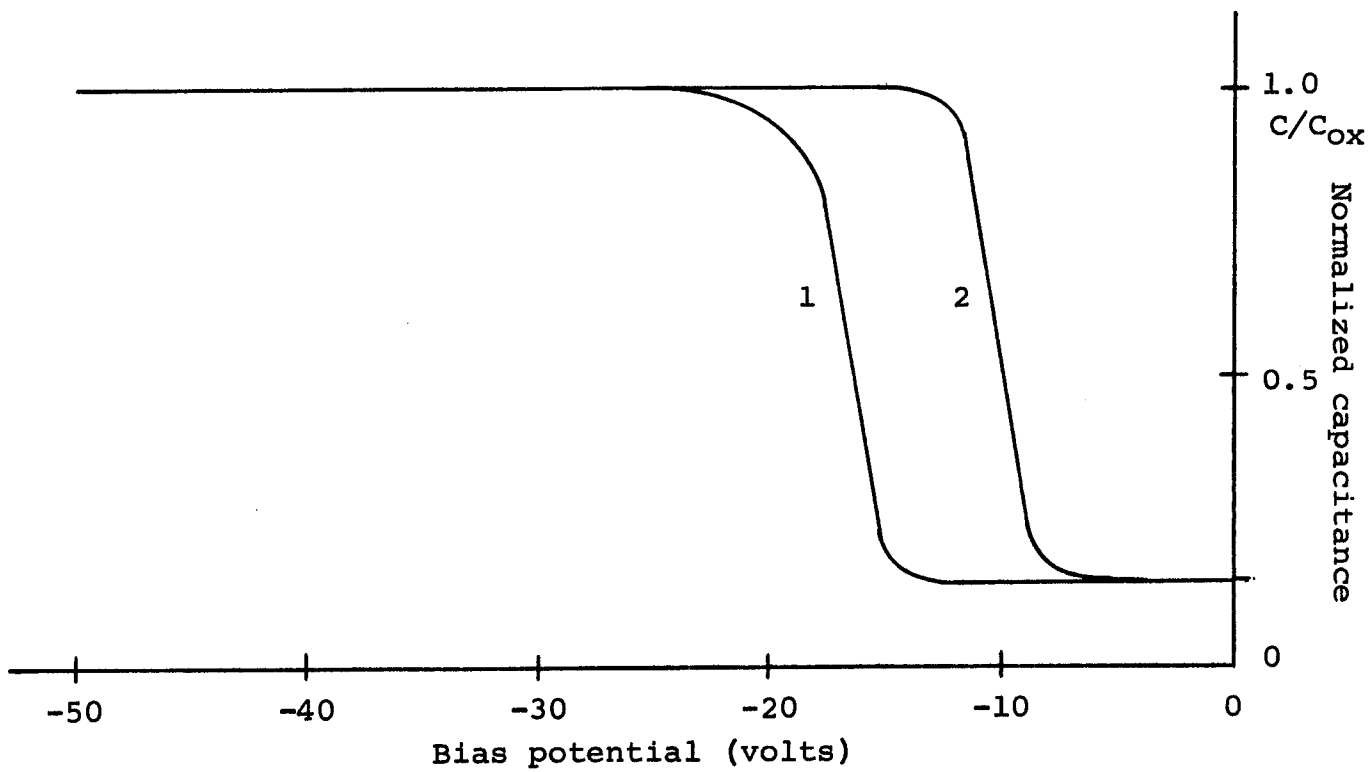


Figure 7.6. Capacitance-bias voltage curves for a typical p-type device: curve (1) was taken before any annealing while curve (2) was taken after a negative bias anneal

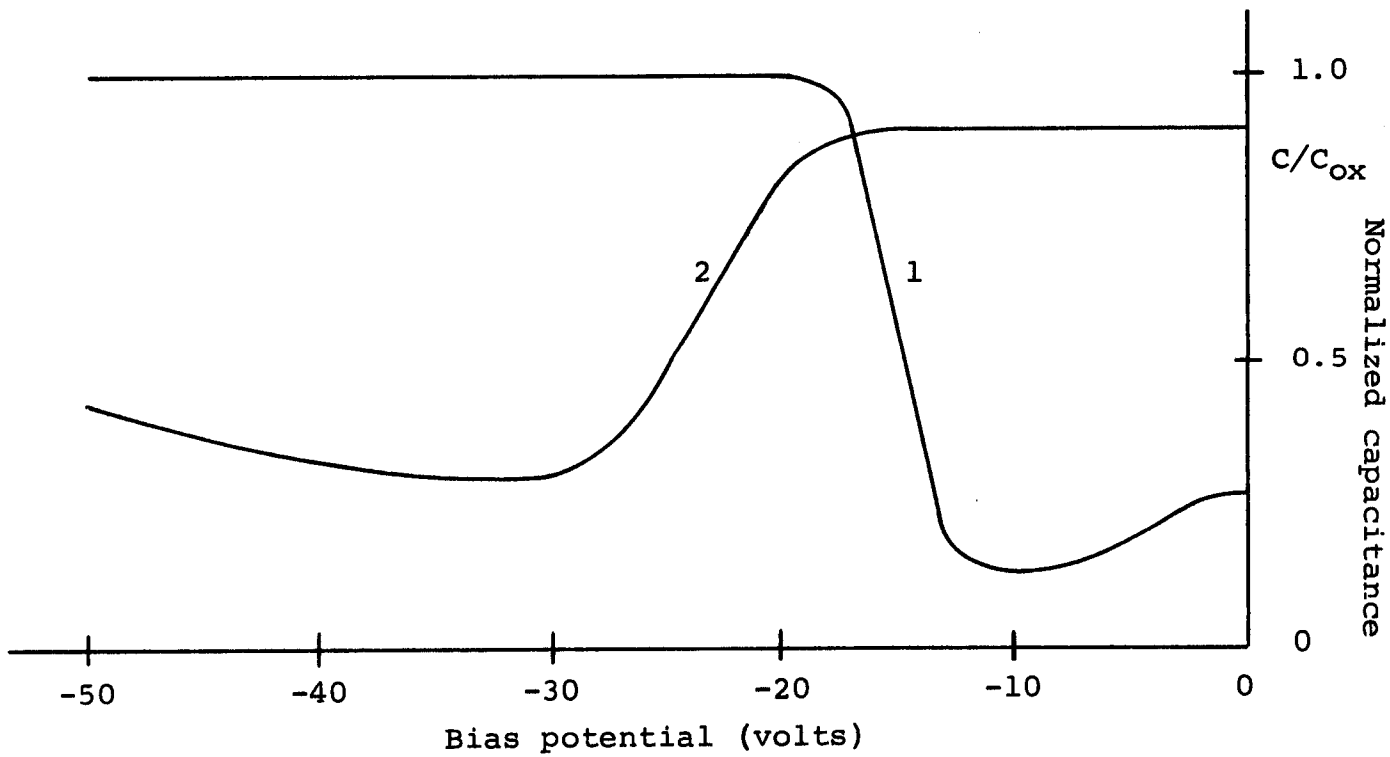


Figure 7.7. Capacitance-bias voltage curves for a typical p-type device showing the effect of permanent surface inversion: curve (1) is in the negative saturation position while curve (2) was taken after a 75°C, positive bias anneal

that it was able to respond to the 100 kHz test signal. The fact that the device curve begins to indicate higher capacitances with greater negative voltages near the high voltage end indicates that the device has gone into the inversion regime of operation and an increasing number of minority carriers (minority carriers at the surface but majority carriers in the substrate bulk) were able to follow the test signal. Although this effect closely resembles the hysteresis effect discussed by Hofstein (1965) it is by no means related thereto since it is not time-dependent.

It was also found that a subsequent negative bias elevated temperature anneal caused the device curve to return to the negative saturation position. Positive bias annealing tests were carried out on six devices and this effect was noted on each.

A negative bias anneal after the device was returned to the negative saturation condition was found to cause no change in the device capacitance-bias voltage curve as was noted for n-type devices. Similarly, no curve change was noted after a short-circuit anneal of a device which was previously in the negative saturation condition. The device curve did, however, move to an intermediate position after an open circuit anneal of a device which was previously in the negative saturation condition. Figure 7.8 shows curve 1 which is for the device in the negative-saturation condition and curve 2 which is in

the intermediate position described above. As can be seen the trends noted for p-type substrate devices are in general the same as those noted for n-substrate devices. Thus, devices fabricated on n-type material were utilized to investigate oxide charge transfer rates in both drift of that charge from the negative saturation distribution and recovery of the charge to that initial distribution. Those investigations along with a temperature-time determination of the mobile ion activation energy are discussed in the next section.

7.5 Oxide Charge Transfer Rates

As mentioned above, it was possible to completely recover the oxide and surface charge states to their negative satusation configuration after any type of anneal. This fact made it possible to study oxide charge transfer rates at different temperatures on the same device. For each study an n-type device was annealed with a negative bias applied to the gate in order to affect any charge change necessary so that the negative saturation charge configuration would result. Several short-term positive bias anneals were then carried out and a capacitance-bias voltage curve taken after each. The curve shift noted was attributed entirely to an oxide charge increase at the oxide-semiconductor interface. It was realized that any charge increase at that interface implied an oxide charge decrease of the same amount at the metal-

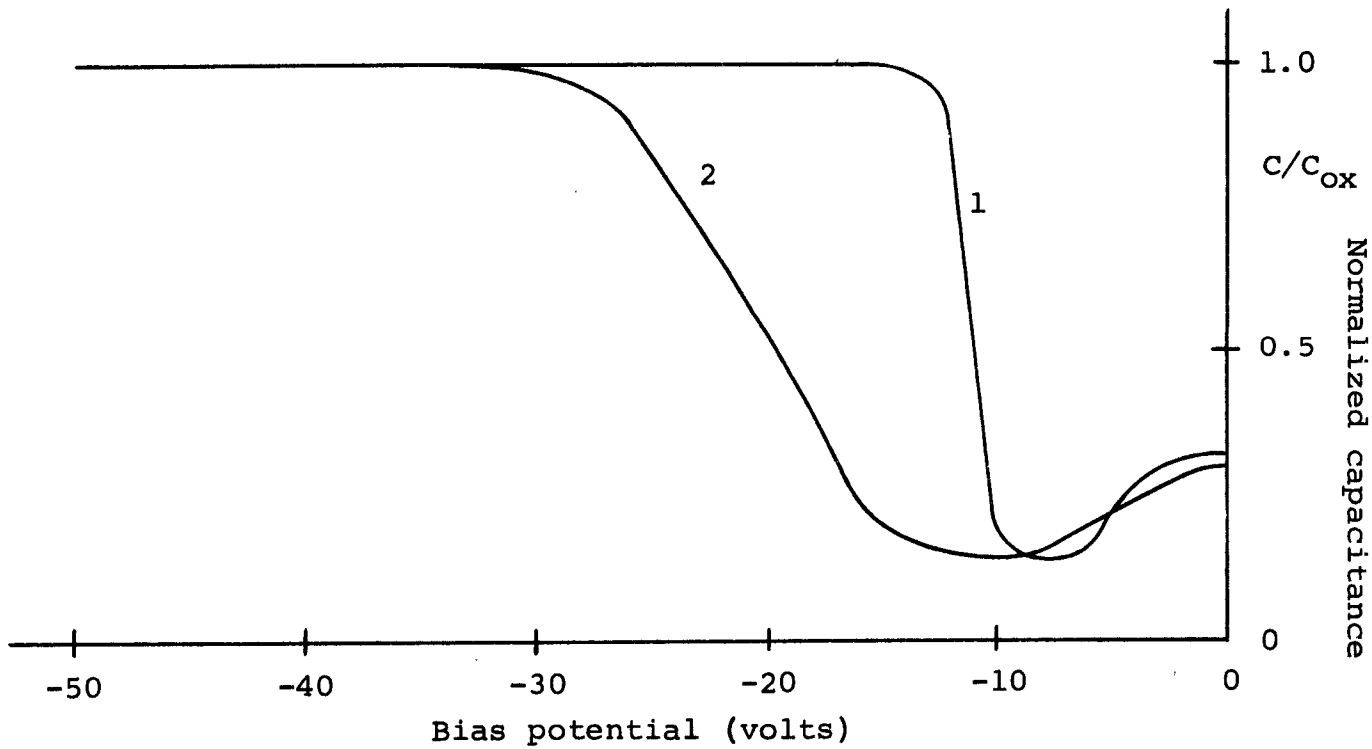


Figure 7.8. Capacitance-bias voltage curves for a p-type device: curve (1) is in the negative saturation position while curve (2) was taken after a 75°C, open circuit anneal

oxide interface. Zaininger (1964) showed that the Debye length of the oxide for a typical charge concentration of 10^{19} cm^{-3} was on the order of 10 angstroms. Thus the oxide charge decrease at the metal-oxide interface played a negligible role in equation (4.2) and hence in inducing surface charge in the semiconductor.

Since a drift of oxide charge to the oxide-semiconductor interface was seen to cause an increase in substrate surface charge density, care had to be taken in the interpretation of the capacitance-bias voltage curves. Curve 1 of Figure 7.9 is for an n-type device in the negative saturation condition while curve 2 is for the same device after a five minute anneal at 75°C during which a -3.0 volt gate bias was applied. The fact that a change in oxide charge distribution causes a parallel shift in the capacitance-bias voltage curves was shown by Snow et al. (1965) and is presented in chapter 4. That an increase in semiconductor surface charge density causes only a decrease in capacitance-bias voltage curve slope and not a curve shift along the voltage axis was shown by Zaininger (1964) and is discussed in chapter 8. Both a horizontal shift and slope change are seen in the device curves after positive bias annealing. The two are, however, relatively easy to separate since the latter does not occur for all values of bias voltage as does the former. The dashed portion of curve 2 in Figure 7.9 illustrates the form which

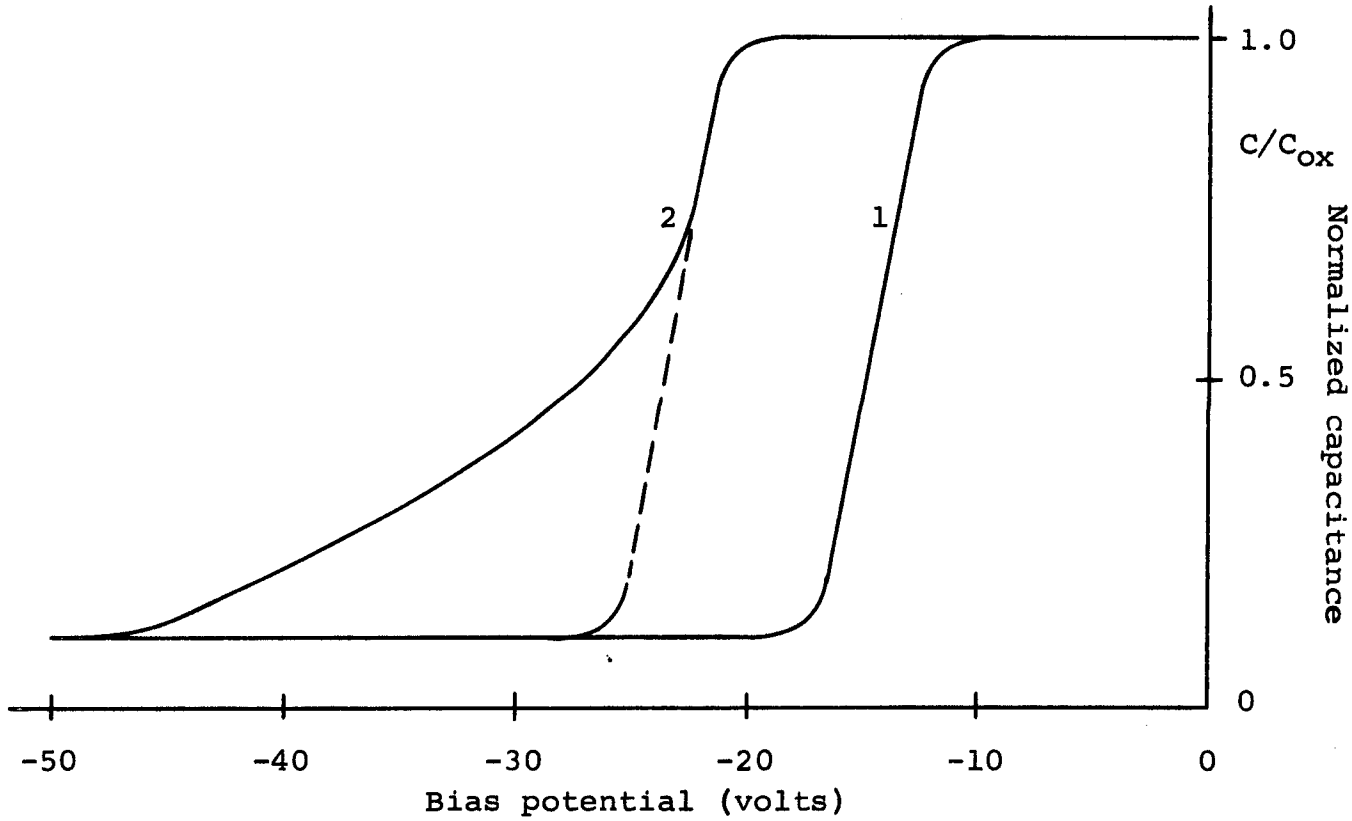


Figure 7.9. Capacitance-bias voltage curves for an n-type device: curve (1) is in the negative saturation position while curve (2) was taken after a 5 minute, 75°C, +3.0 volt anneal

that curve would have taken if the slope had not decreased for all bias voltage beyond a certain value. This technique of extending the capacitance-bias voltage curve from the parallel-shift portions to the region in which the slope had decreased is believed to produce very nearly the same curve as would have resulted in the absence of a surface state charge increase. No reproducability problems were encountered in the use of this technique, hence, it was employed in the reduction of the data presented in the remainder of this chapter.

An annealing bias potential of +3.0 volts was used throughout the device temperature-time studies. Figure 7.10 shows a set of capacitance-bias voltage curves for a positive bias anneal at 75°C. Curve 1 is for the device in the negative saturation condition while curves 2 through 5 were each taken after a five minute positive bias anneal. The above-mentioned system for determining the curve position after a parallel movement was used. Figure 7.11 shows the bias voltage curve displacement and also the calculated oxide charge transfer as a function of time for both the positive bias drift and the negative bias recovery. The charge calculation was made by means of the equation

$$C_{ox}\Delta V = \Delta Q_s \qquad (7.1)$$

which is the incremental form of equation (4.6).

The same device was returned to the negative saturation condition and annealed with +3.0 volt bias at 62°C. Curve 1

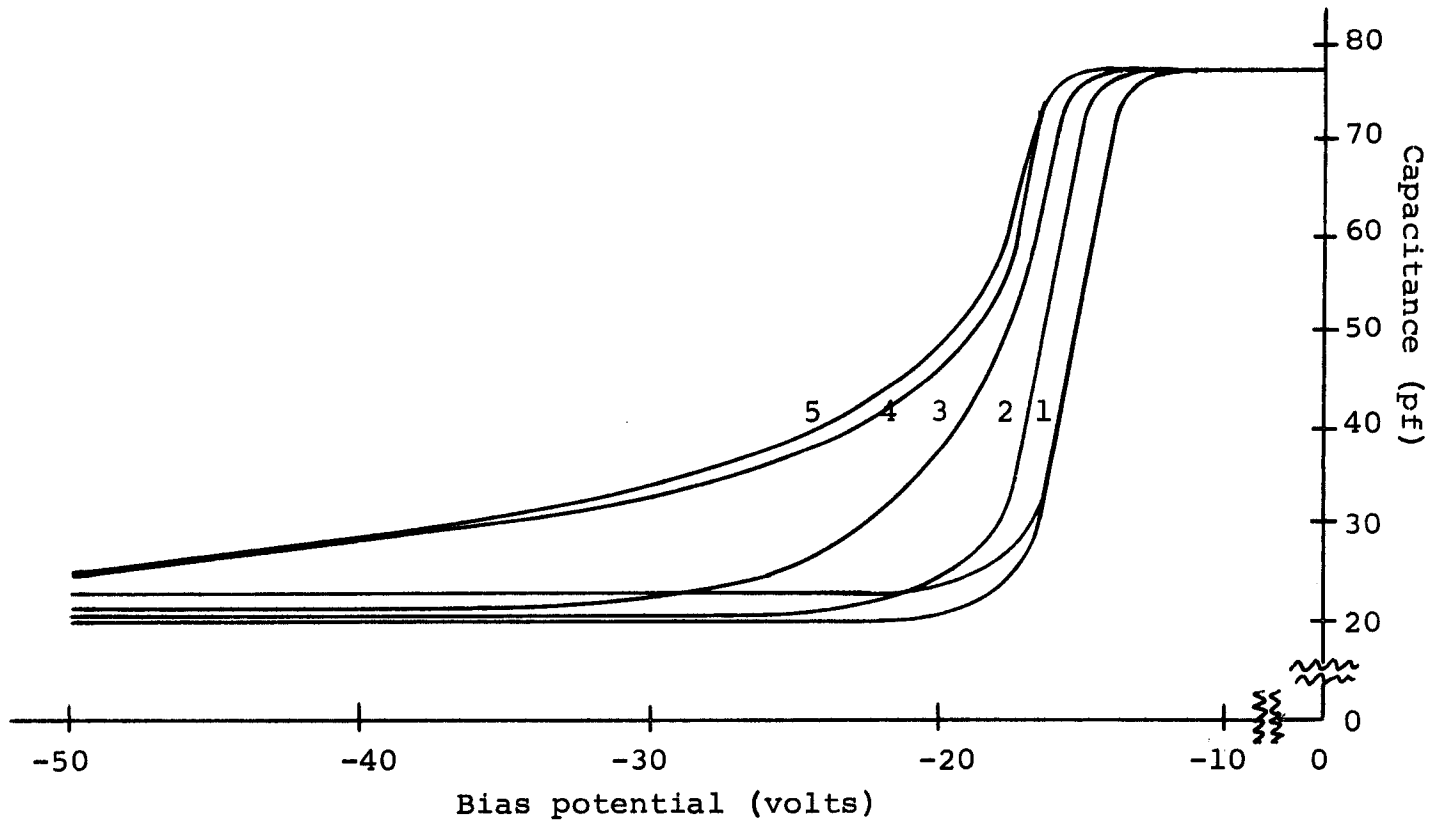


Figure 7.10. Capacitance-bias voltage curves for n-type device, number 14-33: curve (1) is in the negative saturation position while curves (2) through (5) were taken after a 5 minute, 75°C, +3.0 volt anneal

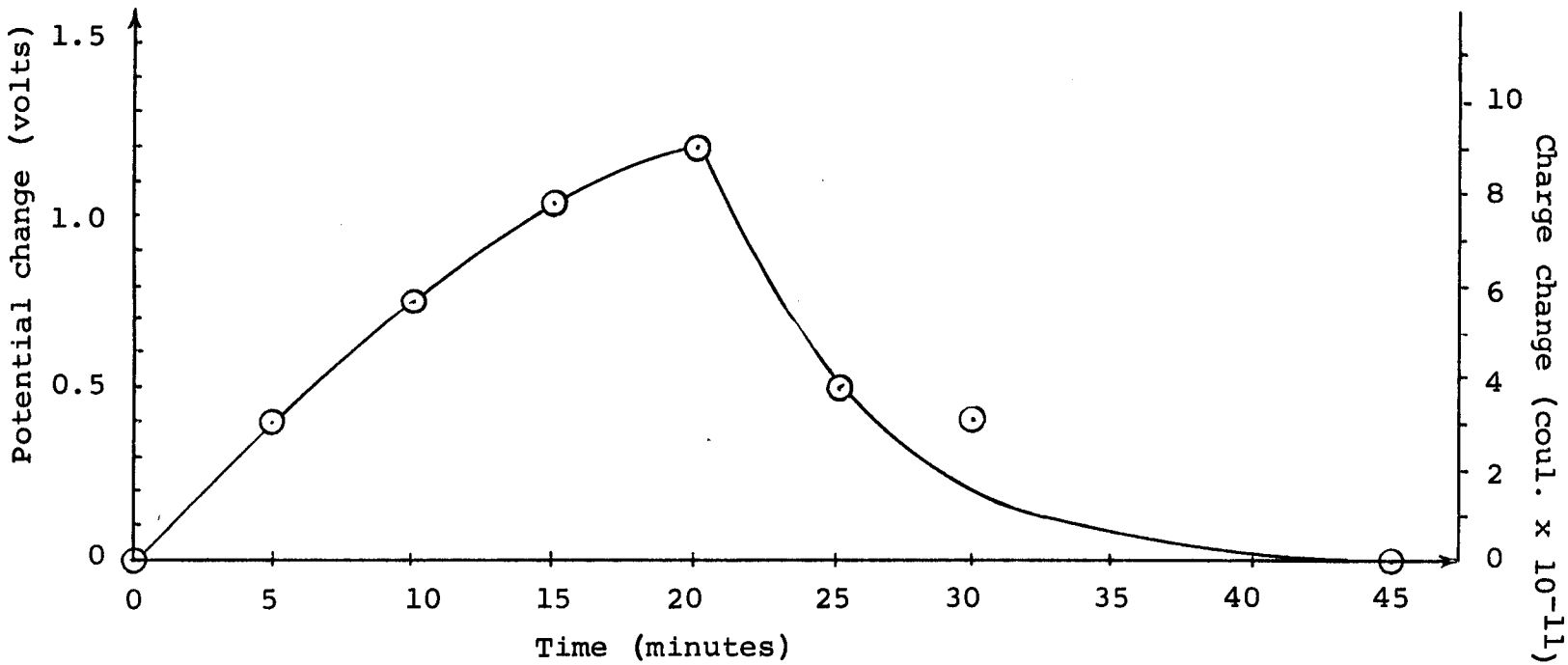


Figure 7.11. Oxide charge transfer and device curve voltage shift as a function of 75°C annealing time as determined from the device curves shown in Figure 7.10

of Figure 7.12 was taken after the device was returned to that negative saturation condition while curves 2 through 5 were each taken after 20 minute annealing periods. The above-mentioned technique for acquisition of parallel device curve displacement information was used. Figure 7.13 shows the device curve voltage displacement and also the calculated charge transfer as a function of time where that charge transfer was determined by the use of equation (7.1).

Finally, that same device was used for positive bias annealing investigations at 50°C. Curve 1 of Figure 7.14 is for the device after it had been returned to the negative saturation condition while curves 2 through 6 were each taken after successive three hour annealing periods during which a +3.0 volt bias was applied to the gate electrode. The above-mentioned technique for determining the effective parallel device curve shift was used. Figure 7.15 shows the device curve voltage displacement along with the transferred oxide charge as calculated by means of equation (7.1).

7.6 Mobile Ion Activation Energy Determination and Conclusions

The charge transfer versus the square root of time information is shown in summary in Figure 7.16 with annealing temperature as a parameter. The initial square root of time dependance of the charge transfer can easily be seen from this figure. The initial slope of each of these curves is

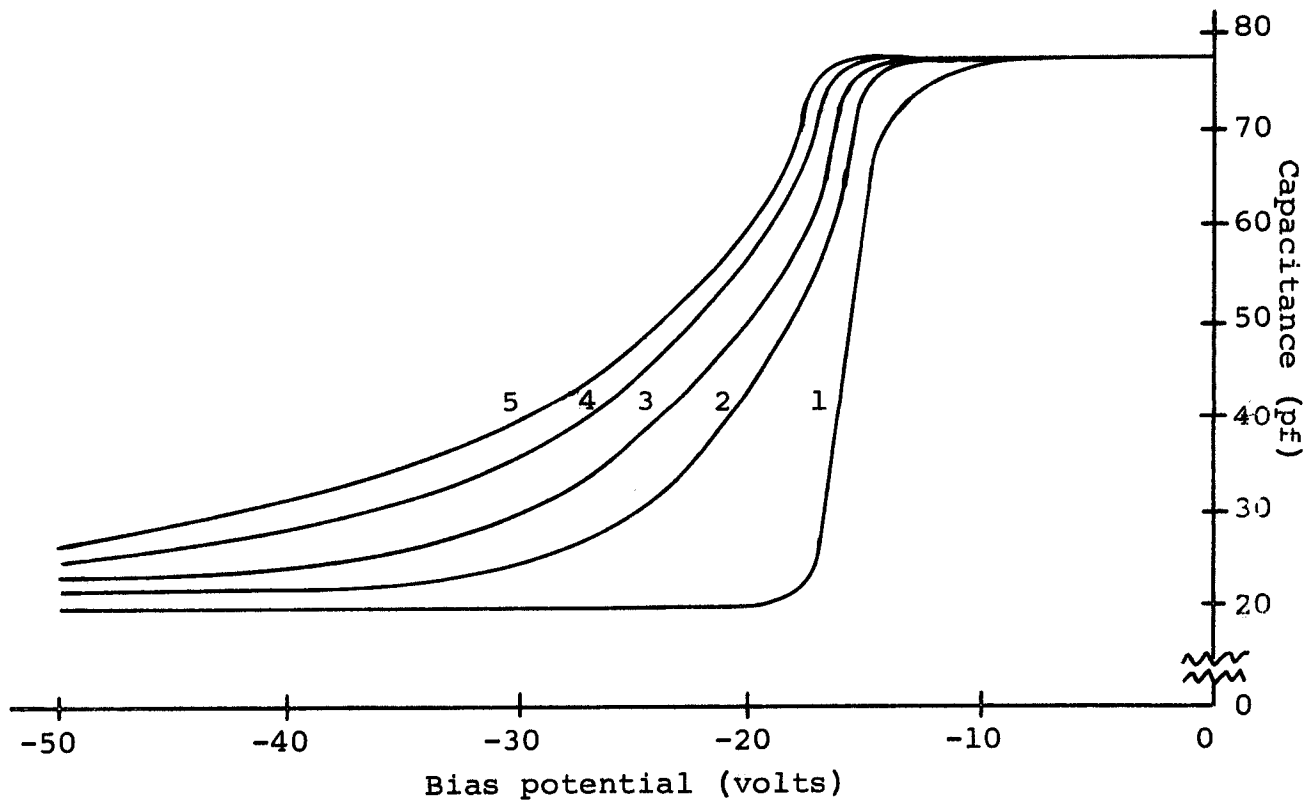


Figure 7.12. Capacitance-bias voltage curves for n-type device, number 14-33: curve (1) is in the negative saturation position while curves (2) through (5) were taken after one 10 minute and three 20 minute, 62°C, +3.0 volt anneals respectively

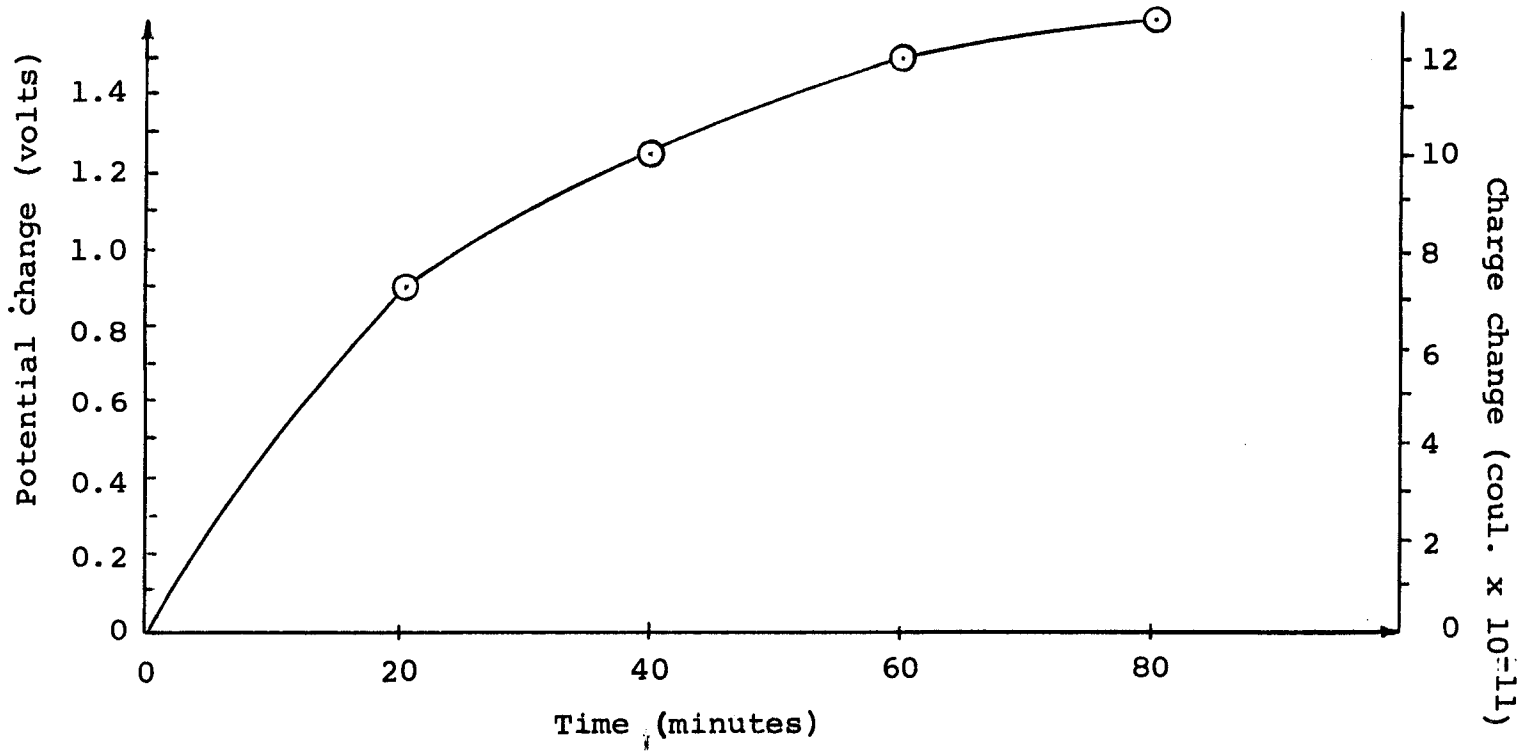


Figure 7.13. Oxide charge transfer and device curve voltage shift as a function of 62°C annealing time as determined from the device curves shown in Figure 7.12

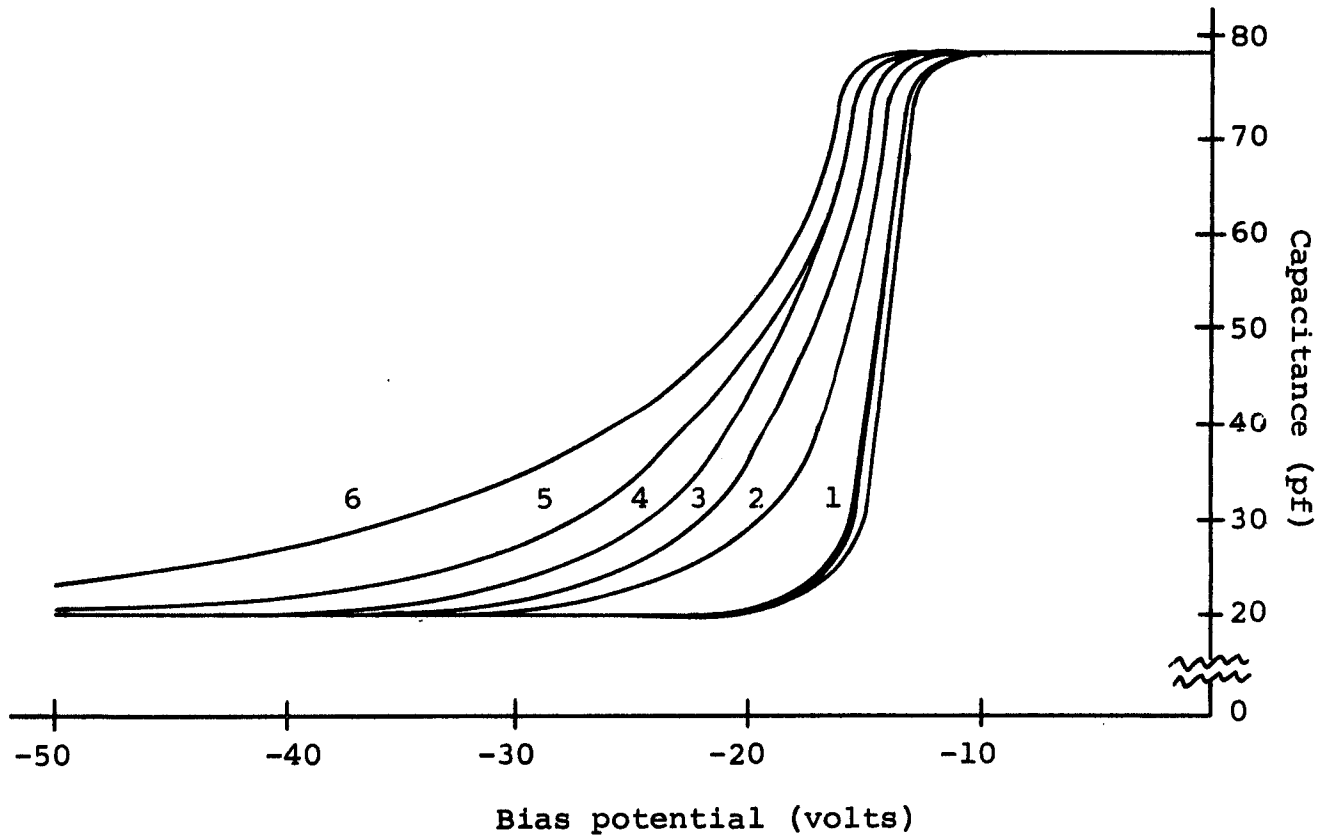


Figure 7.14. Capacitance-bias voltage curves for n-type device number 14-33: curve (1) is in the negative saturation position while curves (2) through (6) were each taken after a 3 hour, 50°C, +3.0 volt bias anneal

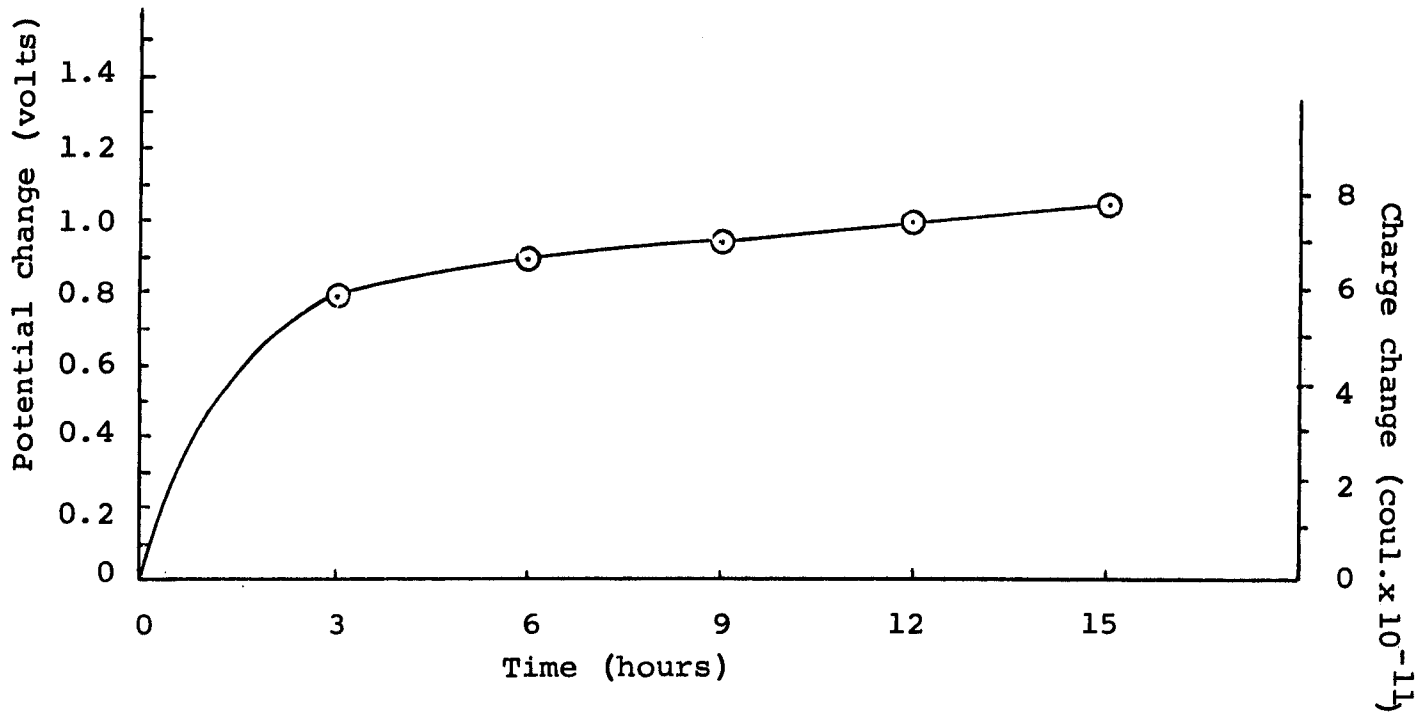


Figure 7.15. Oxide charge transfer and device curve voltage shift as a function of 50°C annealing time as determined from the device curves shown in Figure 7.14

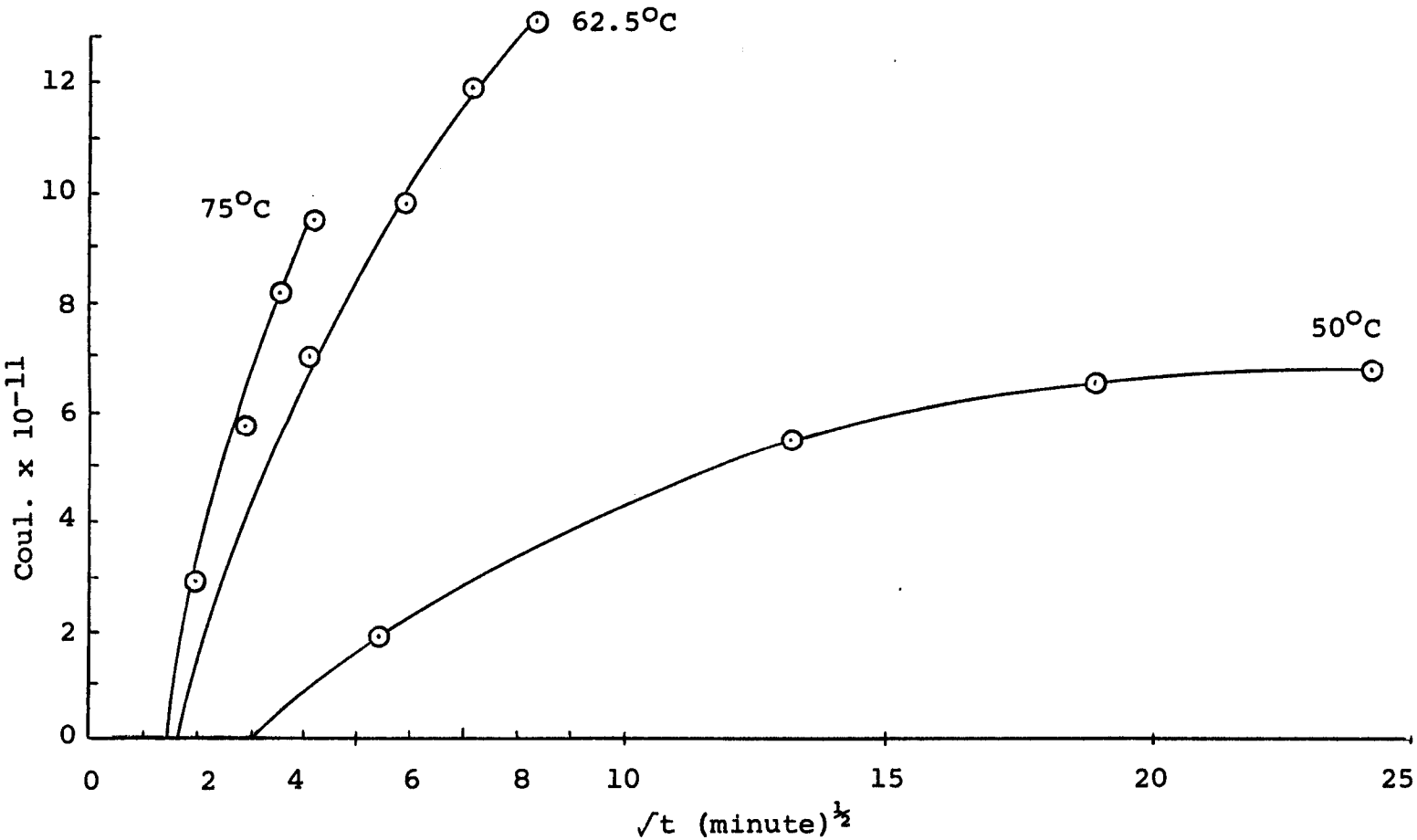


Figure 7.16. Oxide charge transfer as a function of the square root of annealing time for 50°C, 62°C, and 75°C, +3.0 volt anneals

plotted in Figure 7.17 versus the reciprocal of temperature. The solid line in this figure represents the activation energy of ionized sodium in amorphous silicon dioxide. One can see that the three points shown lie relatively near the sodium activation energy line. Since work concerning the activation energy of sodium in a contaminated dry oxygen grown, thermal oxide had already been carried out by Snow et al. (1965) which showed conclusively that an ionic sodium activation energy could be found, only three temperature values were used for confirmation purposes.

It was believed that this fact did not need to be established but only confirmed since the charge drift and recovery curves for the device very closely resembled those found by Snow et al. (1965) and were clearly not of the asymmetrical type reported on for a phosphorous-contaminated device by Hofstein (1966).

In general, work had been performed on thermally grown, dry oxygen oxides which had been purposely contaminated with alkali atoms by Snow et al. (1965), and on thermally grown, dry oxygen oxides with phosphorous present in certain areas of the device surface by Hofstein (1966). No work has yet been reported on ionic motions in steam grown oxides to the author's knowledge. It is concluded on the basis of the data presented above that the charge present in three steam grown oxides is, to a great extent, due to ionized alkali atoms, specifically sodium or lithium.

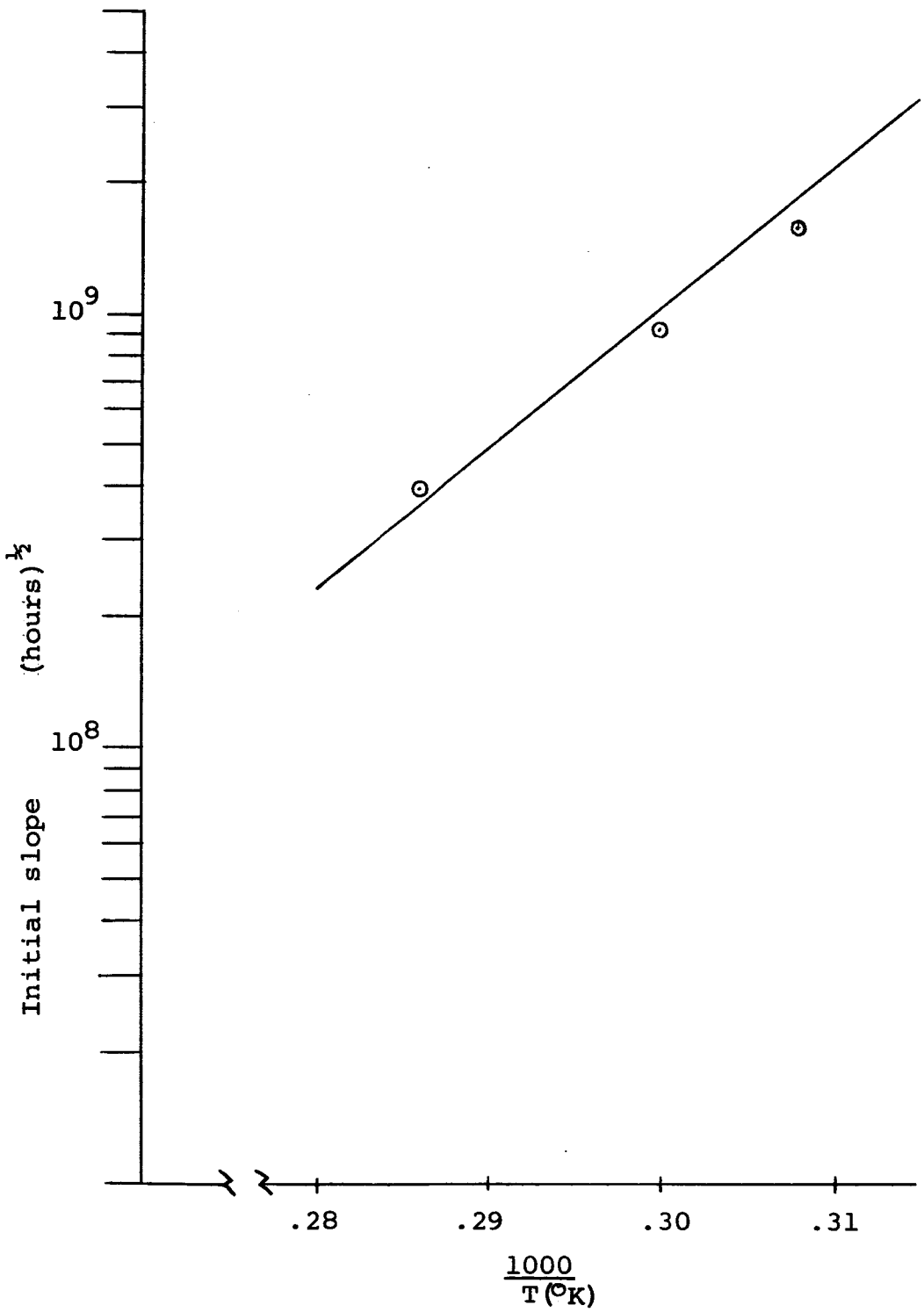


Figure 7.17. Temperature dependence of the initial slopes of the charge transfer curves of Figure 7.16 as a function of the reciprocal of time along with the activation energy line for sodium in fused silica

Pre- and post-gamma irradiation determination of silicon surface state density as a function of energy is discussed and carried out on the basis of the theory presented in chapter 3 in the next chapter.

8. SURFACE STATE DENSITIES FOR NON-IRRADIATED AND GAMMA IRRADIATED DEVICES

8.1 Introduction

This chapter is concerned with the determination of the silicon surface charge density as a function of energy for both non-irradiated and gamma irradiated devices. The theoretical method presented in chapter 3 was used for the surface charge density calculations. Since such calculations are quite tedious, an IBM 1620 Computer was used for the data processing. The method available for entering data into the computer necessitated the taking of capacitance-bias curve data by the point-by-point technique described in chapter 6.

The following sections explain the techniques used in device irradiation, show families of capacitance-bias voltage curves for both n- and p-type substrate devices which resulted after successive gamma flux exposures, present device curves taken by the automatic data acquisition scheme of chapter 6 which act to confirm the point-by-point data, and filally show calculated curves of silicon surface charge density as a function of surface potential for successive integrated gamma exposures.

8.2 Radiation Source and Procedures

A "Gammacell 220" manufactured by Atomic Energy of Canada Limited was used as the gamma radiation source. The curve of

Figure 8.1, which was supplied to the author by the above mentioned manufacturer, shows the known spectrum of energy in the sample chamber of the Gammacell. The output according to chemical dosiometry at the time of the device exposures was 2.18×10^5 roentgens hr^{-1}.

Devices to be irradiated were first set on an aluminum holding block with their leads extending into small holes provided therefore. The block was set inside a glass container and the lid placed on. The container was pumped down to approximately 20 inches of water below atmospheric pressure three times and backfilled each time with argon. The argon was used as in the annealing experiments described in the previous chapter due to the fact that it is chemically inert and would be much less likely to cause chemical reactions both on the silicon dioxide surface and at the metal gate electrode.

The glass container was then placed in the Gammacell at room temperature for a carefully noted amount of time. Upon removal, the container was opened, the devices removed, and measured by one of the two techniques explained in chapter 6.

8.3 Surface State Density Determination For a p-type Substrate Device

Two n- and two p-type substrate MOS capacitors were used in the radiation experiments and the corresponding point-by-point capacitance-bias voltage data accumulated. The devices

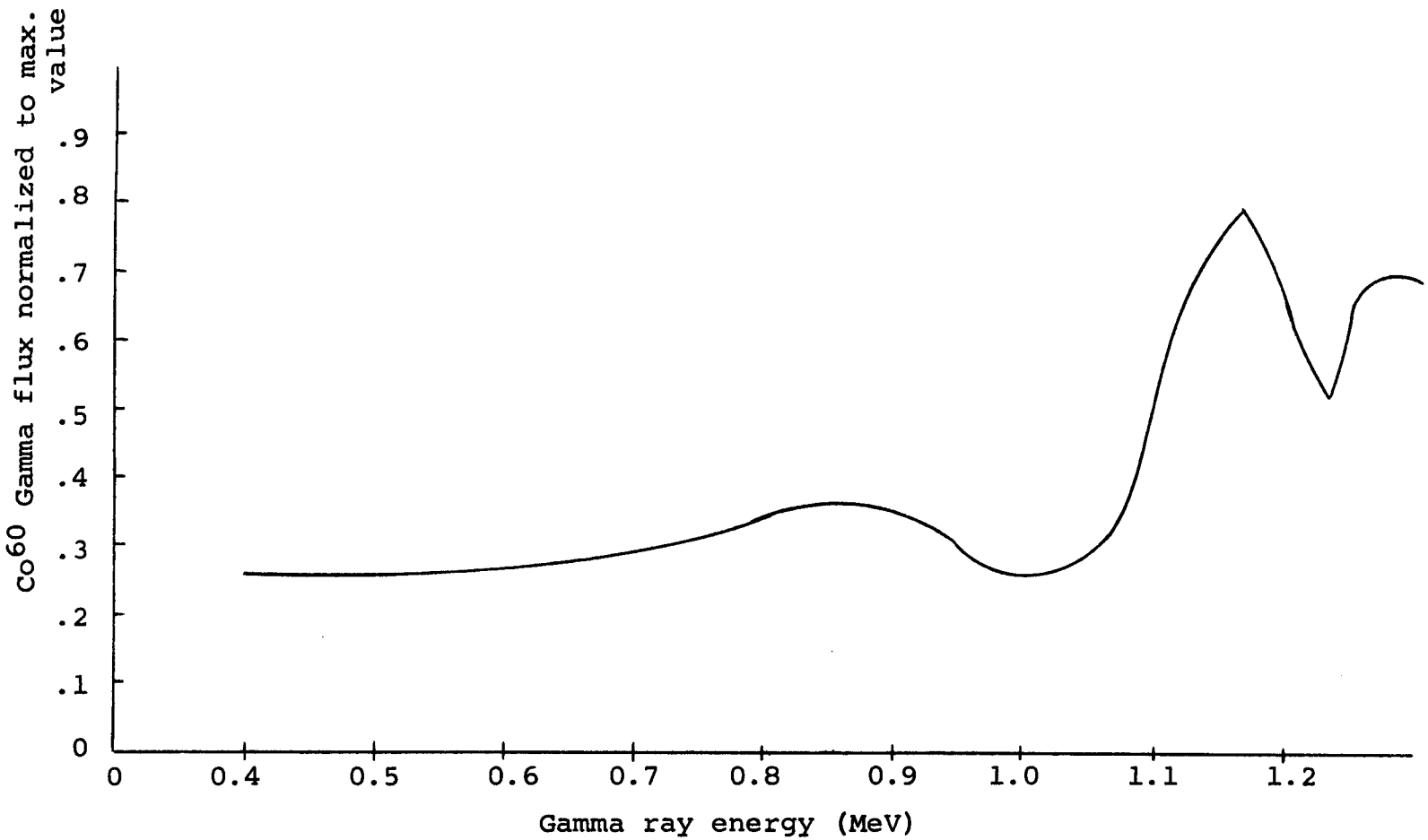


Figure 8.1. Normalized primary photon flux as a function of energy in the sample chamber of the Gammacell 220 (Source: Atomic Energy of Canada, Ltd., Ottawa, Canada)

were irradiated according to the above-mentioned procedures for various lengths of time. The pertinent irradiation information for the p-type device reported on herein is given in Table 8.1. Figure 8.2 shows a composite set of point-by-point capacitance-bias voltage curves taken on p-type device number 36-44. Curve 1 was taken prior to any irradiation or thermal annealing of the device while curves 2 through 17 were each taken after a given exposure time in the Gammacell. Both the incremental and total gamma ray exposure times of the device, before each of the curves of Figure 8.2 can be determined from Table 8.1. One can see from these curves that not only was the slope of each succeeding curve decreased by the gamma radiation but also each curve was shifted toward a more negative bias voltage. The former indicates an increase in surface state density while the latter indicates an increase in the net amount of positive charge in the oxide.

It is perhaps beneficial to state at this point that the surface charge density calculated by the methods of chapter 3 will be invarient with horizontal device curve displacement. Since this fact itself is much more important to the actual surface state density determination than a proof thereof, the latter is presented in Appendix B. Hence, the surface charge state density determination made by means of the point-by-point device curve information in the manner of chapter 3 is truly a determination of the charge state density at the oxide-

Table 8.1. Co^{60} radiation information for p-type device number 36-44.

CV-curve taken after irradiation	Time of irradiation (minutes)	Exposure (roentgens)	Total exposure
1	0	0	0
2	15	$.5 \times 10^5$r	$.5 \times 10^5$r
3	15	$.5 \times 10^5$r	1.0×10^5r
4	15	$.5 \times 10^5$r	1.5×10^5r
5	30	1.0×10^5r	2.5×10^5r
6	30	1.0×10^5r	3.5×10^5r
7	30	1.0×10^5r	4.5×10^5r
8	30	1.0×10^5r	5.5×10^5r
9	30	1.0×10^5r	6.5×10^5r
10	30	1.0×10^5r	7.5×10^5r
11	60	2.0×10^5r	9.5×10^5r
12	60	2.0×10^5r	11.5×10^5r
13	60	2.0×10^5r	13.5×10^5r
14	120	4.0×10^5r	17.5×10^5r
15	120	4.0×10^5r	21.5×10^5r
16	120	4.0×10^5r	25.5×10^5r

silicon interface and is not dependent on the magnitude or polarity of the net oxide charge.

A surface state density determination was made for device 36-44 from the capacitance-bias voltage curves shown in Figure 8.2. Figure 8.3 shows the surface charge state

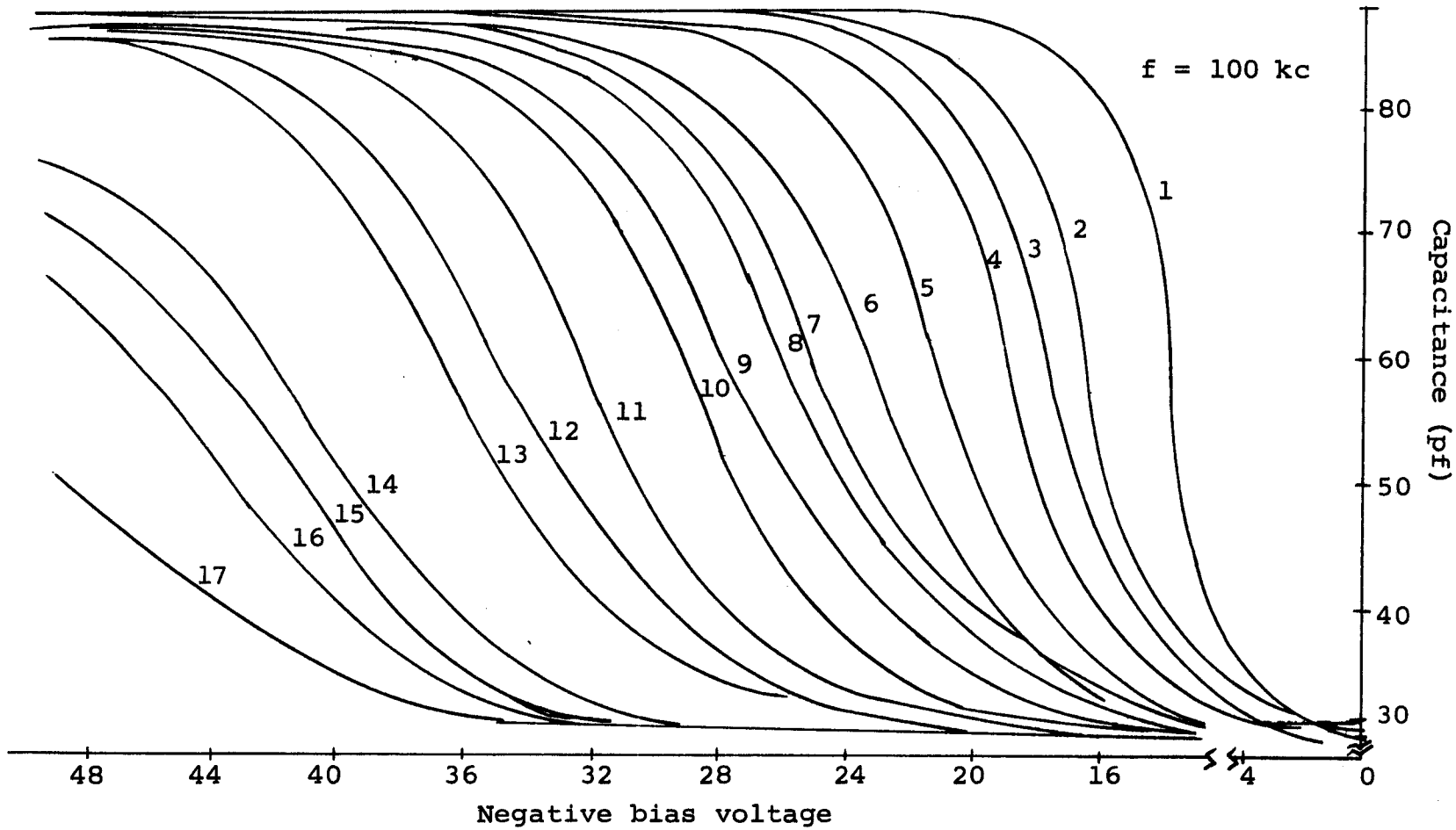


Figure 8.2. Point-by-point capacitance-bias voltage curves for p-type device number 36-44 showing shift of curves toward more negative bias with increasing gamma radiation as given in Table 8.1

density as a function of surface potential, defined in chapter 3, with total gamma irradiation exposure as a parameter. Curve 1 of Figure 8.3 is for the device before any gamma irradiation while the remaining curves are for increasing exposure as shown in Table 8.1.

8.4 Surface State Density Determination For an n-type Substrate Device

Point-by-point capacitance-bias voltage curves were taken for n-type device number 14-45 before and after irradiation and are shown in Figure 8.4. The pertinent radiation information for that device is given in Table 8.2. Curve 1 was taken prior to any irradiation while curves 2 through 7 were taken after subsequent gamma irradiations. As can be seen from Figure 8.4 neither the device curve slope decrease nor the horizontal curve displacement were as great for this n-type device as they were for the p-type device, reported on in the previous section, under nearly the same radiation conditions. Figure 8.5 shows calculated surface charge density-surface potential curves with gamma radiation exposure as a parameter. Curve 1 is for the device before irradiation and corresponds to curve 1 of Figure 8.4. The remainder of the curves are for sequential gamma radiation exposures which are listed in Table 8.2.

The increase in silicon surface charge density of an MOS device due to gamma radiation was first reported on by

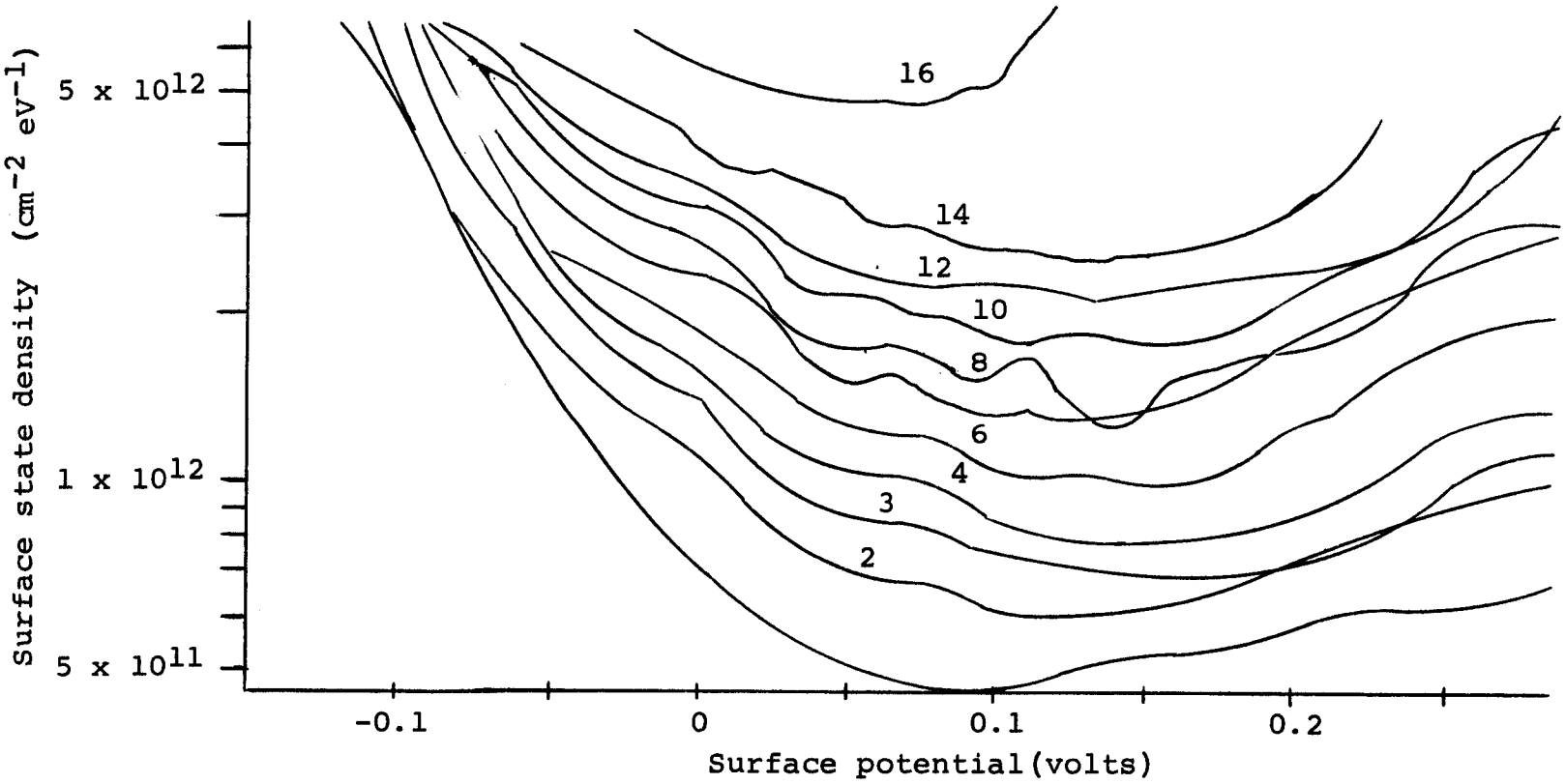


Figure 8.3. Curves of surface state density versus surface potential for increasing gamma irradiation of device number 36-44 as given in Table 8.1

Table 8.2. Co^{60} radiation information for n-type device number 14-45.

CV-curve taken after exposure	Time of irradiation (minutes)	Exposure (roentgens)	Total exposure
1	0	0	0
2	15	$.5 \times 10^5$r	$.5 \times 10^5$r
3	15	$.5 \times 10^5$r	1.0×10^5r
4	30	1.0×10^5r	2.0×10^5r
5	15	$.5 \times 10^5$r	2.5×10^5r
6	15	$.5 \times 10^5$r	3.0×10^5r
7	45	1.5×10^5r	4.5×10^5r

Mattauch and Lade (1965) on the basis of work described herein. Kooi (1965b) later presented device capacitance-bias voltage curves and stated that the decrease in curve slope indicated an increase in surface charge density but did not carry through any calculations. Szedon and Sandor (1965) reported on device capacitance-bias voltage curve changes due to X-ray bombardment of MOS structures. They used the device curve displacement along with equation 7.1 to calculate an effective surface charge density but did not separate the effects of oxide charges and surface charges.

The method used herein to determine surface state density is sensitive only to a change in the slope of the device curve as was previously stated and is shown in Appendix B.

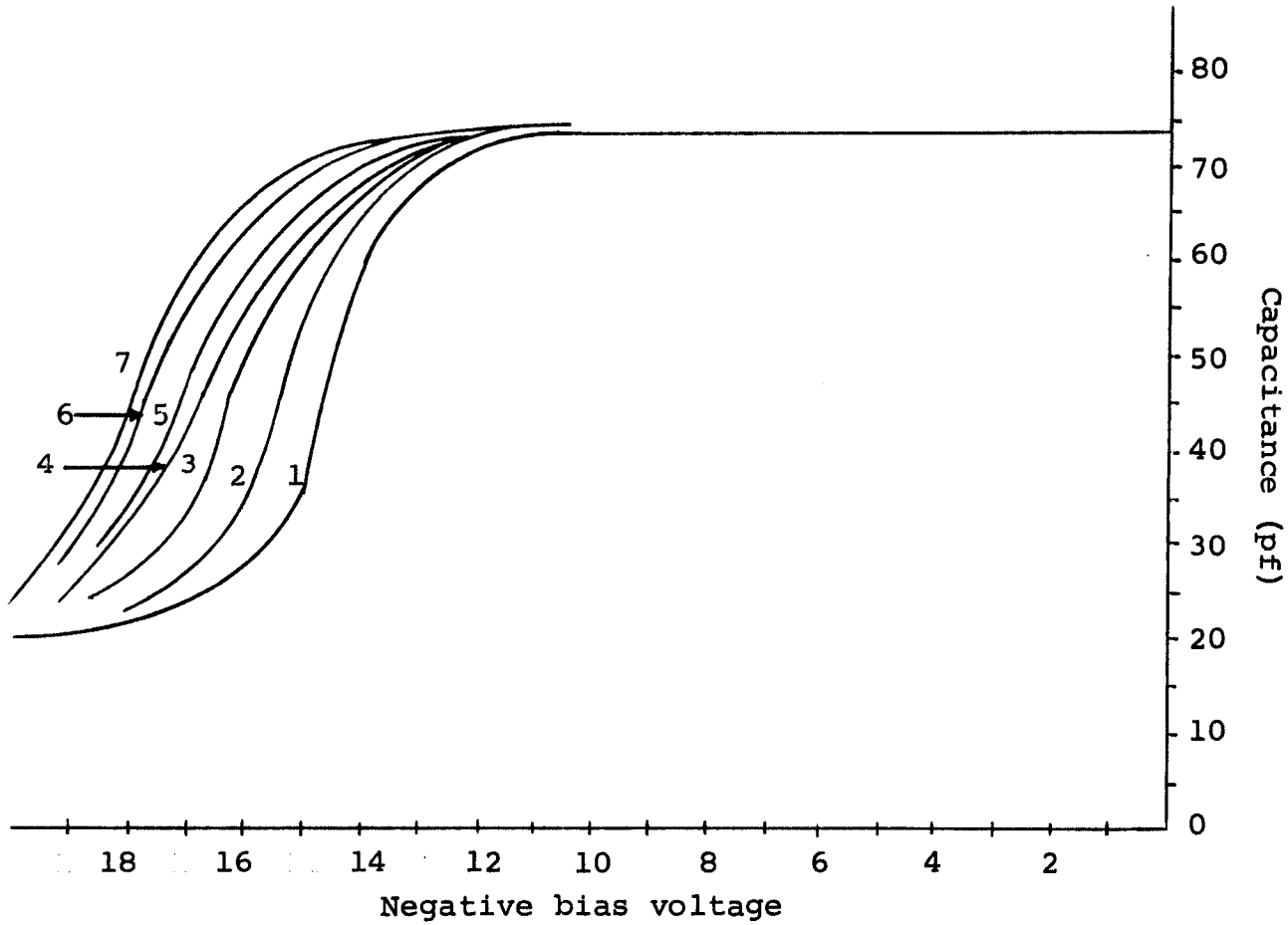


Figure 8.4. Point-by-point capacitance-bias voltage curves for n-type device number 14-43 showing shift of curves toward more negative bias with increasing gamma radiation as given in Table 8.2

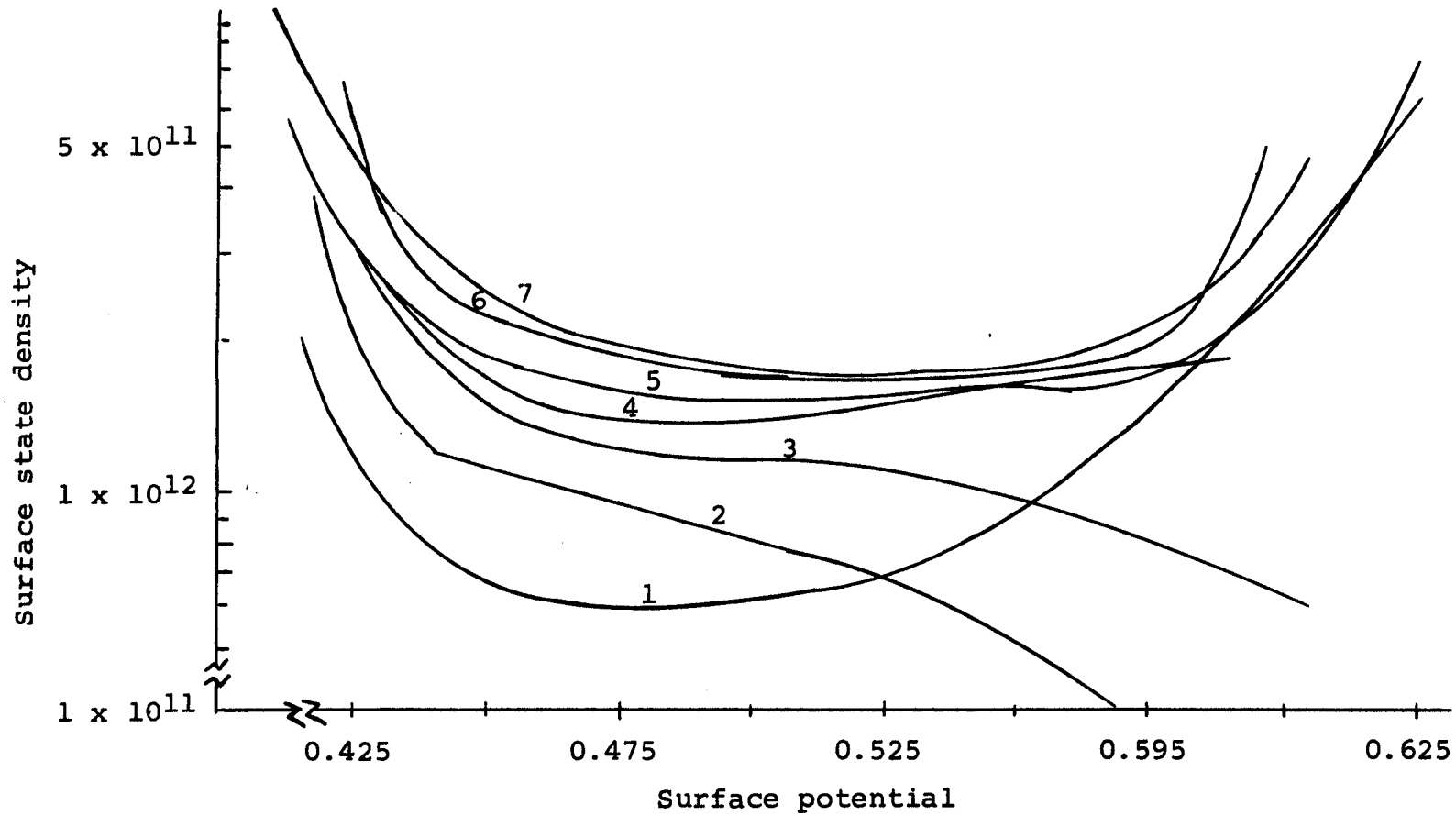


Figure 8.5. Curves of surface state density versus surface potential for increasing gamma irradiation of device number 14-43 as given in Table 8.2

8.5 Device Curve Confirmation Data

Even though two n- and two p-type substrate devices were investigated by the acquisition of point-by-point curves for a sequence of gamma flux exposures, it was felt that the trends observed needed to be confirmed by further device study. For this reason three devices of each type were chosen and irradiated in the sequence shown in Table 8.3. A capacitance-bias voltage curve was taken for each device before each irradiation. Figures 8.6, 8.7, and 8.8 show the device curves for three n-type devices while Figures 8.9, 8.10, and 8.11 show the curves for the three p-type devices. A cursory examination of the curves of these figures and Table 8.3 shows that the curve changes follow generally the same trends as did those of figures 8.2 and 8.4.

The fact that a decrease in device curve slope indicates an increase in surface charge density can be seen from the theoretical treatment of chapter 3. This fact presents a method of examining the device curves for surface charge density trends in a general manner. Specifically, the method entails the drawing of two arbitrary constant capacitance lines over the curves. One line was drawn just below the maximum capacitance asymptote and the other just above the minimum capacitance asymptote as can be seen in Figures 8.6 through 8.11. The values of voltage, indicated on the absicissa, for which a device curve intersects each of the

Table 8.3. Co^{60} radiation information for device numbers 14-15, 14-25, 14-55, 36-41, 36-42, and 36-43. Device curves are shown in Figures 8.6, 8.7, 8.8, 8.9, 8.10, and 8.11 respectively.

CV-curve taken after exposure	Time of irradiation (minutes)	Exposure (roentgens)	Total exposure
1	0	0	0
2	30	1×10^5	1×10^5
3	30	1×10^5	2×10^5
4	60	2×10^5	4×10^5
5	120	4×10^5	8×10^5
6	120	4×10^5	12×10^5
7	240	8×10^5	20×10^5
8	240	8×10^5	28×10^5
9	240	8×10^5	36×10^5

constant capacitance lines were recorded and the magnitude of their difference was found. This voltage magnitude is inversely proportional to the slope of a straight line drawn between those two points of intersection; and, hence, is directly proportional, in a very generalized way, to the surface charge density of the device. Since it is the slope of the curves which is important here, Figures 8.12 and 8.13 show the piecewise-linearized normalized reciprocal slopes for the curves of Figures 8.2 and 8.4 respectively as a

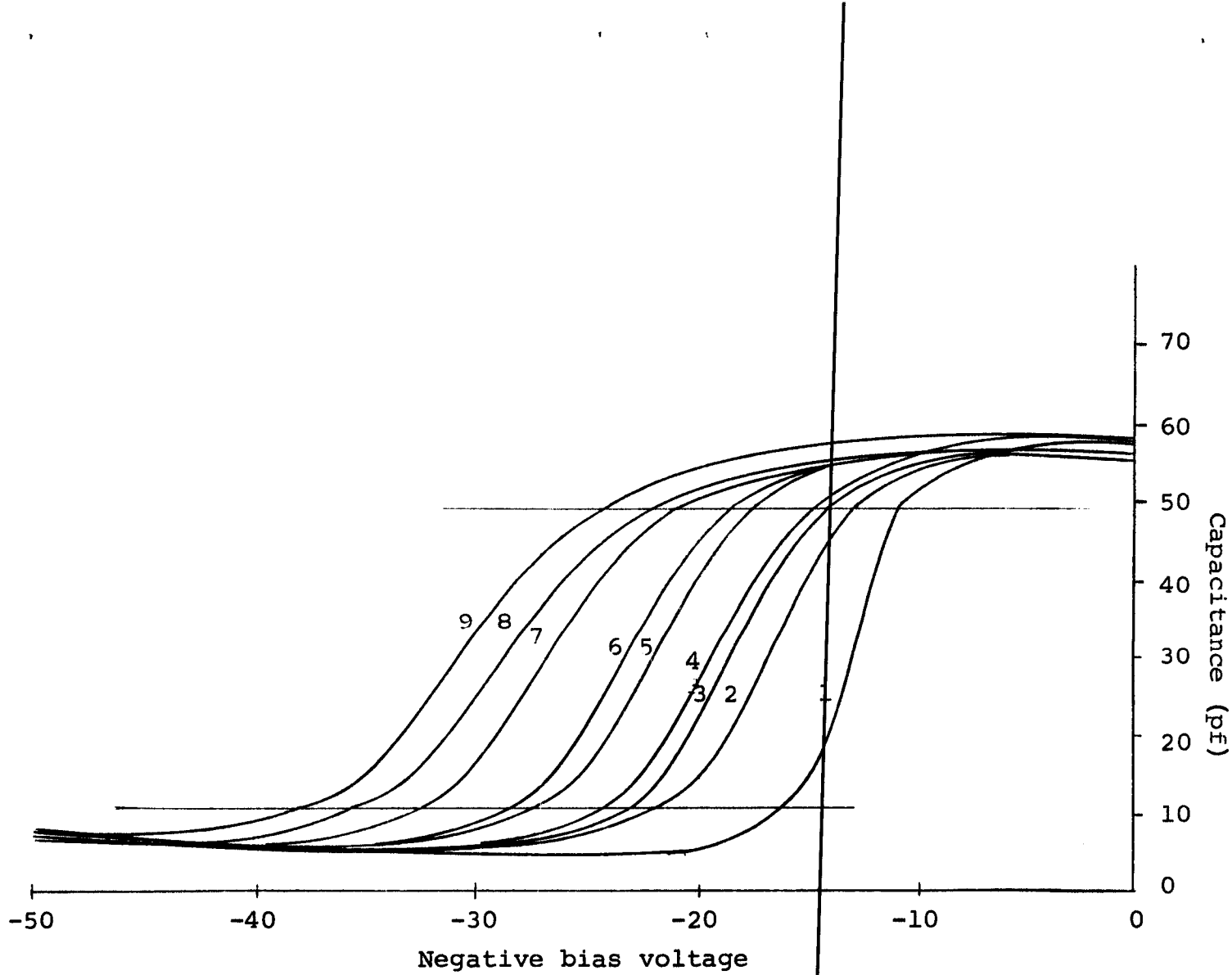


Figure 8.6. Capacitance-bias voltage curves for n-type device number 14-15 with gamma irradiation as a parameter as given in Table 8.3

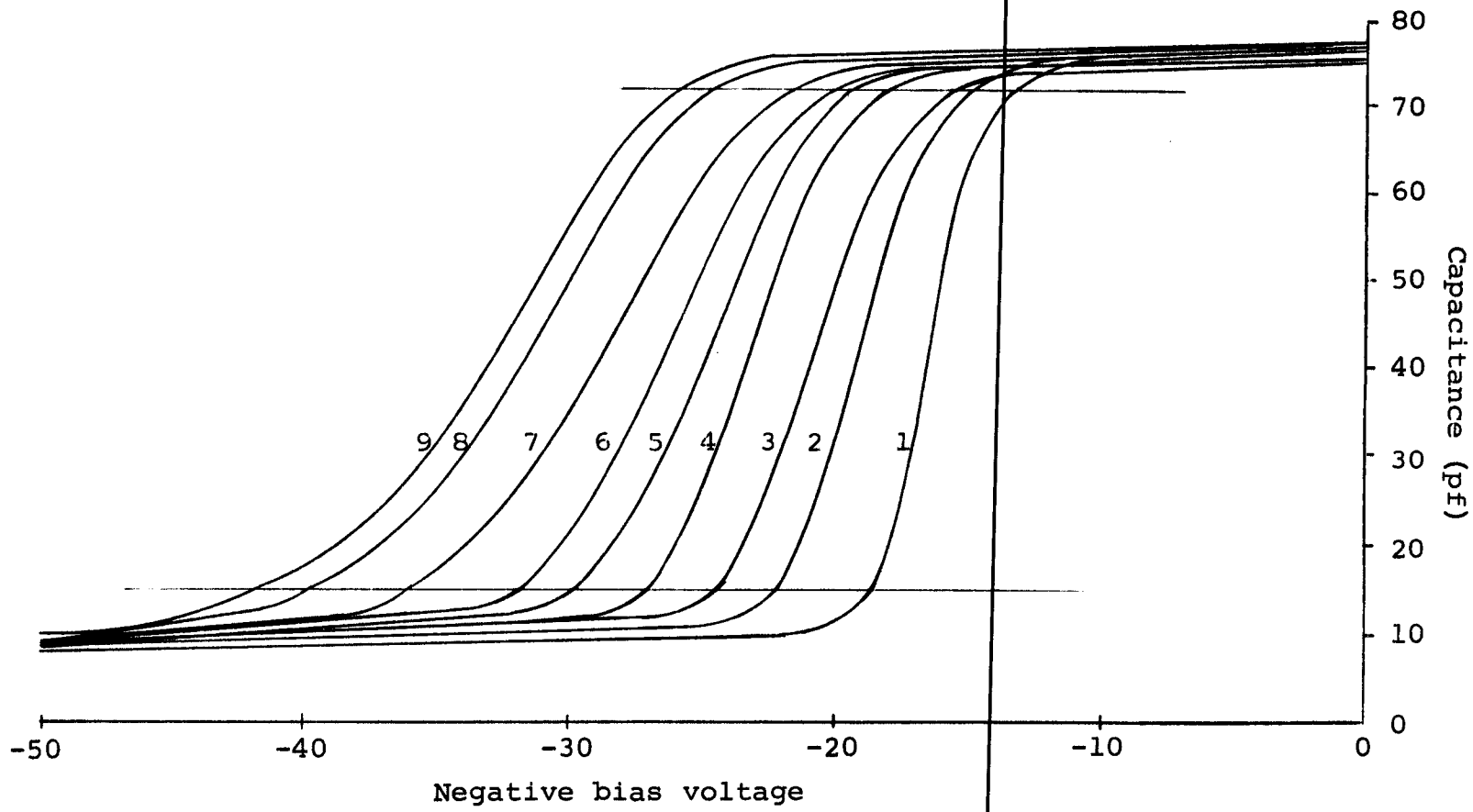


Figure 8.7. Capacitance-bias voltage curves for n-type device number 14-25 with gamma irradiation as a parameter as given in Table 8.3

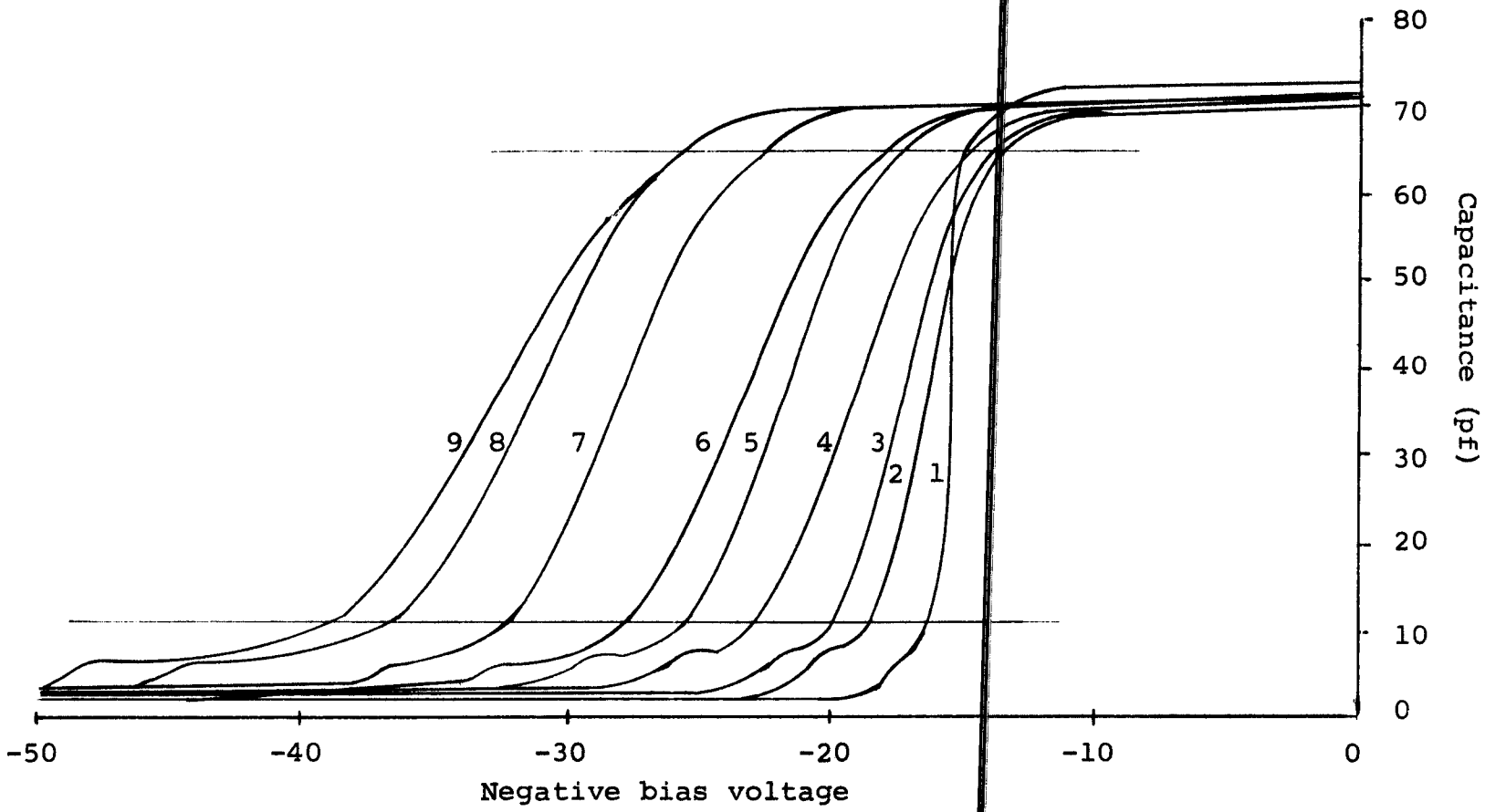


Figure 8.8. Capacitance-bias voltage curves for n-type device number 14-55 with gamma irradiation as a parameter as given in Table 8.3

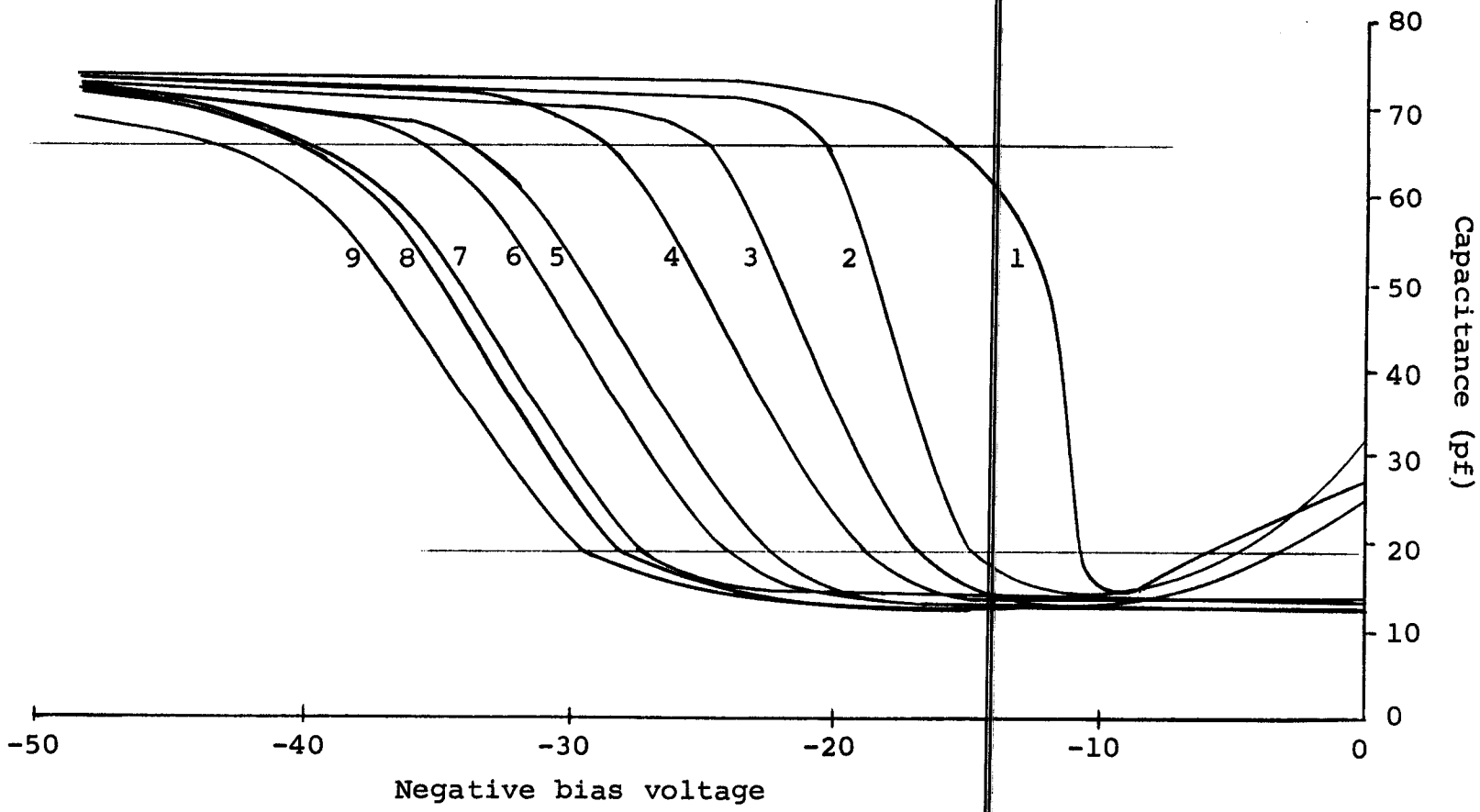


Figure 8.9. Capacitance-bias voltage curves for p-type device number 36-41 with gamma irradiation as a parameter as given in Table 8.3

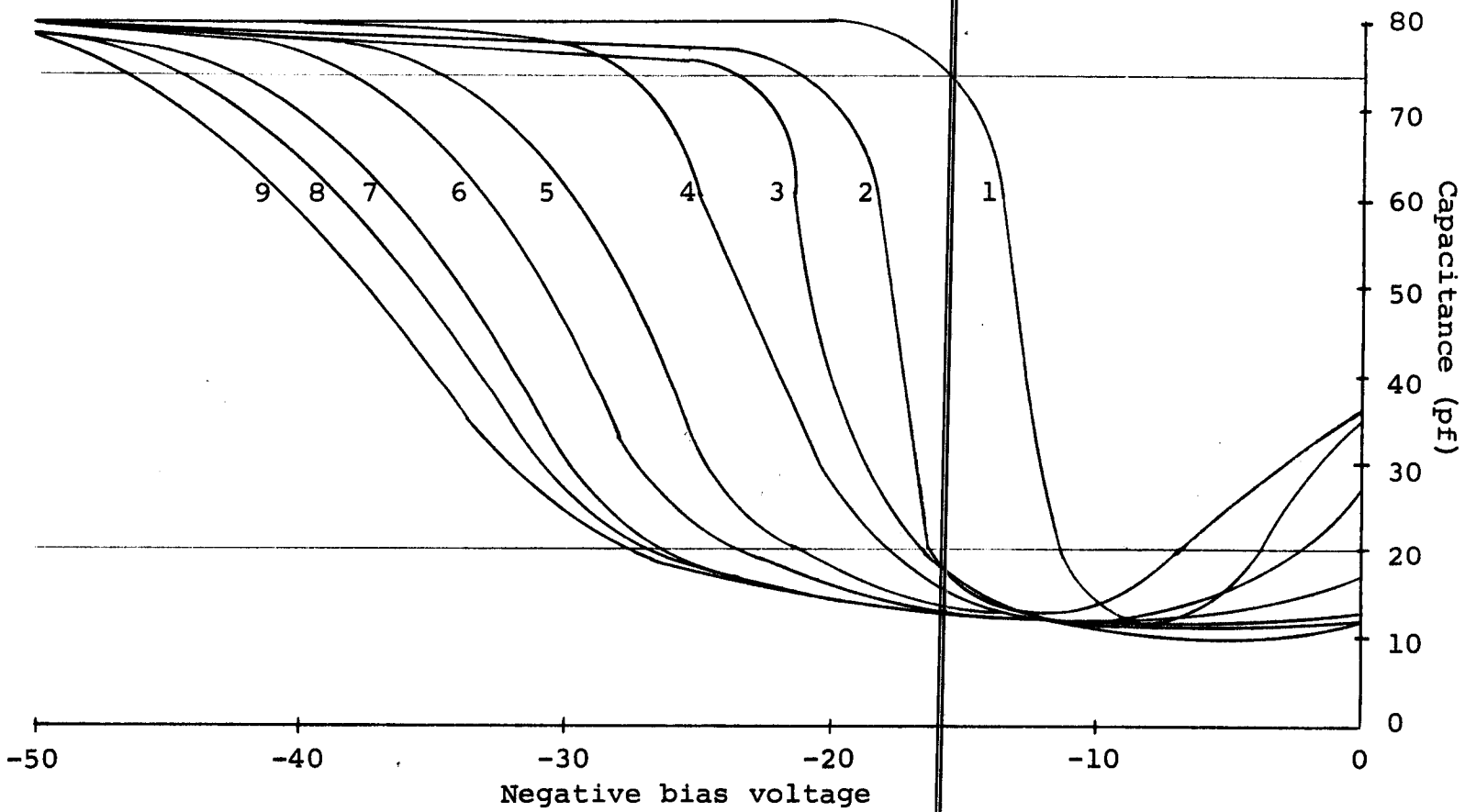


Figure 8.10. Capacitance-bias voltage curves for p-type device number 36-42 with gamma irradiation as a parameter as given in Table 8.3

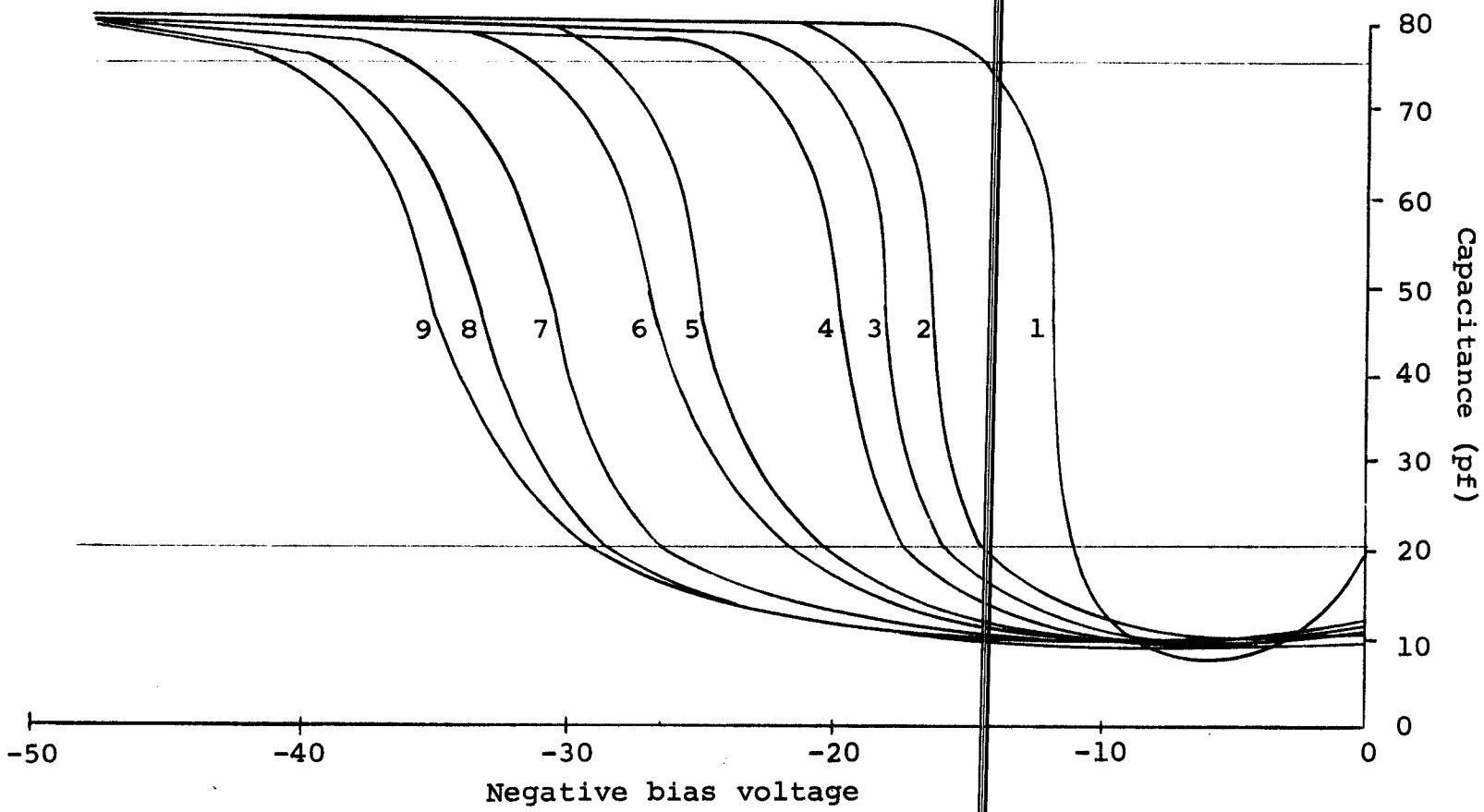


Figure 8.11. Capacitance-bias voltage curves for p-type device number 36-43 with gamma irradiation as a parameter as given in Table 8.3

function of gamma radiation exposure time. These normalized reciprocal slopes were found according to the above-mentioned procedure. For comparison, Figures 8.14 and 8.15 show curves of normalized reciprocal slopes of the curves of Figures 8.6 through 8.8 and 8.9 through 8.11 respectively as a function of total gamma radiation time.

Finally, it is believed that a few words should be said concerning the variation of the surface charge state density curves with a corresponding change in point-by-point capacitance. Since the surface charge density was determined by the differentiation of a curve which was calculated from the experimental capacitance data, a change in that density is dependent not only upon capacitance change but also upon spacing of the values of surface potential which correspond to neighboring capacitance values. In general a 0.1 volt bias increment was used in capacitance data acquisition throughout the important high-slope device curve regions. A determination of the surface charge density variation due to a capacitance change in that region of relatively constant surface potential change indicated that a capacitance change of 0.2 picofarads caused a corresponding surface charge density change of less than 0.2×10^{11} cm^{-2} eV^{-1}.

Generally, the reciprocal slope-gamma exposure curves seem to correspond quite well not only for devices of the same type but also for the remaining devices. The trends

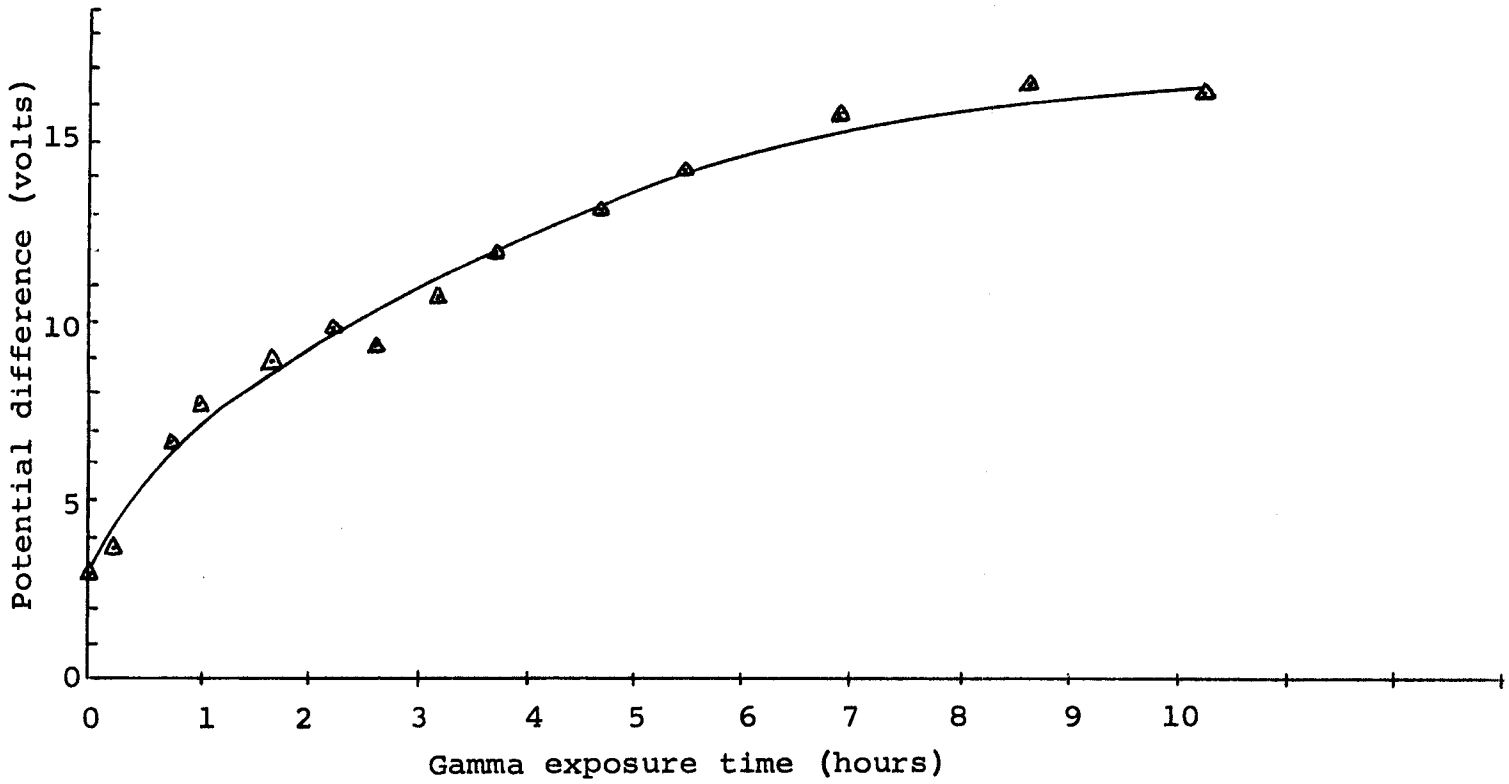


Figure 8.12. Normalized reciprocal transition region slope of device curves shown in Figure 8.2 as a function of gamma exposure time

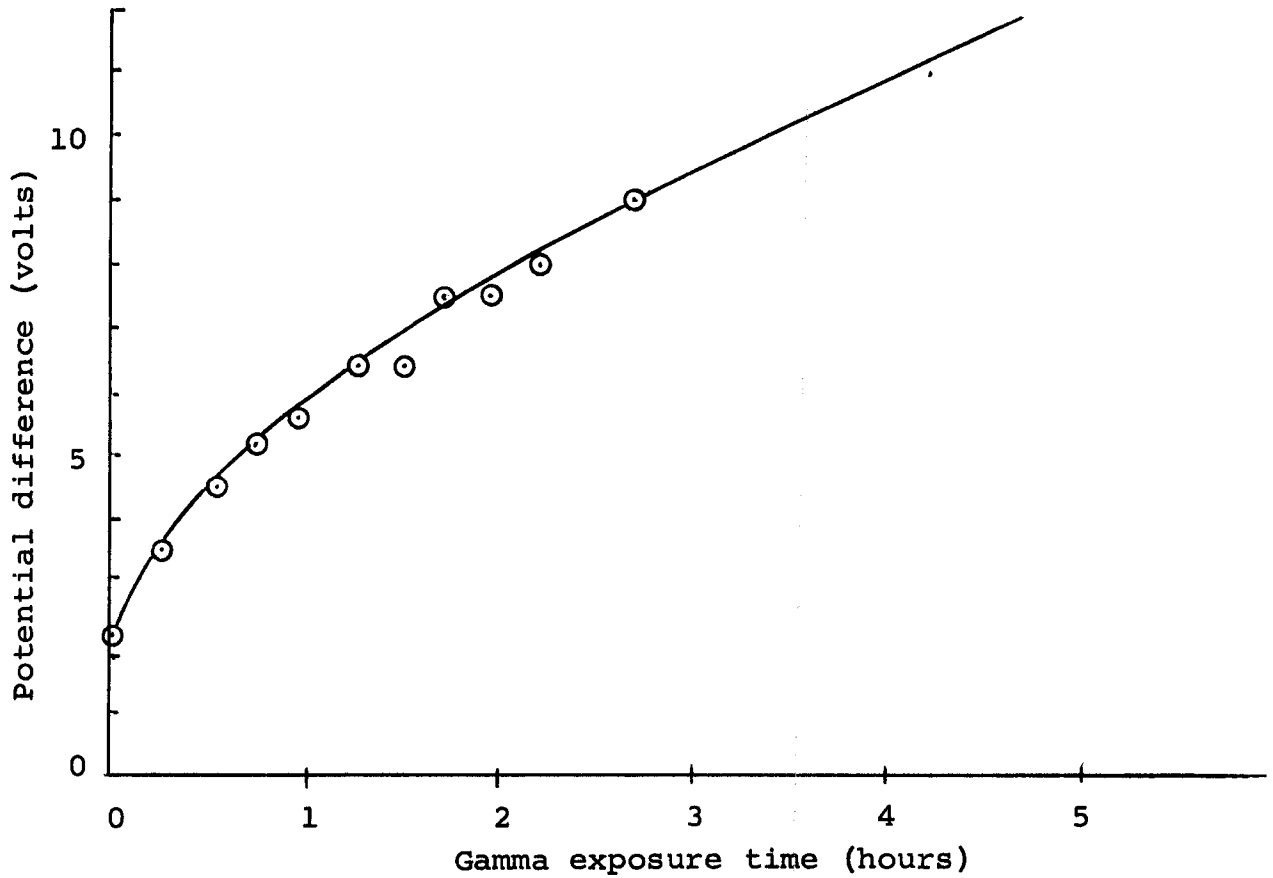


Figure 8.13. Normalized reciprocal transition region slope of device curves shown in Figure 8.4 as a function of gamma exposure time

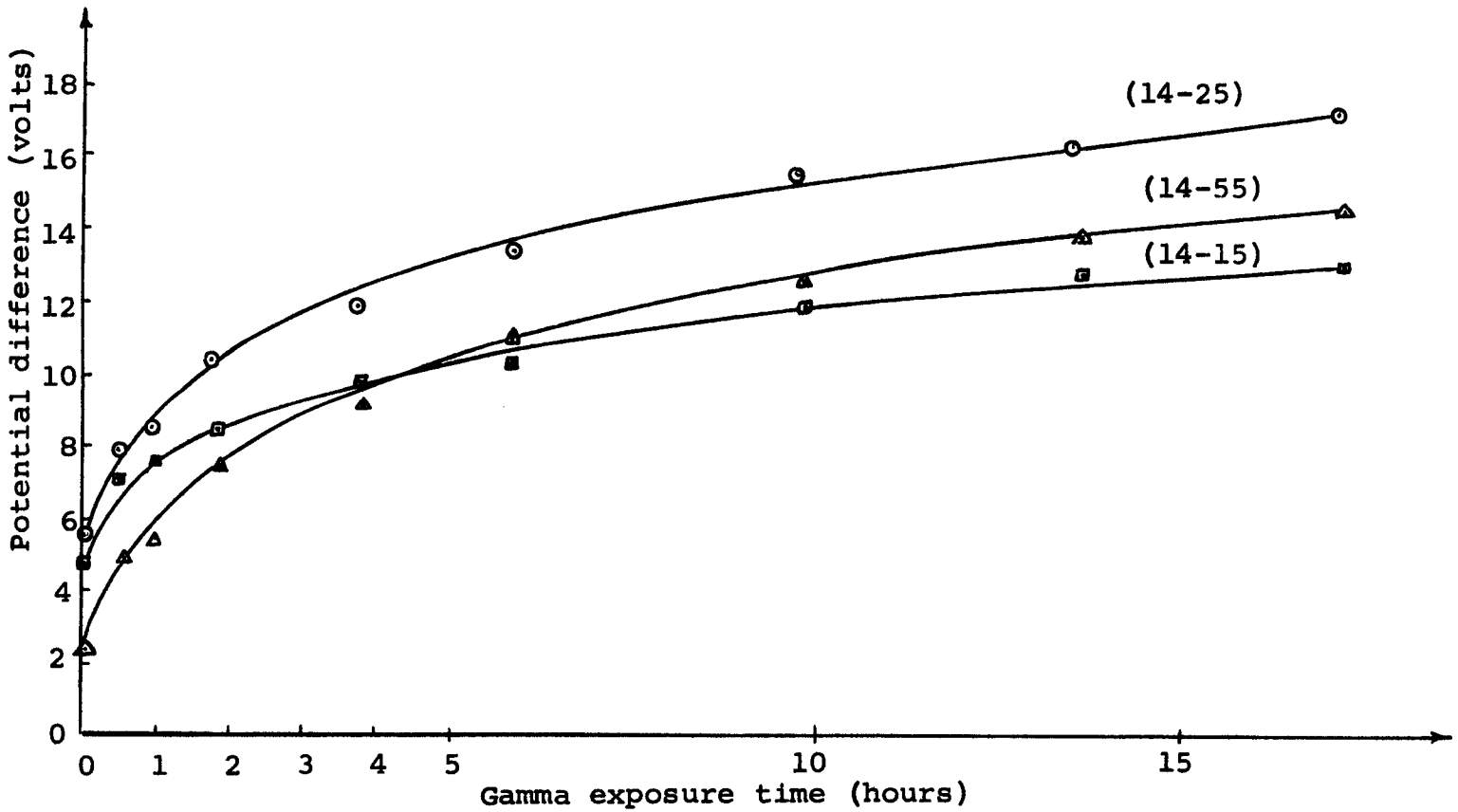


Figure 8.14. Normalized reciprocal transition region slope of device curves shown in Figures 8.6, 8.7, and 8.8 as a function of gamma exposure time

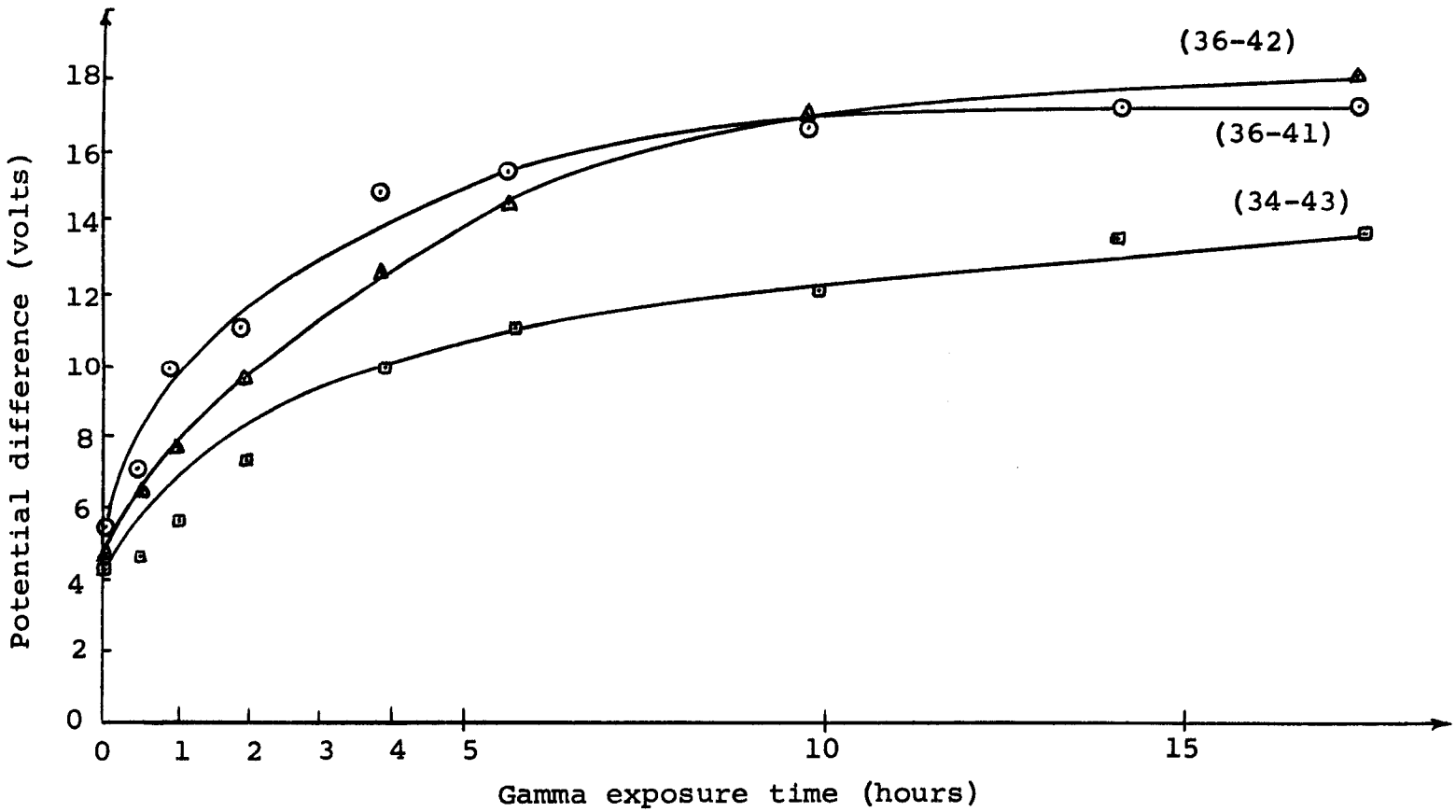


Figure 8.15. Normalized reciprocal transition region slope of device curves shown in Figures 8.9, 8.10, and 8.11 as a function of gamma exposure time

exhibited by the precise surface charge density curves of Figures 8.3 and 8.5 were confirmed very well by the reciprocal slope-gamma exposure comparisons made above.

The following chapter discusses the effect of elevated temperature annealing on the oxide charge of a structure after that device had been irradiated in the same way as the devices discussed in this chapter.

9. RADIATION INDUCED OXIDE CHARGE CHANGE

9.1 Introduction

The purpose of this chapter is to report on radiation data obtained, the oxide charge change affected by the gamma radiation, and a possible model explaining this change. The data was obtained by means of a series of investigations which were carried out in order to determine the effect of gamma radiation on the oxide charge density. Since the data taken when a device was in the negative saturation condition was found to be very reproducable, as was pointed out in chapter 7, that condition was used as a reference for the radiation sequence.

9.2 Radiation Effects on Annealed Device Curves

It was found during the non-irradiation annealing experiments that devices fabricated on p-type substrates developed gate-to-substrate short-circuits under all annealing conditions more readily than did those fabricated on n-type substrates. Because of this, and also since the general annealing trends of chapter 7 were found to be basically the same for both types of devices, only those fabricated on n-type substrates were investigated for radiation effects on the oxide charge density. Four n-type devices which had never previously been irradiated were taken through

a negative bias anneal at 75°C in order to affect a change in the oxide charge to the negative saturation distribution. Since the trends noted were the same for all devices only one is discussed in detail in the remainder of this section.

Device number 14-41 was annealed at 75°C with a -3.0 volt bias for a period of one hour in order to insure a negative saturation oxide condition. A capacitance-bias voltage curve was taken and the device then irradiated for one minute in the Gammacell. The device was then annealed at 75°C with a -3.0 volt bias applied for 15 minutes. A device curve was taken and the same irradiation-anneal-device curve pattern was followed for four more irradiations. The time intervals of each of the subsequent irradiations were 2 minutes, 3 minutes, 2 minutes, and 2 minutes. While curve 1 of Figure 9.1 is for the device before irradiation and curve 2 applies after the first irradiation,curves 3 through 6 are for the subsequent irradiations mentioned above. Curves 7 through 10 of of the same figure are for relatively long-term irradiations of the device. The pertinent radiation information for the above mentioned curves is presented in Table 9.1

A parallel shift of the device curve along the voltage axis is evidence of a change in oxide charge density, oxide charge position, or both. Since curves 1 through 10 of Figure 9.1 are for the device in the negative saturation condition, the voltage change noted between those curves is

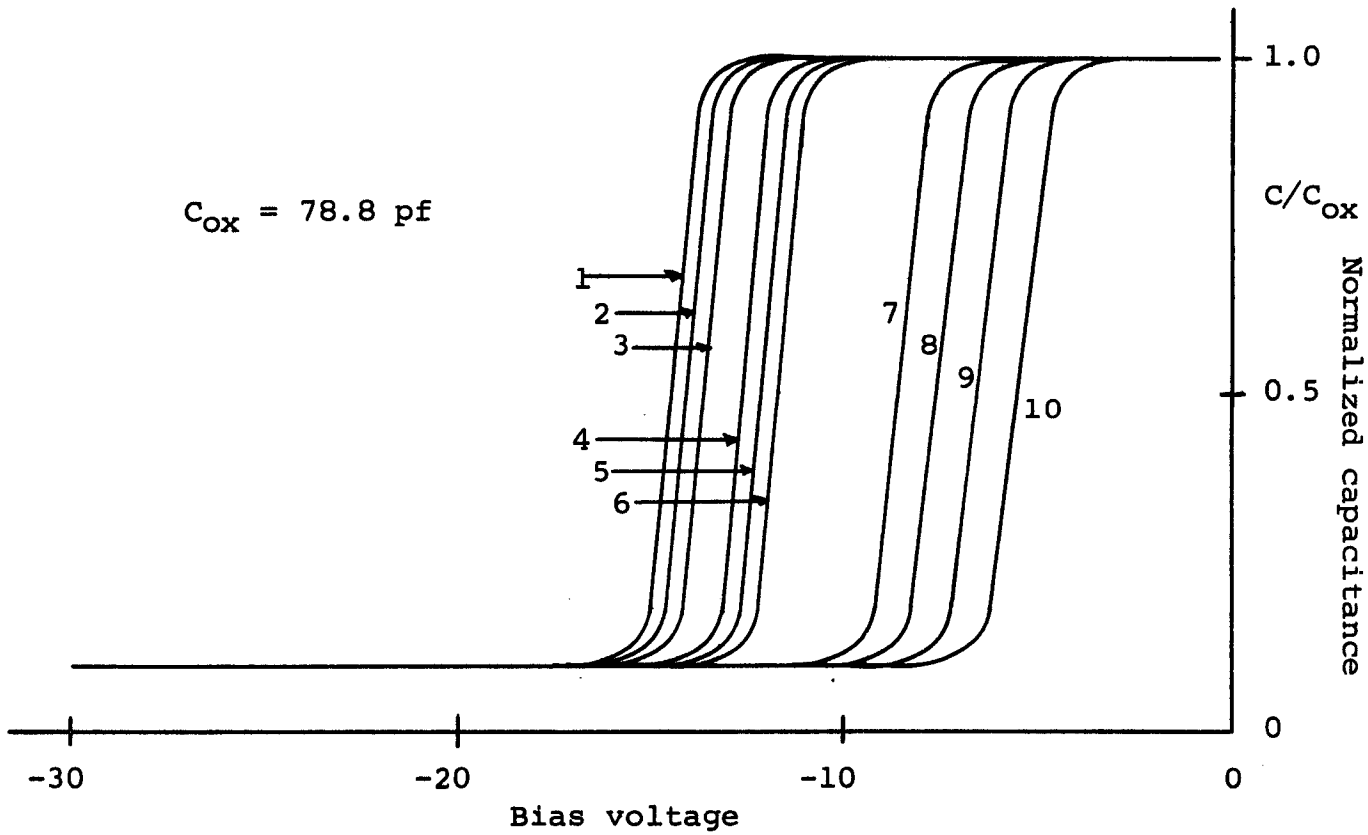


Figure 9.1. Negative saturation capacitance-bias voltage curves: curve (1) was taken prior to irradiation while curves (2) through (10) were taken after irradiation periods as shown in Table 9.1

Table 9.1. Co^{60} irradiation information for device 14-41; see Figure 9.1 for device curves

CV-curve taken after irradiation	Time of irradiation (minutes)	Exposure (roentgens)	Total exposure
1	0	0	0
2	1	1.97×10^3	1.97×10^3
3	2	3.44×10^3	5.37×10^3
4	3	5.91×10^3	1.12×10^4
5	2	3.44×10^3	1.47×10^4
6	2	3.44×10^3	1.81×10^4
7	60	2.00×10^5	2.18×10^5
8	470	1.57×10^6	1.78×10^6
9	600	2.00×10^6	3.78×10^6
10	720	2.40×10^6	6.18×10^6

indicative of a charge change at the semiconductor surface. The change can be calculated by means of equation (7.1). The resulting semiconductor charge change is due in turn to a change in the integrand of equation (4.4). This is treated in the next section.

That semiconductor charge change is shown as a function of total gamma ray exposure time in Figure 9.2 for the initial short-term irradiations and in Figure 9.3 for the long-term exposures. The charge change was calculated by the above-mentioned method.

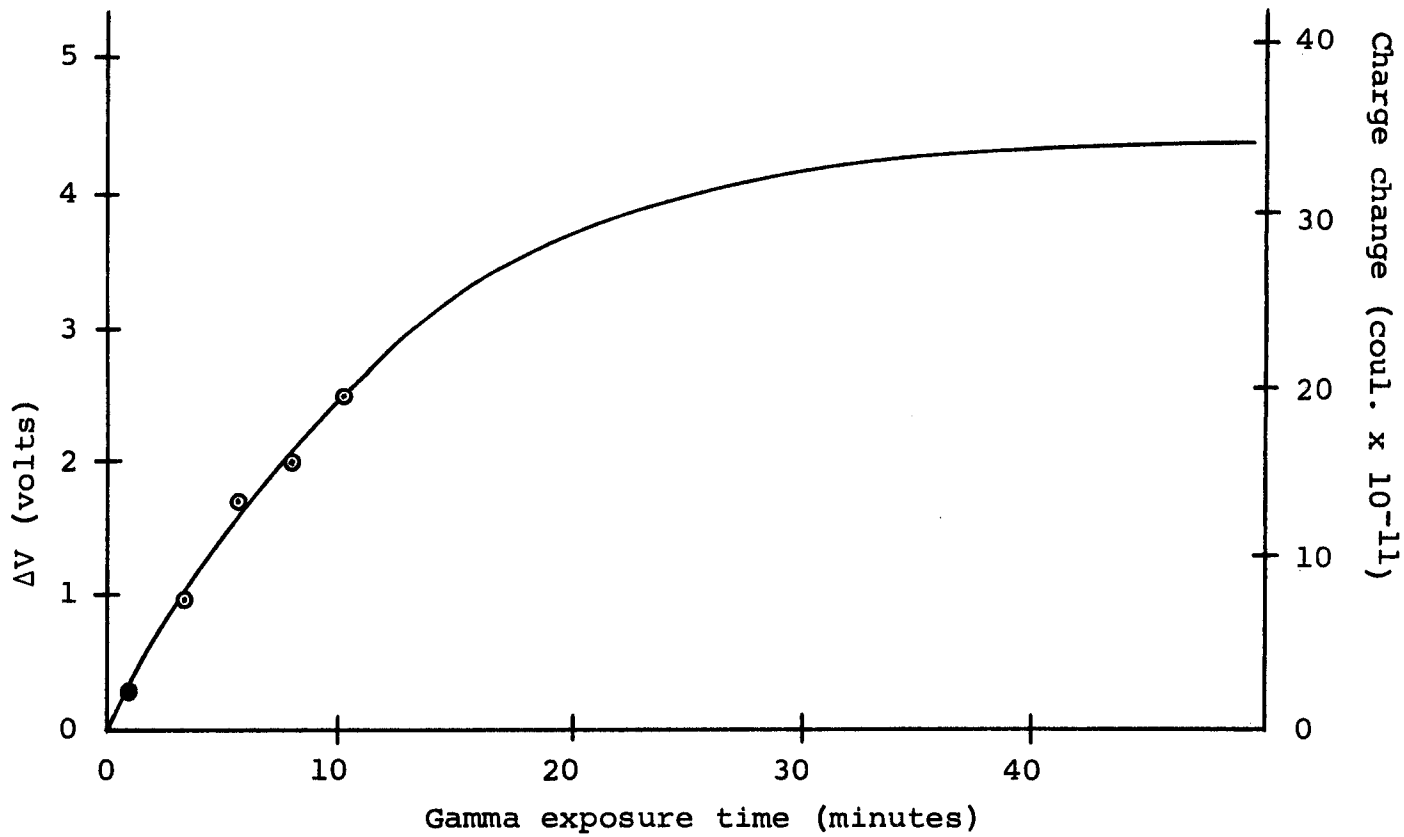


Figure 9.2. Semiconductor charge change and device curve voltage shift as a function of gamma irradiation time for small times

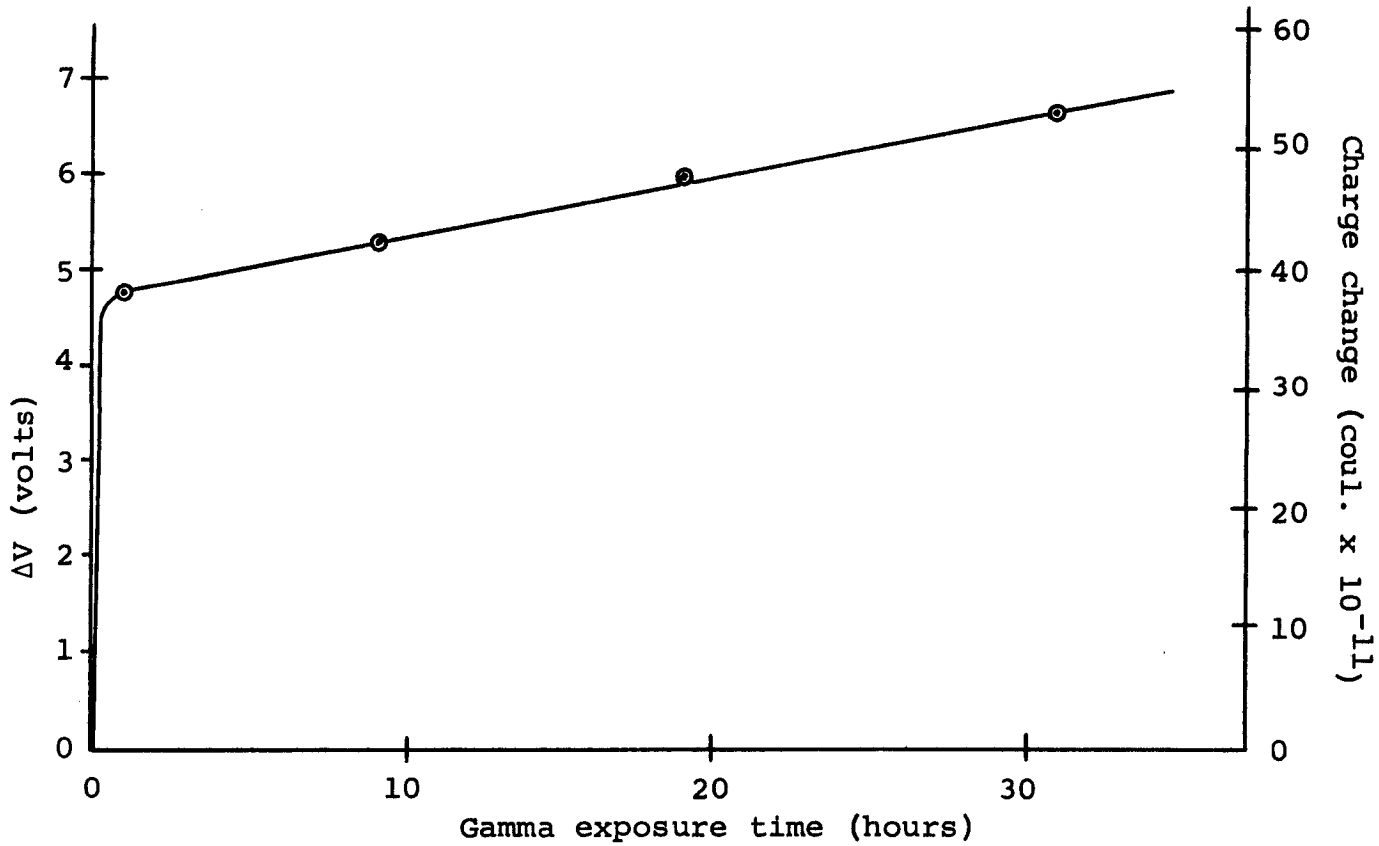


Figure 9.3. Semiconductor charge change and device curve voltage shift as a function of gamma irradiation time for large times

As can be seen from the capacitance-bias voltage curves of Figure 9.1 the surface state density increase due to irradiation was not completely recoverable by annealing techniques. This is so since the curves taken for the device in the negative saturation condition after gamma ray exposures have slightly decreased slopes with respect to the pre-irradiation curve. These surface state density changes due to radiation are, however, negligibly small with respect to those present before annealing.

9.3 A Model for the Calculation of the Oxide Charge Change

Snow et al. (1965) contaminated their oxides with a relatively small amount of sodium chloride. The oxide charge density was thus sufficiently low that the devices could be taken into either strong accumulation or strong inversion regimes of operation, even after all that charge had been drifted to the oxide-semiconductor interface, without worry of oxide breakdown. Those authors drifted all the oxide charge to the oxide-semiconductor interface and hence were able to use equations (4.4) and (7.1) to determine that oxide charge density.

In the case of the steam grown oxides which are investigated herein, the oxide charge density was so great that it was impossible by the application of bias voltage to cause an n-type device to convert from the accumulation regime to the

inversion regime of operation after that oxide charge had been drifted to the oxide-semiconductor interface. This was so since the magnitude of the electric field necessary for such a surface conversion was well above the oxide breakdown value. For this reason a method was developed for estimating the oxide charge change which caused a corresponding horizontal device curve displacement in this case.

All regions of the device curve were found to be easily obtainable with a bias voltage well below the oxide breakdown value when the oxide charge had been drifted to the negative saturation position. Hence, the amount of voltage by which the negative saturation device curve was displaced due to a gamma exposure was recorded and used to determine the semiconductor charge change in the usual manner. That charge change was due to a corresponding change in the net oxide charge which was located at the metal-oxide-interface.

A rather simple model was then fabricated which enabled one to calculate within an order of magnitude the oxide charge change due to the gamma ray exposure. All the oxide charge was assumed located in the region of the oxide immediately adjacent to the metal-oxide-interface. An effective constant charge density, A, was assumed to extend from the metal-oxide-interface a distance, d, into the oxide. Since the oxide was always in the negative saturation condition during acquisition of the device curve data, the total semiconductor charge change

noted as a function of gamma exposure was then due to the oxide charge concentration change. Hence, equation (4.2) relating the semiconductor and oxide charges can then be written

$$dQ_s = \frac{x}{x_o} \; Adx \tag{9.1}$$

where

A = the oxide volume charge density (coul cm^{-3})

x_o = oxide thickness (cm)

x = distance into oxide measured from metal (cm)

Q_s = semiconductor charge density (coul cm^{-2})

Since the oxide charge was assumed present between $x = 0$ and $x = d$, integration of the above equation with these limits yields the following:

$$Q_s = \frac{Ad^2}{2x_o} \tag{9.2}$$

This can be solved for A and written in incremental form as

$$\Delta A = \frac{2x_o \, \Delta Q_s}{d^2} \tag{9.3}$$

The incremental oxide surface charge density can then be written as

$$\Delta N = \frac{\Delta Ad}{q} \tag{9.4}$$

where

ΔN = the oxide charge density change (cm^{-2})

q = the electronic charge (coul.)

This equation, subject to the above mentioned constraints, enables one to calculate the oxide charge density change by the knowledge of the semiconductor charge change. The following section will utilize this equation to determine ΔN and d to within an order of magnitude.

9.4 A Model Explaining the Observed Oxide Charge Variations

The radiation-induced oxide charge change observed and calculated was that of a net decrease in the positive charge density of that oxide. No information is available to determine whether the observed charge was caused by the removal of positive charges or the addition of negative charges tending to neutralize the former. In view of the fact that the amount of charge in the oxide is a constant which cannot be changed by elevated temperature annealing with various applied bias voltages and also since oxide charge is definately not mobile at room temperature, it is assumed that the gamma radiation cannot affect a decrease in the concentration of these alkali ions. It is felt that this is an extremely good assumption since the only method found thus far and reported on in the leterature by Hofstein (1966) to remove oxide charge is that of drifting the charge to the oxide surface and then subsequently removing a layer of that surface.

Evans (1955) discusses general gamma irradiation of materials and presents a diagram showing energies at which each

of the principal gamma ray processes becomes predominant. This diagram is shown in Figure 9.4. Since the energy of the principal gamma flux in the Gammacell sample chamber is 1.175 MeV and the atomic numbers of silicon and oxygen are 8 and 14 respectively, it is concluded that the Compton Effect is the predominant gamma scattering process which occurs in the silicon dioxide. The range of 1.175 MeV gamma rays is greater than 15 gams cm^{-2} as deduced from Price (1958), hence, it is concluded that the Compton Effect occurs uniformly throughout both the oxide and the semiconductor.

The Compton Effect occurs when an impinging photon of energy $h\nu$ strikes and frees an atomic electron leaving behind an electron vacancy, or hole, and giving off another photon of lower energy $h\nu'$ as is shown in Figure 9.5 for silicon. It can thus be assumed that the generation of hole-electron pairs occurs uniformly throughout the oxide. On the basis of information given by Price (1958) one can made a rough calculation of the photon flux rate in the Gammacell sample chamber as being approximately 1.2×10^{11} $cm^{-2}sec^{-1}$.

Figure 9.6 shows a potential band diagram of the oxide in the negative saturation condition. Since the electric field is equal to the negative gradient of the potential, it is concluded that the thin section of oxide adjacent to the metal gate electrode contains a relatively high positive electric field while the remainder of the oxide contains a

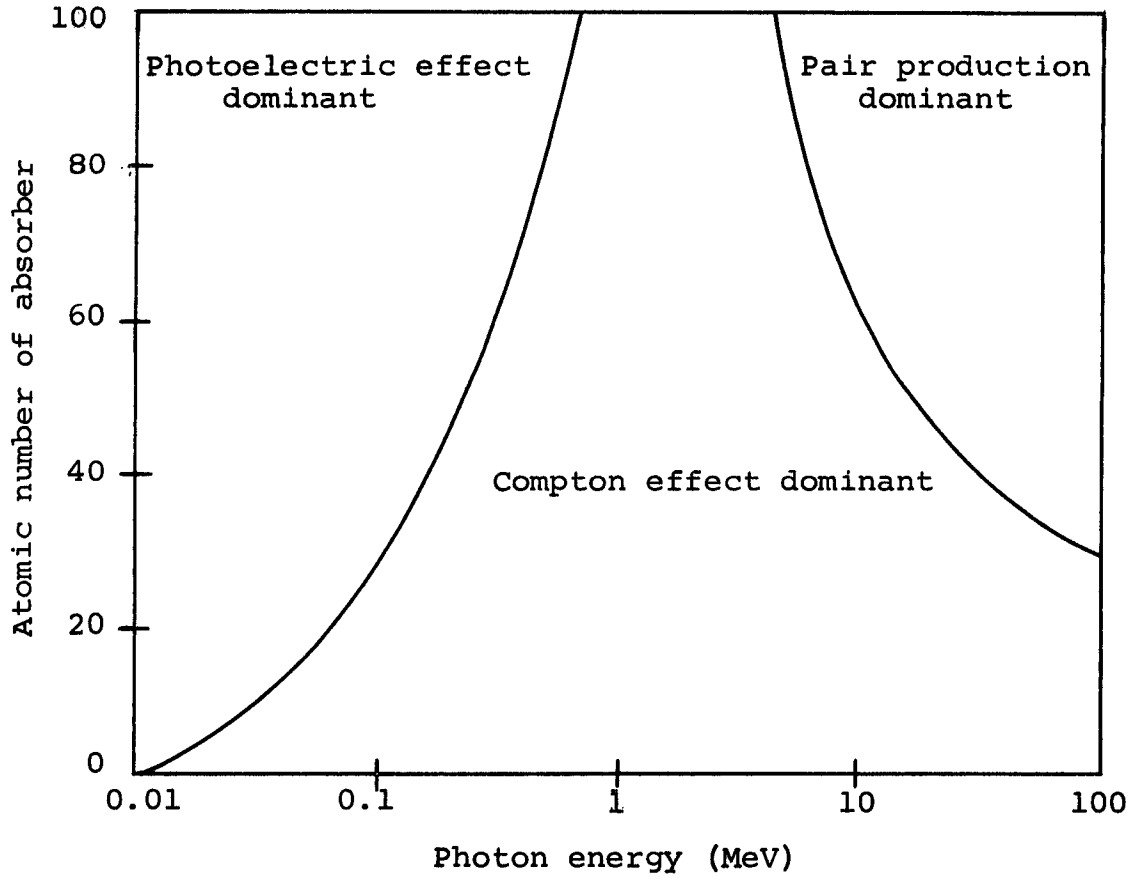


Figure 9.4. Diagram showing energies at which each of the principal gamma ray processes becomes dominant (Source: Evans (1955), p. 712)

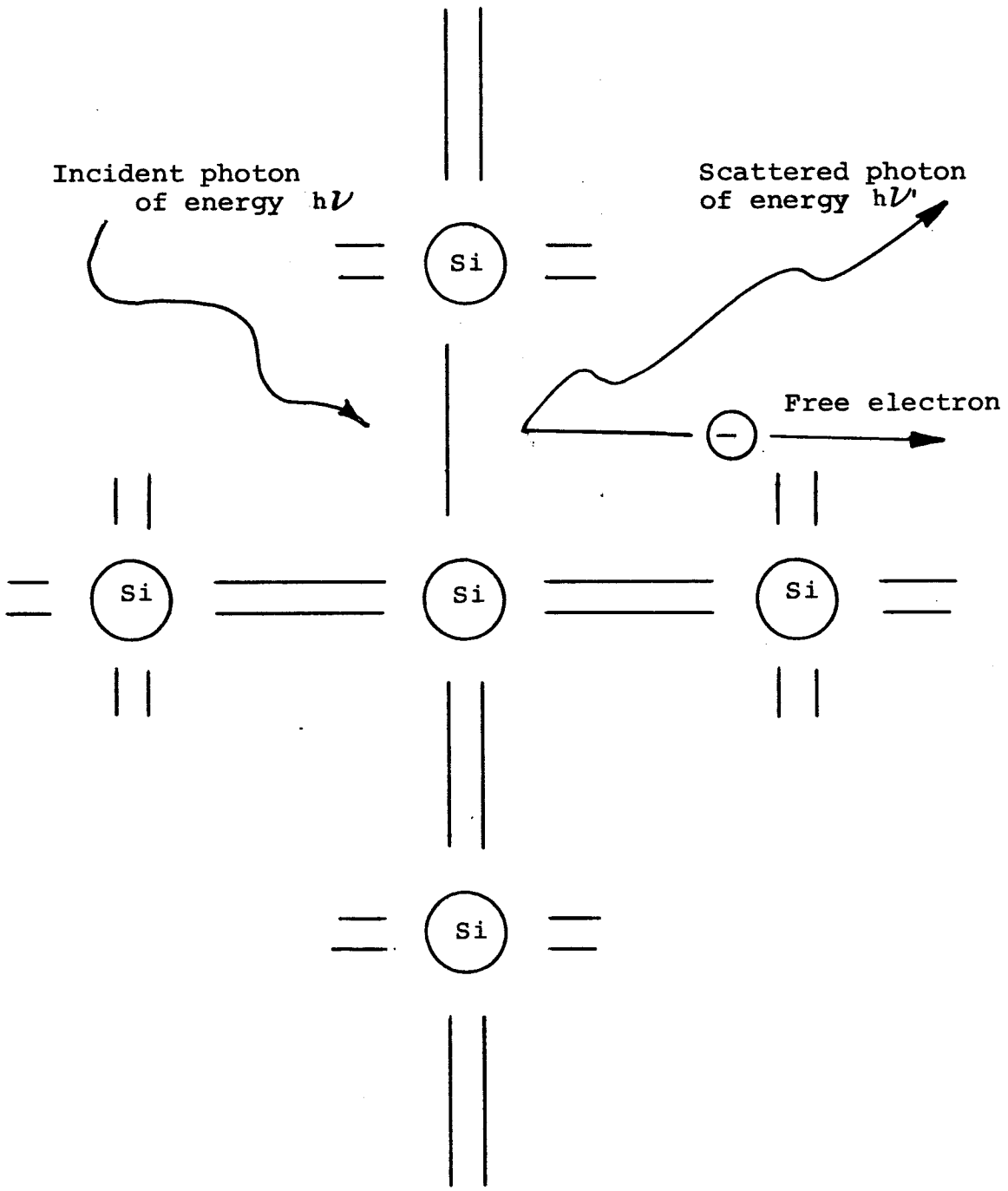


Figure 9.5. Diagram of the Compton effect in silicon

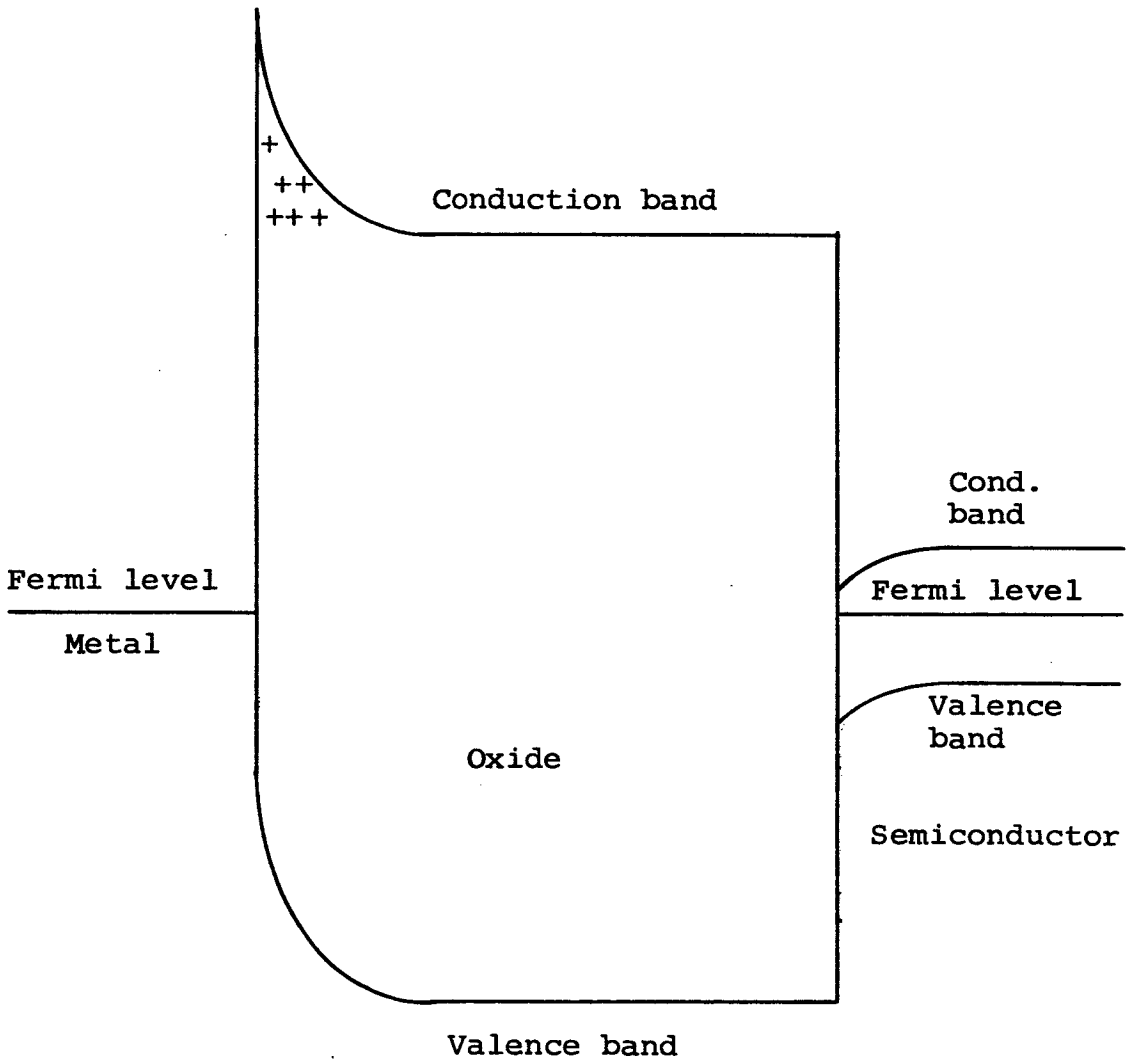


Figure 9.6. Band diagram of the MOS structure with the oxide in the negative saturation condition

much smaller negative electric field. Mobile electrons and holes generated in a thick relatively low electric field region will recombine much more quickly than those generated in a rather thin high field region since they will remain in close proximity for a longer period of time.

On this basis it is concluded that holes generated by the Compton Effect in the metal gate space-charge-region of the oxide are swept to the metal gate while the electrons remaining in the positive space charge oxide region neutralize the alkali-ions therein. The electron-hole pairs generated in the remainder of the oxide are assumed to recombine readily. This process is shown diagrammatically in Figure 9.7.

At this point the material presented in the previous section can be utilized to carry out a calculation for the determination of the approximate oxide charge change and the approximate oxide charge layer thickness.

It is generally assumed in radiation detection work that only one Compton scattering occurs per photon due to a normal 1 MeV photon flux through a one inch thick low density material. This will also be assumed for the dielectric oxide of the devices since it is no greater than 3500 Å thick.

The well-known gamma ray attenuation relation given by Price (1958) can be written as

$$I = I_o \, e^{-\mu x} \tag{9.5}$$

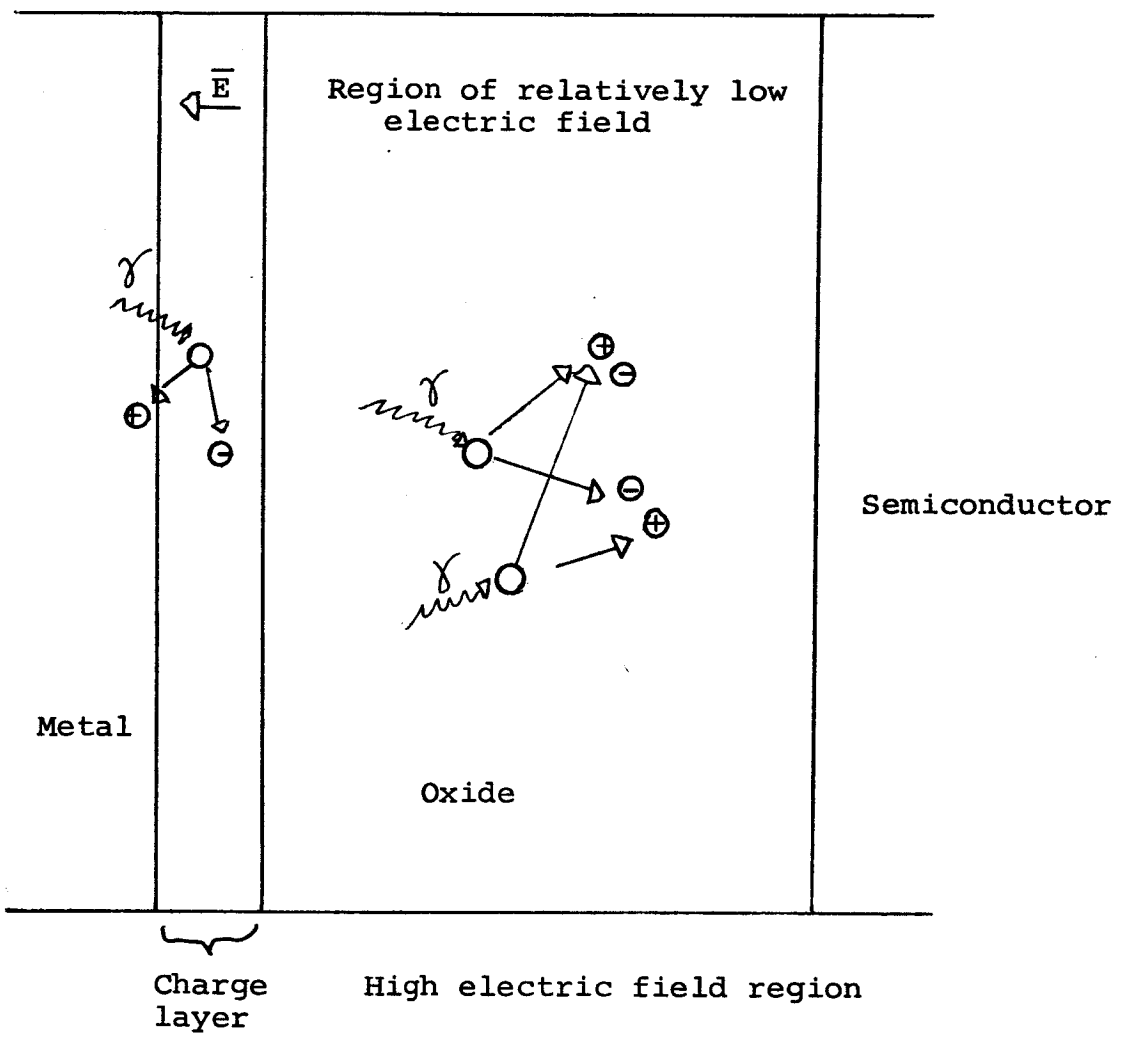


Figure 9.7. Diagram of hole-electron pair generation by the Compton effect in the oxide

where

I = incedent flux of photons (cm^{-2})

I_o = photon flux after traveling a distance x through through the material (cm^{-2})

μ = total linear attenuation coefficient (cm^{-1})

x = distance of photon travel in material (cm)

Since the volume generation rate for electrons is given by the negative divergence of the photon flux the following equation results.

$$g_V = I_o \ \eta \mu e^{-\mu x} \tag{9.6}$$

where

g_V = electron volume generation rate (cm^{-3})

η = quantum efficiency

The number of electrons generated in a given distance and a given time on a per-unit-area basis is then

$$\Delta N = \int_o^d \int_o^t g_V \, dtdx \cong I_o \eta \mu td \tag{9.7}$$

where

d = the region thickness (cm)

t = time of generation (sec)

and where $\mu d << 1$.

By means of equations (9.4) and (9.7) one can predict a value of η with d as a parameter. This quantum efficiency is a ratio of the number of hole-electron pairs generated to the

number of primary gamma photons. Since it is assumed that only one hole-electron pair results from each Compton scattering, the remainder of those generated will be assumed due to the high energy Compton recoil electron. The energy of such a recoil electron is given by Price (1958) as

$$E = E_I \frac{(1 - \cos \theta)\ E_I/mc^2}{1 + (1 - \cos \theta)\ E_I/mc^2} \tag{9.8}$$

where

E_I = energy of primary photon (eV)

θ = scattering angle (degrees)

m = rest mass of an electron (kg)

c = velocity of light (cm sec^{-1})

If θ is allowed to range from 0° to 180° the resulting recoil electron energy will range from 0 to approximately 800 keV. This energy range will be used as a constraint since the energy of each secondary electron will have to lie therein. Since an energy of 3.23 eV is needed to create a hole-electron pair in a 1.1 eV band-gap material such as silicon, according to Baldinger et al. (1960), it seems reasonable that at least 10 eV would be needed to generate a hole-electron pair in an 8.0 eV band-gap material such as silicon dioxide. Hence, it can be stated that the energy of each Compton recoil electron must be approximately equal to the product of the quantum effeciency and the above mentioned 10 eV hole-electron pair generation energy; where the quantum efficiency is assumed much greater than unity. If equations (9.4) and (9.7) are

now used to calculate η and the above relation used to calculate the Compton recoil electron energy where d is given the values 1 Å, 10 Å, 100 Å, and 1000 Å, and a semiconductor charge change of 1.6×10^{-8} coul cm^{-2} is noted in 6 minutes; the recoil electron energies necessary are approximately 10^{10}eV, 100 MeV, 1 MeV, and 210 keV respectively.

It is evident that the 1000 Å oxide charge sheet thickness is the only one in the above group which is within reason as far as recoil-electron energy is concerned. Hence, it is evident that the charge sheet thickness which must be assumed if the charge is taken to be distributed uniformally throughout the region is on the order of 1000 Å. This gives rise to an oxide charge change of approximately $7 \times 10^{11}(cm^{-2})$ which is on the order of the value of charge change reported by Grove and Snow (1966) due to 35 keV X-radiation.

It is worth mentioning, at this point, that a charge density of approcimately $10^{11}cm^{-2}$ distributed over 1000 Å gives rise to an electric field of less than one volt cm^{-1}. This allows one to make the assumption of a negligible voltage drop due to charge distributed throughout the oxide which is mentioned in chapter 3. The above leads to a charge change of approximately $1 \times 10^{11}cm^{-2}$ min^{-1} for the linear portion of the oxide charge change versus radiation time curve. A reason for oxide charge neutralization saturation is now given.

It is assumed that the process of alkali-ion neutralization by electrons continues until the high electric field

is reduced, which corresponds to a total generation of approximately 10^{11}electron-hole pairs (cm^{-2}). With this field reduction, holes remain in the oxide surface region for a greater length of time and thus have a much higher probability of recombining with an electron or being trapped, which tends to further decrease the space charge and thus the field. This explains the occurance of a saturation effect in the net positive charge decrease in the oxide with increasing gamma ray exposure time.

This model, based upon the Compton Effect in the oxide, explains not only the decrease in net positive oxide charge but also the saturation effect in oxide charge change with irradiation time as was noted in all the data.

10. SUMMARY, CONCLUSIONS, AND RECOMMENDATIONS FOR FURTHER STUDY

10.1 Summary and Conclusions

Metal-oxide-semiconductor capacitors were fabricated and capacitance-bias voltage curves were obtained both before and after annealing and gamma radiation sequences.

It was concluded on the basis of parallel device curve shift with annealing time for different temperatures that the mobile oxide charge was positive and had an activation energy very nearly that of the alkali ions, i.e., sodium and lithium. The method of Snow et al. (1965) discussed in chapter 4 of this work was used for oxide charge characteristic determinations.

Surface state density calculations were carried out on the basis of the method of Zaininger (1964) presented in chapter 3. It was found that the gamma radiation did increase the surface charge density by an order of magnitude from $10^{11}cm^{-2}eV^{-1}$ to $10^{12}cm^{-2}eV^{-1}$after a 3.6 x 10^6 roentgen exposure. This was noted for both p- and n-type substrate devices. More important is the fact that a negative-bias elevated-temperature anneal (75°C, -3.0 volt bias for 15 minutes) was found to restore the surface state charge density to vary nearly its original, pre-irradiation value.

Devices fabricated on n-type substrates were taken through a series of annealing and Co^{60} irradiation periods from which it was learned that the effect of the radiation was that of causing a net decrease in the observed oxide

charge density from about 1×10^{12} to $5 \times 10^{11} cm^{-2}$. This charge decrease is attributed to ion neutralization caused by the creation of hole-electron pairs by means of the thermalization of high energy Compton-recoil electrons. A model based upon Compton scattering in the oxide which assumed the the oxide charge to be located in a uniform density sheet of approximately 1000Å thickness was used to predict the oxide charge change due to the 1.175 MeV gamma radiation.

The model yields a quantum efficiency of 2×10^4 for Compton-recoil electrons with energies ranging from 0 to 800 eV which is believed quite reasonable.

10.2 Recommendations for Further Study

A method for confirming the presence of sodium in the oxide is available. It involves the changing of stable sodium to a radioactive isotope by means of thermal neutron radiation. Such a study is recommended in that lithium which has an activation energy relatively near that of sodium is not detectable by such means.

Anisotropies are noted in the growth of silicon dioxide on a silicon substrate. This would lead one to believe that the substrate surface charge density would be a function of the orientation of that surface in the crystal. A study of the dependence of both pre- and post-irradiation surface charge state density as a function of surface orientation in the crystal is recommended in that the obtained results may be

helpful in discovering the cause of the noted oxide growth rate anisotropy.

Since surface recombination velocity measurements can be readily made on semiconductor wafers covered with a transparent oxide, a study involving such measurements is recommended to determine any differences in the oxide-semiconductor interface due both to different oxide growth techniques and also to different crystal surface orientation.

Silicon nitrite is presently being considered as the dielectric material in insulated-gate field-effect transistors. A study similar to the one reported on herein is recommended in order to determine the density, distribution and type of any mobile oxide charges which may be present. After such oxide charge information is gained, a study of radiation effects on those charges is recommended from a commercial standpoint. The above-mentioned studies for silicon dioxide are also recommended for silicon nitride for the same reasons as were mentioned for the former.

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12. APPENDICES

12.1 Appendix A

The following is a summary of the constant field ion transport model of Snow et al. (1965): as can be seen from Figure 4.41 (part a) a zero field plane will be non-existant if the applied bias, V_g, is greater than the zero bias metal-oxide interface voltage, Q_o/C_o volts. If the applied field is increased beyond this point the field depression in the boundary layer caused by the initial charge becomes increasingly unimportant. Hence, Snow et al. (1965) described this situation by assuming a constant field throughout the oxide. This field is due to the applied bias, V_g, and is given by

$$E_o = V_g/x_o \tag{12.1}$$

Equation (4.9) is then given by:

$$\frac{\partial N}{\partial t} = D\,\frac{\partial^2 N}{\partial x^2} - \mu E_o\,\frac{\partial N}{\partial x}\ ,\quad 0 < x < x_o,\ \ t > 0 \tag{12.2}$$

The initial condition of a thin sheet of ions at the metal-oxide interface was given by

$$N(x,0) = (Q_o/q)\ \delta(x), \tag{12.3}$$

where $\delta(x)$ is a delta function of the x domain.

The boundary conditions which dictate conservation of charge in the oxide were given as

$$- D(\partial N/\partial x) + \mu E_o N = 0, \; x = 0, \; x = x_o; \; t > 0 \qquad (12.4)$$

The author assumed that $(Dt)^{\frac{1}{2}}$ and $E_o t$ were each much shorter than x_o which yielded a relatively simple solution to equation (12.2) for small values of time. That solution is given by

$$N(x,t)/(Q_o/q) = \Big[1/(\pi Dt)^{\frac{1}{2}} \exp - \big[x/2(Dt)^{\frac{1}{2}} - \mu E_o t^{\frac{1}{2}}/2D^{\frac{1}{2}}\big]$$
$$- (\mu E_o/2D) \exp \; \mu E_o x/D \cdot \operatorname{erfc} \; (x + \mu E_o t)/2(Dt)^{\frac{1}{2}}\Big] \qquad (12.5)$$

The excess charge induced in the silicon due to this time-varying charge distribution was calculated by means of equation (4.26) and is given as

$$\frac{Q_s'}{Q_o} = - \; 2(Dt)^{\frac{1}{2}}/x_o \;\; K(\mu E_o t^{\frac{1}{2}}/2D^{\frac{1}{2}}) \qquad (12.6)$$

where

$$K(z) = (1/2\pi^{\frac{1}{2}}) \exp(-z^2) - (1/8z) \operatorname{erfc}(z)$$
$$+ z(\tfrac{1}{2} - 1/8z^2)(1 + \operatorname{erfc}(z)) \qquad (12.7)$$

Snow <u>et al</u>. reported that Q_s' is proportional to $t^{\frac{1}{2}}$ for small periods of time, $t \approx D/(\mu E_o)^2$, and is thence proportional to t and E_o.

12.2 Appendix B

The method used for determining surface charge density is outlined at the end of chapter 3. It is assumed that two identically shaped capacitance-bias voltage curves have been obtained and are displaced by an amount ΔV along the voltage

axis. If equation (3.32) is now used, two curves relating $dVsc/d\psi s$ and V will be obtained which are displaced by amount Δ V. Since it was implicitly assumed that both curves have the same value of oxide capacitance and minimum capacitance, the same curve of $dVsc/d\psi s$ versus ψs can be used with each curve of $dVsc/d\psi s$ versus V to obtain V as a function ψs. The two relations between V and ψs will be functionally the same but displaced by V. Hence potential equation (3.18) can be written for both cases as:

$$V(\psi_s) = V_{ss}(\psi_s) + V_{sc}(\psi_s) + \psi_s \qquad (12.8)$$

and

$$V(\psi_s) + \Delta V = V_{ss}(\psi_s) + V_{sc}(\psi_s) + \psi_s \qquad (12.9)$$

Since the surface charge density is given by equation (3.43) as

$$N_{ss} = (C_{ox}/g)(dV_{ss}/d\psi_s) \qquad (12.10)$$

it is evident that N_{ss}' will be the same for both equations (12.8) and (12.9) and hence for both device curves due to the fact that the voltage displacement, ΔV, is a constant.