OCT 8 1965

A NEGATIVE CAPACITY ELECTROMETER USING MOS TRANSISTORS

By Gordon J. Deboo and Clifford N. Burrous

Ames Research Center, NASA
Moffett Field, California

FACILITY FORM 602

N66-85956
(ACCESSION NUMBER)

18
(PAGES)

TMX 56890
(NASA CR OR TMX OR AD NUMBER)

(THRU)

None
(CODE)

(CATEGORY)

[redacted]

Summary

A miniature, high-performance, negative-capacity electrometer preamplifier has been developed. The circuit takes advantage of a new dual MOS transistor, which features high input impedance, low input leakage current, and improved tracking of characteristics with temperature. The need for such an amplifier, and its design and performance are discussed.

Introduction

The preamplifier was originally designed for use with intracellular microelectrodes in recording bioelectric potentials. However, because of its characteristics, it is believed to be applicable to a wide variety of measurement problems, especially where stable wide-band d-c amplification from high impedance sources is required, for example, as a pickup plate video amplifier in storage tube tests,[1] and for pH and ionization chamber measurements.

In studies on individual nerve and muscle cells, potentials are measured with microelectrodes which have extremely small tip diameters. Because of their tiny contact area, such electrodes have very large impedances - of the order of megohms. Since the potentials being measured are of very small magnitude, the circuit input current must be as small as possible for two reasons. First, such currents can polarize the microelectrode, causing voltage drift. Secondly, although the magnitude of the current may be small, the current density may be large, and may damage the tissue being studied.

[redacted]

If the input current is kept below 10^{-13} A, its effects will be suitably minimized.[2,3,4] The only devices that can maintain such a current level without temperature-sensitive balancing schemes are the MOS transistor and the electrometer vacuum tube. The MOS transistor was selected rather than an electrometer tube because of its reliability, power, and size. Miniaturization is desirable since it allows the preamplifier to be mounted close to the source, thereby minimizing stray input capacities.

MOS transistors, in common with other high impedance devices, have higher voltage noise levels than devices that operate at lower impedance levels. While the noise level might be significantly reduced by using junction FET's, for example, the higher input current characteristic of these devices is intolerable. A number of excellent amplifiers have been described in the literature,[2-7] but none of them were suitable for this application either because they used vacuum tubes, required many adjustments, or required painstaking selection of temperature compensation components.

Equivalent Input Circuit

A microelectrode implanted in biological tissue is properly represented by a distributed resistance and capacity network, energized by a group of distributed sources. While a true simulation of this network is not possible, a useful equivalent input circuit for the system is shown in Figure 1, where V is the potential being measured and R_e is the source or microelectrode resistance. The total capacity that shunts the input resistance has three components.

The first is the input capacity, C_a, of the preamplifier which depends on the interelectrode capacities, the preamplifier gain, and the circuit configuration used. The second component, C_s, is the capacity from the amplifier input lead to the surroundings. The third component, C_e, is the source capacity which, in the case of the intercellular microelectrode, appears because the electrode and the cellular tissue form two conductors isolated from each other by an insulator, thereby forming a capacitor. In the equivalent circuit, the various components are assumed to be lumped. If the probe resistances were typically of the order of $2 \times 10^7\ \Omega$ and the total capacities were as much as 10^{-11} F, the frequency response would be limited to about 800 cps, which is an order of magnitude less than that desired.

Circuit Design

The requirements for low input current, high input resistance, low noise, low output impedance, and small size can easily be met by using an MOS transistor in conjunction with bipolar transistors.

If all three electrodes of the input transistor, plus a shield covering the preamplifier input lead, are driven at a potential close to that of the input of the preamplifier, the effect of $C_a + C_s$ can be minimized. This technique will not work for reducing C_e, however, because C_e may not be accessible.

It is possible to compensate for the effects of C_a, C_s, and C_e by using an input circuit which, in effect, has a negative input capacity as shown in Figure 2. When C_1 is made equal to $-C_2$, the effective capacity from point Y to ground is zero. Figure 3 is a

block diagram of such a circuit. It is assumed that amplifiers A and B have infinite input resistance, zero output impedance, and zero phase shift. Amplifier A has a gain of unity and B has a gain of K; R_e is the source resistance, C_t is the sum of all components of capacity appearing at the input, and C_f is a capacitor that provides positive feedback since there is zero phase shift around the loop. The principle of operation is explained in the following paragraphs.

Remove the connection between points P and Q. If a square wave, e_1, is fed into the input, the voltage, e_2, will have an identical waveform and amplitude because of the characteristics of amplifier A given above. The voltage e_3 will also have the same waveform as e_1 because of the characteristics of amplifier B, but will have an amplitude

$$e_3 = Ke_2 = Ke_1 \tag{1}$$

C_f and C_t form a voltage divider such that

$$e_4 = \frac{e_3(1/j\omega C_t)}{(1/j\omega C_t) + (1/j\omega C_f)} = Ke_1 \frac{C_f}{C_f + C_t} \tag{2}$$

Since this expression is independent of frequency, e_4 has the same waveform as e_1.

Now choose K so that

$$K = \frac{C_f + C_t}{C_f} \tag{3}$$

Then

$$e_4 = e_1 \tag{4}$$

The potentials at points P and Q are therefore equal, independent of frequency, and can be connected without disturbing the circuit

operation. Thus, a square wave input e_1 results in an identical output e_2 in spite of the presence of resistance R_e and shunt capacity C_t.

Figure 4 is a circuit diagram of a practical negative-capacity preamplifier. The input signal is coupled to the gate of Q_1a, which is one-half of a dual MOS transistor used in a differential amplifier configuration. This type of circuit has a number of advantages. Temperature compensation is achieved automatically by differential action and because both transistors are diffused on a single substrate. Also, having two input terminals available simplifies the design of the circuit since both positive and negative feedback from a single-ended output is required. The circuit configuration requires isolated source leads from Q_1. Although the dual MOS transistor used has common source leads, it has separate drain leads, so advantage was taken of the symmetry of the device and the drain and source leads were interchanged. Since the leads for the sources are electrically isolated and can be at different potentials, the MOS body could not be connected to the sources, as is usual. Instead, it was connected to the positive supply, which maintains the necessary bias condition. The required open-loop gain is provided by Q_2, Q_3, and Q_5 and a low output impedance by Q_6. The temperature drift of Q_4, a constant-current generator, is compensated by C_{R_1}. The selection of values for R_1 and R_c is interesting for two reasons. First, they cannot be omitted because the source currents would then be limited to the base currents of Q_2 and Q_3. Such a low current would result in a voltage gain of considerably less

than unity for Q_1a and Q_1b, because of the low transconductance achieved with MOS devices at low current levels. Secondly, it is possible to adjust the drain current so that the temperature coefficient of the gate-to-source voltage is approximately zero. This is done by adjusting R_1 and R_6 to allow for drain currents of approximately 250 μA. R_7 and R_8 form a 2 to 1 negative feedback potential divider, which sets the closed-loop gain at 2. The feedback capacitor value can be calculated from equation (3) if the maximum shunt capacity at the input is assumed to be 10 pf. Rearranging equation (3) yields

$$C_f = \frac{C_t}{K - 1} = \frac{10}{2 - 1} = 10 \text{ pf}$$

Care must be taken to insure the stability of a circuit which has a high open-loop gain with both overall positive and negative feedback. In the present design, resistor R_2 (22K) is shunted with C_1 (470 pf), giving the 20 db/decade roll-off in open-loop frequency response necessary for stability.

If the negative capacity control, R_{11}, is overadjusted the circuit will oscillate, but when the circuit is adjusted for critical damping, it is stable.

Performance

The measured performance of the negative capacity preamplifier is tabulated below:

Voltage gain	2
Bandwidth - 50 Ω source	0 - 140 kcps

Input time constant with compensation adjusted for critical damping with:	
(a) 22 MΩ source	9 μs
(b) 100 MΩ source	12 μs
Input resistance	$> 10^{14}$ Ω
Drift measured at preamplifier output	75 μV/°C
Input leakage current	0.9×10^{-15}A
Equivalent input noise voltage*	
(a) With a 22 MΩ source resistance, measured over a 3 db bandwidth of 17.8 kcps, corresponding to a 9 μs input time constant.	198 μV RMS
(b) With a 100 MΩ source resistance, measured over a 3 db bandwidth of 13.3 kcps, corresponding to a 12 μs input time constant.	234 μV RMS
Power required	±9.4 V at 2.4 mA
Weight	4 g
Volume	3.6 × 1.1 × 1.0 cm

*A 22 MΩ resistor generates 104 μV RMS over a 3 db bandwidth of 17.8 kc, while a 100 MΩ resistor generates 187 μV RMS over a 3 db bandwidth of 13.3 kc.

Figure 5 shows the response of the circuit to a square wave input with a 22 MΩ source impedance. The square wave cannot be applied from a voltage source through a resistor because the shunt capacity of the resistor causes a peaking effect which results in an apparent rise

time faster than the real one. Instead, a triangular wave is fed through a very small differentiating capacitor to the preamplifier input,[8] which is shunted by both the resistance and the capacity of the 22 MΩ resistor. Thus, the capacity of the source appears like any other input shunt capacity and can be effectively removed by appropriate adjustment of the negative capacity control, and the differentiated triangular wave produces the desired square wave input to the preamplifier.

Figure 5(a) shows the input waveform and Figure 5(b) the output waveform with zero positive feedback, that is, no negative capacity. The output time constant is about 100 μs, indicating an actual input capacity of about 5 pf. Figure 5(c) shows the output waveform with optimum adjustment of the negative capacity control R_{11}. Figure 5(d) shows the effect of too much negative capacity, specifically, with 20 percent more positive feedback than was used in Figure 5(c). Figure 5(e) is an expanded version of Figure 5(c), with optimum adjustment of negative capacity control. The measured time constant is 9 μs. To obtain this time constant with a 22 MΩ source, the effective input capacity must have been 0.4 pf, which represents an effective reduction in input capacity by more than an order of magnitude.

Construction

Figure 6 is a photograph of the preamplifier. To achieve the small size, and for ease of construction, the circuit was packaged in a Rexolite former in which suitable sized holes were drilled for

each component. The individual parts were fixed in position with a drop of acrylic encapsulant and their leads were bent over and soldered.

The negative capacity control is a screwdriver adjustment type; thus, the feedback level cannot be changed accidentally once it has been set.

Conclusion

The preamplifier described appears to be superior to previous tube-type designs because of its performance as well as its reduced power consumption and size. Its input current is four or five orders of magnitude lower than that of junction FET circuits.

A feature of the circuit is its simplicity of operation. The number of adjustments is limited to the one necessary for regulating the negative capacity to suit different source impedances.

Finally, the circuit is constructed in a manner which permits easy and repeatable assembly in spite of its small size, and it is not necessary to specially select any values.

References

1. B. Chance, "Waveforms," Mass. Institute Tech., Radiation Lab. Series, No. 19, McGraw-Hill, pp. 767-770, 1949.

2. C. Guld, "Cathode follower and negative capacitance as high input impedance circuits," Proceedings of the IRE, Vol. 50, No. 9, pp. 1912-1927, September, 1962.

3. J. W. Moore and J. H. Gebhart, "Stabilized wide-band potentiometric preamplifiers," Proceedings of the IRE, Vol. 50, No. 9, pp. 1929-1941, September, 1962.

4. R. L. Schoenfeld, "Bandwidth limits for neutralized input capacity amplifiers," Proceedings of the IRE, pp. 1942-1950, September, 1962.

5. H. Fein, "Solid state electrometers and input capacitance neutralization," IEEE Transactions on Bio-Medical Engineering, Vol. BME-11, Nos. 1 and 2, pp. 13-18, January-April, 1964.

6. W. L. Nastuk and A. L. Hodgkin, "The electrical activity of single muscle fibers," J. Cellular and Comp. Physiology, Vol. 35, pp. 39-73, 1950.

7. S. J. Solms, W. L. Nastuk, and J. T. Alexander, Review of Scientific Instruments, Vol. 24, No. 10, pp. 960-967, October, 1953.

8. J. Y. Lettvin, B. Howland, and R. C. Gestland, "Footnotes on a headstage," IRE Trans. on Med. Elec., No. PGME-10, pp. 26-28, March, 1958.

Figure Titles

Figure 1.- Effective equivalent input circuit.

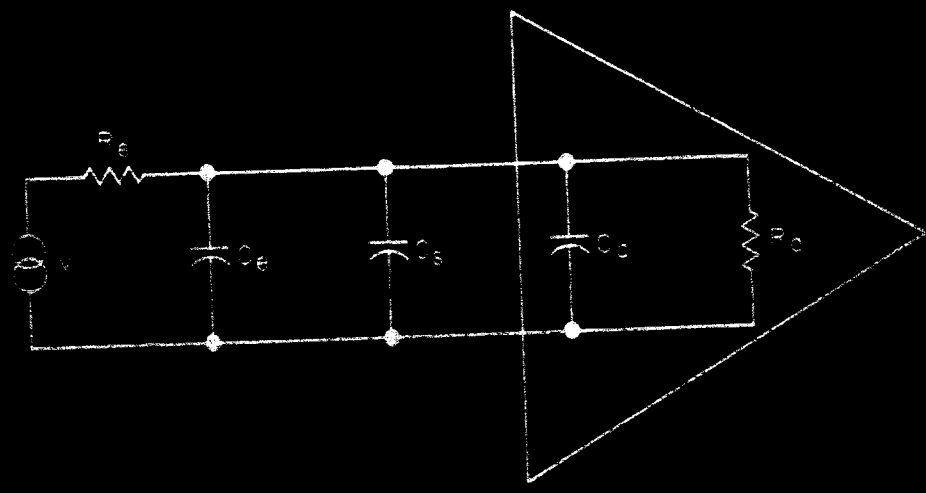
Figure 2.- Negative capacity principle.

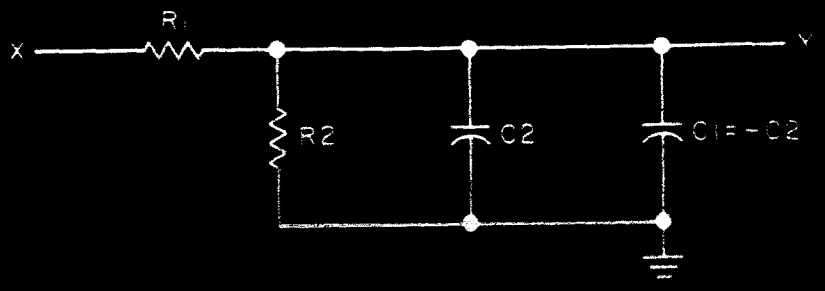
Figure 3.- Block diagram of negative capacity preamplifier.

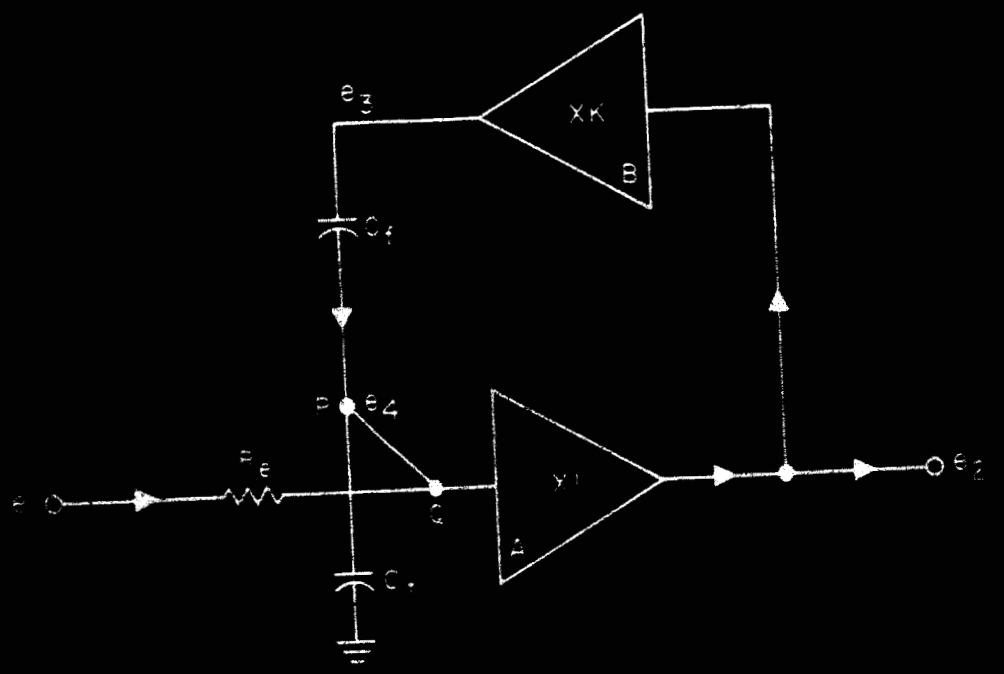
Figure 4.- Circuit diagram of negative capacity preamplifier.

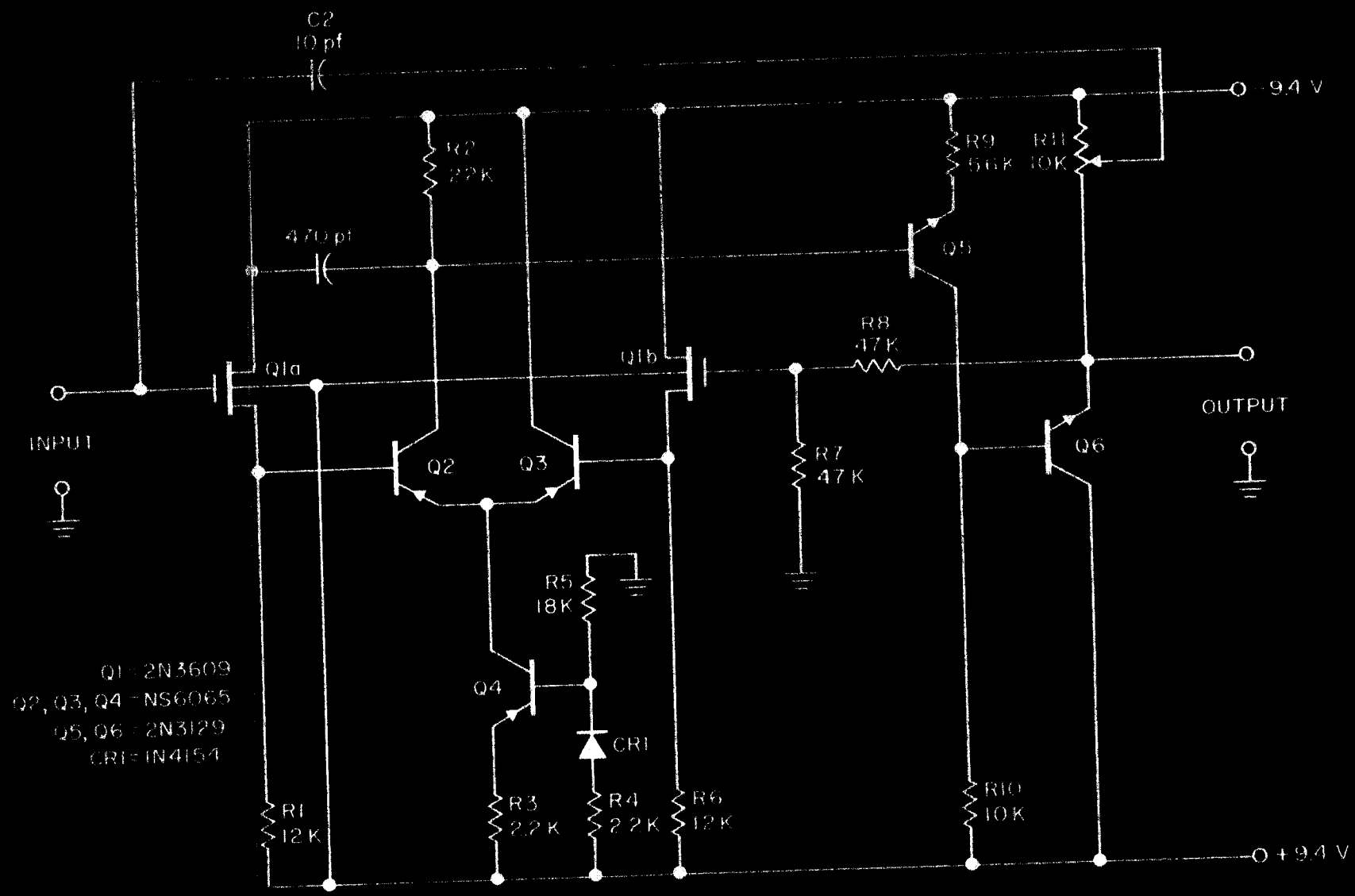
Figure 5.- Waveforms showing effect of negative capacity adjustment.

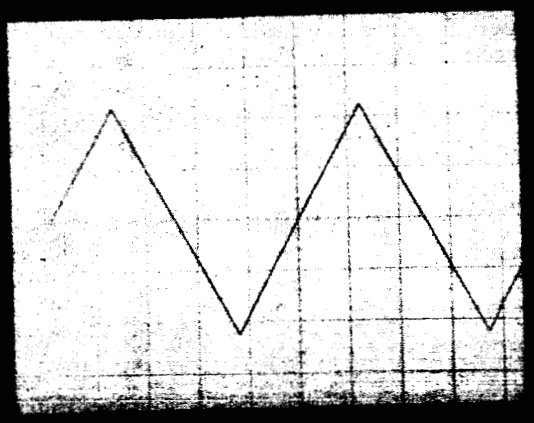
Figure 6.- Photograph of preamplifier.


Re
V
Ce
Cs
Cd
Ro

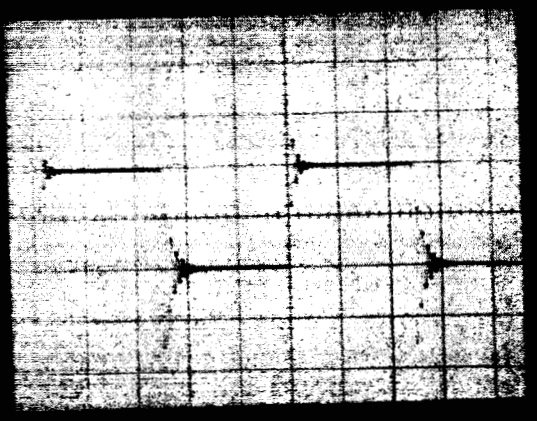

R1
X
Y
R2
C2
C1F-C2


XK
B
YI
A

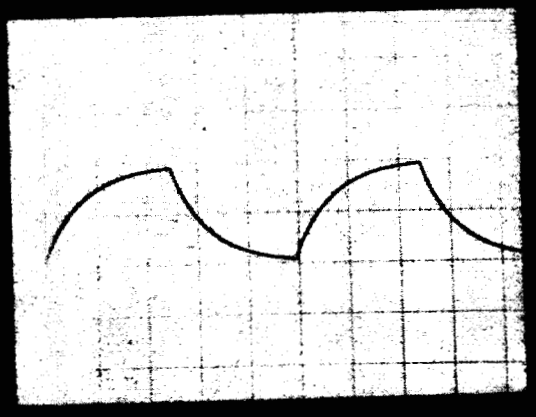

C2
10 pf
-9.4 V
R2
22K
R9
56K
R11
10K
470 pf
Q5
R8
47K
Q1a
Q1b
INPUT
OUTPUT
Q2
Q3
R7
47K
Q6
R5
18K
Q1 = 2N3609
Q2, Q3, Q4 = NS6065
Q5, Q6 = 2N3129
CR1 = IN4154
Q4
CR1
R1
12K
R3
2.2K
R4
2.2K
R6
12K
R10
10K
+9.4 V



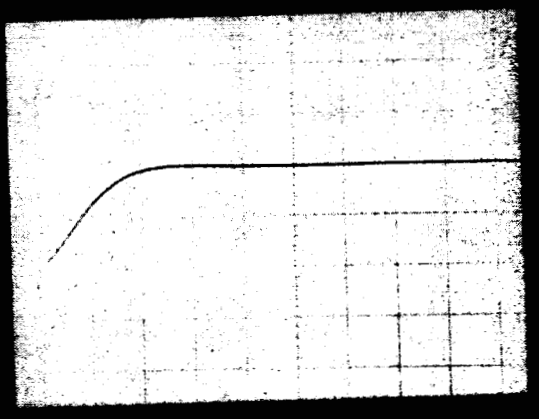
a



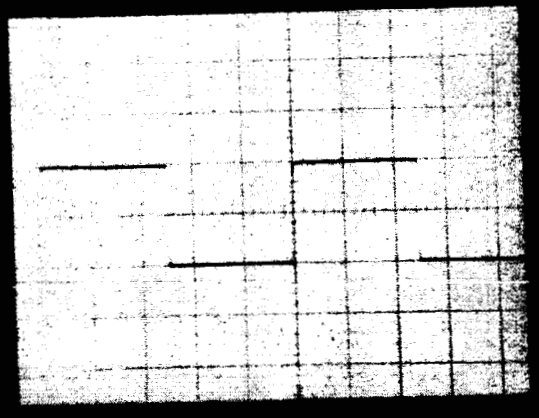
d



b



e

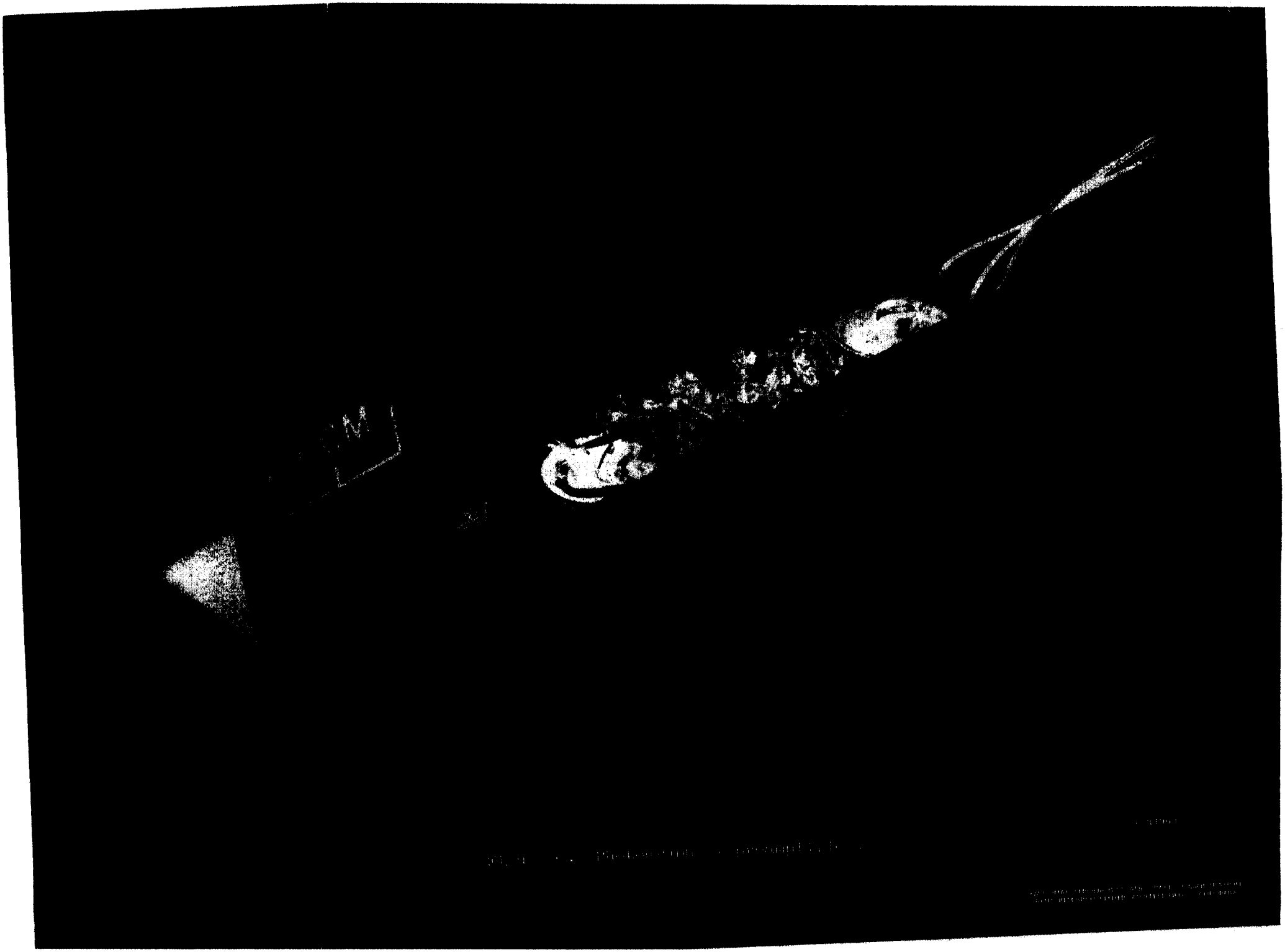


c

Scales

Horiz: a,b,c,d, 100 μs/cm

e, 10 μs/cm

Vert: a 5 V/cm

b,c,d,e, 0.1 V/cm